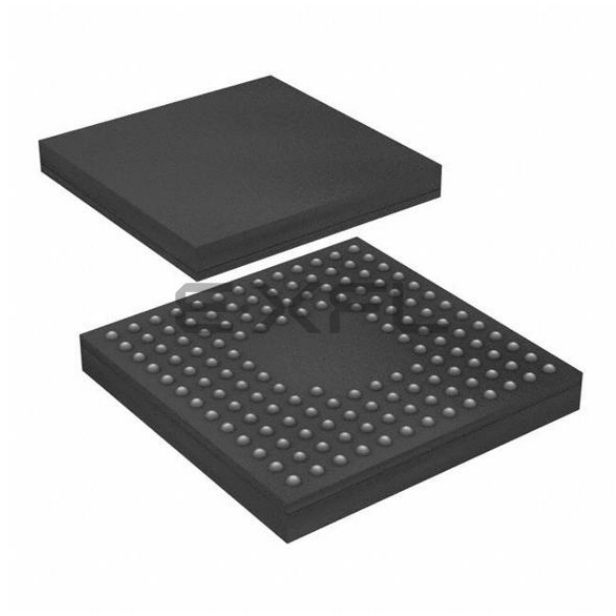
Renesas Electronics America Inc - R5F52108BDLK#U0 Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	RX
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	EBI/EMI, I²C, SCI, SPI
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	122
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	8K x 8
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	1.62V ~ 5.5V
Data Converters	A/D 16x12b; D/A 2x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	145-TFLGA
Supplier Device Package	145-TFLGA (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f52108bdlk-u0

Table 1.1 Outline of Specifications (3 / 5)

Classification	Module/Function	Description
Timers	16-bit timer pulse unit (TPUa)	• (16 bits × 6 channels) × 1 unit • Maximum of 16 pulse-input/output possible • Select from among seven or eight counter-input clock signals for each channel • Supports the input capture/output compare function • Output of PWM waveforms in up to 15 phases in PWM mode • Support for buffered operation, phase-counting mode (two-phase encoder input) and cascade-connected operation (32 bits × 2 channels) depending on the channel. • Capable of generating conversion start triggers for the A/D converters • Signals from the input capture pins are input via a digital filter • Clock frequency measuring method (Products with 144 or more pins incorporate a TPU.)
	Multi-function timer pulse unit 2 (MTU2a)	• (16 bits × 6 channels) × 1 unit • Up to 16 pulse-input/output lines and three pulse-input lines are available with six 16-bit timer channels • Select from among eight or seven counter-input clock signals for each channel (PCLK/1, PCLK/4, PCLK/16, PCLK/64, PCLK/256, PCLK/1024, MTCLKA, MTCLKB, MTCLKC, MTCLKD) other than channel 5, for which only four signals are available. • Input capture function • 21 output compare/input capture registers • Pulse output mode • Complementary PWM output mode • Reset synchronous PWM mode • Phase-counting mode • Generation of triggers for A/D converter conversion
	Port output enable 2 (POE2a)	Controls the high-impedance state of the MTU's waveform output pins
	8-bit timer (TMR)	• (8 bits × 2 channels) × 2 units • Select from among seven internal clock signals (PCLK1, PCLK/2, PCLK/8, PCLK/32, PCLK/64, PCLK/1024, PCLK/8192) and one external clock signal • Capable of output of pulse trains with desired duty cycles or of PWM signals • The 2 channels of each unit can be cascaded to create a 16-bit timer • Capable of generating baud-rate clocks for SCI5, SCI6, and SCI12
	Compare match timer (CMT)	• (16 bits × 2 channels) × 2 units • Select from among four clock signals (PCLK/8, PCLK/32, PCLK/128, PCLK/512)
	Watchdog timer (WDTA)	• 14 bits × 1 channel • Select from among six counter-input clock signals (PCLK/4, PCLK/64, PCLK/128, PCLK/512, PCLK/2048, PCLK/8192)
	Independent watchdog timer (IWDTa)	• 14 bits × 1 channel • Counter-input clock: IWDT-dedicated on-chip oscillator Frequency divided by 1, 16, 32, 64, 128, or 256
	Realtime clock (RTCb)	• Clock source: Sub-clock • Time/calendar • Interrupt sources: Alarm interrupt, periodic interrupt, and carry interrupt • Time-capture facility for three values

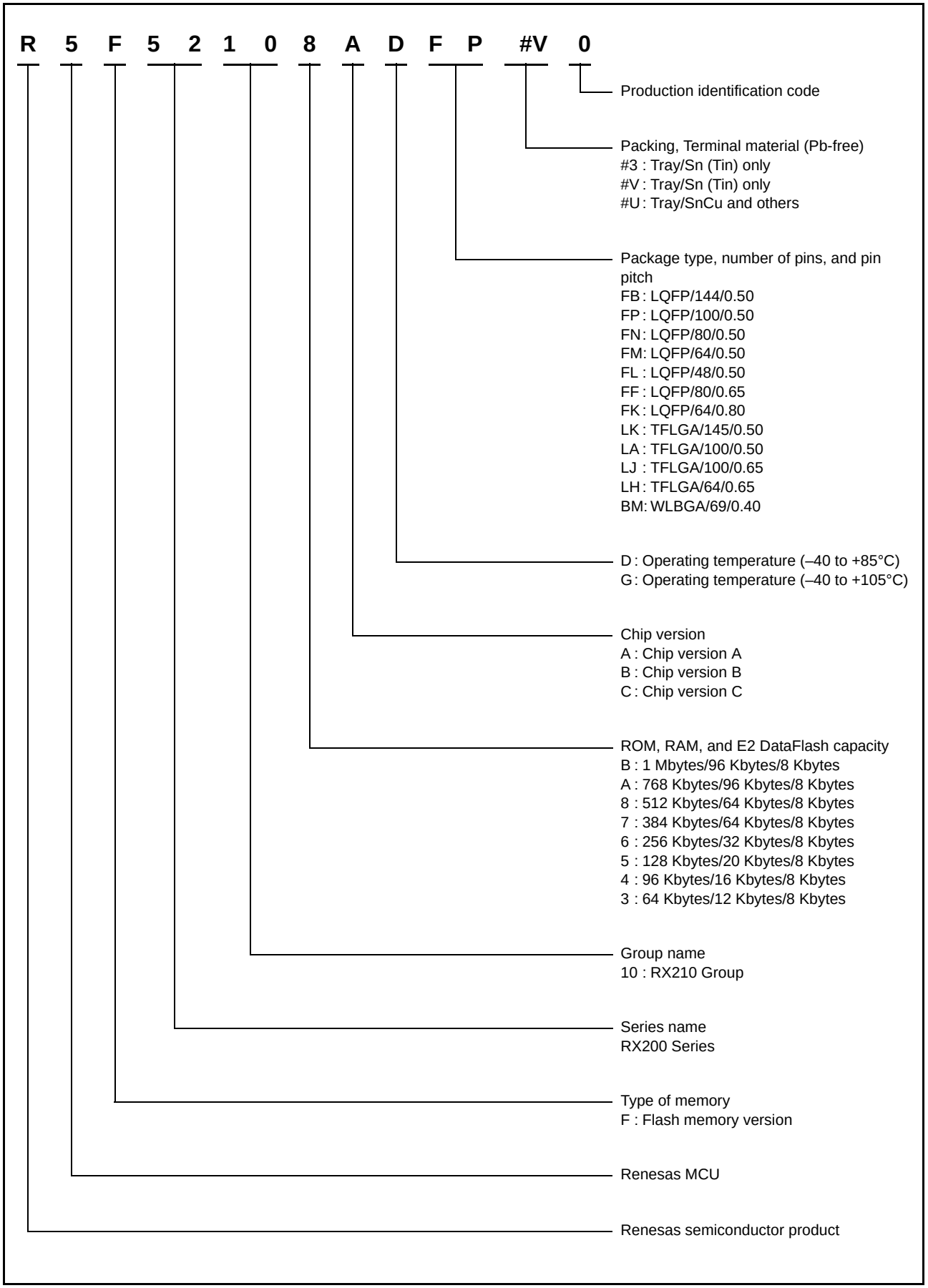


Figure 1.1 How to Read the Product Part No., Memory Capacity, and Package Type

1.4 Pin Functions

Table 1.8 lists the pin functions.

Table 1.8 Pin Functions (1 / 4)

Classifications	Pin Name	I/O	Description
Power supply	VCC	Input	Power supply pin. Connect it to the system power supply.
	VCL	—	Connect this pin to the VSS pin via the 0.1 µF smoothing capacitor used to stabilize the internal power supply. Place the capacitor close to the pin.
	VSS	Input	Ground pin. Connect it to the system power supply (0 V).
Clock	XTAL	Output	Pins for connecting a crystal resonator. An external clock signal can be input through the EXTAL pin.
	EXTAL	Input	
	BCLK	Output	Outputs the external bus clock for external devices.
	XCIN	Input	Input/output pins for the sub-clock oscillator. Connect a crystal resonator between XCIN and XCOUT.
	XCOUT	Output	
Operating mode control	MD	Input	Pin for setting the operating mode. The signal levels on this pin must not be changed during operation.
System control	RES#	Input	Reset pin. This LSI enters the reset state when this signal goes low.
CAC	CACREF	Input	Input pin for the clock frequency accuracy measurement circuit.
On-chip emulator	FINED	I/O	FINE interface pin.
Address bus	A0 to A23	Output	Output pins for the address.
Data bus	D0 to D15	I/O	Input and output pins for the bidirectional data bus.
Multiplexed bus	A0/D0 to A15/D15	I/O	Address/data multiplexed bus
Bus control	RD#	Output	Strobe signal which indicates that reading from the external bus interface space is in progress.
	WR#	Output	Strobe signal which indicates that writing to the external bus interface space is in progress, in single-write strobe mode.
	WR0#, WR1#	Output	Strobe signals which indicate that either group of data bus pins (D7 to D0, and D15 to D8) is valid in writing to the external bus interface space, in byte strobe mode.
	BC0#, BC1#	Output	Strobe signals which indicate that either group of data bus pins (D7 to D0 and D15 to D8) is valid in access to the external bus interface space, in single-write strobe mode.
	CS0# to CS3#	Output	Select signals for areas 0 to 3.
	WAIT#	Input	Input pin for wait request signals in access to the external space.
	ALE	Output	Address latch signal when address/data multiplexed bus is selected.
Interrupt	NMI	Input	Non-maskable interrupt request pin.
	IRQ0 to IRQ7	Input	Interrupt request pins.

Table 1.8 Pin Functions (2 / 4)

Classifications	Pin Name	I/O	Description
16-bit timer pulse unit	TIOCA0, TIOCB0 TIOCC0, TIOCD0	I/O	The TGRA0 to TGRD0 input capture input/output compare output/ PWM output pins.
	TIOCA1, TIOCB1	I/O	The TGRA1 and TGRB1 input capture input/output compare output/ PWM output pins.
	TIOCA2, TIOCB2	I/O	The TGRA2 and TGRB2 input capture input/output compare output/ PWM output pins.
	TIOCA3, TIOCB3 TIOCC3, TIOCD3	I/O	The TGRA3 to TGRD3 input capture input/output compare output/ PWM output pins.
	TIOCA4, TIOCB4	I/O	The TGRA4 and TGRB4 input capture input/output compare output/ PWM output pins.
	TIOCA5, TIOCB5	I/O	The TGRA5 and TGRB5 input capture input/output compare output/ PWM output pins.
	TCLKA, TCLKB TCLKC, TCLKD	Input	Input pins for external clock signals.
Multi-function timer pulse unit 2	MTIOC0A, MTIOC0B MTIOC0C, MTIOC0D	I/O	The TGRA0 to TGRD0 input capture input/output compare output/ PWM output pins.
	MTIOC1A, MTIOC1B	I/O	The TGRA1 and TGRB1 input capture input/output compare output/ PWM output pins.
	MTIOC2A, MTIOC2B	I/O	The TGRA2 and TGRB2 input capture input/output compare output/ PWM output pins.
	MTIOC3A, MTIOC3B MTIOC3C, MTIOC3D	I/O	The TGRA3 to TGRD3 input capture input/output compare output/ PWM output pins.
	MTIOC4A, MTIOC4B MTIOC4C, MTIOC4D	I/O	The TGRA4 to TGRD4 input capture input/output compare output/ PWM output pins.
	MTIC5U, MTIC5V, MTIC5W	Input	The TGRU5, TGRV5, and TGRW5 input capture input/external pulse input pins.
	MTCLKA, MTCLKB, MTCLKC, MTCLKD	Input	Input pins for the external clock.
Port output enable 2	POE0# to POE3#, POE8#	Input	Input pins for request signals to place the MTU pins in the high impedance state.
8-bit timer	TMO0 to TMO3	Output	Compare match output pins.
	TMCI0 to TMCI3	Input	Input pins for external clocks to be input to the counter.
	TMRI0 to TMRI3	Input	Input pins for the counter reset.
Realtime clock	RTCOUT	Output	Output pin for 1-Hz clock.
	RTCIC0 to RTCIC2	Input	Time capture event input pins.
Serial communications interface (SCIc)	• Asynchronous mode/clock synchronous mode		
	SCK0 to SCK11	I/O	Input/output pins for the clock
	RXD0 to RXD11	Input	Input pins for received data
	TXD0 to TXD11	Output	Output pins for transmitted data
	CTS0# to CTS11#	Input	Input pins for controlling the start of transmission and reception
	RTS0# to RTS11#	Output	Output pins for controlling the start of transmission and reception
	• Simple I^2C mode		
	SSCL0 to SSCL11	I/O	Input/output pins for the I^2C clock
	SSDA0 to SSDA11	I/O	Input/output pins for the I^2C data
	• Simple SPI mode		
	SCK0 to SCK11	I/O	Input/output pins for the clock
	SMISO0 to SMISO11	I/O	Input/output pins for slave transmission of data
	SMOSI0 to SMOSI11	I/O	Input/output pins for master transmission of data
	SS0# to SS11#	Input	Chip-select input pins

Table 1.8 Pin Functions (4 / 4)

Classifications	Pin Name	I/O	Description
Analog power supply	AVCC0	Input	Analog voltage supply pin for the 12-bit A/D converter. Connect this pin to VCC if the 12-bit A/D converter is not to be used.
	AVSS0	Input	Analog ground pin for the 12-bit A/D converter. Connect this pin to VSS if the 12-bit A/D converter is not to be used.
	VREFH0	Input	Analog reference voltage supply pin for the 12-bit A/D converter. Connect this pin to VCC if the 12-bit A/D converter is not to be used.
	VREFL0	Input	Analog reference ground pin for the 12-bit A/D converter. Connect this pin to VSS if the 12-bit A/D converter is not to be used.
	VREFH	Input	Analog voltage supply pin for the D/A converter. Connect this pin to VCC if the D/A converter is not to be used.
	VREFL	Input	Analog ground pin for the D/A converter. Connect this pin to VSS if the D/A converter is not to be used.
I/O ports	P00 to P03, P05, P07	I/O	6-bit input/output pins.
	P12 to P17	I/O	6-bit input/output pins.
	P20 to P27	I/O	8-bit input/output pins.
	P30 to P37	I/O	8-bit input/output pins. (P35 input pin)
	P40 to P47	I/O	8-bit input/output pins.
	P50 to P56	I/O	7-bit input/output pins.
	P60 to P67	I/O	8-bit input/output pins.
	P70 to P77	I/O	8-bit input/output pins.
	P80 to P83, P86, P87	I/O	6-bit input/output pins.
	P90 to P93	I/O	4-bit input/output pins.
	PA0 to PA7	I/O	8-bit input/output pins.
	PB0 to PB7	I/O	8-bit input/output pins.
	PC0 to PC7	I/O	8-bit input/output pins.
	PD0 to PD7	I/O	8-bit input/output pins.
	PE0 to PE7	I/O	8-bit input/output pins.
	PF5	I/O	1-bit input/output pin.
	PH0 to PH3	I/O	4-bit input/output pins.
	PJ1, PJ3, PJ5	I/O	3-bit input/output pins.
	PK2 to PK5	I/O	4-bit input/output pins.
	PL0, PL1	I/O	2-bit input/output pins.

Table 1.9 List of Pins and Pin Functions (145-Pin TFLGA) (4 / 4)

Pin No.	Power Supply, Clock, System Control	I/O Port	External Bus	Timers (MTU, TMR, POE)	Communications (SCIc, SCId, RSPI, RIIC)	Others
M11		PC0	A16	MTIOC3C/TCLKC	CTS5#/RTS5#/SS5#/ SSLA1	
M12		PC1	A17	MTIOC3A/TCLKD	SCK5/SSLA2	
M13		PL1				
N1		P21		MTIOC1B/TMCI0/ TIOCA3	RXD0/SMISO0/SSCL0	
N2		P20		MTIOC1A/TMRI0/ TIOCB3	TXD0/SMOSI0/SSDA0	
N3		P87		TIOCA2		
N4		P14		MTIOC3A/MTCLKA/ TMRI2/TIOCB5/TCLKA	CTS1#/RTS1#/SS1#	IRQ4
N5		PH2		TMRI0		IRQ1
N6		PH1		TMO0		IRQ0
N7		P55	WAIT#	MTIOC4D/TMO3		
N8	VSS					
N9		PC7	A23/CS0#	MTIOC3A/TMO2/ MTCLKB	TXD8/SMOSI8/SSDA8/ MISOA	CACREF
N10		P82		MTIOC4A	TXD10/SMOSI10/SSDA10	
N11		PC3	A19	MTIOC4D/TCLKB	TXD5/SMOSI5/SSDA5	
N12		P75			SCK11	
N13		P74			CTS11#/RTS11#/SS11#	

Note: • Pin names to which –DS is appended are for pins that can be used to trigger release from deep software standby mode.
Note: • Leave the NC pin open.

Table 1.11 List of Pins and Pin Functions (100-Pin TFLGA) (3 / 3)

Pin No.	Power Supply, Clock, System Control	I/O Port	External Bus	Timers (MTU, TMR, POE)	Communications (SCIc, SCId, RSPI, RIIC)	Others
J4		P13		MTIOC0B/TMO3	SDA	IRQ3
J5		PH0				CACREF
J6		PH3		TMCI0		
J7		P50	WR0#/WR#			
J8		PC4	A20/CS3#	MTIOC3D/MTCLKC/ TMCI1/POE0#	SCK5/CTS8#/RTS8#/ SS8#/SSLA0	
J9		PC0	A16	MTIOC3C	CTS5#/RTS5#/SS5#/ SSLA1	
J10		PC1	A17	MTIOC3A	SCK5/SSLA2	
K1		P23		MTIOC3D/MTCLKD	CTS0#/RTS0#/SS0#	
K2		P22		MTIOC3B/MTCLKC/ TMO0	SCK0	
K3		P20		MTIOC1A/TMRI0	TXD0/SMOSI0/SSDA0	
K4		P14		MTIOC3A/MTCLKA/ TMRI2	CTS1#/RTS1#/SS1#	IRQ4
K5		PH2		TMRI0		IRQ1
K6		PH1		TMO0		IRQ0
K7		P51	WR1#/BC1#/WAIT#			
K8		PC5	A21/CS2#/WAIT#	MTIOC3B/MTCLKD/ TMRI2	SCK8/RSPCKA	
K9		PC3	A19	MTIOC4D	TXD5/SMOSI5/SSDA5	
K10		PC2	A18	MTIOC4B	RXD5/SMISO5/SSCL5/ SSLA3	

Note: • Pin names to which –DS is appended are for pins that can be used to trigger release from deep software standby mode.

Table 1.14 List of Pins and Pin Functions (69-Pin WLBGA) (2 / 2)

Pin No.	Power Supply, Clock, System Control	I/O Port	Timers (MTU, TMR, POE)	Communications (SCIc, SCId, RSPI, RIIC)	Others
G3	NC				
G4		P54	MTIOC4B/TMCI1		
G5		PH1	TMO0		IRQ0
G6		P14	MTIOC3A/MTCLKA/TMRI2	CTS1#/RTS1#/SS1#	IRQ4
G7		P27	MTIOC2B/TMCI3	SCK1	
G8		P32	MTIOC0C/TMO3	TXD6/SMOSI6/SSDA6	IRQ2-DS/RTCOUT/ RTCIC2
G9		P35			NMI
H1		PB7	MTIOC3B	TXD9/SMOSI9/SSDA9	
H2		PC3	MTIOC4D	TXD5/SMOSI5/SSDA5	
H3		PC5	MTIOC3B/MTCLKD/TMRI2	SCK8/RSPCKA	
H4		PC6	MTIOC3C/MTCLKA/TMCI2	RXD8/SMISO8/SSCL8/MOSIA	
H5		P55	MTIOC4D/TMO3		
H6		PH3	TMCI0		
H7		P17	MTIOC3A/MTIOC3B/TMO1/ POE8#	SCK1/MISOA/SDA-DS	IRQ7
H8		P26	MTIOC2A/TMO1	TXD1/SMOSI1/SSDA1	
H9		P30	MTIOC4B/TMRI3/POE8#	RXD1/SMISO1/SSCL1	IRQ0-DS/RTCIC0
J1	NC				
J2		PC2	MTIOC4B	RXD5/SMISO5/SSCL5/SSLA3	
J3		PC4	MTIOC3D/MTCLKC/TMCI1/ POE0#	SCK5/CTS8#/RTS8#/SS8#/ SSLA0	
J4		PC7	MTIOC3A/TMO2/MTCLKB	TXD8/SMOSI8/SSDA8/MISOA	CACREF
J5		PH0			CACREF
J6		PH2	TMRI0		IRQ1
J7		P15	MTIOC0B/MTCLKB/TMCI2	RXD1/SMISO1/SSCL1	IRQ5
J8		P16	MTIOC3C/MTIOC3D/TMO2	TXD1/SMOSI1/SSDA1/ MOSIA/SCL-DS	IRQ6/RTCOUT/ ADTRG0#
J9	NC				

Note: • Pin names to which –DS is appended are for pins that can be used to trigger release from deep software standby mode.
Note: • Leave the NC pin open.

Table 1.15 List of Pins and Pin Functions (64-Pin TFLGA) (1 / 2)

Pin No.	Power Supply, Clock, System Control	I/O Port	Timers (MTU, TMR, POE)	Communication (SCIc, SCId, RSPI, RIIC)	Others
A1		P05			DA1
A2	AVCC0				
A3	VREFH0				
A4	VREFL0				
A5	VREFH				
A6	VREFL				
A7		PE2	MTIOC4A	RXD12/RXDX12/SMISO12/ SSCL12	IRQ7-DS/AN010/ CVREFB0
A8		PE3	MTIOC4B/POE8#	CTS12#/RTS12#/SS12#	AN011/CMPA1
B1	VCL				
B2	AVSS0				
B3		P40			AN000
B4		P42			AN002
B5		P44			AN004
B6		P46			AN006
B7		PE1	MTIOC4C	TXD12/TXDX12/SIOX12/ SMOSI12/SSDA12	AN009/CMPB0
B8		PE4	MTIOC4D/MTIOC1A		AN012/CMPA2
C1	XCIN				
C2	MD				FINED
C3		P03			DA0
C4		P41			AN001
C5		P43			AN003
C6		PE0		SCK12	AN008
C7		PE5	MTIOC4C/MTIOC2B		IRQ5/AN013
C8		PA0	MTIOC4A	SSLA1	CACREF
D1	XCOUT				
D2	RES#				
D3		P27	MTIOC2B/TMCI3	SCK1	
D4		P14	MTIOC3A/MTCLKA/TMRI2	CTS1#/RTS1#/SS1#	IRQ4
D5		PA6	MTIC5V/MTCLKB/TMCI3/ POE2#	CTS5#/RTS5#/SS5#/MOSIA	
D6		PA4	MTIC5U/MTCLKA/TMRI0	TXD5/SMOSI5/SSDA5/SSLA0	IRQ5-DS/CVREFB1
D7		PA1	MTIOC0B/MTCLKC	SCK5/SSLA2	CVREFA
D8		PA3	MTIOC0D/MTCLKD	RXD5/SMISO5/SSCL5	IRQ6-DS/CMPB1
E1	VSS				
E2		P32	MTIOC0C/TMO3	TXD6/SMOSI6/SSDA6	IRQ2-DS/RTCOUT/ RTCIC2
E3		P30	MTIOC4B/TMRI3/POE8#	RXD1/SMISO1/SSCL1	IRQ0-DS/RTCIC0
E4		P16	MTIOC3C/MTIOC3D/TMO2	TXD1/SMOSI1/SSDA1/MOSIA/ SCL-DS	IRQ6/RTCOUT/ ADTRG0#
E5		PC4	MTIOC3D/MTCLKC/TMCI1/ POE0#	SCK5/CTS8#/RTS8#/SS8#/ SSLA0	
E6	VCC				
E7	VSS				
E8		PB0	MTIC5W	RXD6/SMISO6/SSCL6/RSPCKA	
F1	VCC				
F2		P35			NMI
F3		P31	MTIOC4D/TMCI2	CTS1#/RTS1#/SS1#	IRQ1-DS/RTCIC1
F4		PC5	MTIOC3B/MTCLKD/TMRI2	SCK8/RSPCKA	

Table 4.1 List of I/O Registers (Address Order) (10 / 29)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles: ICLK ≥ PCLK	Number of Access Cycles: ICLK < PCLK
0008 738A2	ICU	Interrupt source priority register 162	IPR162	8	8		2 ICLK
0008 73A4h	ICU	Interrupt source priority register 164	IPR164	8	8		2 ICLK
0008 73A6h	ICU	Interrupt source priority register 166	IPR166	8	8		2 ICLK
0008 73AAh	ICU	Interrupt source priority register 170	IPR170	8	8		2 ICLK
0008 73ABh	ICU	Interrupt source priority register 171	IPR171	8	8		2 ICLK
0008 73AEh	ICU	Interrupt source priority register 174	IPR174	8	8		2 ICLK
0008 73B1h	ICU	Interrupt source priority register 177	IPR177	8	8		2 ICLK
0008 73B4h	ICU	Interrupt source priority register 180	IPR180	8	8		2 ICLK
0008 73B7h	ICU	Interrupt source priority register 183	IPR183	8	8		2 ICLK
0008 73BAh	ICU	Interrupt source priority register 186	IPR186	8	8		2 ICLK
0008 73BEh	ICU	Interrupt source priority register 190	IPR190	8	8		2 ICLK
0008 73C2h	ICU	Interrupt source priority register 194	IPR194	8	8		2 ICLK
0008 73C6h	ICU	Interrupt source priority register 198	IPR198	8	8		2 ICLK
0008 73C7h	ICU	Interrupt source priority register 199	IPR199	8	8		2 ICLK
0008 73C8h	ICU	Interrupt source priority register 200	IPR200	8	8		2 ICLK
0008 73C9h	ICU	Interrupt source priority register 201	IPR201	8	8		2 ICLK
0008 73CEh	ICU	Interrupt source priority register 206	IPR206	8	8		2 ICLK
0008 73D2h	ICU	Interrupt source priority register 210	IPR210	8	8		2 ICLK
0008 73D6h	ICU	Interrupt source priority register 214	IPR214	8	8		2 ICLK
0008 73DAh	ICU	Interrupt source priority register 218	IPR218	8	8		2 ICLK
0008 73DEh	ICU	Interrupt source priority register 222	IPR222	8	8		2 ICLK
0008 73E2h	ICU	Interrupt source priority register 226	IPR226	8	8		2 ICLK
0008 73E6h	ICU	Interrupt source priority register 230	IPR230	8	8		2 ICLK
0008 73EAh	ICU	Interrupt source priority register 234	IPR234	8	8		2 ICLK
0008 73EEh	ICU	Interrupt source priority register 238	IPR238	8	8		2 ICLK
0008 73F2h	ICU	Interrupt source priority register 242	IPR242	8	8		2 ICLK
0008 73F3h	ICU	Interrupt source priority register 243	IPR243	8	8		2 ICLK
0008 73F4h	ICU	Interrupt source priority register 244	IPR244	8	8		2 ICLK
0008 73F5h	ICU	Interrupt source priority register 245	IPR245	8	8		2 ICLK
0008 73F6h	ICU	Interrupt source priority register 246	IPR246	8	8		2 ICLK
0008 73F7h	ICU	Interrupt source priority register 247	IPR247	8	8		2 ICLK
0008 73F8h	ICU	Interrupt source priority register 248	IPR248	8	8		2 ICLK
0008 73F9h	ICU	Interrupt source priority register 249	IPR249	8	8		2 ICLK
0008 73FAh	ICU	Interrupt source priority register 250	IPR250	8	8		2 ICLK
0008 7400h	ICU	DMAC activation request select register 0	DMRSR0	8	8		2 ICLK
0008 7404h	ICU	DMAC activation request select register 1	DMRSR1	8	8		2 ICLK
0008 7408h	ICU	DMAC activation request select register 2	DMRSR2	8	8		2 ICLK
0008 740Ch	ICU	DMAC activation request select register 3	DMRSR3	8	8		2 ICLK
0008 7500h	ICU	IRQ control register 0	IRQCR0	8	8		2 ICLK
0008 7501h	ICU	IRQ control register 1	IRQCR1	8	8		2 ICLK
0008 7502h	ICU	IRQ control register 2	IRQCR2	8	8		2 ICLK
0008 7503h	ICU	IRQ control register 3	IRQCR3	8	8		2 ICLK
0008 7504h	ICU	IRQ control register 4	IRQCR4	8	8		2 ICLK
0008 7505h	ICU	IRQ control register 5	IRQCR5	8	8		2 ICLK
0008 7506h	ICU	IRQ control register 6	IRQCR6	8	8		2 ICLK
0008 7507h	ICU	IRQ control register 7	IRQCR7	8	8		2 ICLK
0008 7510h	ICU	IRQ pin digital filter enable register 0	IRQFLTE0	8	8		2 ICLK
0008 7514h	ICU	IRQ pin digital filter setting register 0	IRQFLTC0	16	16		2 ICLK
0008 7580h	ICU	Non-maskable interrupt status register	NMISR	8	8		2 ICLK
0008 7581h	ICU	Non-maskable interrupt enable register	NMIER	8	8		2 ICLK
0008 7582h	ICU	Non-maskable interrupt clear register	NMICLR	8	8		2 ICLK

Table 5.4 DC Characteristics (3)

Conditions: VCC = AVCC0 = 1.62 to 5.5 V, VSS = AVSS0 = VREFL = VREFL0 = 0 V, T_a = –40 to +105°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Input leakage current	RES#, MD pin, P35/NMI	$\lvert I_{in} \rvert$	—	—	1.0	µA	V_{in} = 0 V, VCC
Three-state leakage current (off-state)	Port 4	$\lvert I_{TSI} \rvert$	—	—	1.0	µA	V_{in} = 0 V, VCC
	Other pins except for ports for 5 V tolerant and port 4		—	—	0.2		
	Ports for 5 V tolerant		—	—	1.0		V_{in} = 0 V, 5.8 V
Input capacitance	All input pins (except for ports 12, 13, 16, 17, 4, A1, A3, A4, and E)	C_{in}	—	—	15	pF	V_{in} = 0 V, f = 1 MHz, T_a = 25°C
	Ports 12, 13, 16, 17, 4, A1, A3, A4, and E		—	—	30		

Table 5.5 DC Characteristics (4)

Conditions: VCC = AVCC0 = 1.62 to 5.5 V, VSS = AVSS0 = VREFL = VREFL0 = 0 V, T_a = –40 to +105°C

Item		Symbol	VCC						Unit	Test Conditions
			1.62 to 2.7 V		2.7 to 4.0 V		4.0 to 5.5 V			
			Min.	Max.	Min.	Max.	Min.	Max.		
Input pull-up MOS current	All ports (except for port 35)	I_p	–150	–5	–200	–10	–400	–50	µA	V_{in} = 0 V

[Chip version A]

Table 5.6 DC Characteristics (5)

Conditions: VCC = AVCC0 = 2.7 to 5.5 V, VSS = AVSS0 = VREFL = VREFL0 = 0 V, T_a = –40 to +105°C

Item					Symbol	Typ.	Max.	Unit	Test Conditions
Supply current*1	High-speed operating mode	Normal operating mode	No peripheral operation*2	ICLK = 50 MHz	I_{CC}	10	—	mA	
			All peripheral operation: Normal*3	ICLK = 50 MHz		31.5	—		
			All peripheral operation: Max.*3	ICLK = 50 MHz		—	55		
		Sleep mode	No peripheral operation	ICLK = 50 MHz		7.5	—		
			All peripheral operation: Normal	ICLK = 50 MHz		17.5	—		
		All-module clock stop mode		ICLK = 50 MHz		6.7	—		
		Increase during BGO operation*4				25	—		

Note 1. Supply current values do not include output charge/discharge current from all pins. The values apply when internal pull-up MOSs are in the off state.

Note 2. Clock supply to the peripheral functions is stopped. This does not include BGO operation. The clock source is PLL and the VCO oscillation frequency is 100 MHz. BCLK, FCLK, and PCLK are set to divided by 64.

Note 3. Clocks are supplied to the peripheral functions. This does not include BGO operation. The clock source is PLL and the VCO oscillation frequency is 100 MHz. BCLK, FCLK, and PCLK are ICLK divided by 2.

Note 4. This is the increase if data is programmed to or erasing from the ROM or E2 DataFlash during program execution.

Item					Symbol	Typ.	Max.	Unit	Test Conditions
Supply current*1	Low-speed operating mode 1	Normal operating mode	No peripheral operation*7	ICLK = 8 MHz	I_{CC}	2.1	—	mA	
				ICLK = 4 MHz		1.7	—		
				ICLK = 2 MHz		1.5	—		
			All peripheral operation: Normal*8	ICLK = 8 MHz		7.3	—		
				ICLK = 4 MHz		4.5	—		
				ICLK = 2 MHz		3.1	—		
			All peripheral operation: Max.*7	ICLK = 8 MHz		—	12		
				ICLK = 4 MHz		—	—		
				ICLK = 2 MHz		—	—		
		Sleep mode	No peripheral operation	ICLK = 8 MHz		1.5	—		
				ICLK = 4 MHz		1.4	—		
				ICLK = 2 MHz		1.3	—		
			All peripheral operation: Normal	ICLK = 8 MHz		4.1	—		
				ICLK = 4 MHz		3.0	—		
				ICLK = 2 MHz		2.3	—		
		All-module clock stop mode		ICLK = 8 MHz		1.4	—		
				ICLK = 4 MHz		1.3	—		
				ICLK = 2 MHz		1.2	—		
	Low-speed operating mode 2	Normal operating mode	No peripheral operation*9	ICLK = 32 kHz		0.022	—		
			All peripheral operation: Normal*10	ICLK = 32 kHz		0.06	—		
			All peripheral operation: Max.*10	ICLK = 32 kHz		—	3*11		
		Sleep mode	No peripheral operation	ICLK = 32 kHz		0.017	—		
			All peripheral operation: Normal	ICLK = 32 kHz		0.036	—		
		All-module clock stop mode				0.017	—		

Note 1. Supply current values do not include output charge/discharge current from all pins. The values apply when internal pull-up MOSs are in the off state.
Note 2. Clock supply to the peripheral functions is stopped. This does not include BGO operation. The clock source is PLL and the VCO oscillation frequency is 64 MHz. BCLK, FCLK, and PCLK are set to divided by 64.
Note 3. Clock supply to the peripheral functions is stopped. This does not include BGO operation. The clock source is HOCO and the oscillation frequency is 40 MHz. BCLK, FCLK, and PCLK are set to divided by 64.
Note 4. Clocks are supplied to the peripheral functions. This does not include BGO operation. The clock source is PLL and the VCO oscillation frequency is 64 MHz. BCLK, FCLK, and PCLK are ICLK divided by 1.
Note 5. Clocks are supplied to the peripheral functions. This does not include BGO operation. The clock source is HOCO and the oscillation frequency is 40 MHz. BCLK, FCLK, and PCLK are ICLK divided by 1.
Note 6. This is the increase if data is programmed to or erasing from the ROM or E2 DataFlash during program execution.
Note 7. Clock supply to the peripheral functions is stopped. This does not include BGO operation. The clock source is HOCO and the oscillation frequency is 32 MHz. BCLK, FCLK, and PCLK are set to divided by 64.
Note 8. Clocks are supplied to the peripheral functions. This does not include BGO operation. The clock source is HOCO and the oscillation frequency is 32 MHz. BCLK, FCLK, and PCLK are ICLK divided by 1.
Note 9. Clock supply to the peripheral functions is stopped. This does not include BGO operation. The clock source is the sub oscillation circuit. BCLK, FCLK, and PCLK are set to divided by 64.
Note 10. Clocks are supplied to the peripheral functions. This does not include BGO operation. The clock source is the sub oscillation circuit. BCLK, FCLK, and PCLK are ICLK divided by 1.
Note 11. Value when the main clock continues oscillating at 12.5 MHz.

[Chip versions B and C]

Table 5.31 Output Values of Voltage (4)

Conditions: VCC = AVCC0 = 2.7 to 4.0 V, VSS = AVSS0 = VREFL = VREFL0 = 0 V, T_a = –40 to +105°C

Item			Symbol	Min.	Max.	Unit	Test Conditions
Output low	All output pins (other than RIIC)	Normal output mode	V_{OL}	—	0.5	V	I_{OL} = 1.0 mA
		High-drive output mode		—	0.5		I_{OL} = 2.0 mA
	RIIC pins			—	0.4		I_{OL} = 3.0 mA
				—	0.6		I_{OL} = 6.0 mA
Output high	All output pins	Normal output mode	V_{OH}	VCC – 0.5	—	V	I_{OH} = –1.0 mA
		High-drive output mode		VCC – 0.5	—		I_{OH} = –2.0 mA

[Chip versions B and C]

Table 5.32 Output Values of Voltage (5)

Conditions: VCC = AVCC0 = 4.0 to 5.5 V, VSS = AVSS0 = VREFL = VREFL0 = 0 V, T_a = –40 to +105°C

Item			Symbol	Min.	Max.	Unit	Test Conditions
Output low	All output pins (other than RIIC)	Normal output mode	V_{OL}	—	0.8	V	I_{OL} = 2.0 mA
		High-drive output mode		—	0.8		I_{OL} = 4.0 mA
	RIIC pins			—	0.4		I_{OL} = 3.0 mA
				—	0.6		I_{OL} = 6.0 mA
Output high	All output pins	Normal output mode	V_{OH}	VCC – 0.8	—	V	I_{OH} = –2.0 mA
		High-drive output mode		VCC – 0.8	—		I_{OH} = –4.0 mA

5.2.1 Standard I/O Pin Output Characteristics (1)

Figure 5.45 to Figure 5.49 show the characteristics when normal output is selected by the drive capacity control register.

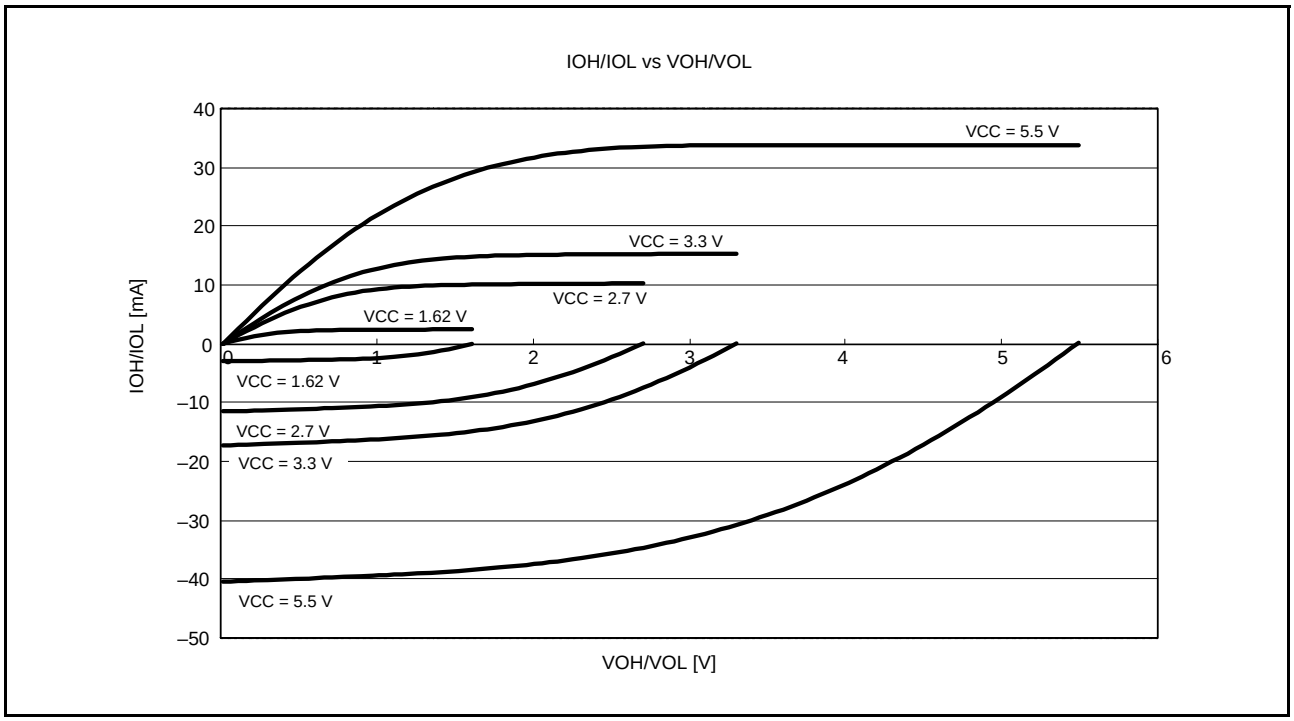


Figure 5.45 VOH/VOL and IOH/IOL Voltage Characteristics at Ta = 25°C when Normal Output is Selected (Reference Data)

5.3.3 Timing of Recovery from Low Power Consumption Modes

[Chip versions A and C]

Table 5.46 Timing of Recovery from Low Power Consumption Modes

Conditions: VCC = AVCC0 = 1.62 to 5.5 V, VSS = AVSS0 = VREFL = VREFL0 = 0 V, T_a = –40 to +105°C

Item			Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Recovery time after cancellation of software standby mode (flash memory, HOCO power supplied) (SOFTCUT[2:0] bits = 000b)*1	Crystal resonator connected to main clock oscillator*2	Main clock oscillator operating	t_{SBYMC}	—	3	—	ms	Figure 5.72
		Main clock oscillator and PLL circuit operating	t_{SBYPC}	—	3.5	—	ms	
	External clock input to main clock oscillator	Main clock oscillator operating	t_{SBYEX}	10	—	—	µs	
		Main clock oscillator and PLL circuit operating	t_{SBYPE}	0.5	—	—	ms	
	Sub-clock oscillator operating		t_{SBYSC}	2*3	—	—	s	
	HOCO clock oscillator operating		t_{SBYHO}	—	—	500	µs	
	LOCO clock oscillator operating		t_{SBYLO}	—	—	90	µs	
Recovery time after cancellation of software standby mode (flash memory power supplied, HOCO power not supplied) (SOFTCUT[2:0] bits = 110b)*1	Crystal resonator connected to main clock oscillator*2	Main clock oscillator operating	t_{SBYMC}	—	3	—	ms	Figure 5.72
		Main clock oscillator and PLL circuit operating	t_{SBYPC}	—	3.5	—	ms	
	External clock input to main clock oscillator	Main clock oscillator operating	t_{SBYEX}	40	—	—	µs	
		Main clock oscillator and PLL circuit operating	t_{SBYPE}	0.5	—	—	ms	
	Sub-clock oscillator operating		t_{SBYSC}	2*3	—	—	s	
	HOCO clock oscillator operating		t_{SBYHO}	—	—	1.2	ms	
	LOCO clock oscillator operating		t_{SBYLO}	—	—	90	µs	
Recovery time after cancellation of software standby mode (flash memory, HOCO power not supplied) (SOFTCUT[2:0] bits = 111b)*1	Crystal resonator connected to main clock oscillator*2	Main clock oscillator operating	t_{SBYMC}	—	3	—	ms	Figure 5.72
		Main clock oscillator and PLL circuit operating	t_{SBYPC}	—	3.5	—	ms	
	External clock input to main clock oscillator	Main clock oscillator operating	t_{SBYEX}	100	—	—	µs	
		Main clock oscillator and PLL circuit operating	t_{SBYPE}	0.5	—	—	ms	
	Sub-clock oscillator operating		t_{SBYSC}	2*4	—	—	s	
	HOCO clock oscillator operating		t_{SBYHO}	—	—	1.2	ms	
	LOCO clock oscillator operating		t_{SBYLO}	—	—	10	ms	
Recovery time after cancellation of deep software standby mode			t_{DSBY}	—	—	8	ms	Figure 5.73
Wait time after cancellation of deep software standby mode			t_{DSBYWT}	—	—	0.8	ms	

Note 1. The recovery time varies depending on the state of each oscillator when the WAIT instruction is executed. The recovery time when multiple oscillators are operating varies depending on the operating state of the oscillators that are not selected as the system clock source, and depends on the time set in the wait control registers corresponding to the oscillators.
Note 2. The indicated value is measured for an 8 MHz crystal resonator.
Note 3. When RCR3.RTCEN = 1, the time will be the time set in the SOSCWTCR register minus 2 s.
Note 4. When RCR3.RTCEN = 1, the time will be the time set in the SOSCWTCR register minus 2 s and plus 31.25 ms.

Item				Symbol	Min.	Max.	Unit*1	Test Conditions
RSPI	Data input setup time	Master	2.7 V ≤ VCC ≤ 5.5 V	t_{SU}	10	—	ns	C = 30pF Figure 5.92 to Figure 5.97
			1.8 V ≤ VCC < 2.7 V		25	—		
			1.62 V ≤ VCC < 1.8 V		30	—		
		Slave			25 – t_{Pcyc}	—		
	Data input hold time	Master	PCLKB set to a division ratio other than divided by 2	t_H	t_{Pcyc}	—	ns	
			PCLKB set to divided by 2*2	t_{HF}	0	—		
		Slave		t_H	20 + 2 × t_{Pcyc}	—		
	SSL setup time	Master		t_{LEAD}	1	8	t_{SPcyc}	
		Slave			4	—	t_{Pcyc}	
	SSL hold time	Master		t_{LAG}	1	8	t_{SPcyc}	
		Slave			4	—	t_{Pcyc}	
	Data output delay time	Master	2.7 V ≤ VCC ≤ 5.5 V	t_{OD}	—	14	ns	
			1.8 V ≤ VCC < 2.7 V		—	20		
			1.62 V ≤ VCC < 1.8 V		—	25		
		Slave	2.7 V ≤ VCC ≤ 5.5 V		—	3 × t_{Pcyc} + 65		
			1.8 V ≤ VCC < 2.7 V		—	3 × tPcyc +85		
			1.62 V ≤ VCC < 1.8 V		—	3 × tPcyc +95		
	Data output hold time	Master		t_{OH}	0	—	ns	
		Slave			0	—		
	Successive transmission delay time	Master		t_{TD}	t_{SPcyc} + 2 × t_{Pcyc}	8 × t_{SPcyc} + 2 × t_{Pcyc}	ns	
		Slave			4 × t_{Pcyc}	—		
	MOSI and MISO rise/fall time	Output	2.7 V ≤ VCC ≤ 5.5 V	t_{Dr}, t_{Df}	—	10	ns	
			1.8 V ≤ VCC < 2.7 V		—	15		
			1.62 V ≤ VCC < 1.8 V		—	20		
		Input			—	1	µs	
	SSL rise/fall time	Output	2.7 V ≤ VCC ≤ 5.5 V	t_{SSLr}, t_{SSLf}	—	10	ns	
			1.8 V ≤ VCC < 2.7 V		—	15		
			1.62 V ≤ VCC < 1.8 V		—	20		
		Input			—	1	µs	
	Slave access time		2.7 V ≤ VCC ≤ 5.5 V	t_{SA}	—	6	t_{Pcyc}	C = 30pF Figure 5.96 and Figure 5.97
			1.8 V ≤ VCC < 2.7 V		—	7		
			1.62 V ≤ VCC < 1.8 V		—	7		
	Slave output release time		2.7 V ≤ VCC ≤ 5.5 V	t_{REL}	—	5	t_{Pcyc}	
			1.8 V ≤ VCC < 2.7 V		—	6		
			1.62 V ≤ VCC < 1.8 V		—	6		

Note 1. t_{Pcyc}: PCLK cycle
Note 2. Divided by 2 can be set only in packages with 768 Kbytes/1 Mbyte of flash memory or 144/145 pins.

Table 5.58 Timing of On-Chip Peripheral Modules (4)

Conditions: VCC = AVCC0 = 1.62 to 5.5 V, VSS = AVSS0 = VREFL = VREFL0 = 0 V, T_a = –40 to +105°C
When high-drive output is selected by the drive capacity register

Item			Symbol	Min.	Max.	Unit*1	Test Conditions
Simple SPI	SCK clock cycle output (master)		t_{SPcyc}	4	65536	t_{Pcyc}	C = 30 pF Figure 5.91
	SCK clock cycle input (slave)			6	65536		
	SCK input clock high pulse width		t_{SPCKWH}	0.4	0.6	t_{SPcyc}	
	SCK input clock low pulse width		t_{SPCKWL}	0.4	0.6	t_{SPcyc}	
	SCK output clock high pulse width	2.7 V ≤ VCC ≤ 5.5 V	t_{SPCKWH}	0.4	0.6	t_{SPcyc}	
		1.8 V ≤ VCC < 2.7 V		0.35	0.65		
		1.62 V ≤ VCC < 1.8 V		0.35	0.65		
	SCK output clock low pulse width	2.7 V ≤ VCC ≤ 5.5 V	t_{SPCKWL}	0.4	0.6	t_{SPcyc}	
		1.8 V ≤ VCC < 2.7 V		0.35	0.65		
		1.62 V ≤ VCC < 1.8 V		0.35	0.65		
	SCK clock rise/fall time		t_{SPCKr}, t_{SPCKf}	—	20	ns	
	Data input setup time (Master)	2.7 V ≤ VCC ≤ 5.5 V	t_{SU}	65	—	ns	C = 30 pF Figure 5.92 to Figure 5.97
		1.8 V ≤ VCC < 2.7 V		75	—		
		1.62 V ≤ VCC < 1.8 V		80	—		
	Data input setup time (Slave)			40	—		
	Data input hold time		t_H	40	—	ns	
	SS input setup time		t_{LEAD}	6	—	t_{Pcyc}	
	SS input hold time		t_{LAG}	6	—	t_{Pcyc}	
	Data output delay time (Master)		t_{OD}	—	40	ns	
	Data output delay time (Slave)	2.7 V ≤ VCC ≤ 5.5 V		—	65		
		1.8 V ≤ VCC < 2.7 V		—	85		
		1.62 V ≤ VCC < 1.8 V		—	95		
	Data output hold time		t_{OH}	–10	—	ns	
	Data rise/fall time		t_{Dr}, t_{Df}	—	20	ns	
	SS input rise/fall time		t_{SSLr}, t_{SSLf}	—	20	ns	
	Slave access time		t_{SA}	—	6	t_{Pcyc}	C = 30 pF Figure 5.96 and Figure 5.97
	Slave output release time		t_{REL}	—	6	t_{Pcyc}	

Note 1. t_{Pcyc}: PCLK cycle

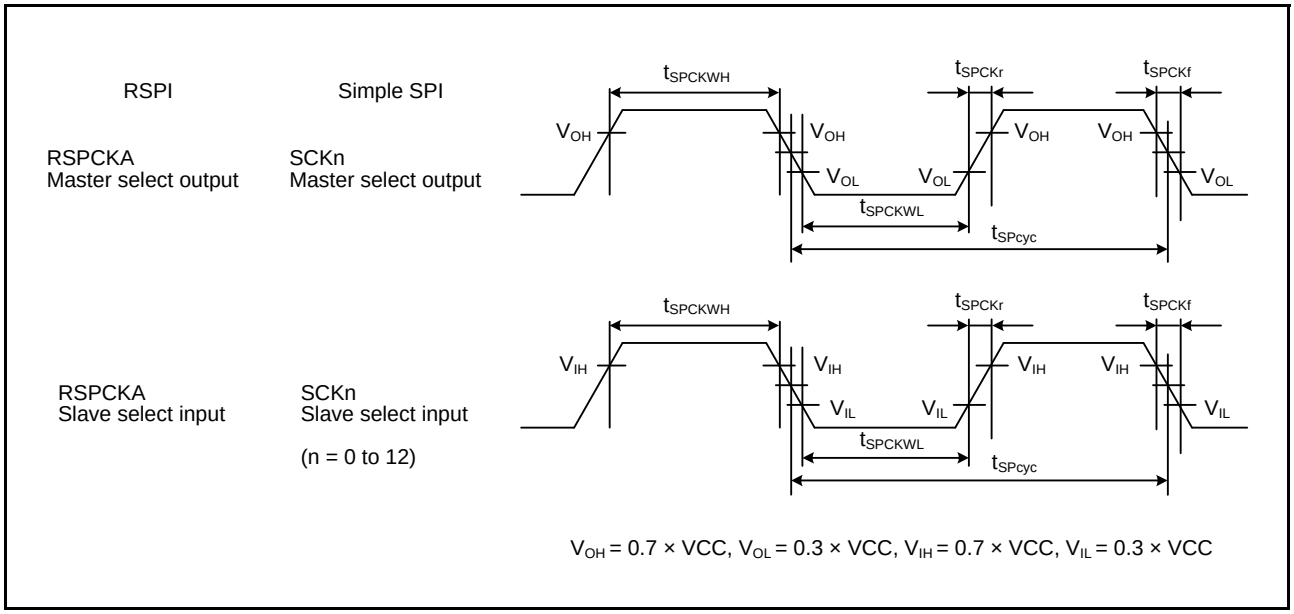
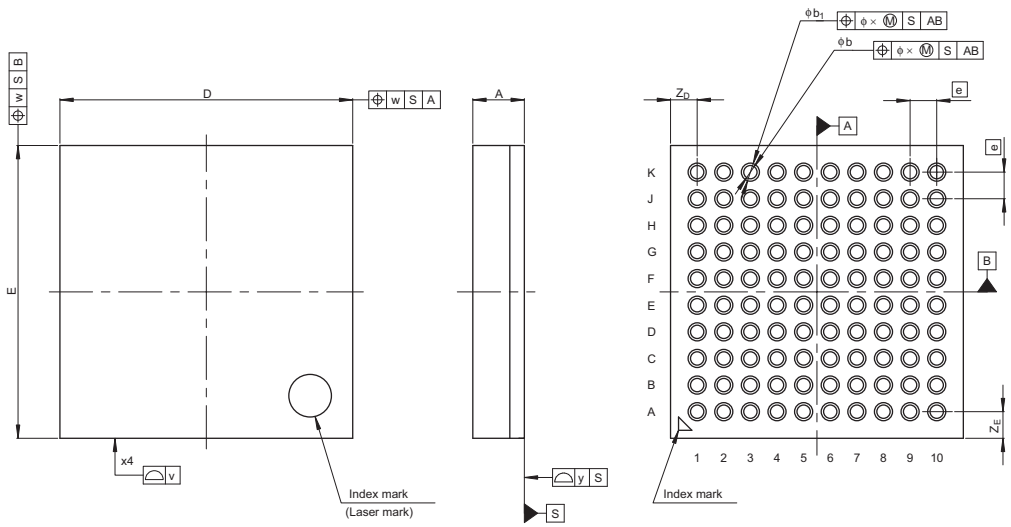


Figure 5.91 RSPI Clock Timing and Simple SPI Clock Timing

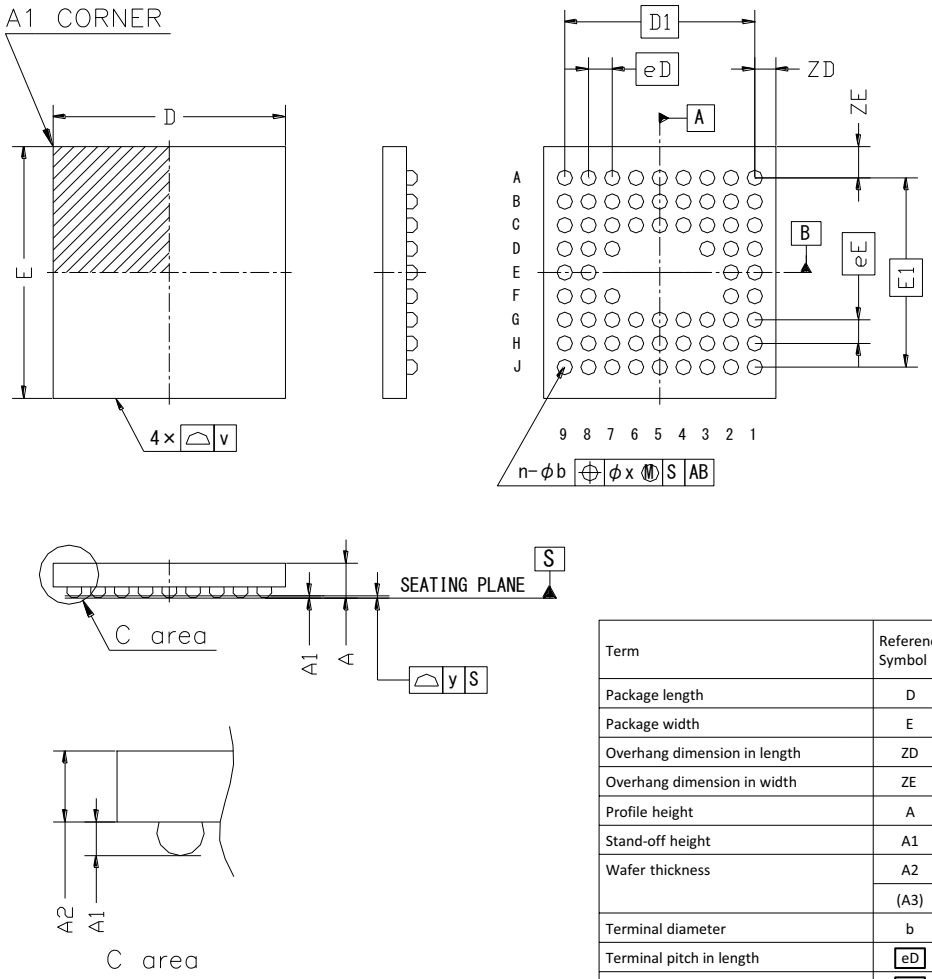
JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-TFLGA100-5.5x5.5-0.50	PTLG0100KA-A	100F0M	0.1g



Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	—	5.5	—
E	—	5.5	—
v	—	—	0.15
w	—	—	0.20
A	—	—	1.05
e	—	0.5	—
b	0.21	0.25	0.29
b_1	0.29	0.34	0.39
x	—	—	0.08
y	—	—	0.08
Z_D	—	0.5	—
Z_E	—	0.5	—

Figure D 100-Pin TFLGA (PTLG0100KA-A)

JEITA Package code	RENESAS Code	Previous Code	MASS(TYP.)[g]
S-WFBGA69-3.91x4.26-0.40	SWBG0069LA-A	—	0.02



注記:
1. 端子ﾋﾟｯﾁは端子中央部の位置で規定する。
2. ﾃﾞｰﾀﾑA及びBは、ﾎﾞｰﾙｸﾞﾘｯﾄﾞｾﾝﾀを称す。

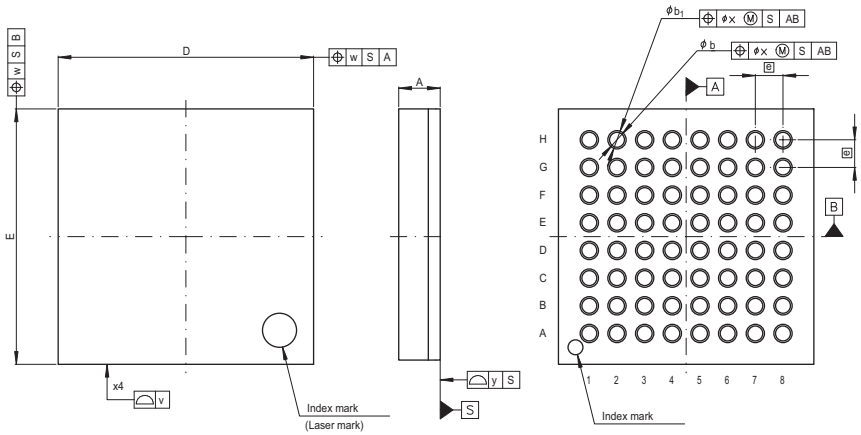
Note:
1. Ball pitch dimension is specified with the center of balls.
2. Datum A and B are axes defined by the ball grid array, not by the PKG outline.

Dimensions in millimeters

Term	Reference Symbol	Specification		
		Min	Nom	Max
Package length	D	3.86	3.91	3.96
Package width	E	4.21	4.26	4.31
Overhang dimension in length	ZD	0.305	0.355	0.405
Overhang dimension in width	ZE	0.48	0.53	0.58
Profile height	A	—	—	0.70
Stand-off height	A1	0.15	0.19	0.23
Wafer thickness	A2	0.36	0.40	0.44
	(A3)	—	—	—
Terminal diameter	b	0.22	0.27	0.32
Terminal pitch in length	eD		0.4	(BSC)
Terminal pitch in width	eE		0.4	(BSC)
Center terminal position in D-direction	SD		—	(BSC)
Center terminal position in E-direction	SE		—	(BSC)
Edge ball center to center in D-direction	D1		3.2	(BSC)
Edge ball center to center in D-direction	E1		3.2	(BSC)
Number of terminals	n		69	
Tolerance of package lateral profile	v		0.05	
Positional tolerance of terminals	x		0.05	
Coplanarity	y		0.08	

Figure E 69-Pin WLBGA (SWBG0069LA-A)

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-TFLGA64-6x6-0.65	PTLG0064JA-A	64F0G	0.07g



Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	—	6.0	—
E	—	6.0	—
v	—	—	0.15
w	—	—	0.20
A	—	—	1.05
e	—	0.65	—
b	0.31	0.35	0.39
b_1	0.39	0.43	0.47
x	—	—	0.08
y	—	—	0.10

Figure F 64-Pin TFLGA (PTLG0064JA-A)