Renesas Electronics America Inc - R5F52108CDFF#V0 Datasheet

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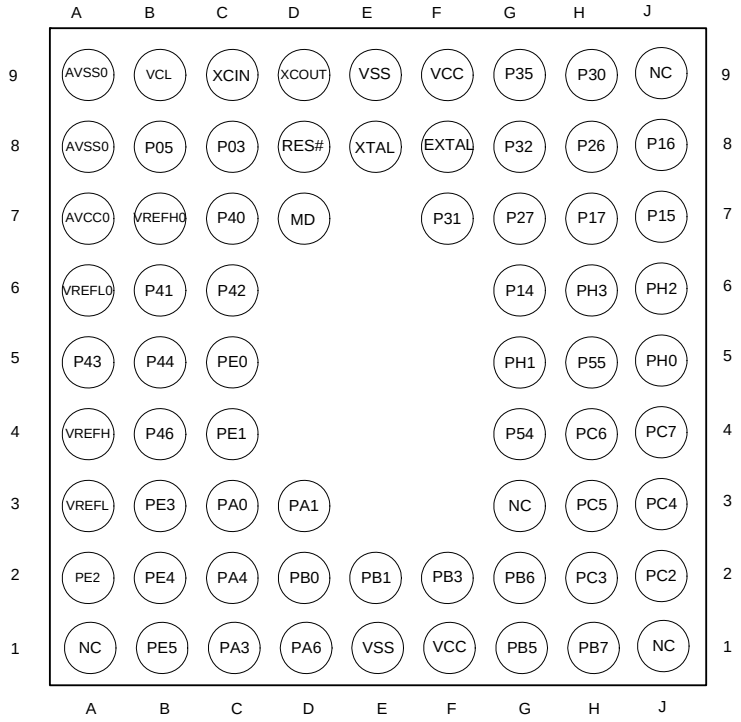
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	RX
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	I²C, SCI, SPI
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	64
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	8K x 8
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	1.62V ~ 5.5V
Data Converters	A/D 14x12b; D/A 2x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	80-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f52108cdff-v0

RX210 Group
SWBG0069LA-A
(69-pin WLBGA)
(Top view)



Note: • This figure indicates the power supply pins and I/O ports.
For the pin configuration, see the table “List of Pins and Pin Functions (69-Pin WLBGA)”.
Note: • For the position of A1 pin in the package, see “Package Dimensions”.
Note: • Leave the NC pin open.

Figure 1.8 Pin Assignments of the 69-Pin WLBGA

Table 1.17 List of Pins and Pin Functions (48-Pin LQFP) (2 / 2)

Pin No.	Power Supply, Clock, System Control	I/O Port	Timers (MTU, TMR, POE)	Communication (SCIc, SCId, RSPI, RIIC)	Others
44	VREFL0				
45		P40			AN000
46	VREFH0				
47	AVCC0				
48	AVSS0				

Note: • Pin names to which –DS is appended are for pins that can be used to trigger release from deep software standby mode.

Table 4.1 List of I/O Registers (Address Order) (16 / 29)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles: ICLK ≥ PCLK	Number of Access Cycles: ICLK < PCLK
0008 8896h	MTU5	Timer I/O control register V	TIORV	8	8	2, 3 PCLKB	2 ICLK
0008 88A0h	MTU5	Timer counter W	TCNTW	16	16	2, 3 PCLKB	2 ICLK
0008 88A2h	MTU5	Timer general register W	TGRW	16	16	2, 3 PCLKB	2 ICLK
0008 88A4h	MTU5	Timer control register W	TCRW	8	8	2, 3 PCLKB	2 ICLK
0008 88A6h	MTU5	Timer I/O control register W	TIORW	8	8	2, 3 PCLKB	2 ICLK
0008 88B2h	MTU5	Timer interrupt enable register	TIER	8	8	2, 3 PCLKB	2 ICLK
0008 88B4h	MTU5	Timer start register	TSTR	8	8	2, 3 PCLKB	2 ICLK
0008 88B6h	MTU5	Timer compare match clear register	TCNTCMPCLR	8	8	2, 3 PCLKB	2 ICLK
0008 8900h	POE	Input level control/status register 1	ICSR1	16	8, 16	2, 3 PCLKB	2 ICLK
0008 8902h	POE	Output level control/status register 1	OCSR1	16	8, 16	2, 3 PCLKB	2 ICLK
0008 8908h	POE	Input level control/status register 2	ICSR2	16	8, 16	2, 3 PCLKB	2 ICLK
0008 890Ah	POE	Software port output enable register	SPOER	8	8	2, 3 PCLKB	2 ICLK
0008 890Bh	POE	Port output enable control register 1	POECR1	8	8	2, 3 PCLKB	2 ICLK
0008 890Ch	POE	Port output enable control register 2	POECR2	8	8	2, 3 PCLKB	2 ICLK
0008 890Eh	POE	Input level control/status register 3	ICSR3	16	8, 16	2, 3 PCLKB	2 ICLK
0008 9000h	S12AD	A/D control register	ADCSR	16	16	2, 3 PCLKB	2 ICLK
0008 9004h	S12AD	A/D channel select register A	ADANSA	16	16	2, 3 PCLKB	2 ICLK
0008 9008h	S12AD	A/D-converted value addition mode select register	ADADS	16	16	2, 3 PCLKB	2 ICLK
0008 900Ch	S12AD	A/D-converted value addition count select register	ADADC	8	8	2, 3 PCLKB	2 ICLK
0008 900Eh	S12AD	A/D control extended register	ADCER	16	16	2, 3 PCLKB	2 ICLK
0008 9010h	S12AD	A/D start trigger select register	ADSTRGR	16	16	2, 3 PCLKB	2 ICLK
0008 9012h	S12AD	A/D converted extended input control register	ADEXICR	16	16	2, 3 PCLKB	2 ICLK
0008 9014h	S12AD	A/D channel select register B	ADANSB	16	16	2, 3 PCLKB	2 ICLK
0008 9018h	S12AD	A/D double register	ADDBLDR	16	16	2, 3 PCLKB	2 ICLK
0008 901Ah	S12AD	A/D temperature sensor data register	ADTSDR	16	16	2, 3 PCLKB	2 ICLK
0008 901Ch	S12AD	A/D internal reference voltage data register	ADOCDR	16	16	2, 3 PCLKB	2 ICLK
0008 901Eh	S12AD	A/D self-diagnosis data register	ADRD	16	16	2, 3 PCLKB	2 ICLK
0008 9020h	S12AD	A/D data register 0	ADDR0	16	16	2, 3 PCLKB	2 ICLK
0008 9022h	S12AD	A/D data register 1	ADDR1	16	16	2, 3 PCLKB	2 ICLK
0008 9024h	S12AD	A/D data register 2	ADDR2	16	16	2, 3 PCLKB	2 ICLK
0008 9026h	S12AD	A/D data register 3	ADDR3	16	16	2, 3 PCLKB	2 ICLK
0008 9028h	S12AD	A/D data register 4	ADDR4	16	16	2, 3 PCLKB	2 ICLK
0008 902Ah	S12AD	A/D data register 5	ADDR5	16	16	2, 3 PCLKB	2 ICLK
0008 902Ch	S12AD	A/D data register 6	ADDR6	16	16	2, 3 PCLKB	2 ICLK
0008 902Eh	S12AD	A/D data register 7	ADDR7	16	16	2, 3 PCLKB	2 ICLK
0008 9030h	S12AD	A/D data register 8	ADDR8	16	16	2, 3 PCLKB	2 ICLK
0008 9032h	S12AD	A/D data register 9	ADDR9	16	16	2, 3 PCLKB	2 ICLK
0008 9034h	S12AD	A/D data register 10	ADDR10	16	16	2, 3 PCLKB	2 ICLK
0008 9036h	S12AD	A/D data register 11	ADDR11	16	16	2, 3 PCLKB	2 ICLK
0008 9038h	S12AD	A/D data register 12	ADDR12	16	16	2, 3 PCLKB	2 ICLK
0008 903Ah	S12AD	A/D data register 13	ADDR13	16	16	2, 3 PCLKB	2 ICLK
0008 903Ch	S12AD	A/D data register 14	ADDR14	16	16	2, 3 PCLKB	2 ICLK
0008 903Eh	S12AD	A/D data register 15	ADDR15	16	16	2, 3 PCLKB	2 ICLK
0008 9060h	S12AD	A/D sampling state register 0	ADSSTR0	8	8	2, 3 PCLKB	2 ICLK
0008 9061h	S12AD	A/D sampling state register L	ADSSTRL	8	8	2, 3 PCLKB	2 ICLK
0008 9066h	S12AD	A/D sample and hold circuit register	ADSHCR	16	16	2, 3 PCLKB	2 ICLK
0008 9070h	S12AD	A/D sampling state register T	ADSSTRT	8	8	2, 3 PCLKB	2 ICLK
0008 9071h	S12AD	A/D sampling state register O	ADSSTRO	8	8	2, 3 PCLKB	2 ICLK
0008 9073h	S12AD	A/D sampling state register 1	ADSSTR1	8	8	2, 3 PCLKB	2 ICLK
0008 9074h	S12AD	A/D sampling state register 2	ADSSTR2	8	8	2, 3 PCLKB	2 ICLK
0008 9075h	S12AD	A/D sampling state register 3	ADSSTR3	8	8	2, 3 PCLKB	2 ICLK

Table 4.1 List of I/O Registers (Address Order) (19 / 29)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles: ICLK ≥ PCLK	Number of Access Cycles: ICLK < PCLK
0008 A0CDh	SCI6	SPI mode register	SPMR	8	8	2, 3 PCLKB	2 ICLK
0008 A0E0h	SCI7	Serial mode register	SMR	8	8	2, 3 PCLKB	2 ICLK
0008 A0E1h	SCI7	Bit rate register	BRR	8	8	2, 3 PCLKB	2 ICLK
0008 A0E2h	SCI7	Serial control register	SCR	8	8	2, 3 PCLKB	2 ICLK
0008 A0E3h	SCI7	Transmit data register	TDR	8	8	2, 3 PCLKB	2 ICLK
0008 A0E4h	SCI7	Serial status register	SSR	8	8	2, 3 PCLKB	2 ICLK
0008 A0E5h	SCI7	Receive data register	RDR	8	8	2, 3 PCLKB	2 ICLK
0008 A0E6h	SCI7	Smart card mode register	SCMR	8	8	2, 3 PCLKB	2 ICLK
0008 A0E7h	SCI7	Serial extended mode register	SEMR	8	8	2, 3 PCLKB	2 ICLK
0008 A0E8h	SCI7	Noise filter setting register	SNFR	8	8	2, 3 PCLKB	2 ICLK
0008 A0E9h	SCI7	I^2C mode register 1	SIMR1	8	8	2, 3 PCLKB	2 ICLK
0008 A0EAh	SCI7	I^2C mode register 2	SIMR2	8	8	2, 3 PCLKB	2 ICLK
0008 A0EBh	SCI7	I^2C mode register 3	SIMR3	8	8	2, 3 PCLKB	2 ICLK
0008 A0ECh	SCI7	I^2C status register	SISR	8	8	2, 3 PCLKB	2 ICLK
0008 A0EDh	SCI7	SPI mode register	SPMR	8	8	2, 3 PCLKB	2 ICLK
0008 A100h	SCI8	Serial mode register	SMR	8	8	2, 3 PCLKB	2 ICLK
0008 A101h	SCI8	Bit rate register	BRR	8	8	2, 3 PCLKB	2 ICLK
0008 A102h	SCI8	Serial control register	SCR	8	8	2, 3 PCLKB	2 ICLK
0008 A103h	SCI8	Transmit data register	TDR	8	8	2, 3 PCLKB	2 ICLK
0008 A104h	SCI8	Serial status register	SSR	8	8	2, 3 PCLKB	2 ICLK
0008 A105h	SCI8	Receive data register	RDR	8	8	2, 3 PCLKB	2 ICLK
0008 A106h	SCI8	Smart card mode register	SCMR	8	8	2, 3 PCLKB	2 ICLK
0008 A107h	SCI8	Serial extended mode register	SEMR	8	8	2, 3 PCLKB	2 ICLK
0008 A108h	SCI8	Noise filter setting register	SNFR	8	8	2, 3 PCLKB	2 ICLK
0008 A109h	SCI8	I^2C mode register 1	SIMR1	8	8	2, 3 PCLKB	2 ICLK
0008 A10Ah	SCI8	I^2C mode register 2	SIMR2	8	8	2, 3 PCLKB	2 ICLK
0008 A10Bh	SCI8	I^2C mode register 3	SIMR3	8	8	2, 3 PCLKB	2 ICLK
0008 A10Ch	SCI8	I^2C status register	SISR	8	8	2, 3 PCLKB	2 ICLK
0008 A10Dh	SCI8	SPI mode register	SPMR	8	8	2, 3 PCLKB	2 ICLK
0008 A120h	SCI9	Serial mode register	SMR	8	8	2, 3 PCLKB	2 ICLK
0008 A121h	SCI9	Bit rate register	BRR	8	8	2, 3 PCLKB	2 ICLK
0008 A122h	SCI9	Serial control register	SCR	8	8	2, 3 PCLKB	2 ICLK
0008 A123h	SCI9	Transmit data register	TDR	8	8	2, 3 PCLKB	2 ICLK
0008 A124h	SCI9	Serial status register	SSR	8	8	2, 3 PCLKB	2 ICLK
0008 A125h	SCI9	Receive data register	RDR	8	8	2, 3 PCLKB	2 ICLK
0008 A126h	SCI9	Smart card mode register	SCMR	8	8	2, 3 PCLKB	2 ICLK
0008 A127h	SCI9	Serial extended mode register	SEMR	8	8	2, 3 PCLKB	2 ICLK
0008 A128h	SCI9	Noise filter setting register	SNFR	8	8	2, 3 PCLKB	2 ICLK
0008 A129h	SCI9	I^2C mode register 1	SIMR1	8	8	2, 3 PCLKB	2 ICLK
0008 A12Ah	SCI9	I^2C mode register 2	SIMR2	8	8	2, 3 PCLKB	2 ICLK
0008 A12Bh	SCI9	I^2C mode register 3	SIMR3	8	8	2, 3 PCLKB	2 ICLK
0008 A12Ch	SCI9	I^2C status register	SISR	8	8	2, 3 PCLKB	2 ICLK
0008 A12Dh	SCI9	SPI mode register	SPMR	8	8	2, 3 PCLKB	2 ICLK
0008 A140h	SCI10	Serial mode register	SMR	8	8	2, 3 PCLKB	2 ICLK
0008 A141h	SCI10	Bit rate register	BRR	8	8	2, 3 PCLKB	2 ICLK
0008 A142h	SCI10	Serial control register	SCR	8	8	2, 3 PCLKB	2 ICLK
0008 A143h	SCI10	Transmit data register	TDR	8	8	2, 3 PCLKB	2 ICLK
0008 A144h	SCI10	Serial status register	SSR	8	8	2, 3 PCLKB	2 ICLK
0008 A145h	SCI10	Receive data register	RDR	8	8	2, 3 PCLKB	2 ICLK
0008 A146h	SCI10	Smart card mode register	SCMR	8	8	2, 3 PCLKB	2 ICLK
0008 A147h	SCI10	Serial extended mode register	SEMR	8	8	2, 3 PCLKB	2 ICLK

Table 5.4 DC Characteristics (3)

Conditions: VCC = AVCC0 = 1.62 to 5.5 V, VSS = AVSS0 = VREFL = VREFL0 = 0 V, T_a = –40 to +105°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Input leakage current	RES#, MD pin, P35/NMI	$\lvert I_{in} \rvert$	—	—	1.0	µA	V_{in} = 0 V, VCC
Three-state leakage current (off-state)	Port 4	$\lvert I_{TSI} \rvert$	—	—	1.0	µA	V_{in} = 0 V, VCC
	Other pins except for ports for 5 V tolerant and port 4		—	—	0.2		
	Ports for 5 V tolerant		—	—	1.0		V_{in} = 0 V, 5.8 V
Input capacitance	All input pins (except for ports 12, 13, 16, 17, 4, A1, A3, A4, and E)	C_{in}	—	—	15	pF	V_{in} = 0 V, f = 1 MHz, T_a = 25°C
	Ports 12, 13, 16, 17, 4, A1, A3, A4, and E		—	—	30		

Table 5.5 DC Characteristics (4)

Conditions: VCC = AVCC0 = 1.62 to 5.5 V, VSS = AVSS0 = VREFL = VREFL0 = 0 V, T_a = –40 to +105°C

Item		Symbol	VCC						Unit	Test Conditions
			1.62 to 2.7 V		2.7 to 4.0 V		4.0 to 5.5 V			
			Min.	Max.	Min.	Max.	Min.	Max.		
Input pull-up MOS current	All ports (except for port 35)	I_p	–150	–5	–200	–10	–400	–50	µA	V_{in} = 0 V

[Chip version A]

Table 5.6 DC Characteristics (5)

Conditions: VCC = AVCC0 = 2.7 to 5.5 V, VSS = AVSS0 = VREFL = VREFL0 = 0 V, T_a = –40 to +105°C

Item					Symbol	Typ.	Max.	Unit	Test Conditions
Supply current*1	High-speed operating mode	Normal operating mode	No peripheral operation*2	ICLK = 50 MHz	I_{CC}	10	—	mA	
			All peripheral operation: Normal*3	ICLK = 50 MHz		31.5	—		
			All peripheral operation: Max.*3	ICLK = 50 MHz		—	55		
		Sleep mode	No peripheral operation	ICLK = 50 MHz		7.5	—		
			All peripheral operation: Normal	ICLK = 50 MHz		17.5	—		
		All-module clock stop mode		ICLK = 50 MHz		6.7	—		
		Increase during BGO operation*4				25	—		

Note 1. Supply current values do not include output charge/discharge current from all pins. The values apply when internal pull-up MOSs are in the off state.

Note 2. Clock supply to the peripheral functions is stopped. This does not include BGO operation. The clock source is PLL and the VCO oscillation frequency is 100 MHz. BCLK, FCLK, and PCLK are set to divided by 64.

Note 3. Clocks are supplied to the peripheral functions. This does not include BGO operation. The clock source is PLL and the VCO oscillation frequency is 100 MHz. BCLK, FCLK, and PCLK are ICLK divided by 2.

Note 4. This is the increase if data is programmed to or erasing from the ROM or E2 DataFlash during program execution.

[Chip version B with 768 Kbytes/1 Mbyte of flash memory and 100 to 145 pins]

Table 5.15 DC Characteristics (14)

Conditions: VCC = AVCC0 = 2.7 to 5.5 V, VSS = AVSS0 = VREFL = VREFL0 = 0 V, T_a = –40 to +105°C

Item					Symbol	Typ.	Max.	Unit	Test Conditions
Supply current*1	High-speed operating mode	Normal operating mode	No peripheral operation*2	ICLK = 50 MHz	I_{CC}	7.8	—	mA	
			All peripheral operation: Normal*3	ICLK = 50 MHz		29.8	—		
			All peripheral operation: Max.*3	ICLK = 50 MHz		—	45		
		Sleep mode	No peripheral operation	ICLK = 50 MHz		4.3	—		
			All peripheral operation: Normal	ICLK = 50 MHz		13.5	—		
		All-module clock stop mode				3.7	—		
		Increase during BGO operation*4				23	—		

Note 1. Supply current values do not include output charge/discharge current from all pins. The values apply when internal pull-up MOSs are in the off state.

Note 2. Clock supply to the peripheral functions is stopped. This does not include BGO operation. The clock source is PLL and the VCO oscillation frequency is 100 MHz. BCLK, FCLK, and PCLK are set to divided by 64.

Note 3. Clocks are supplied to the peripheral functions. This does not include BGO operation. The clock source is PLL and the VCO oscillation frequency is 100 MHz. BCLK, FCLK, and PCLK are ICLK divided by 2.

Note 4. This is the increase if data is programmed to or erasing from the ROM or E2 DataFlash during program execution.

Item					Symbol	Typ.	Max.	Unit	Test Conditions
Supply current*1	Low-speed operating mode 1	Normal operating mode	No peripheral operation*7	ICLK = 8 MHz	I_{CC}	2.0	—	mA	
				ICLK = 4 MHz		1.6	—		
				ICLK = 2 MHz		1.5	—		
			All peripheral operation: Normal*8	ICLK = 8 MHz		6.4	—		
				ICLK = 4 MHz		4.0	—		
				ICLK = 2 MHz		2.8	—		
			All peripheral operation: Max.*8	ICLK = 8 MHz		—	12		
				ICLK = 4 MHz		—	—		
				ICLK = 2 MHz		—	—		
		Sleep mode	No peripheral operation	ICLK = 8 MHz		1.5	—		
				ICLK = 4 MHz		1.4	—		
				ICLK = 2 MHz		1.3	—		
			All peripheral operation: Normal	ICLK = 8 MHz		3.9	—		
				ICLK = 4 MHz		2.8	—		
				ICLK = 2 MHz		2.2	—		
		All-module clock stop mode		ICLK = 8 MHz		1.4	—		
				ICLK = 4 MHz		1.3	—		
				ICLK = 2 MHz		1.2	—		
	Low-speed operating mode 2	Normal operating mode	No peripheral operation*9	ICLK = 32 kHz		0.021	—		
			All peripheral operation: Normal*10	ICLK = 32 kHz		0.06	—		
			All peripheral operation: Max.*10	ICLK = 32 kHz		—	3*11		
		Sleep mode	No peripheral operation	ICLK = 32 kHz		0.017	—		
			All peripheral operation: Normal	ICLK = 32 kHz		0.035	—		
		All-module clock stop mode				0.016	—		

Note 1. Supply current values do not include output charge/discharge current from all pins. The values apply when internal pull-up MOSs are in the off state.
Note 2. Clock supply to the peripheral functions is stopped. This does not include BGO operation. The clock source is PLL and the VCO oscillation frequency is 64 MHz. BCLK, FCLK, and PCLK are set to divided by 64.
Note 3. Clock supply to the peripheral functions is stopped. This does not include BGO operation. The clock source is HOCO and the oscillation frequency is 40 MHz. BCLK, FCLK, and PCLK are set to divided by 64.
Note 4. Clocks are supplied to the peripheral functions. This does not include BGO operation. The clock source is PLL and the VCO oscillation frequency is 64 MHz. BCLK, FCLK, and PCLK are ICLK divided by 1.
Note 5. Clocks are supplied to the peripheral functions. This does not include BGO operation. The clock source is HOCO and the oscillation frequency is 40 MHz. BCLK, FCLK, and PCLK are ICLK divided by 1.
Note 6. This is the increase if data is programmed to or erasing from the ROM or E2 DataFlash during program execution.
Note 7. Clock supply to the peripheral functions is stopped. This does not include BGO operation. The clock source is HOCO and the oscillation frequency is 32 MHz. BCLK, FCLK, and PCLK are set to divided by 64.
Note 8. Clocks are supplied to the peripheral functions. This does not include BGO operation. The clock source is HOCO and the oscillation frequency is 32 MHz. BCLK, FCLK, and PCLK are ICLK divided by 1.
Note 9. Clock supply to the peripheral functions is stopped. This does not include BGO operation. The clock source is the sub oscillation circuit. BCLK, FCLK, and PCLK are set to divided by 64.
Note 10. Clocks are supplied to the peripheral functions. This does not include BGO operation. The clock source is the sub oscillation circuit. BCLK, FCLK, and PCLK are ICLK divided by 1.
Note 11. Value when the main clock continues oscillating at 12.5 MHz.

Table 5.27 Permissible Output Currents (2)

Conditions: VCC = AVCC0 = 1.62 to 5.5 V, VSS = AVSS0 = VREFL = VREFL0 = 0 V, when total power (mW) ≥ 1000 – 10 × Ta

Item			Symbol	Max.	Unit
Permissible output low current (average value per 1 pin)		Normal output mode	I_{OL}	2.0	mA
		High-drive output mode		4.0	
Permissible output low current (maximum value per 1 pin)		Normal output mode		2.0	mA
		High-drive output mode		4.0	
Permissible output low current (total)	Total of all output pins		ΣI_{OL}	40	mA
Permissible output high current (average value per 1 pin)		Normal output mode	I_{OH}	–2.0	mA
		High-drive output mode		–4.0	
Permissible output high current (maximum value per 1 pin)		Normal output mode		–2.0	mA
		High-drive output mode		–4.0	
Permissible output high current (total)	Total of all output pins		ΣI_{OH}	–40	mA

[Chip version A]

Table 5.28 Output Values of Voltage (1)

Conditions: VCC = AVCC0 = 1.62 to 2.7 V, VSS = AVSS0 = VREFL = VREFL0 = 0 V, T_a = –40 to +105°C

Item			Symbol	Min.	Max.	Unit	Test Conditions
Output low	All output pins (other than RIIC)	Normal output mode	V_{OL}	—	0.4	V	I_{OL} = 0.5 mA
		High-drive output mode		—	0.4		I_{OL} = 1.0 mA
Output high	All output pins	Normal output mode	V_{OH}	VCC – 0.4	—	V	I_{OH} = –0.5 mA
		High-drive output mode		VCC – 0.4	—		I_{OH} = –1.0 mA

[Chip version A]

Table 5.29 Output Values of Voltage (2)

Conditions: VCC = AVCC0 = 2.7 to 5.5 V, VSS = AVSS0 = VREFL = VREFL0 = 0 V, T_a = –40 to +105°C

Item			Symbol	Min.	Max.	Unit	Test Conditions	
							VCC = 2.7 to 4.0 V	VCC = 4.0 to 5.5 V
Output low	All output pins (other than RIIC)	Normal output mode	V_{OL}	—	1.0	V	I_{OL} = 3.0 mA	I_{OL} = 4.0 mA
		High-drive output mode		—	1.0		I_{OL} = 5.0 mA	I_{OL} = 8.0 mA
	RIIC pins			—	0.4		I_{OL} = 3.0 mA	
				—	0.6		I_{OL} = 6.0 mA	
Output high	All output pins	Normal output mode	V_{OH}	VCC – 1.0	—	V	I_{OH} = – 3.0 mA	I_{OH} = – 4.0 mA
		High-drive output mode		VCC – 1.0	—		I_{OH} = – 5.0 mA	I_{OH} = – 8.0 mA

[Chip versions B and C]

Table 5.30 Output Values of Voltage (3)

Conditions: VCC = AVCC0 = 1.62 to 2.7 V, VSS = AVSS0 = VREFL = VREFL0 = 0 V, T_a = –40 to +105°C

Item			Symbol	Min.	Max.	Unit	Test Conditions
Output low	All output pins (other than RIIC)	Normal output mode	V_{OL}	—	0.3	V	I_{OL} = 0.5 mA
		High-drive output mode		—	0.3		I_{OL} = 1.0 mA
Output high	All output pins	Normal output mode	V_{OH}	VCC – 0.3	—	V	I_{OH} = –0.5 mA
		High-drive output mode		VCC – 0.3	—		I_{OH} = –1.0 mA

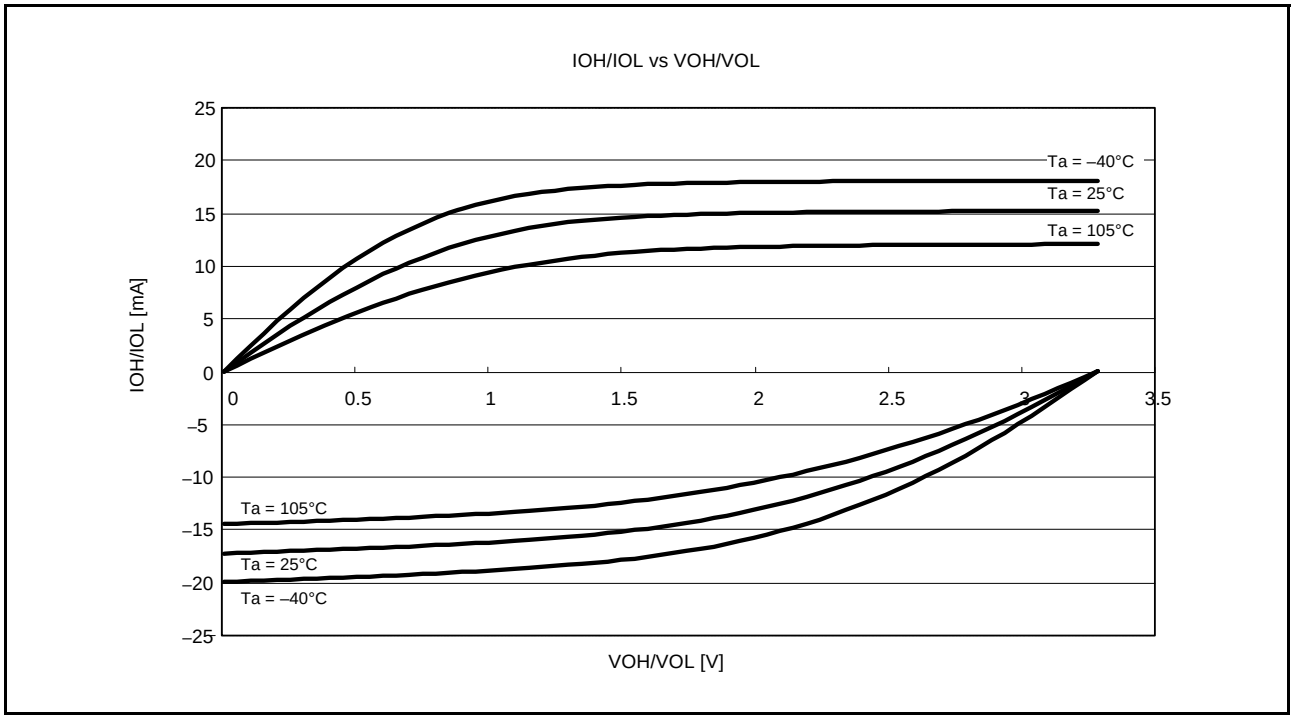


Figure 5.48 VOH/VOL and IOH/IOL Temperature Characteristics at VCC = 3.3 V when Normal Output is Selected (Reference Data)

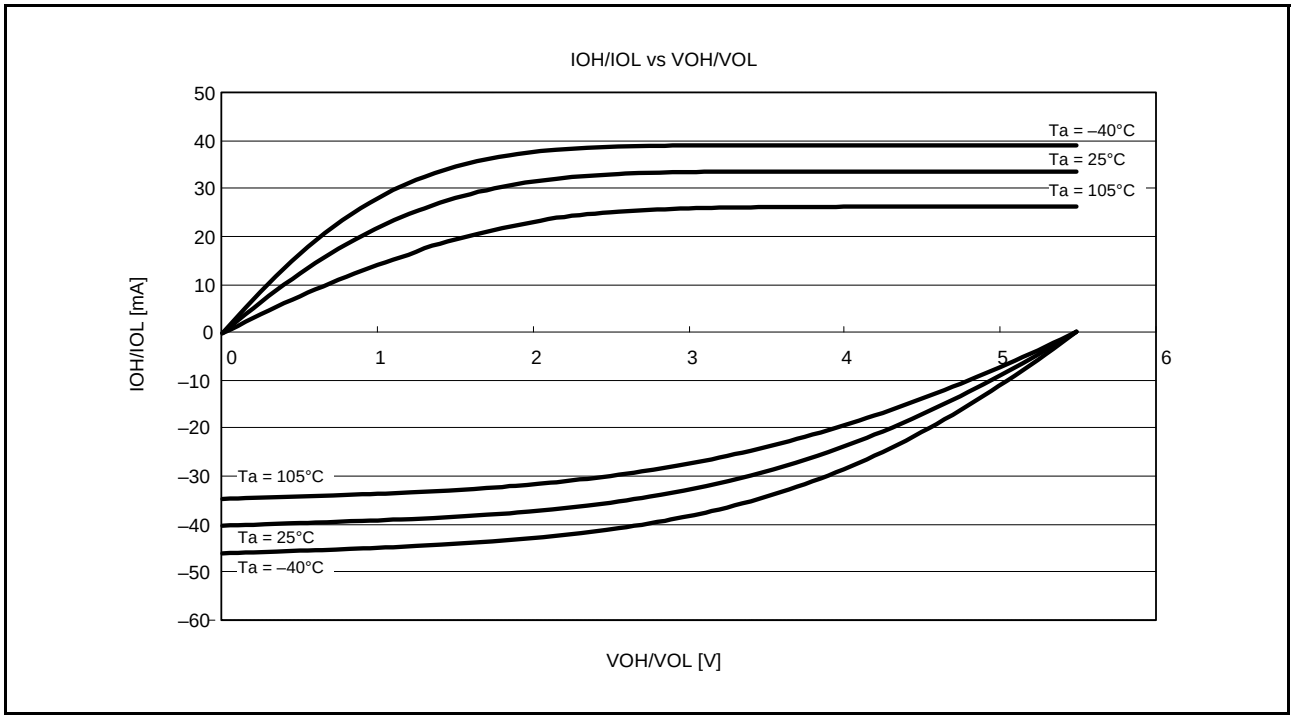


Figure 5.49 VOH/VOL and IOH/IOL Temperature Characteristics at VCC = 5.5 V when Normal Output is Selected (Reference Data)

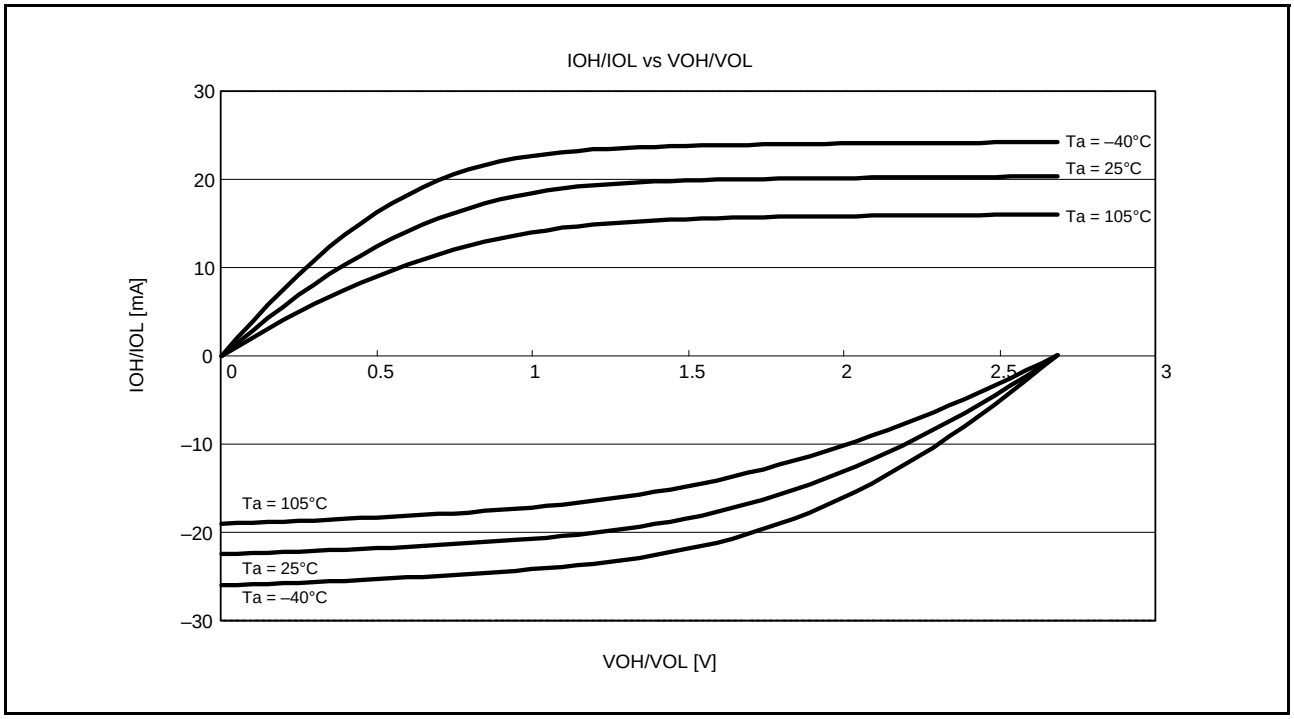


Figure 5.52 VOH/VOL and IOH/IOL Temperature Characteristics at VCC = 2.7 V when High-Drive Output is Selected (Reference Data)

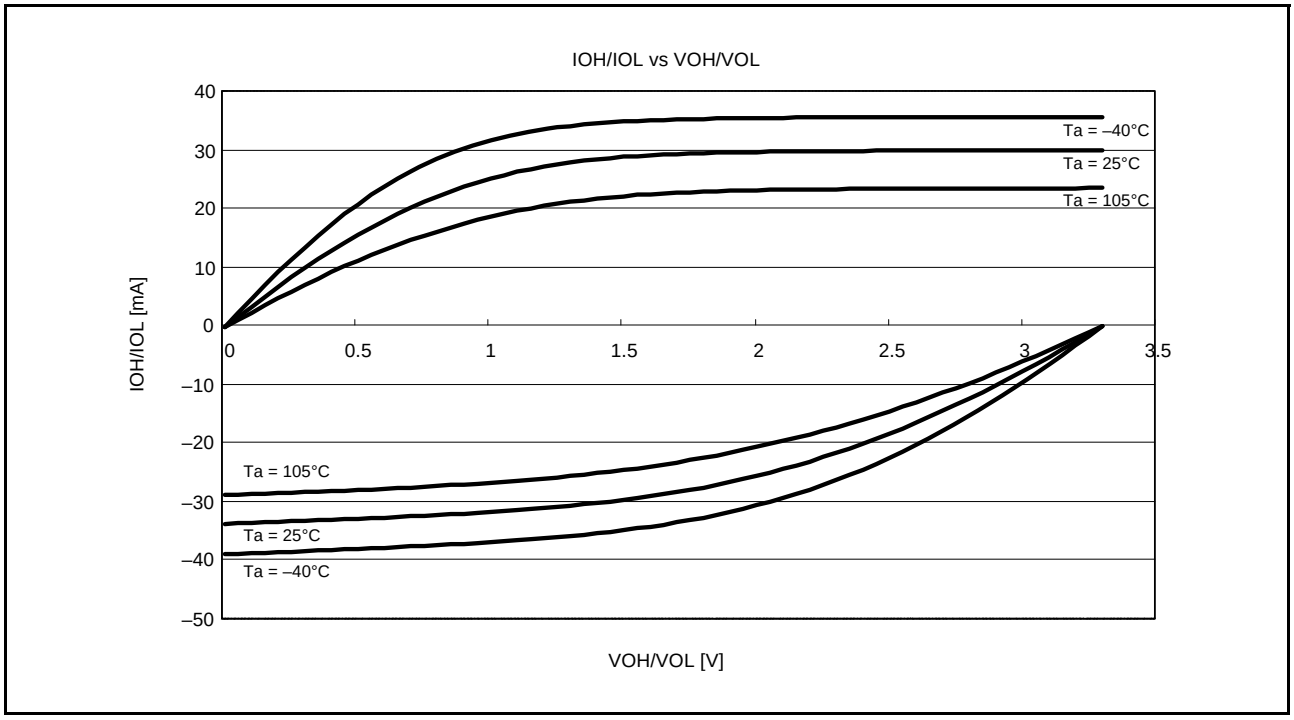


Figure 5.53 VOH/VOL and IOH/IOL Temperature Characteristics at VCC = 3.3 V when High-Drive Output is Selected (Reference Data)

[Chip version B]

Table 5.39 Operation Frequency Value (Low-Speed Operating Mode 1)

Conditions: VCC = AVCC0 = 1.62 to 5.5 V, VSS = AVSS0 = VREFL = VREFL0 = 0 V, T_a = –40 to +105°C

Item		Symbol	VCC			Unit
			1.62 to 1.8 V	1.8 to 2.7 V	2.7 to 5.5 V	
Maximum operating frequency	System clock (ICLK)	f_{max}	2	4	8	MHz
	FlashIF clock (FCLK)*1		2	4	8	
	Peripheral module clock (PCLKB)		2	4	8	
	Peripheral module clock (PCLKD)*2		2	4	8	
	External bus clock (BCLK)		2	4	8	
	BCLK pin output		2	4	8	

Note 1. Programming and erasing the flash memory is impossible.
Note 2. The lower-limit frequency of PCLKD is 1 MHz when the A/D converter is in use.

[Chip versions A, B, and C]

Table 5.40 Operation Frequency Value (Low-Speed Operating Mode 2)

Conditions: VCC = AVCC0 = 1.62 to 5.5 V, VSS = AVSS0 = VREFL=VREFL0 = 0 V, T_a = –40 to +105°C

Item		Symbol	VCC			Unit
			1.62 to 1.8 V	1.8 to 2.7 V	2.7 to 5.5 V	
Maximum operating frequency	System clock (ICLK)	f_{max}	32.768	32.768	32.768	kHz
	FlashIF clock (FCLK)*1		32.768	32.768	32.768	
	Peripheral module clock (PCLKB)		32.768	32.768	32.768	
	Peripheral module clock (PCLKD)*2		32.768	32.768	32.768	
	External bus clock (BCLK)		32.768	32.768	32.768	
	BCLK pin output		32.768	32.768	32.768	

Note 1. Programming and erasing the flash memory is impossible.
Note 2. The A/D converter cannot be used.

Table 5.44 Clock Timing

Conditions: VCC = AVCC0 = 1.62 to 5.5 V, VSS = AVSS0 = VREFL = VREFL0 = 0 V, T_a = –40 to +105°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
EXTAL external clock input cycle time		t_{EXcyc}	50	—	—	ns	Figure 5.60
EXTAL external clock input high pulse width		t_{EXH}	20	—	—	ns	
EXTAL external clock input low pulse width		t_{EXL}	20	—	—	ns	
EXTAL external clock rising time		t_{EXr}	—	—	5	ns	
EXTAL external clock falling time		t_{EXf}	—	—	5	ns	
EXTAL external clock input wait time*1		t_{EXWT}	1	—	—	ms	
Main clock oscillator oscillation frequency*2		f_{MAIN}	1	—	20	MHz	
Main clock oscillation stabilization time (crystal)*2		$t_{MAINOSC}$	—	3	—	ms	Figure 5.61
Main clock oscillation stabilization time (ceramic resonator)*2		$t_{MAINOSC}$	—	50		µs	
Main clock oscillation stabilization wait time (crystal)*2		$t_{MAINOSCWT}$	—	6	—	ms	
Main clock oscillation stabilization wait time (ceramic resonator)*2		$t_{MAINOSCWT}$	—	100		µs	
LOCO clock cycle time		t_{cyc}	7.27	8	8.89	µs	
LOCO clock oscillation frequency*6		f_{LOCO}	112.5	125	137.5	kHz	
LOCO clock oscillation stabilization wait time		t_{LOCOWT}	—	—	20	µs	Figure 5.62
HOCO clock oscillation frequency*7		f_{HOCO}	31.680	32	32.320	MHz	Ta = 0 to 50°C
			36.495	36.864	37.233		
			39.600	40	40.400		
			49.500	50	50.500		
			31.520	32	32.480		Ta = -40 to 105°C
			36.311	36.864	37.417		
			39.400	40	40.600		
			49.250	50	50.750		
HOCO clock oscillation stabilization time 1		t_{HOCO1}	—	—	300	µs	Figure 5.63
HOCO clock oscillation stabilization time 2		t_{HOCO2}	—	—	175	µs	Figure 5.64
HOCO clock oscillation stabilization wait time		t_{HOCOWT}	—	—	350	µs	Figure 5.64
HOCO clock power supply stabilization time		t_{HOCOP}	—	—	350	µs	Figure 5.65
PLL input frequency		f_{PLLIN}	4	—	12.5	MHz	
PLL circuit oscillation frequency		f_{PLL}	50	—	100	MHz	
PLL clock oscillation stabilization time	PLL operation started after main clock oscillation has settled	t_{PLL1}	—	—	500	µs	Figure 5.66
PLL clock oscillation stabilization wait time		t_{PLLWT1}	1.5	—	—	ms	
PLL clock oscillation stabilization time*4	PLL operation started before main clock oscillation has settled	t_{PLL2}	—	3.5*3	—	ms	Figure 5.67
PLL clock oscillation stabilization wait time*4		t_{PLLWT2}	—	7	—	ms	
PLL clock power supply stabilization time (for chip version B only)		t_{PLLPW}	—	—	30	µs	Figure 5.68
Sub-clock oscillator oscillation frequency		f_{SUB}	—	32.768	—	kHz	
Sub-clock oscillation stabilization time*5		t_{SUBOSC}	2	—	—	s	Figure 5.69
Sub-clock oscillation stabilization wait time*5		$t_{SUBOSCWT}$	4	—	—	s	

Note 1. The time interval from the time P36 and P37 are configured for input and the main clock oscillator stopping bit (MOSCCR.MOSTP) is set to 0 (operating) until the clock becomes available.

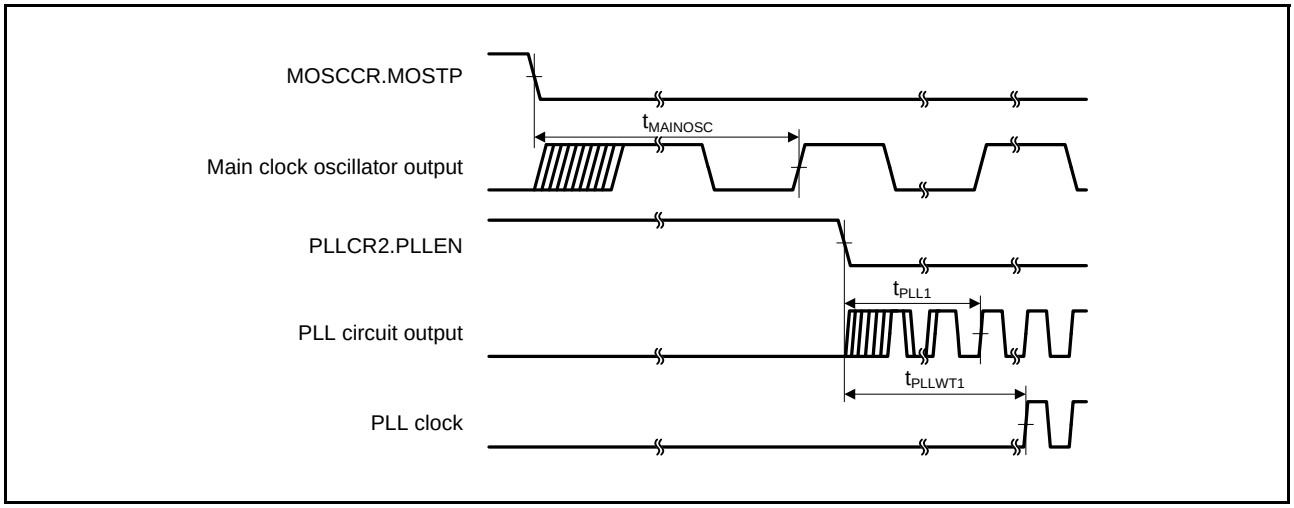


Figure 5.66 PLL Clock Oscillation Start Timing (PLL is Operated after Main Clock Oscillation Has Settled)

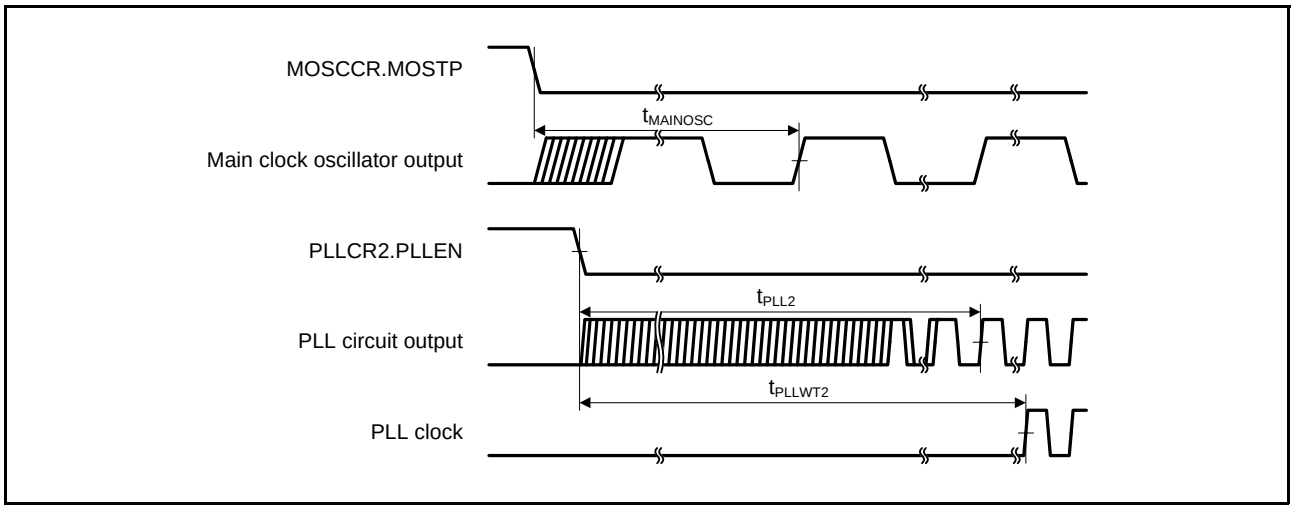


Figure 5.67 PLL Clock Oscillation Start Timing (PLL is Operated before Main Clock Oscillation Has Settled)

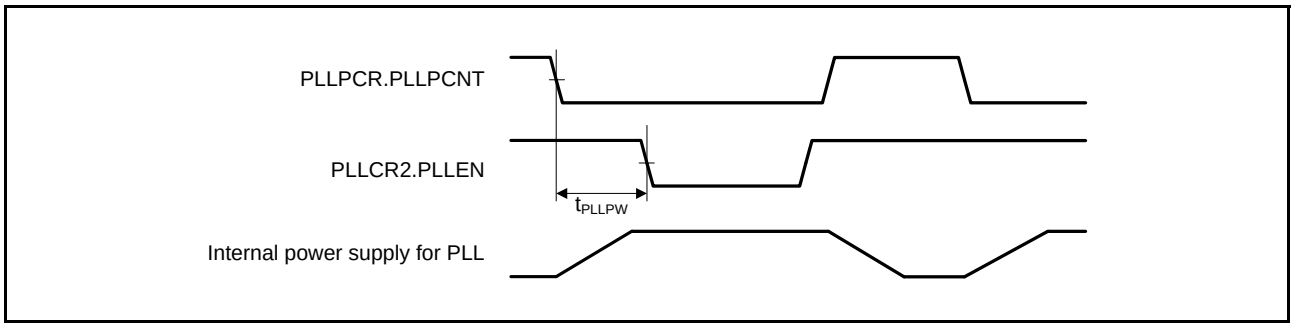


Figure 5.68 PLL Power Control Timing

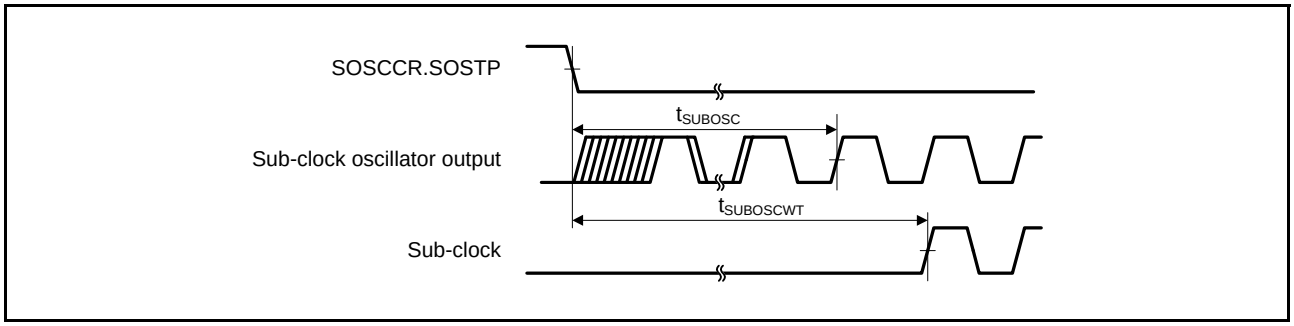


Figure 5.69 Sub-clock Oscillation Start Timing

Table 5.58 Timing of On-Chip Peripheral Modules (4)

Conditions: VCC = AVCC0 = 1.62 to 5.5 V, VSS = AVSS0 = VREFL = VREFL0 = 0 V, T_a = –40 to +105°C
When high-drive output is selected by the drive capacity register

Item			Symbol	Min.	Max.	Unit*1	Test Conditions
Simple SPI	SCK clock cycle output (master)		t_{SPcyc}	4	65536	t_{Pcyc}	C = 30 pF Figure 5.91
	SCK clock cycle input (slave)			6	65536		
	SCK input clock high pulse width		t_{SPCKWH}	0.4	0.6	t_{SPcyc}	
	SCK input clock low pulse width		t_{SPCKWL}	0.4	0.6	t_{SPcyc}	
	SCK output clock high pulse width	2.7 V ≤ VCC ≤ 5.5 V	t_{SPCKWH}	0.4	0.6	t_{SPcyc}	
		1.8 V ≤ VCC < 2.7 V		0.35	0.65		
		1.62 V ≤ VCC < 1.8 V		0.35	0.65		
	SCK output clock low pulse width	2.7 V ≤ VCC ≤ 5.5 V	t_{SPCKWL}	0.4	0.6	t_{SPcyc}	
		1.8 V ≤ VCC < 2.7 V		0.35	0.65		
		1.62 V ≤ VCC < 1.8 V		0.35	0.65		
	SCK clock rise/fall time		t_{SPCKr}, t_{SPCKf}	—	20	ns	
	Data input setup time (Master)	2.7 V ≤ VCC ≤ 5.5 V	t_{SU}	65	—	ns	C = 30 pF Figure 5.92 to Figure 5.97
		1.8 V ≤ VCC < 2.7 V		75	—		
		1.62 V ≤ VCC < 1.8 V		80	—		
	Data input setup time (Slave)			40	—		
	Data input hold time		t_H	40	—	ns	
	SS input setup time		t_{LEAD}	6	—	t_{Pcyc}	
	SS input hold time		t_{LAG}	6	—	t_{Pcyc}	
	Data output delay time (Master)		t_{OD}	—	40	ns	
	Data output delay time (Slave)	2.7 V ≤ VCC ≤ 5.5 V		—	65		
		1.8 V ≤ VCC < 2.7 V		—	85		
		1.62 V ≤ VCC < 1.8 V		—	95		
	Data output hold time		t_{OH}	–10	—	ns	
	Data rise/fall time		t_{Dr}, t_{Df}	—	20	ns	
	SS input rise/fall time		t_{SSLr}, t_{SSLf}	—	20	ns	
	Slave access time		t_{SA}	—	6	t_{Pcyc}	C = 30 pF Figure 5.96 and Figure 5.97
	Slave output release time		t_{REL}	—	6	t_{Pcyc}	

Note 1. t_{Pcyc}: PCLK cycle

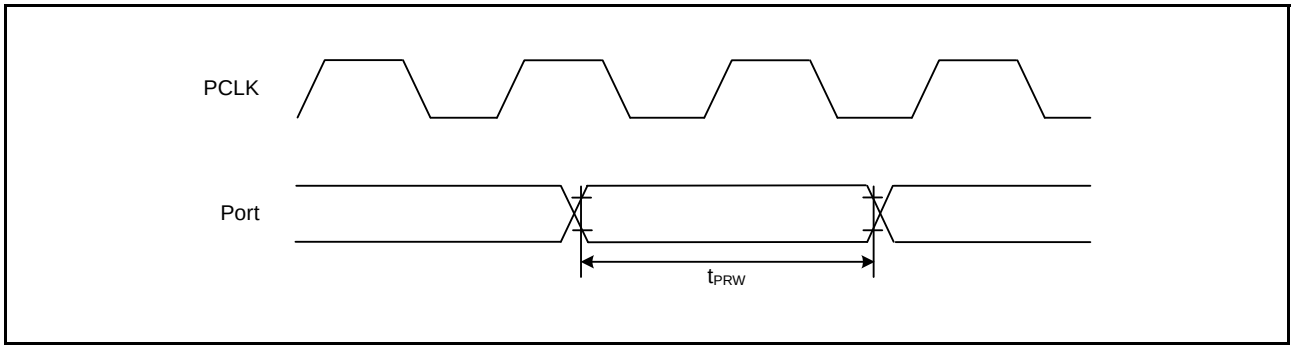


Figure 5.83 I/O Port Input Timing

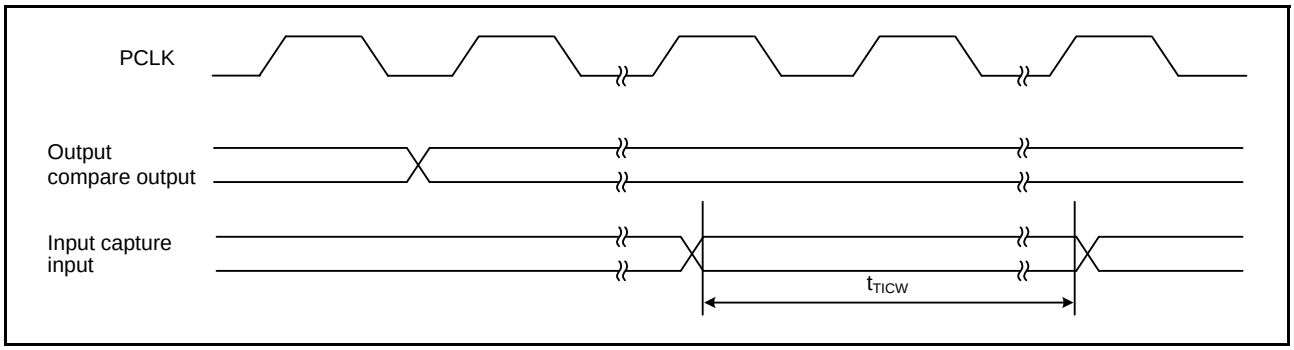


Figure 5.84 MTU/TPU Input/Output Timing

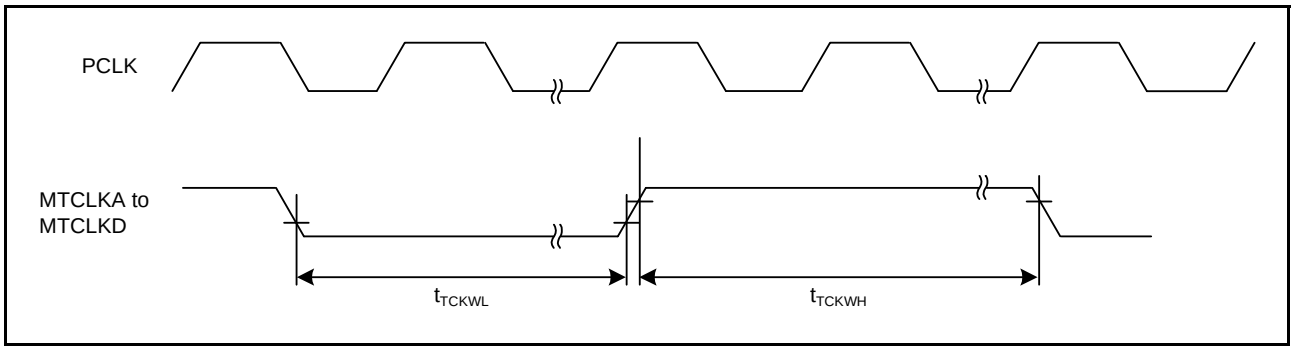


Figure 5.85 MTU/TPU Clock Input Timing

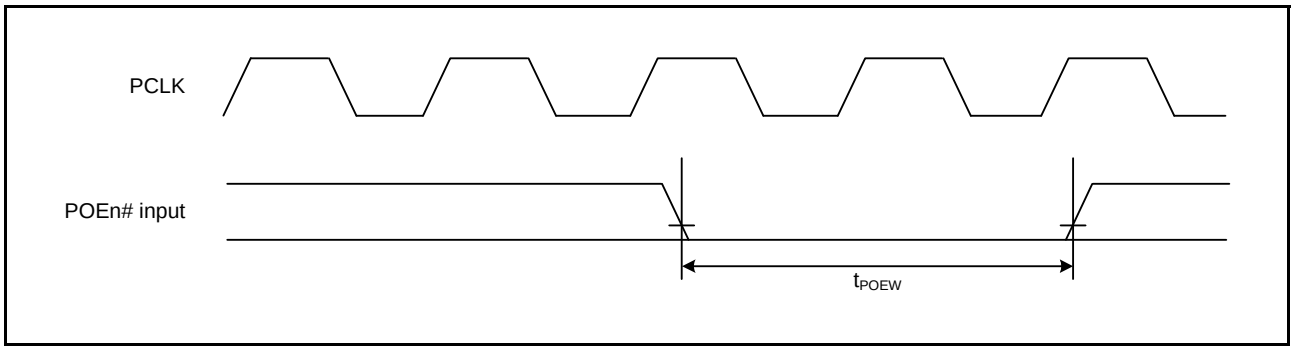


Figure 5.86 POE# Input Timing

[Chip versions A and C]

Table 5.77 ROM (Flash Memory for Code Storage) Characteristics (4) : middle-speed operating mode 1B

Conditions: VCC = AVCC0 = 1.62 to 3.6 V, VREFH = VREFH0 = AVCC0, VSS = AVSS0 = VREFL = VREFL0 = 0 V
Temperature range for the programming/erasure operation: T_a = –40 to +105°C

Item		Symbol	FCLK = 4 MHz			FCLK = 32 MHz*1			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Programming time when N_{PEC} ≤ 100 times	2 bytes	t_{P2}	—	0.69	6.0	—	0.30	3.5	ms
	8 bytes	t_{P8}	—	0.69	6.0	—	0.30	3.5	
	128 bytes	t_{P128}	—	1.76	14.2	—	0.85	8.3	
Programming time when N_{PEC} > 100 times	2 bytes	t_{P2}	—	0.81	7.1	—	0.35	4.2	ms
	8 bytes	t_{P8}	—	0.81	7.6	—	0.35	4.5	
	128 bytes	t_{P128}	—	1.99	17.5	—	0.96	10	
Erasure time when N_{PEC} ≤ 100 times	2 Kbytes	t_{E2K}	—	24.5	113.7	—	19.0	46	ms
Erasure time when N_{PEC} > 100 times	2 Kbytes	t_{E2K}	—	29.8	225.8	—	23.2	90 (1000 times ≥ N_{PEC} > 100 times), 98 (10000 times ≥ N_{PEC} > 1000 times)	ms
Suspend delay time during programming (in programming/erasure priority mode)		t_{SPD}	—	—	1.7	—	—	1.6	ms
First suspend delay time during programming (in suspend priority mode)		t_{SPSD1}	—	—	220	—	—	120	µs
Second suspend delay time during programming (in suspend priority mode)		t_{SPSD2}	—	—	1.7	—	—	1.6	ms
Suspend delay time during erasing (in programming/erasure priority mode)		t_{SED}	—	—	1.7	—	—	1.6	ms
First suspend delay time during erasing (in suspend priority mode)		t_{SESD1}	—	—	220	—	—	120	µs
Second suspend delay time during erasing (in suspend priority mode)		t_{SESD2}	—	—	1.7	—	—	1.6	ms
FCU reset time		t_{FCUR}	20 µs or longer and FCLK × 6 or greater	—	—	20 µs or longer and FCLK × 6 or greater	—	—	µs

Note 1. The operating frequency is 20 MHz (max.) when the voltage is in the range from 1.62 V to less than 1.8 V.

5.11 E2 DataFlash Characteristics

[Chip version A]

Table 5.80 E2 DataFlash Characteristics (1)

Item	Symbol	Min.	Typ.	Max.	Unit	Conditions
Reprogramming/erasure cycle*1	N_{DPEC}	100000	—	—	Times	
Data hold time	t_{DRP}	10*2	—	—	Year	

Note 1. The reprogram/erase cycle is the number of erasing for each block. When the reprogram/erase cycle is n times (n = 100000), erasing can be performed n times for each block. For instance, when 8-byte programming is performed 16 times for different addresses in 128-byte block and then the entire block is erased, the reprogram/erase cycle is counted as one. However, programming the same address for several times as one erasing is not enabled (overwriting is prohibited).

Note 2. This result is obtained from reliability testing.

[Chip versions B and C]

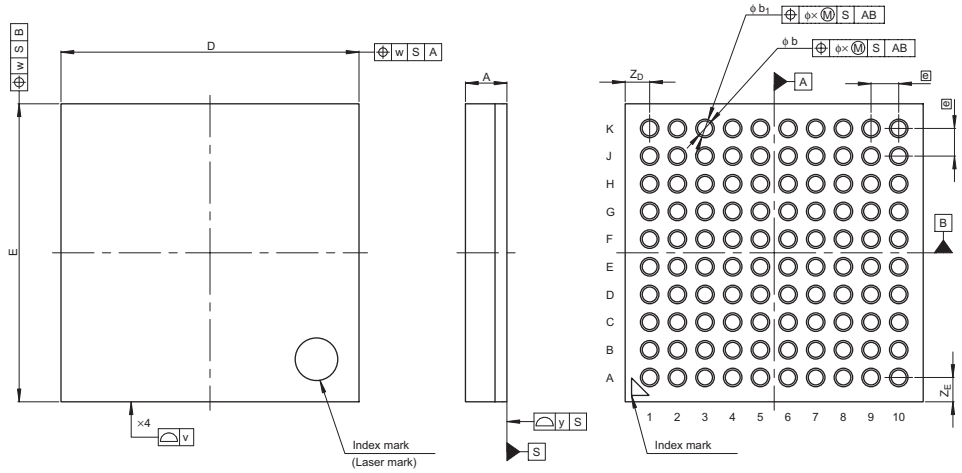
Table 5.81 E2 DataFlash Characteristics (2)

Item		Symbol	Min.	Typ.	Max.	Unit	Conditions
Reprogramming/erasure cycle*1		N_{DPEC}	100000	—	—	Times	
Data hold time	After 100000 times of N_{DPEC}	t_{DRP}	30*2	—	—	Year	Ta = +85°C

Note 1. The reprogram/erase cycle is the number of erasing for each block. When the reprogram/erase cycle is n times (n = 100000), erasing can be performed n times for each block. For instance, when 8-byte programming is performed 16 times for different addresses in 128-byte block and then the entire block is erased, the reprogram/erase cycle is counted as one. However, programming the same address for several times as one erasing is not enabled (overwriting is prohibited).

Note 2. This result is obtained from reliability testing.

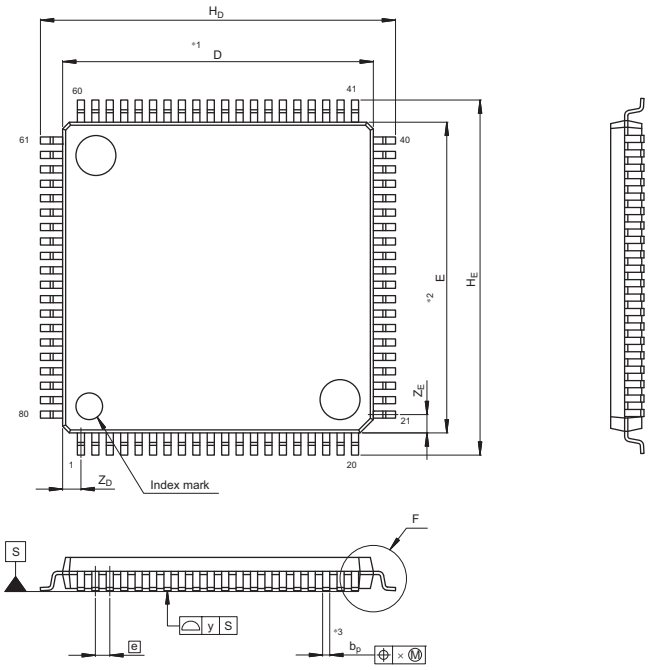
JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-TFLGA100-7x7-0.65	PTLG0100JA-A	100F0G	0.1g

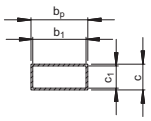


Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	—	7.0	—
E	—	7.0	—
v	—	—	0.15
w	—	—	0.20
A	—	—	1.05
e	—	0.65	—
b	0.31	0.35	0.39
b_1	0.385	0.435	0.485
x	—	—	0.08
y	—	—	0.10
Z_D	—	0.575	—
Z_E	—	0.575	—

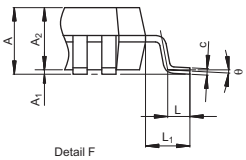
Figure C 100-Pin TFLGA (PTLG0100JA-A)

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LQFP80-14x14-0.65	PLQP0080JA-A	FP-80W / FP-80WV	0.6g





Terminal cross section



Detail F

NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	13.9	14.0	14.1
E	13.9	14.0	14.1
A_2	—	1.4	—
H_D	15.8	16.0	16.2
H_E	15.8	16.0	16.2
A	—	—	1.7
A_1	0.05	0.1	0.15
b_p	0.27	0.32	0.37
b_1	—	0.30	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	8°
e	—	0.65	—
x	—	—	0.13
y	—	—	0.10
Z_D	—	0.825	—
Z_E	—	0.825	—
L	0.35	0.5	0.65
L_1	—	1.0	—

Figure I 80-Pin LQFP (PLQP0080JA-A)