Renesas Electronics America Inc - R5F52108CDFM#30 Datasheet

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Discontinued at Digi-Key
Core Processor	RX
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	I²C, SCI, SPI
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	48
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	8K x 8
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	1.62V ~ 5.5V
Data Converters	A/D 12x12b; D/A 2x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LFQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f52108cdfm-30

1.Overview

1.1 Outline of Specifications

Table 1.1 lists the specifications in outline, and Table 1.2 gives a comparison of the functions of products in different packages.
Table 1.1 is for products with the greatest number of functions, so numbers of peripheral modules and channels will differ in accord with the package. For details, see Table 1.2, Comparison of Functions for Different Packages.
This product includes chip version A (part no.: R5F5210xAxxx), chip version B (part no.: R5F5210xBxxx), and chip version C (part no: R5F5210xCxxx).
For the specification differences between chip versions A, B, and C, see Table 1, Specification Differences Depending on Chip Versions.

Table 1.1 Outline of Specifications (1 / 5)

Classification	Module/Function	Description
CPU	CPU	• Maximum operating frequency: 50 MHz • 32-bit RX CPU • Minimum instruction execution time: One instruction per state (cycle of the system clock) • Address space: 4-Gbyte linear • Register General purpose: Sixteen 32-bit registers Control: Eight 32-bit registers Accumulator: One 64-bit register • Basic instructions: 73 • DSP instructions: 9 • Addressing modes: 10 • Data arrangement Instructions: Little endian Data: Selectable as little endian or big endian • On-chip 32-bit multiplier: 32 × 32 → 64 bits • On-chip divider: 32 / 32 → 32 bits • Barrel shifter: 32 bits
Memory	ROM	• Capacity: 64 K/96 K/128 K/256 K/384 K/512 K/768 Kbytes/1 Mbyte • 50 MHz, no-wait memory access • On-board programming: 3 types Off-board programming
	RAM	• Capacity: 12 K/16 K/20 K/32 K/64 K/96 Kbytes • 50 MHz, no-wait memory access
	E2 DataFlash	• Capacity: 8 Kbytes • Number of times for programming/erasing: 100,000
MCU operating mode		Single-chip mode, on-chip ROM enabled expansion mode, and on-chip ROM disabled expansion mode (software switching)
Clock	Clock generation circuit	• Main clock oscillator, sub-clock oscillator, low-speed on-chip oscillator, high-speed on-chip oscillator, PLL frequency synthesizer, and IWDT-dedicated on-chip oscillator • Oscillation stop detection • Measuring circuit for accuracy of clock frequency (clock-accuracy check: CAC) • Independent settings for the system clock (ICLK), peripheral module clock (PCLK), external bus clock (BCLK), and FlashIF clock (FCLK) The CPU and system sections such as other bus masters run in synchronization with the system clock (ICLK): 50 MHz (at max.) Peripheral modules run in synchronization with the peripheral module clock (PCLK): 32 MHz (at max.) Devices connected to the external bus run in synchronization with the external bus clock (BCLK): 12.5 MHz (at max.) The flash peripheral circuit runs in synchronization with the FlashIF clock (FCLK): 32 MHz (at max.)
Reset		RES# pin reset, power-on reset, voltage monitoring reset, watchdog timer reset, independent watchdog timer reset, deep software standby reset, and software reset
Voltage detection	Voltage detection circuit (LVDAa)	• When the voltage on VCC falls below the voltage detection level, an internal reset or internal interrupt is generated. Voltage detection circuit 0 is capable of selecting the detection voltage from 4 levels Voltage detection circuit 1 is capable of selecting the detection voltage from 16 levels Voltage detection circuit 2 is capable of selecting the detection voltage from 16 levels

Table 1.2 Comparison of Functions for Different Packages

Module/Functions		RX210 Group				
		144, 145 Pins	**100 Pins**	**80 Pins**	**64, 69 Pins**	**48 Pins**
External bus	External bus width	16 bits		Not supported		
Interrupt	External interrupts	NMI, IRQ0 to IRQ7			NMI, IRQ0 to IRQ2, IRQ4 to IRQ7	NMI, IRQ0, IRQ1, IRQ4 to IRQ7
DMA	DMA controller	4 channels (DMAC0 to DMAC3)				
	Data transfer controller	Supported				
Timers	16-bit timer pulse unit	6 channels (TPU0 to TPU5)	Not supported			
	Multi-function timer pulse unit 2	6 channels (MTU0 to MTU5)				
	Port output enable 2	POE0# to POE3#, POE8#				
	8-bit timer	2 channels × 2 units				
	Compare match timer	2 channels × 2 units				
	Realtime clock	Supported				Not supported
	Watchdog timer	Supported				
	Independent watchdog timer	Supported				
Communication functions	Serial communications interface (SCIc)	12 channels (SCI0 to 11)	6 channels (SCI0, 1, 5, 6, 8, 9)		5 channels (SCI1, 5, 6, 8, 9)	4 channels (SCI1, 5, 6, 8)
	Serial communications interface (SCId)	1 channel (SCI12)				
	I^2C bus interface	1 channel				
	Serial peripheral interface	1 channel				
12-bit A/D converter		16 channels (AN000 to AN015)		14 channels (AN000 to AN013)	12 channels (AN000 to AN004, AN006, AN008 to AN013)	8 channels (AN000 to AN002, AN006, AN009 to AN012)
Temperature sensor		Supported				
D/A converter		2 channels				Not supported
CRC calculator		Supported				
Event link controller		Supported				
Comparator A		2 channels				
Comparator B		2 channels				
Packages		145-pin TFLGA 144-pin LQFP	100-pin TFLGA 100-pin LQFP	80-pin LQFP	69-pin WLBGA 64-pin TFLGA 64-pin LQFP	48-pin LQFP

Table 1.8 Pin Functions (3 / 4)

Classifications	Pin Name	I/O	Description
Serial communications interface (SCId)	• Asynchronous mode/clock synchronous mode		
	SCK12	I/O	Input/output pin for the clock
	RXD12	Input	Input pin for received data
	TXD12	Output	Output pin for transmitted data
	CTS12#	Input	Input pin for controlling the start of transmission and reception
	RTS12#	Output	Output pin for controlling the start of transmission and reception
	• Simple I^2C mode		
	SSCL12	I/O	Input/output pin for the I^2C clock
	SSDA12	I/O	Input/output pin for the I^2C data
	• Simple SPI mode		
	SCK12	I/O	Input/output pin for the clock
	SMISO12	I/O	Input/output pin for slave transmit data
	SMOSI12	I/O	Input/output pin for master transmit data
	SS12#	Input	Chip-select input pin
	• Extended serial mode		
	RXDX12	Input	Input pin for data reception by SCId
	TXDX12	Output	Output pin for data transmission by SCId
	SIOX12	I/O	Input/output pin for data reception or transmission by SCId
I^2C bus interface	SCL	I/O	Input/output pin for I^2C bus interface clocks. Bus can be directly driven by the N-channel open-drain output.
	SDA	I/O	Input/output pin for I^2C bus interface data. Bus can be directly driven by the N-channel open-drain output.
Serial peripheral interface	RSPCKA	I/O	Clock input/output pin for the RSPI.
	MOSIA	I/O	Input or output data output from the master for the RSPI.
	MISOA	I/O	Input or output data output from the slave for the RSPI.
	SSLA0	I/O	Input/output pin to select the slave for the RSPI.
	SSLA1 to SSLA3	Output	Output pins to select the slave for the RSPI.
12-bit A/D converter	AN000 to AN015	Input	Input pins for the analog signals to be processed by the A/D converter.
	ADTRG0#	Input	Input pin for the external trigger signals that start the A/D conversion.
D/A converter	DA0, DA1	Output	Output pins for the analog signals to be processed by the D/A converter.
Comparator A	CMPA1	Input	Input pin for the comparator A1 analog signal.
	CMPA2	Input	Input pin for the comparator A2 analog signal.
	CVREFA	Input	Input pin for the comparator reference voltage.
Comparator B	CMPB0	Input	Input pin for the comparator B0 analog signal.
	CVREFB0	Input	Input pin for the comparator B0 reference voltage.
	CMPB1	Input	Input pin for the comparator B1 analog signal.
	CVREFB1	Input	Input pin for the comparator B1 reference voltage.

1.5 Pin Assignments

Figure 1.3 to Figure 1.11 show the pin assignments. Table 1.9 to Table 1.17 show the lists of pins and pin functions.

	A	B	C	D	E	F	G	H	J	K	L	M	N	
13	PE3	PE4	PK4	PE6	P67	PA2	PA4	PA7	PB1	PB5	PL0	PL1	P74	13
12	PE1	PE2	P70	PE5	P65	PA1	VCC	PB0	PB2	PB6	P73	PC1	P75	12
11	P62	P61	PE0	PK5	P66	VSS	PA6	P71	PB4	PB7	PC2	PC0	PC3	11
10	PK3	PK2	P63	PE7	PA0	PA3	PA5	P72	PB3	P76	PC4	P77	P82	10
9	PD6	PD4	PD7	P64						P80	PC5	P81	PC7	9
8	PD2	PD0	PD3	P60						VCC	P83	PC6	VSS	8
7	P92	P91	PD1	PD5						P51	P52	P50	P55	7
6	P90	P47	VSS	P93						P53	P56	PH0	PH1	6
5	P45	P43	P46	VCC	P44					P54	P13	PH3	PH2	5
4	P42	VREFL0	P41	P01	NC	PJ1	NC	P35	P30	P15	P24	P12	P14	4
3	P40	P05	VREFH0	P03	PJ5	PJ3	MD	VSS	P32	P31	P16	P86	P87	3
2	P07	AVCC0	P02	PF5	VCL	XCOUT	RES#	VCC	P33	P26	P23	P17	P20	2
1	AVSS0	VREFH	VREFL	P00	VSS	XCIN	XTAL	EXTAL	P34	P27	P25	P22	P21	1
	A	B	C	D	E	F	G	H	J	K	L	M	N	

RX210 Group
PTLG0145KA-A
(145-pin TFLGA)
(Upper perspective view)

Note: • This figure indicates the power supply pins and I/O port pins. For the pin configuration, see the table “List of Pins and Pin Functions (145-Pin TFLGA)”.
Note: • For the position of A1 pin in the package, see “Package Dimensions”.

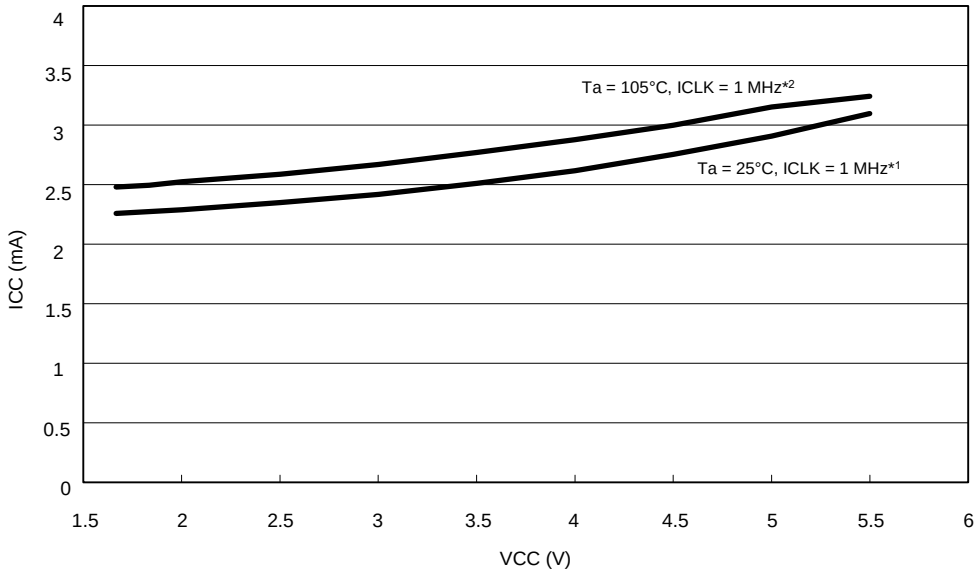
Figure 1.3 Pin Assignments of the 145-Pin TFLGA (Upper Perspective View)

Table 1.13 List of Pins and Pin Functions (80-Pin LQFP) (1 / 2)

Pin No.	Power Supply, Clock, System Control	I/O Port	Timers (MTU, TMR, POE)	Communications (SCIc, SCId, RSPI, RIIC)	Others
1	VREFH				
2		P03			DA0
3	VREFL				
4	VCL				
5		PJ1	MTIOC3A		
6	MD				FINED
7	XCIN				
8	XCOUT				
9	RES#				
10	XTAL	P37			
11	VSS				
12	EXTAL	P36			
13	VCC				
14		P35			NMI
15		P34	MTIOC0A/TMCI3/POE2#	SCK6	IRQ4
16		P32	MTIOC0C/TMO3	TXD6/SMOSI6/SSDA6	IRQ2-DS/RTCOUT/ RTCIC2
17		P31	MTIOC4D/TMCI2	CTS1#/RTS1#/SS1#	IRQ1-DS/RTCIC1
18		P30	MTIOC4B/TMRI3/POE8#	RXD1/SMISO1/SSCL1	IRQ0-DS/RTCIC0
19		P27	MTIOC2B/TMCI3	SCK1	
20		P26	MTIOC2A/TMO1	TXD1/SMOSI1/SSDA1	
21		P21	MTIOC1B/TMCI0	RXD0/SSCL0	
22		P20	MTIOC1A/TMRI0	TXD0/SSDA0	
23		P17	MTIOC3A/MTIOC3B/TMO1/ POE8#	SCK1/MISOA/ SDA-DS	IRQ7
24		P16	MTIOC3C/MTIOC3D/TMO2	TXD1/SMOSI1/SSDA1/MOSIA/ SCL-DS	IRQ6/RTCOUT/ ADTRG0#
25		P15	MTIOC0B/MTCLKB/TMCI2	RXD1/SMISO1/SSCL1	IRQ5
26		P14	MTIOC3A/MTCLKA/TMRI2	CTS1#/RTS1#/SS1#	IRQ4
27		P13	MTIOC0B/TMO3	SDA	IRQ3
28		P12	TMCI1	SCL	IRQ2
29		PH3	TMCI0		
30		PH2	TMRI0		IRQ1
31		PH1	TMO0		IRQ0
32		PH0			CACREF
33		P55	MTIOC4D/TMO3		
34		P54	MTIOC4B/TMCI1		
35		PC7	MTIOC3A/TMO2/MTCLKB	TXD8/SMOSI8/SSDA8/MISOA	CACREF
36		PC6	MTIOC3C/MTCLKA/TMCI2	RXD8/SMISO8/SSCL8/MOSIA	
37		PC5	MTIOC3B/MTCLKD/TMRI2	SCK8/RSPCKA	
38		PC4	MTIOC3D/MTCLKC/TMCI1/ POE0#	SCK5/CTS8#/RTS8#/SS8#/ SSLA0	
39		PC3	MTIOC4D	TXD5/SMOSI5/SSDA5	
40		PC2	MTIOC4B	RXD5/SMISO5/SSCL5/SSLA3	
41		PB7	MTIOC3B	TXD9/SMOSI9/SSDA9	
42		PB6	MTIOC3D	RXD9/SMISO9/SSCL9	
43		PB5	MTIOC2A/MTIOC1B/TMRI1/ POE1#	SCK9	
44		PB4		CTS9#/RTS9#/SS9#	

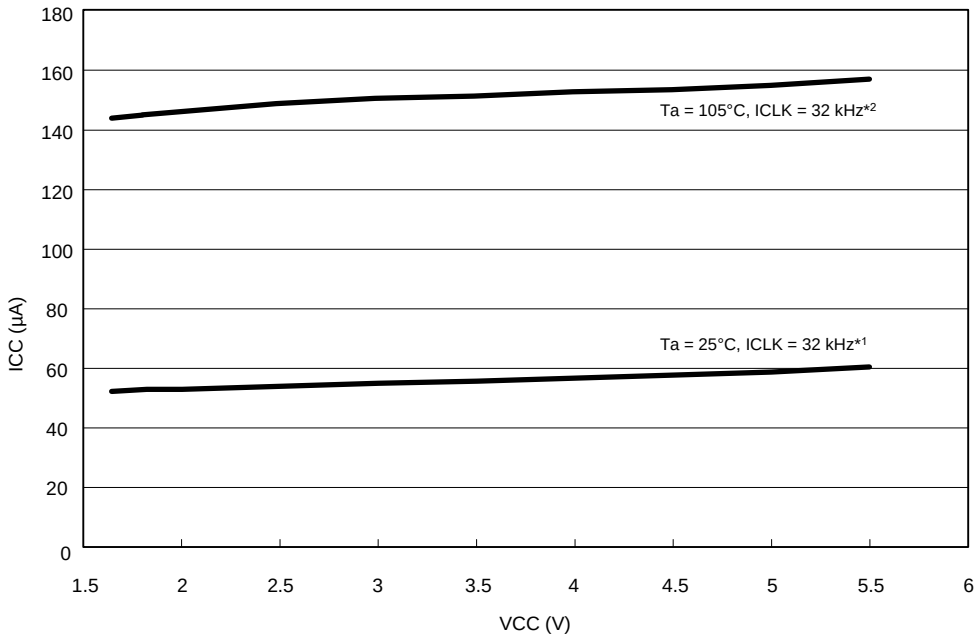
Table 4.1 List of I/O Registers (Address Order) (19 / 29)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles: ICLK ≥ PCLK	Number of Access Cycles: ICLK < PCLK
0008 A0CDh	SCI6	SPI mode register	SPMR	8	8	2, 3 PCLKB	2 ICLK
0008 A0E0h	SCI7	Serial mode register	SMR	8	8	2, 3 PCLKB	2 ICLK
0008 A0E1h	SCI7	Bit rate register	BRR	8	8	2, 3 PCLKB	2 ICLK
0008 A0E2h	SCI7	Serial control register	SCR	8	8	2, 3 PCLKB	2 ICLK
0008 A0E3h	SCI7	Transmit data register	TDR	8	8	2, 3 PCLKB	2 ICLK
0008 A0E4h	SCI7	Serial status register	SSR	8	8	2, 3 PCLKB	2 ICLK
0008 A0E5h	SCI7	Receive data register	RDR	8	8	2, 3 PCLKB	2 ICLK
0008 A0E6h	SCI7	Smart card mode register	SCMR	8	8	2, 3 PCLKB	2 ICLK
0008 A0E7h	SCI7	Serial extended mode register	SEMR	8	8	2, 3 PCLKB	2 ICLK
0008 A0E8h	SCI7	Noise filter setting register	SNFR	8	8	2, 3 PCLKB	2 ICLK
0008 A0E9h	SCI7	I^2C mode register 1	SIMR1	8	8	2, 3 PCLKB	2 ICLK
0008 A0EAh	SCI7	I^2C mode register 2	SIMR2	8	8	2, 3 PCLKB	2 ICLK
0008 A0EBh	SCI7	I^2C mode register 3	SIMR3	8	8	2, 3 PCLKB	2 ICLK
0008 A0ECh	SCI7	I^2C status register	SISR	8	8	2, 3 PCLKB	2 ICLK
0008 A0EDh	SCI7	SPI mode register	SPMR	8	8	2, 3 PCLKB	2 ICLK
0008 A100h	SCI8	Serial mode register	SMR	8	8	2, 3 PCLKB	2 ICLK
0008 A101h	SCI8	Bit rate register	BRR	8	8	2, 3 PCLKB	2 ICLK
0008 A102h	SCI8	Serial control register	SCR	8	8	2, 3 PCLKB	2 ICLK
0008 A103h	SCI8	Transmit data register	TDR	8	8	2, 3 PCLKB	2 ICLK
0008 A104h	SCI8	Serial status register	SSR	8	8	2, 3 PCLKB	2 ICLK
0008 A105h	SCI8	Receive data register	RDR	8	8	2, 3 PCLKB	2 ICLK
0008 A106h	SCI8	Smart card mode register	SCMR	8	8	2, 3 PCLKB	2 ICLK
0008 A107h	SCI8	Serial extended mode register	SEMR	8	8	2, 3 PCLKB	2 ICLK
0008 A108h	SCI8	Noise filter setting register	SNFR	8	8	2, 3 PCLKB	2 ICLK
0008 A109h	SCI8	I^2C mode register 1	SIMR1	8	8	2, 3 PCLKB	2 ICLK
0008 A10Ah	SCI8	I^2C mode register 2	SIMR2	8	8	2, 3 PCLKB	2 ICLK
0008 A10Bh	SCI8	I^2C mode register 3	SIMR3	8	8	2, 3 PCLKB	2 ICLK
0008 A10Ch	SCI8	I^2C status register	SISR	8	8	2, 3 PCLKB	2 ICLK
0008 A10Dh	SCI8	SPI mode register	SPMR	8	8	2, 3 PCLKB	2 ICLK
0008 A120h	SCI9	Serial mode register	SMR	8	8	2, 3 PCLKB	2 ICLK
0008 A121h	SCI9	Bit rate register	BRR	8	8	2, 3 PCLKB	2 ICLK
0008 A122h	SCI9	Serial control register	SCR	8	8	2, 3 PCLKB	2 ICLK
0008 A123h	SCI9	Transmit data register	TDR	8	8	2, 3 PCLKB	2 ICLK
0008 A124h	SCI9	Serial status register	SSR	8	8	2, 3 PCLKB	2 ICLK
0008 A125h	SCI9	Receive data register	RDR	8	8	2, 3 PCLKB	2 ICLK
0008 A126h	SCI9	Smart card mode register	SCMR	8	8	2, 3 PCLKB	2 ICLK
0008 A127h	SCI9	Serial extended mode register	SEMR	8	8	2, 3 PCLKB	2 ICLK
0008 A128h	SCI9	Noise filter setting register	SNFR	8	8	2, 3 PCLKB	2 ICLK
0008 A129h	SCI9	I^2C mode register 1	SIMR1	8	8	2, 3 PCLKB	2 ICLK
0008 A12Ah	SCI9	I^2C mode register 2	SIMR2	8	8	2, 3 PCLKB	2 ICLK
0008 A12Bh	SCI9	I^2C mode register 3	SIMR3	8	8	2, 3 PCLKB	2 ICLK
0008 A12Ch	SCI9	I^2C status register	SISR	8	8	2, 3 PCLKB	2 ICLK
0008 A12Dh	SCI9	SPI mode register	SPMR	8	8	2, 3 PCLKB	2 ICLK
0008 A140h	SCI10	Serial mode register	SMR	8	8	2, 3 PCLKB	2 ICLK
0008 A141h	SCI10	Bit rate register	BRR	8	8	2, 3 PCLKB	2 ICLK
0008 A142h	SCI10	Serial control register	SCR	8	8	2, 3 PCLKB	2 ICLK
0008 A143h	SCI10	Transmit data register	TDR	8	8	2, 3 PCLKB	2 ICLK
0008 A144h	SCI10	Serial status register	SSR	8	8	2, 3 PCLKB	2 ICLK
0008 A145h	SCI10	Receive data register	RDR	8	8	2, 3 PCLKB	2 ICLK
0008 A146h	SCI10	Smart card mode register	SCMR	8	8	2, 3 PCLKB	2 ICLK
0008 A147h	SCI10	Serial extended mode register	SEMR	8	8	2, 3 PCLKB	2 ICLK



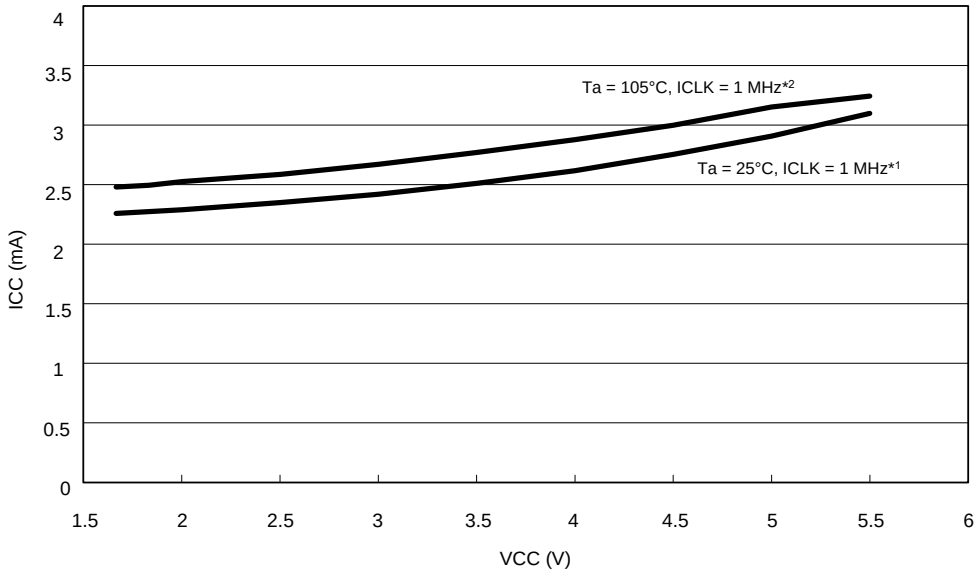
Note 1. All peripheral operation is normal.
Average value of the tested middle samples during product evaluation.
Note 2. All peripheral operation is maximum.
Average value of the tested upper-limit samples during product evaluation.

Figure 5.3 Voltage Dependency in Low-Speed Operating Mode 1 (Reference Data) for Chip Version A



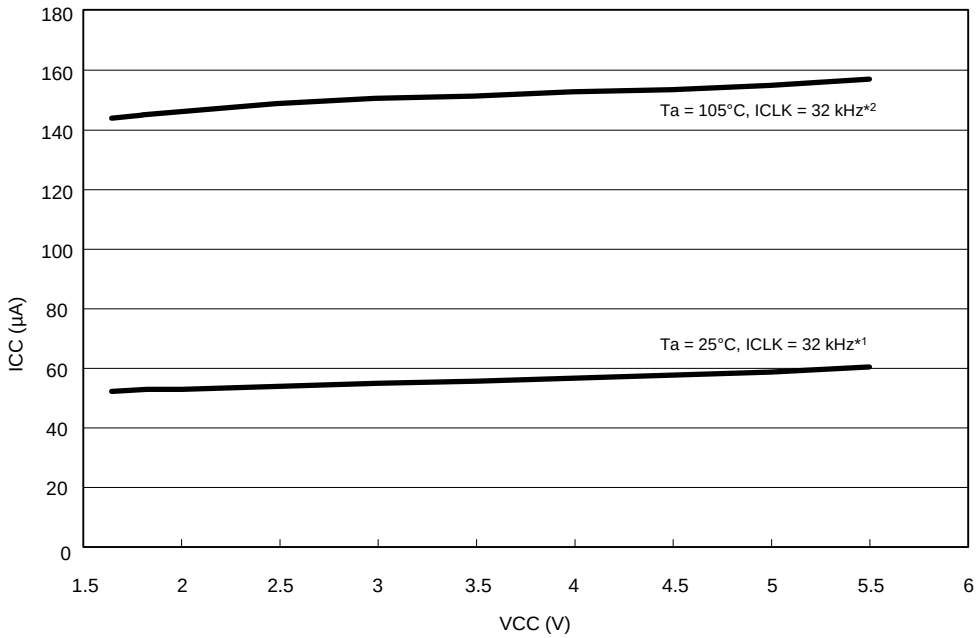
Note 1. All peripheral operation is normal.
Average value of the tested middle samples during product evaluation.
Note 2. All peripheral operation is maximum.
Average value of the tested upper-limit samples during product evaluation.

Figure 5.4 Voltage Dependency in Low-Speed Operating Mode 2 (Reference Data) for Chip Version A



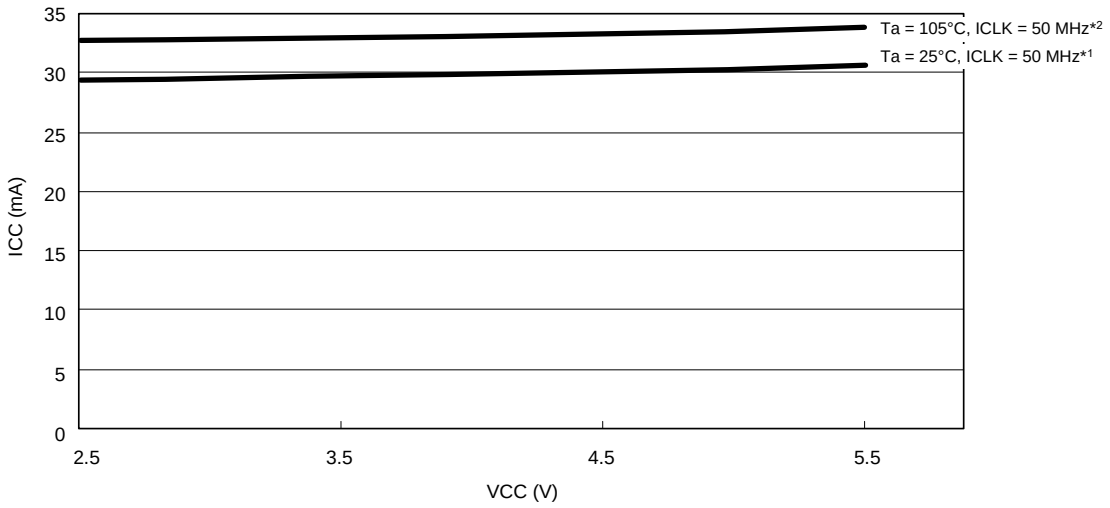
Note 1. All peripheral operation is normal.
Average value of the tested middle samples during product evaluation.
Note 2. All peripheral operation is maximum.
Average value of the tested upper-limit samples during product evaluation.

Figure 5.11 Voltage Dependency in Low-Speed Operating Mode 1 (Reference Data) for Chip Version C



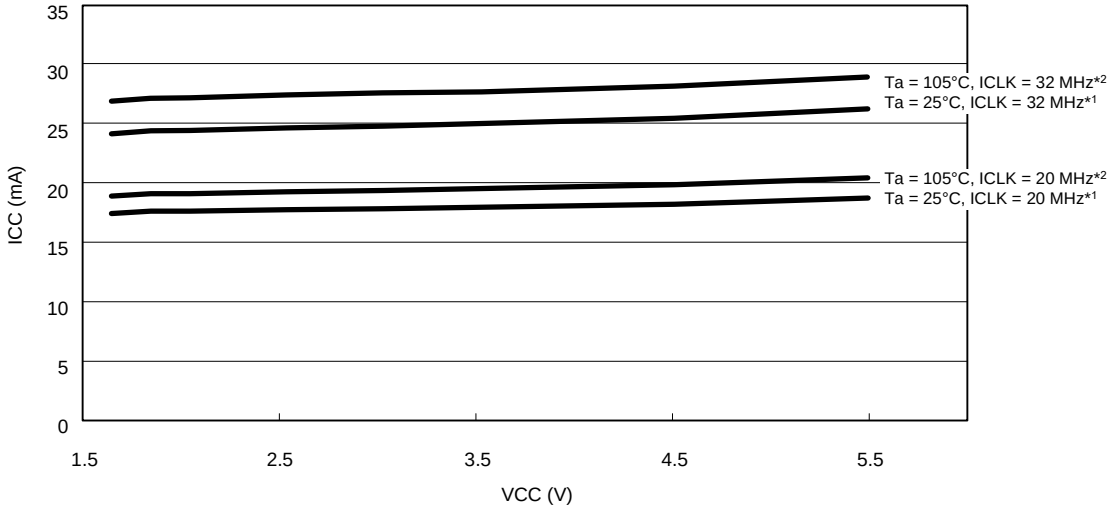
Note 1. All peripheral operation is normal.
Average value of the tested middle samples during product evaluation.
Note 2. All peripheral operation is maximum.
Average value of the tested upper-limit samples during product evaluation.

Figure 5.12 Voltage Dependency in Low-Speed Operating Mode 2 (Reference Data) for Chip Version C



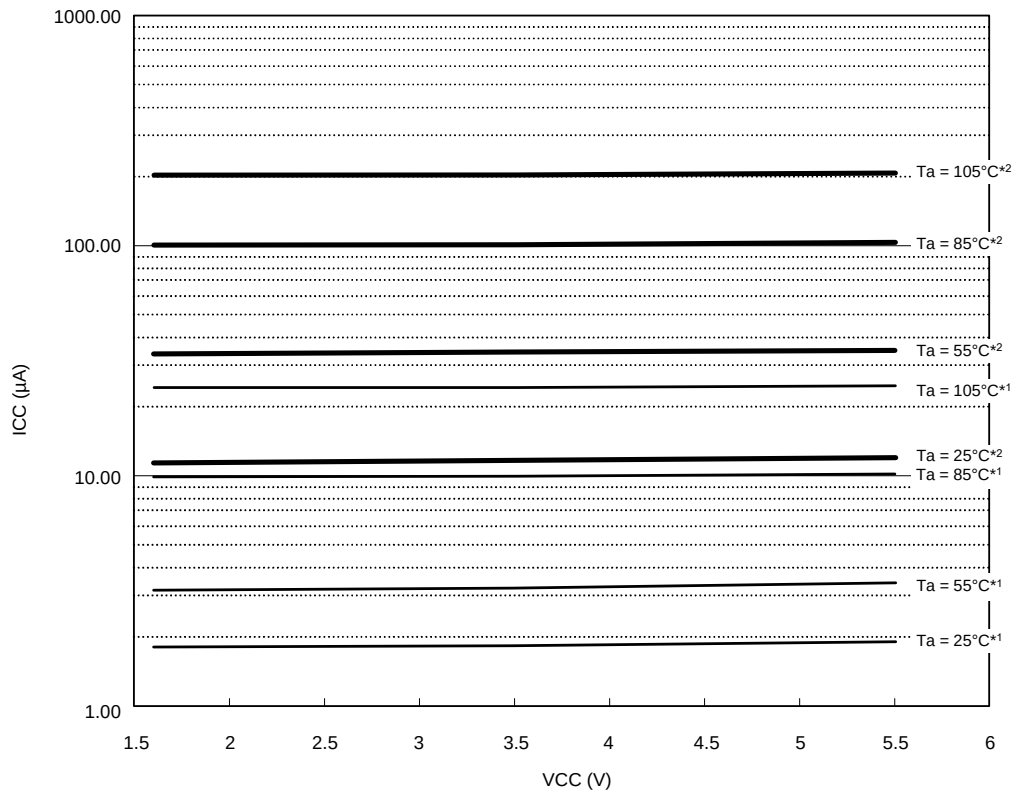
Note 1. All peripheral operation is normal. This does not include BGO operation.
Average value of the tested middle samples during product evaluation.
Note 2. All peripheral operation is maximum. This does not include BGO operation.
Average value of the tested upper-limit samples during product evaluation.

Figure 5.26 Voltage Dependency in High-Speed Operating Mode (Reference Data) for Chip Version B with 768 Kbytes/1 Mbyte of Flash Memory and 100 to 145 Pins



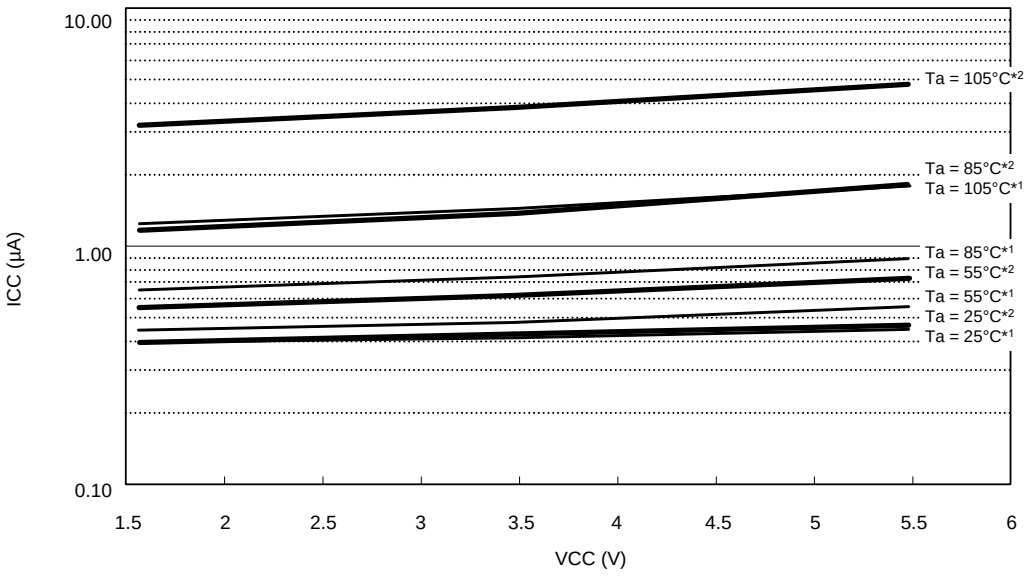
Note 1. All peripheral operation is normal. This does not include BGO operation.
Average value of the tested middle samples during product evaluation.
Note 2. All peripheral operation is maximum. This does not include BGO operation.
Average value of the tested upper-limit samples during product evaluation.

Figure 5.27 Voltage Dependency in Middle-Speed Operating Modes 1A and 1B (Reference Data) for Chip Version B with 768 Kbytes/1 Mbyte of Flash Memory and 100 to 145 Pins



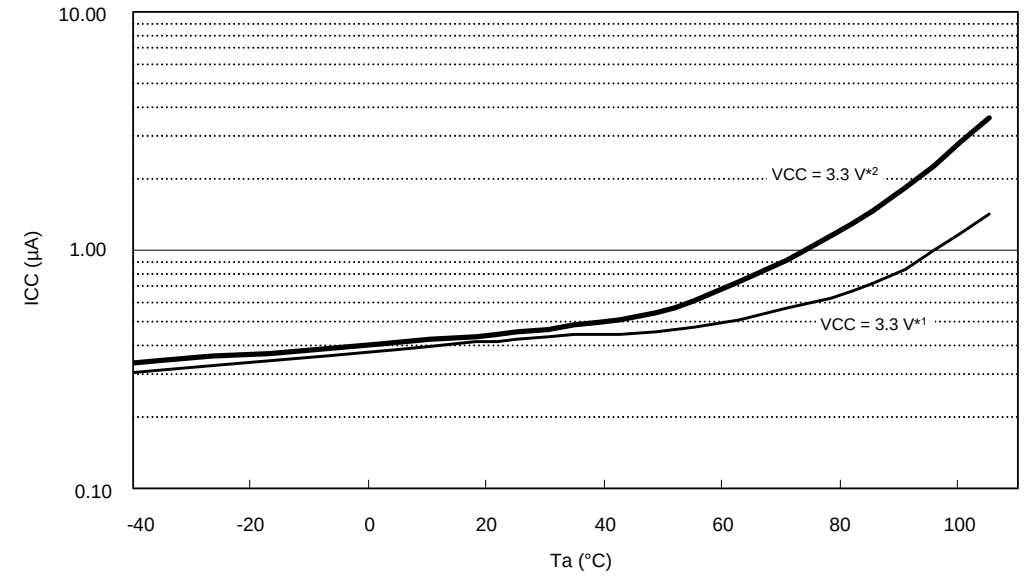
Note 1. Average value of the tested middle samples during product evaluation.
Note 2. Average value of the tested upper-limit samples during product evaluation.

Figure 5.31 Voltage Dependency in Software Standby Mode (SOFTCUT[2:0] Bits = 110b) (Reference Data) for Chip Version B with 768 Kbytes/1 Mbyte of Flash Memory and 100 to 145 Pins



Note 1. Average value of the tested middle samples during product evaluation.
Note 2. Average value of the tested upper-limit samples during product evaluation.

Figure 5.33 Voltage Dependency in Deep Software Standby Mode (DEEPCUT1 Bit = 1) (Reference Data) for Chip Version B with 768 Kbytes/1 Mbyte of Flash Memory and 100 to 145 Pins



Note 1. Average value of the tested middle samples during product evaluation.
Note 2. Average value of the tested upper-limit samples during product evaluation.

Figure 5.34 Temperature Dependency in Deep Software Standby Mode (DEEPCUT1 Bit = 1) (Reference Data) for Chip Version B with 768 Kbytes/1 Mbyte of Flash Memory and 100 to 145 Pins

[Chip version B with 512 Kbytes or less of flash memory and 144 and 145 pins]

Table 5.19 DC Characteristics (18)

Conditions: VCC = AVCC0 = 1.62 to 5.5 V, VSS = AVSS0 = VREFL = VREFL0 = 0 V, T_a = –40 to +105°C

Item					Symbol	Typ.	Max.	Unit	Test Conditions
Supply current*1	Middle-speed operating modes 1A and 1B	Normal operating mode	No peripheral operation	ICLK = 32 MHz*2	I_{CC}	5.3	—	mA	
				ICLK = 20 MHz*3		4.6	—		
			All peripheral operation: Normal	ICLK = 32 MHz*4		22.3	—		
				ICLK = 20 MHz*5		15.6	—		
			All peripheral operation: Max.	ICLK = 32 MHz*4		—	35		
				ICLK = 20 MHz*5		—	—		
		Sleep mode	No peripheral operation	ICLK = 32 MHz		3.4	—		
				ICLK = 20 MHz		3.3	—		
			All peripheral operation: Normal	ICLK = 32 MHz		12.8	—		
				ICLK = 20 MHz		9.8	—		
		All-module clock stop mode		ICLK = 32 MHz		3	—		
				ICLK = 20 MHz		3	—		
		Increase during BGO operation*6	Middle-speed operating mode 1A			21	—		
			Middle-speed operating mode 1B			19	—		
	Middle-speed operating modes 2A and 2B	Normal operating mode	No peripheral operation*2	ICLK = 32 MHz		4.7	—		
				ICLK = 16 MHz		3.4	—		
				ICLK = 8 MHz		2.7	—		
			All peripheral operation: Normal*4	ICLK = 32 MHz*3		21.7	—		
				ICLK = 16 MHz*3		12.3	—		
				ICLK = 8 MHz		7.6	—		
			All peripheral operation: Max.*4	ICLK = 32 MHz*3		—	34		
				ICLK = 16 MHz*3		—	—		
				ICLK = 8 MHz		—	—		
		Sleep mode	No peripheral operation	ICLK = 32 MHz		2.9	—		
				ICLK = 16 MHz		2.5	—		
				ICLK = 8 MHz		2.2	—		
			All peripheral operation: Normal	ICLK = 32 MHz		12.3	—		
				ICLK = 16 MHz		7.8	—		
				ICLK = 8 MHz		5.6	—		
		All-module clock stop mode		ICLK = 32 MHz		2.5	—		
				ICLK = 16 MHz		2.2	—		
				ICLK = 8 MHz		2.1	—		
		Increase during BGO operation*6	Middle-speed operating mode 1A			21	—		
			Middle-speed operating mode 1B			19	—		

[Chip version B]

Table 5.39 Operation Frequency Value (Low-Speed Operating Mode 1)

Conditions: VCC = AVCC0 = 1.62 to 5.5 V, VSS = AVSS0 = VREFL = VREFL0 = 0 V, T_a = –40 to +105°C

Item		Symbol	VCC			Unit
			1.62 to 1.8 V	1.8 to 2.7 V	2.7 to 5.5 V	
Maximum operating frequency	System clock (ICLK)	f_{max}	2	4	8	MHz
	FlashIF clock (FCLK)*1		2	4	8	
	Peripheral module clock (PCLKB)		2	4	8	
	Peripheral module clock (PCLKD)*2		2	4	8	
	External bus clock (BCLK)		2	4	8	
	BCLK pin output		2	4	8	

Note 1. Programming and erasing the flash memory is impossible.
Note 2. The lower-limit frequency of PCLKD is 1 MHz when the A/D converter is in use.

[Chip versions A, B, and C]

Table 5.40 Operation Frequency Value (Low-Speed Operating Mode 2)

Conditions: VCC = AVCC0 = 1.62 to 5.5 V, VSS = AVSS0 = VREFL=VREFL0 = 0 V, T_a = –40 to +105°C

Item		Symbol	VCC			Unit
			1.62 to 1.8 V	1.8 to 2.7 V	2.7 to 5.5 V	
Maximum operating frequency	System clock (ICLK)	f_{max}	32.768	32.768	32.768	kHz
	FlashIF clock (FCLK)*1		32.768	32.768	32.768	
	Peripheral module clock (PCLKB)		32.768	32.768	32.768	
	Peripheral module clock (PCLKD)*2		32.768	32.768	32.768	
	External bus clock (BCLK)		32.768	32.768	32.768	
	BCLK pin output		32.768	32.768	32.768	

Note 1. Programming and erasing the flash memory is impossible.
Note 2. The A/D converter cannot be used.

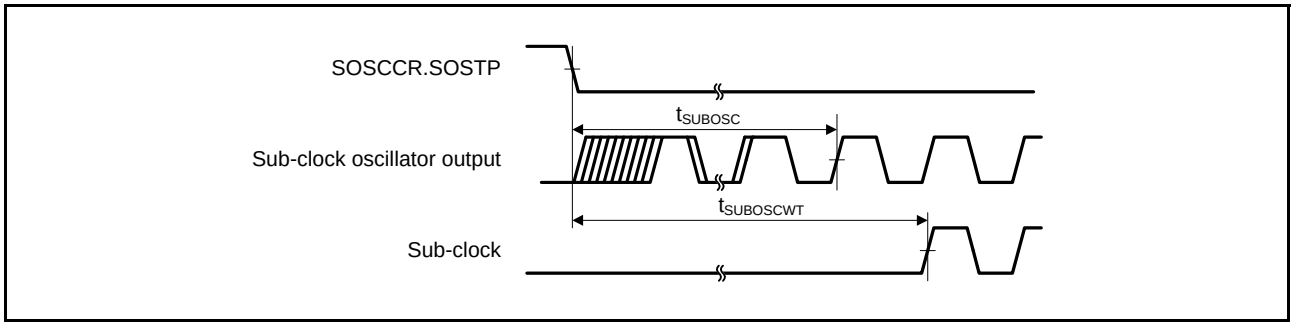


Figure 5.69 Sub-clock Oscillation Start Timing

5.3.3 Timing of Recovery from Low Power Consumption Modes

[Chip versions A and C]

Table 5.46 Timing of Recovery from Low Power Consumption Modes

Conditions: VCC = AVCC0 = 1.62 to 5.5 V, VSS = AVSS0 = VREFL = VREFL0 = 0 V, T_a = –40 to +105°C

Item			Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Recovery time after cancellation of software standby mode (flash memory, HOCO power supplied) (SOFTCUT[2:0] bits = 000b)*1	Crystal resonator connected to main clock oscillator*2	Main clock oscillator operating	t_{SBYMC}	—	3	—	ms	Figure 5.72
		Main clock oscillator and PLL circuit operating	t_{SBYPC}	—	3.5	—	ms	
	External clock input to main clock oscillator	Main clock oscillator operating	t_{SBYEX}	10	—	—	µs	
		Main clock oscillator and PLL circuit operating	t_{SBYPE}	0.5	—	—	ms	
	Sub-clock oscillator operating		t_{SBYSC}	2*3	—	—	s	
	HOCO clock oscillator operating		t_{SBYHO}	—	—	500	µs	
	LOCO clock oscillator operating		t_{SBYLO}	—	—	90	µs	
Recovery time after cancellation of software standby mode (flash memory power supplied, HOCO power not supplied) (SOFTCUT[2:0] bits = 110b)*1	Crystal resonator connected to main clock oscillator*2	Main clock oscillator operating	t_{SBYMC}	—	3	—	ms	Figure 5.72
		Main clock oscillator and PLL circuit operating	t_{SBYPC}	—	3.5	—	ms	
	External clock input to main clock oscillator	Main clock oscillator operating	t_{SBYEX}	40	—	—	µs	
		Main clock oscillator and PLL circuit operating	t_{SBYPE}	0.5	—	—	ms	
	Sub-clock oscillator operating		t_{SBYSC}	2*3	—	—	s	
	HOCO clock oscillator operating		t_{SBYHO}	—	—	1.2	ms	
	LOCO clock oscillator operating		t_{SBYLO}	—	—	90	µs	
Recovery time after cancellation of software standby mode (flash memory, HOCO power not supplied) (SOFTCUT[2:0] bits = 111b)*1	Crystal resonator connected to main clock oscillator*2	Main clock oscillator operating	t_{SBYMC}	—	3	—	ms	Figure 5.72
		Main clock oscillator and PLL circuit operating	t_{SBYPC}	—	3.5	—	ms	
	External clock input to main clock oscillator	Main clock oscillator operating	t_{SBYEX}	100	—	—	µs	
		Main clock oscillator and PLL circuit operating	t_{SBYPE}	0.5	—	—	ms	
	Sub-clock oscillator operating		t_{SBYSC}	2*4	—	—	s	
	HOCO clock oscillator operating		t_{SBYHO}	—	—	1.2	ms	
	LOCO clock oscillator operating		t_{SBYLO}	—	—	10	ms	
Recovery time after cancellation of deep software standby mode			t_{DSBY}	—	—	8	ms	Figure 5.73
Wait time after cancellation of deep software standby mode			t_{DSBYWT}	—	—	0.8	ms	

Note 1. The recovery time varies depending on the state of each oscillator when the WAIT instruction is executed. The recovery time when multiple oscillators are operating varies depending on the operating state of the oscillators that are not selected as the system clock source, and depends on the time set in the wait control registers corresponding to the oscillators.
Note 2. The indicated value is measured for an 8 MHz crystal resonator.
Note 3. When RCR3.RTCEN = 1, the time will be the time set in the SOSCWTCR register minus 2 s.
Note 4. When RCR3.RTCEN = 1, the time will be the time set in the SOSCWTCR register minus 2 s and plus 31.25 ms.

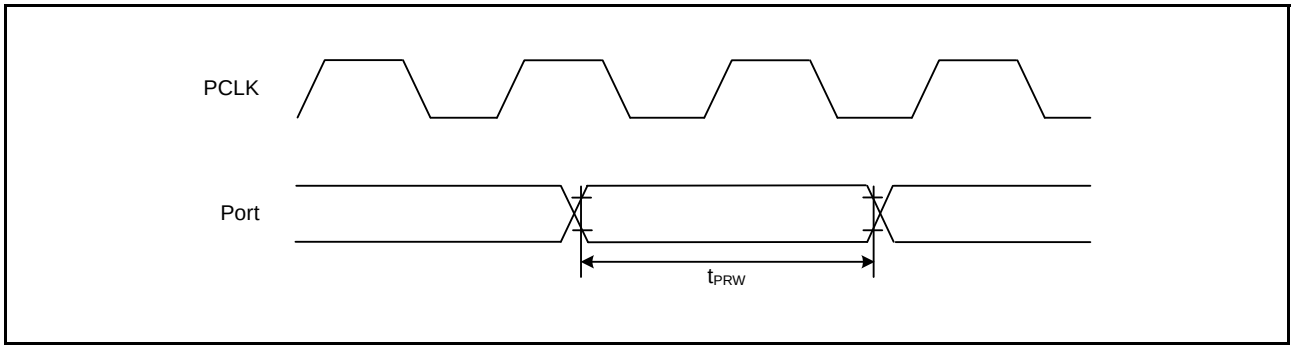


Figure 5.83 I/O Port Input Timing

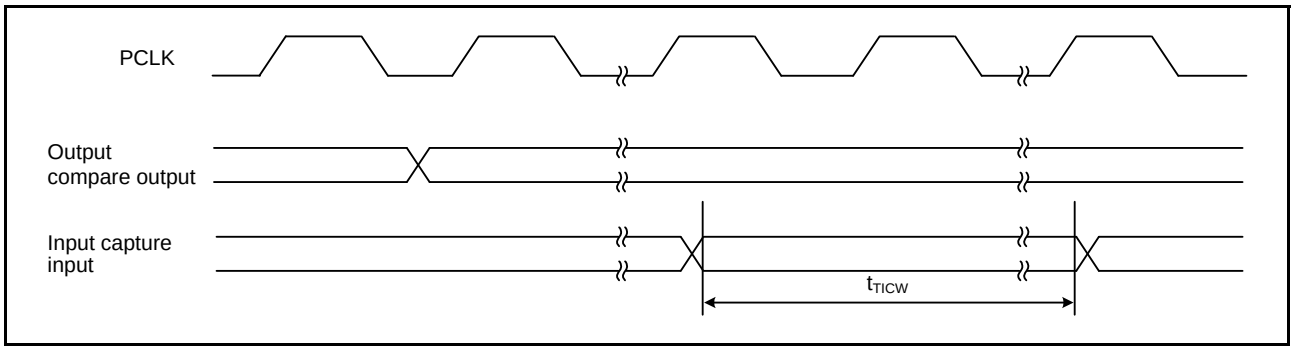


Figure 5.84 MTU/TPU Input/Output Timing

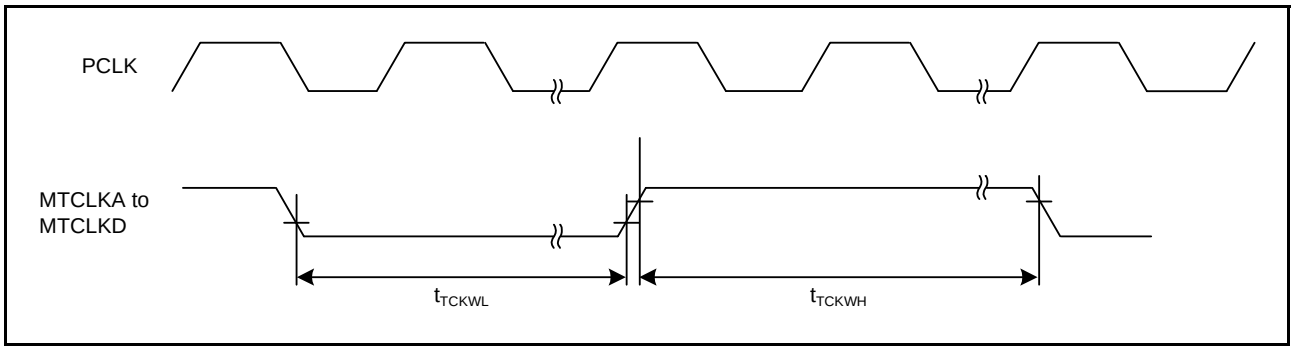


Figure 5.85 MTU/TPU Clock Input Timing

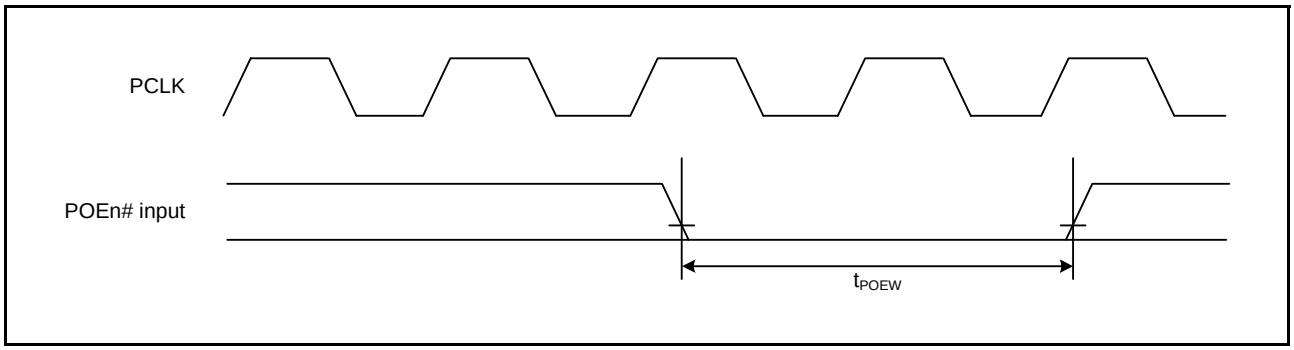


Figure 5.86 POE# Input Timing

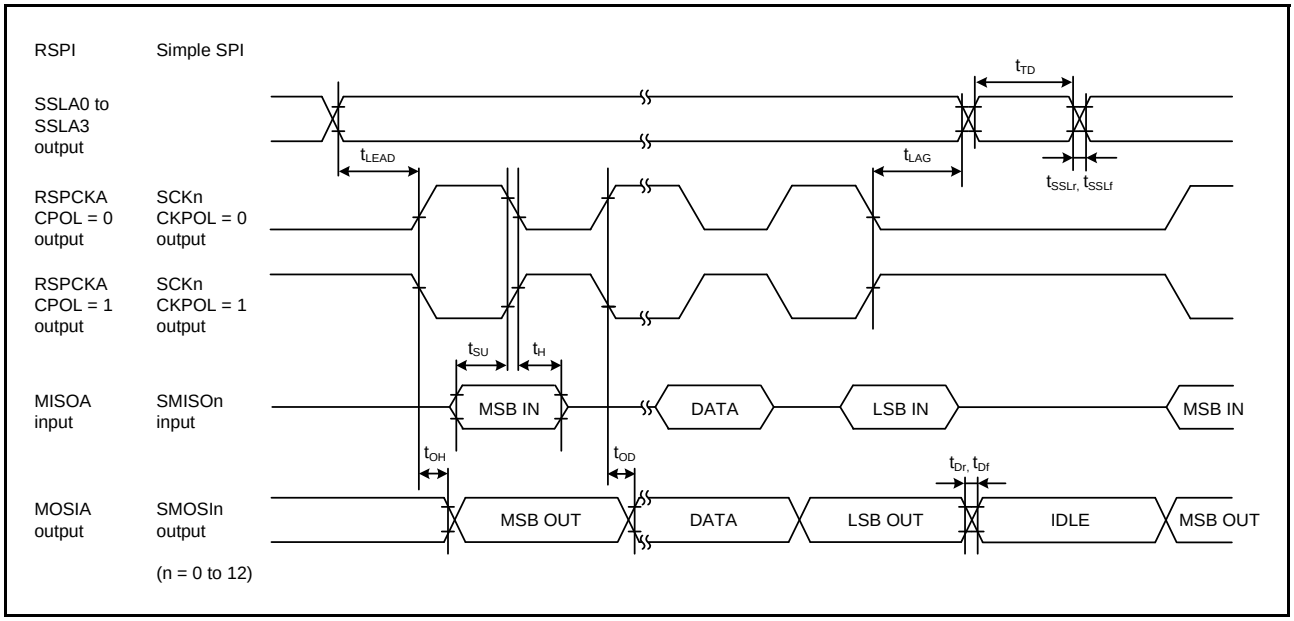


Figure 5.94 RSPI Timing (Master, CPHA = 1) (Bit Rate: PCLKB Set to Division Ratio Other Than Divided by 2) and Simple SPI Timing (Master, CKPH = 0)

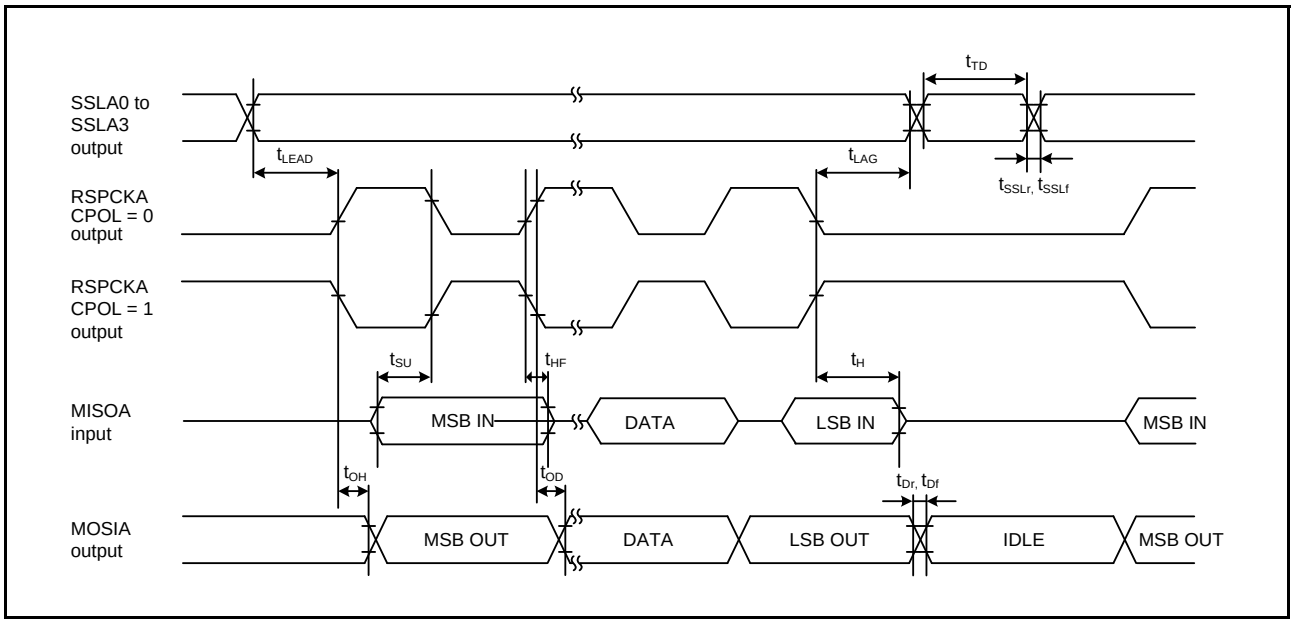


Figure 5.95 RSPI Timing (Master, CPHA = 1) (Bit Rate: PCLKB Set to Divided by 2)

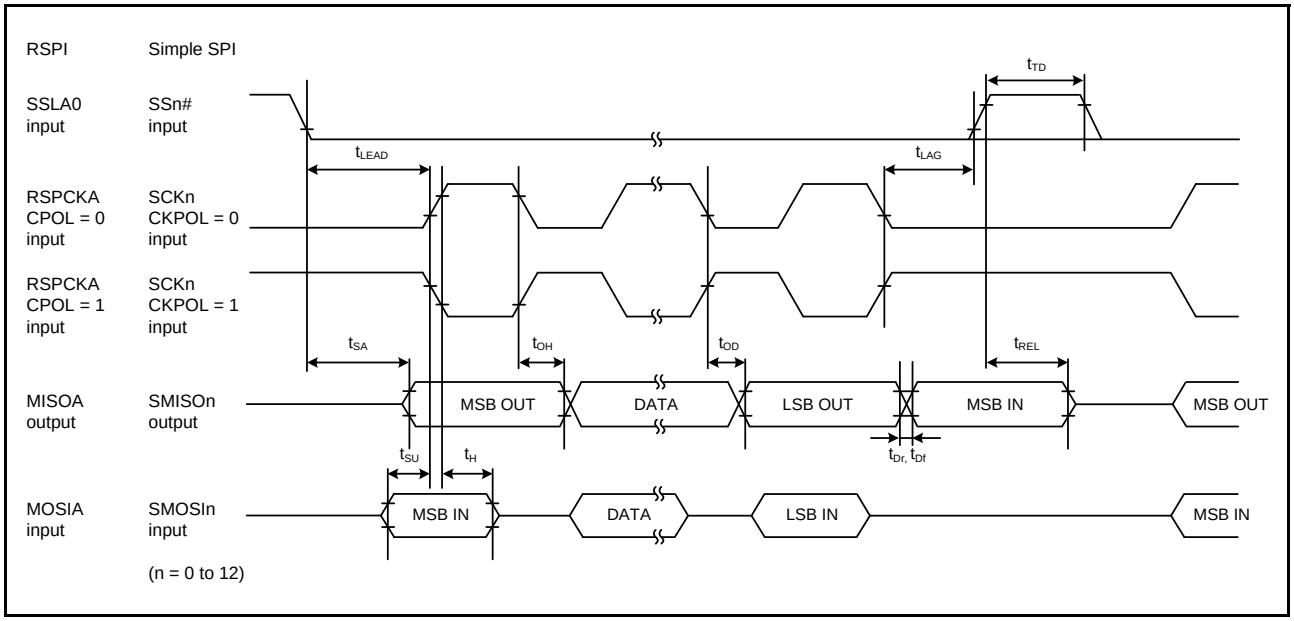


Figure 5.96 RSPI Timing (Slave, CPHA = 0) and Simple SPI Timing (Slave, CKPH = 1)

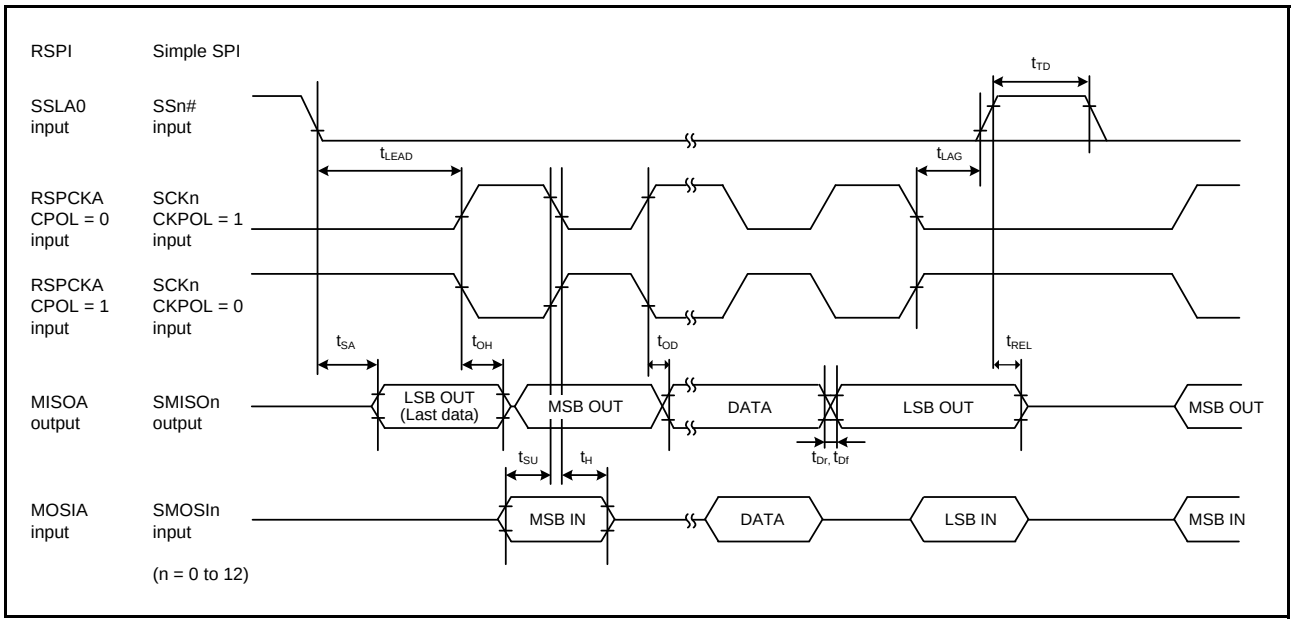


Figure 5.97 RSPI Timing (Slave, CPHA = 1) and Simple SPI Timing (Slave, CKPH = 0)

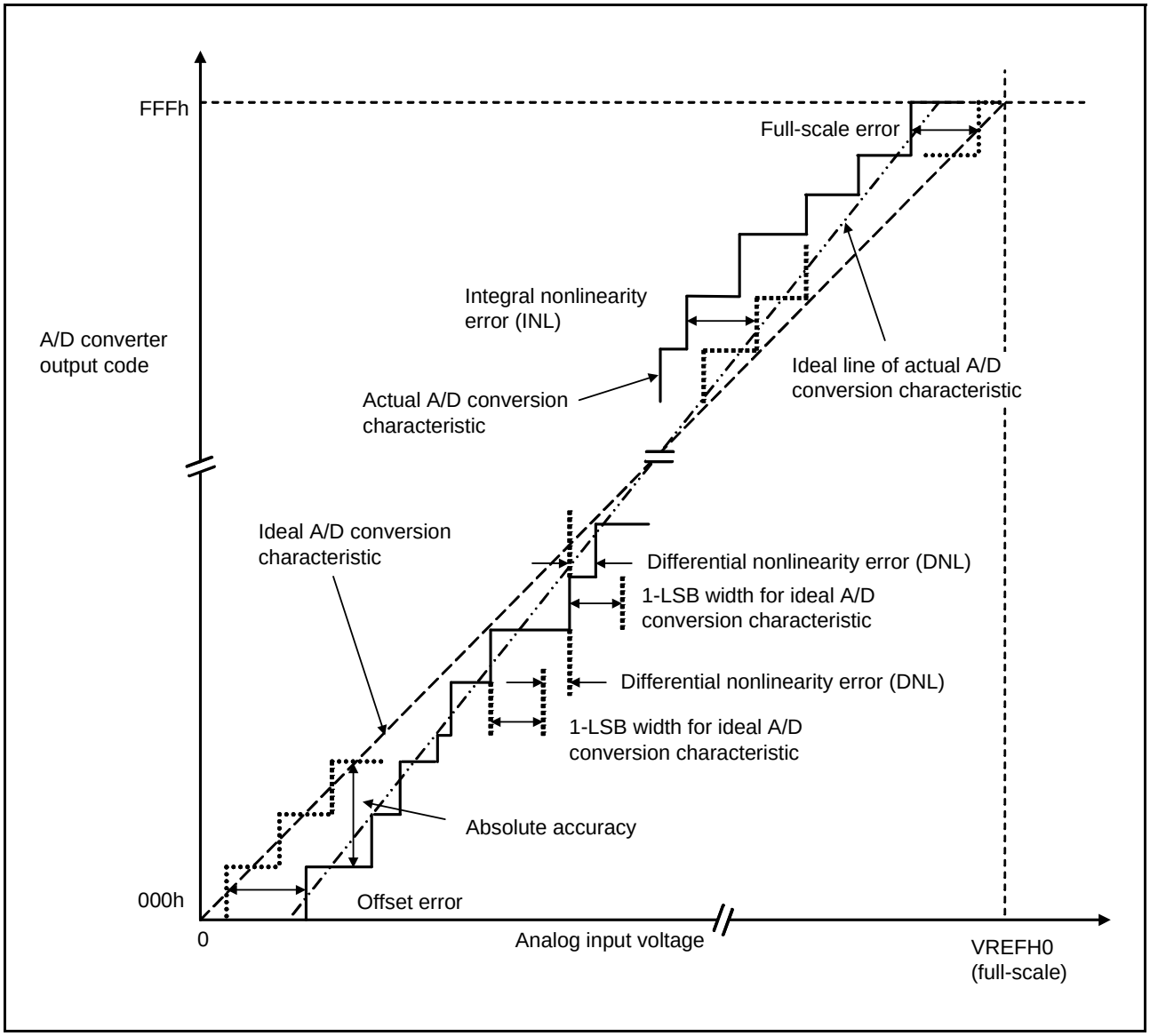


Figure 5.101 Illustration of A/D Converter Characteristic Terms

Absolute accuracy

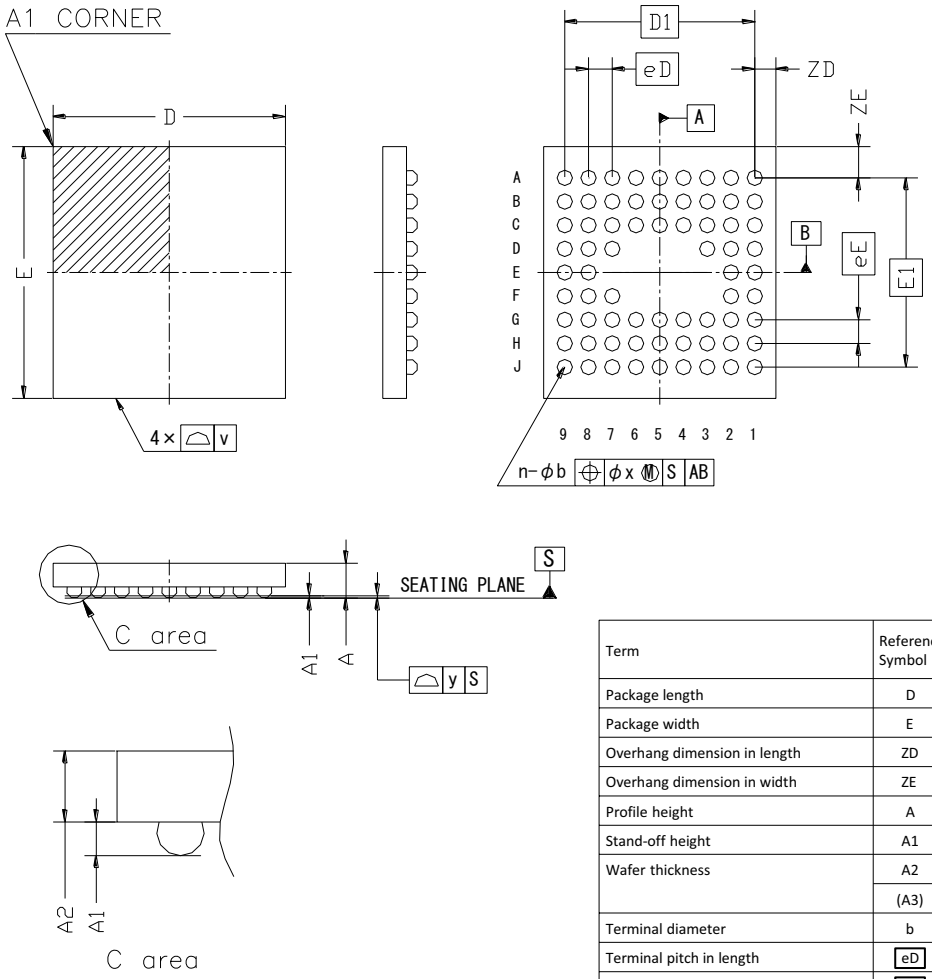
Absolute accuracy is the difference between output code based on the theoretical A/D conversion characteristics, and the actual A/D conversion result. When measuring absolute accuracy, the voltage at the midpoint of the width of analog input voltage (1-LSB width), that can meet the expectation of outputting an equal code based on the theoretical A/D conversion characteristics, is used as an analog input voltage. For example, if 12-bit resolution is used and if reference voltage (VREFH0 = 5.12 V), then 1-LSB width becomes 1.25 mV, and 0 mV, 1.25 mV, 2.5 mV, ... are used as analog input voltages.

If analog input voltage is 10 mV, absolute accuracy = ±5 LSB means that the actual A/D conversion result is in the range of 003h to 00Dh though an output code, 008h, can be expected from the theoretical A/D conversion characteristics.

Integral nonlinearity error (INL)

Integral nonlinearity error is the maximum deviation between the ideal line when the measured offset and full-scale errors are zeroed, and the actual output code.

JEITA Package code	RENESAS Code	Previous Code	MASS(TYP.)[g]
S-WFBGA69-3.91x4.26-0.40	SWBG0069LA-A	—	0.02



注記:
1. 端子ﾋﾟｯﾁは端子中央部の位置で規定する。
2. ﾃﾞｰﾀﾑA及びBは、ﾎﾞｰﾙｸﾞﾘｯﾄﾞｾﾝﾀを称す。

Note:
1. Ball pitch dimension is specified with the center of balls.
2. Datum A and B are axes defined by the ball grid array, not by the PKG outline.

Dimensions in millimeters

Term	Reference Symbol	Specification		
		Min	Nom	Max
Package length	D	3.86	3.91	3.96
Package width	E	4.21	4.26	4.31
Overhang dimension in length	ZD	0.305	0.355	0.405
Overhang dimension in width	ZE	0.48	0.53	0.58
Profile height	A	—	—	0.70
Stand-off height	A1	0.15	0.19	0.23
Wafer thickness	A2	0.36	0.40	0.44
	(A3)	—	—	—
Terminal diameter	b	0.22	0.27	0.32
Terminal pitch in length	eD		0.4	(BSC)
Terminal pitch in width	eE		0.4	(BSC)
Center terminal position in D-direction	SD		—	(BSC)
Center terminal position in E-direction	SE		—	(BSC)
Edge ball center to center in D-direction	D1		3.2	(BSC)
Edge ball center to center in D-direction	E1		3.2	(BSC)
Number of terminals	n		69	
Tolerance of package lateral profile	v		0.05	
Positional tolerance of terminals	x		0.05	
Coplanarity	y		0.08	

Figure E 69-Pin WLBGA (SWBG0069LA-A)