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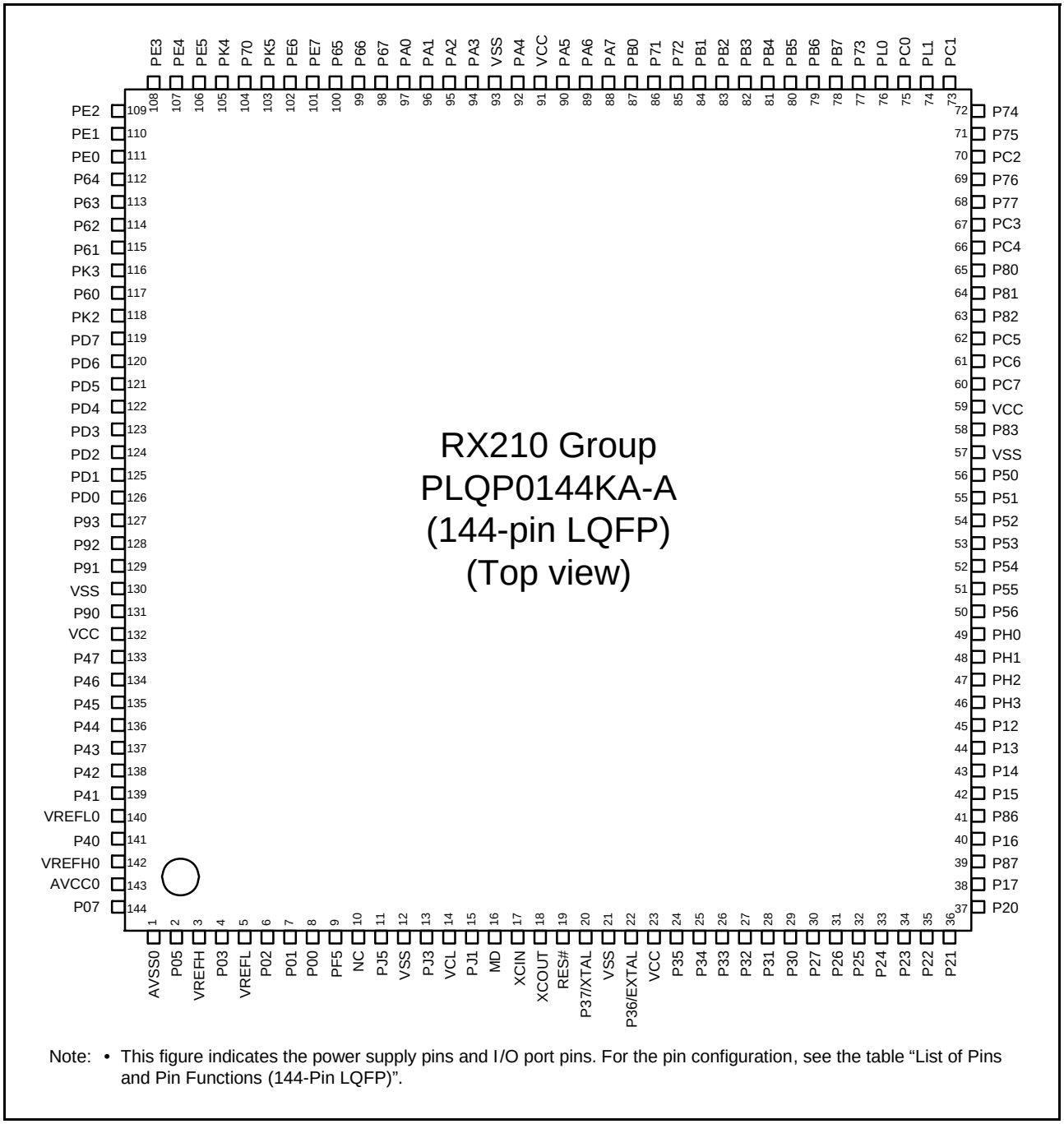
What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

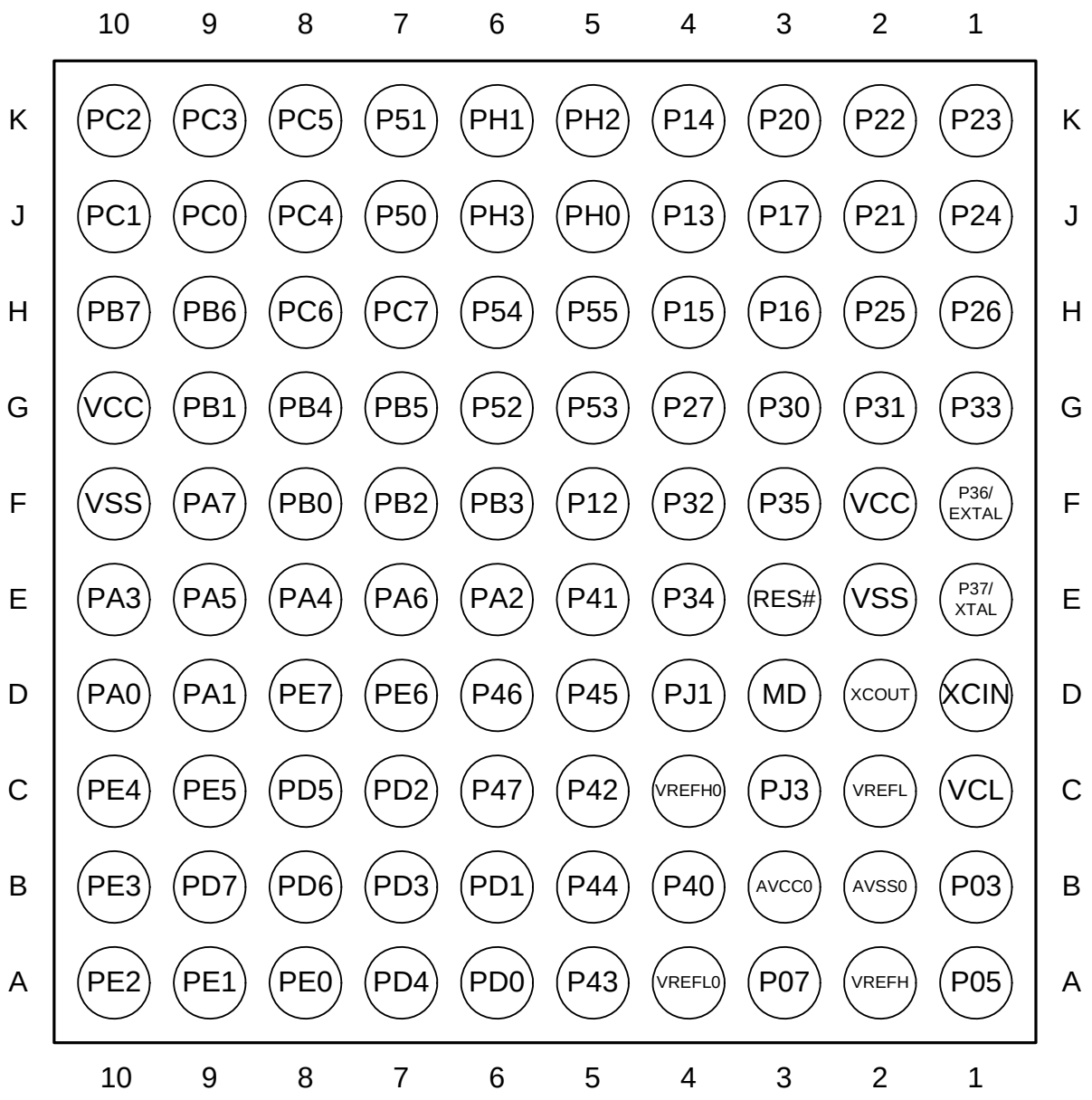
Details	
Product Status	Not For New Designs
Core Processor	RX
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	I²C, SCI, SPI
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	64
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	8K x 8
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	1.62V ~ 5.5V
Data Converters	A/D 14x12b; D/A 2x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	80-LQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f52108cdfn-30



Note: • This figure indicates the power supply pins and I/O port pins. For the pin configuration, see the table “List of Pins and Pin Functions (144-Pin LQFP)”.

Figure 1.4 Pin Assignments of the 144-Pin LQFP

RX210 Group
PTLG0100JA-A
(100-pin TFLGA)
(Upper perspective view)

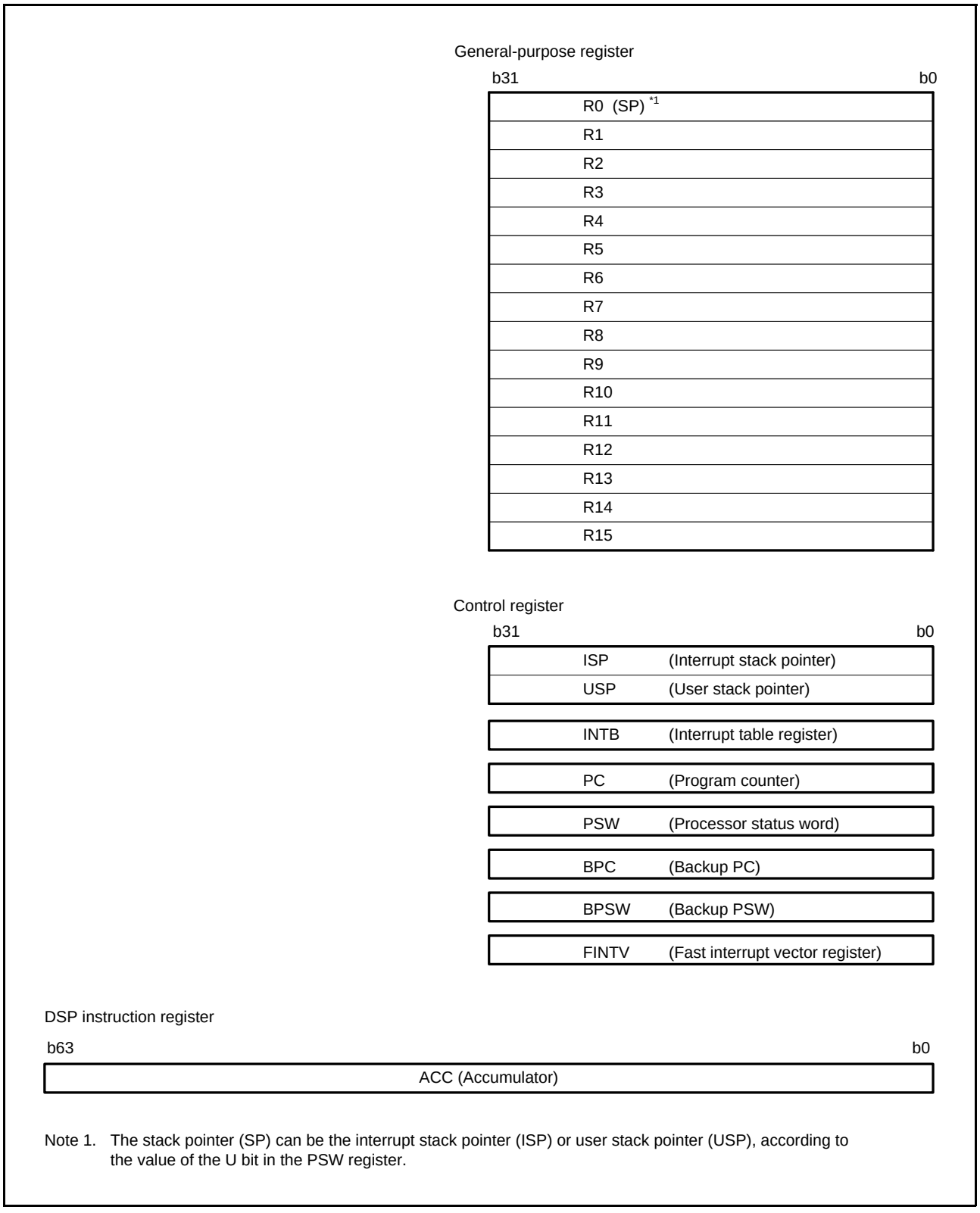


Note: • This figure indicates the power supply pins and I/O port pins. For the pin configuration, see the table “List of Pins and Pin Functions (100-Pin TFLGA)”.
Note: • For the position of A1 pin in the package, see “Package Dimensions”.

Figure 1.5 Pin Assignments of the 100-Pin TFLGA (Upper Perspective View)

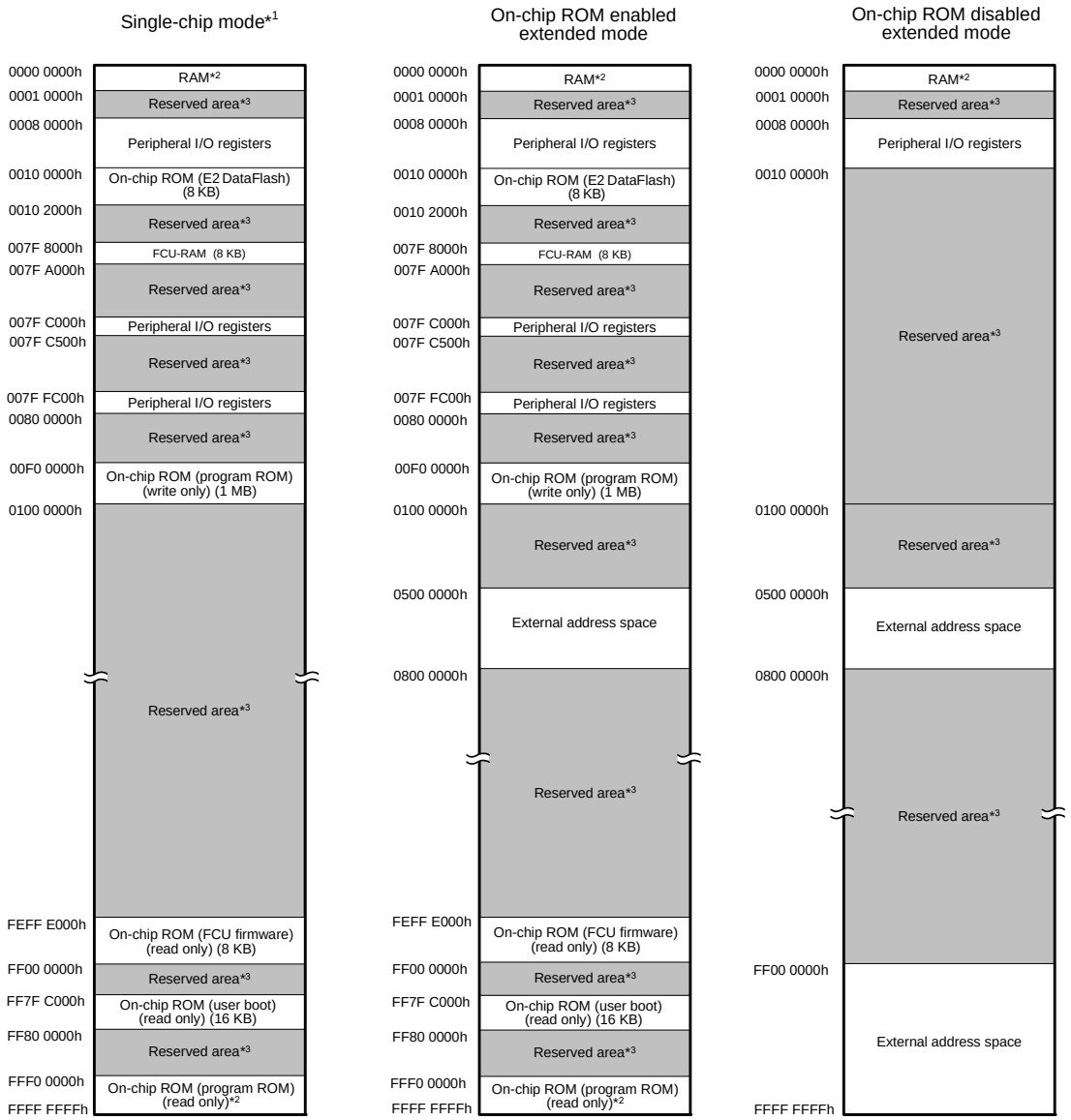
2. CPU

Figure 2.1 shows the register set of the CPU.



Note 1. The stack pointer (SP) can be the interrupt stack pointer (ISP) or user stack pointer (USP), according to the value of the U bit in the PSW register.

Figure 2.1 Register Set of the CPU



Note 1. The address space in boot mode and user boot mode is the same as the address space in single-chip mode.
Note 2. The capacity of ROM/RAM differs depending on the products.

ROM (bytes)		RAM (bytes)	
Capacity	**Address**	**Capacity**	**Address**
1 M	FFF0 0000h to FFFF FFFFh	96 K	0000 0000h to 0001 7FFFh
768 K	FFF4 0000h to FFFF FFFFh		
512 K	FFF8 0000h to FFFF FFFFh	64 K	0000 0000h to 0000 FFFFh
384 K	FFFA 0000h to FFFF FFFFh		
256 K	FFFC 0000h to FFFF FFFFh	32 K	0000 0000h to 0000 7FFFh
128 K	FFFE 0000h to FFFF FFFFh	20 K	0000 0000h to 0000 4FFFh
96 K	FFFE 8000h to FFFF FFFFh	16 K	0000 0000h to 0000 3FFFh
64 K	FFFF 0000h to FFFF FFFFh	12 K	0000 0000h to 0000 2FFFh

Note:•See Table 1.3 to Table 1.7 List of Products, for the product type name.

Note 3. Reserved areas should not be accessed.

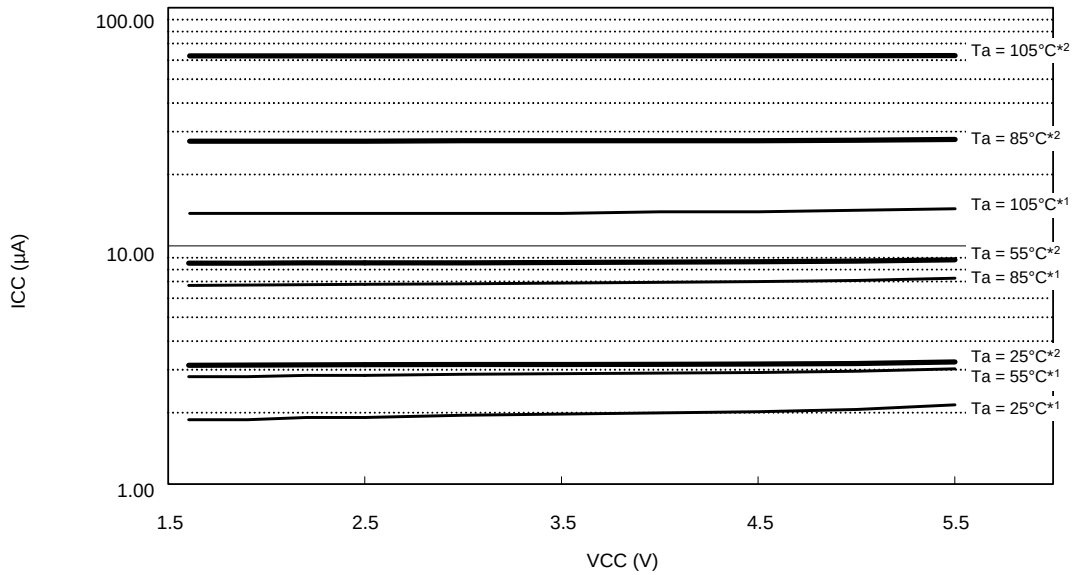
Figure 3.1 Memory Map in Each Operating Mode

Table 4.1 List of I/O Registers (Address Order) (7 / 29)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles ICLK ≥ PCLK	Number of Access Cycles ICLK < PCLK
0008 7179h	ICU	DTC activation enable register 121	DTCER121	8	8		2 ICLK
0008 717Ah	ICU	DTC activation enable register 122	DTCER122	8	8		2 ICLK
0008 717Dh	ICU	DTC activation enable register 125	DTCER125	8	8		2 ICLK
0008 717Eh	ICU	DTC activation enable register 126	DTCER126	8	8		2 ICLK
0008 7181h	ICU	DTC activation enable register 129	DTCER129	8	8		2 ICLK
0008 7182h	ICU	DTC activation enable register 130	DTCER130	8	8		2 ICLK
0008 7183h	ICU	DTC activation enable register 131	DTCER131	8	8		2 ICLK
0008 7184h	ICU	DTC activation enable register 132	DTCER132	8	8		2 ICLK
0008 7186h	ICU	DTC activation enable register 134	DTCER134	8	8		2 ICLK
0008 7187h	ICU	DTC activation enable register 135	DTCER135	8	8		2 ICLK
0008 7188h	ICU	DTC activation enable register 136	DTCER136	8	8		2 ICLK
0008 7189h	ICU	DTC activation enable register 137	DTCER137	8	8		2 ICLK
0008 718Ah	ICU	DTC activation enable register 138	DTCER138	8	8		2 ICLK
0008 718Bh	ICU	DTC activation enable register 139	DTCER139	8	8		2 ICLK
0008 718Ch	ICU	DTC activation enable register 140	DTCER140	8	8		2 ICLK
0008 718Dh	ICU	DTC activation enable register 141	DTCER141	8	8		2 ICLK
0008 718Eh	ICU	DTC activation enable register 142	DTCER142	8	8		2 ICLK
0008 718Fh	ICU	DTC activation enable register 143	DTCER143	8	8		2 ICLK
0008 7190h	ICU	DTC activation enable register 144	DTCER144	8	8		2 ICLK
0008 7191h	ICU	DTC activation enable register 145	DTCER145	8	8		2 ICLK
0008 7193h	ICU	DTC activation enable register 147	DTCER147	8	8		2 ICLK
0008 7194h	ICU	DTC activation enable register 148	DTCER148	8	8		2 ICLK
0008 7197h	ICU	DTC activation enable register 151	DTCER151	8	8		2 ICLK
0008 7198h	ICU	DTC activation enable register 152	DTCER152	8	8		2 ICLK
0008 719Bh	ICU	DTC activation enable register 155	DTCER155	8	8		2 ICLK
0008 719Ch	ICU	DTC activation enable register 156	DTCER156	8	8		2 ICLK
0008 719Dh	ICU	DTC activation enable register 157	DTCER157	8	8		2 ICLK
0008 719Eh	ICU	DTC activation enable register 158	DTCER158	8	8		2 ICLK
0008 71A0h	ICU	DTC activation enable register 160	DTCER160	8	8		2 ICLK
0008 71A1h	ICU	DTC activation enable register 161	DTCER161	8	8		2 ICLK
0008 71A4h	ICU	DTC activation enable register 164	DTCER164	8	8		2 ICLK
0008 71A5h	ICU	DTC activation enable register 165	DTCER165	8	8		2 ICLK
0008 71AEh	ICU	DTC activation enable register 174	DTCER174	8	8		2 ICLK
0008 71AFh	ICU	DTC activation enable register 175	DTCER175	8	8		2 ICLK
0008 71B1h	ICU	DTC activation enable register 177	DTCER177	8	8		2 ICLK
0008 71B2h	ICU	DTC activation enable register 178	DTCER178	8	8		2 ICLK
0008 71B4h	ICU	DTC activation enable register 180	DTCER180	8	8		2 ICLK
0008 71B5h	ICU	DTC activation enable register 181	DTCER181	8	8		2 ICLK
0008 71B7h	ICU	DTC activation enable register 183	DTCER183	8	8		2 ICLK
0008 71B8h	ICU	DTC activation enable register 184	DTCER184	8	8		2 ICLK
0008 71BBh	ICU	DTC activation enable register 187	DTCER187	8	8		2 ICLK
0008 71BCh	ICU	DTC activation enable register 188	DTCER188	8	8		2 ICLK
0008 71BFh	ICU	DTC activation enable register 191	DTCER191	8	8		2 ICLK
0008 71C0h	ICU	DTC activation enable register 192	DTCER192	8	8		2 ICLK
0008 71C3h	ICU	DTC activation enable register 195	DTCER195	8	8		2 ICLK
0008 71C4h	ICU	DTC activation enable register 196	DTCER196	8	8		2 ICLK
0008 71C6h	ICU	DTC activation enable register 198	DTCER198	8	8		2 ICLK
0008 71C7h	ICU	DTC activation enable register 199	DTCER199	8	8		2 ICLK
0008 71C8h	ICU	DTC activation enable register 200	DTCER200	8	8		2 ICLK
0008 71C9h	ICU	DTC activation enable register 201	DTCER201	8	8		2 ICLK
0008 71CFh	ICU	DTC activation enable register 207	DTCER207	8	8		2 ICLK

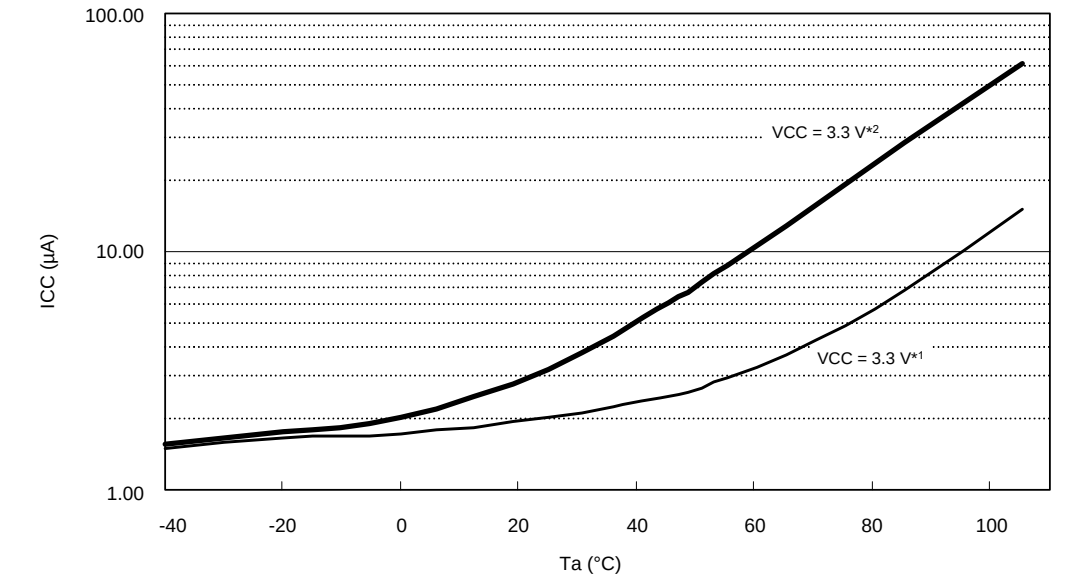
Table 4.1 List of I/O Registers (Address Order) (27 / 29)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles: ICLK ≥ PCLK	Number of Access Cycles: ICLK < PCLK
0008 C16Dh	MPC	P55 pin function control register	P55PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C16Eh	MPC	P56 pin function control register	P56PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C170h	MPC	P60 pin function control register	P60PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C171h	MPC	P61 pin function control register	P61PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C178h	MPC	P70 pin function control register	P70PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C17Ch	MPC	P74 pin function control register	P74PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C17Dh	MPC	P75 pin function control register	P75PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C17Eh	MPC	P76 pin function control register	P76PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C17Fh	MPC	P77 pin function control register	P77PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C180h	MPC	P80 pin function control register	P80PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C181h	MPC	P81 pin function control register	P81PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C182h	MPC	P82 pin function control register	P82PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C183h	MPC	P83 pin function control register	P83PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C186h	MPC	P86 pin function control register	P865PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C187h	MPC	P87 pin function control register	P87PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C188h	MPC	P90 pin function control register	P90PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C189h	MPC	P91 pin function control register	P91PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C18Ah	MPC	P92 pin function control register	P92PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C18Bh	MPC	P93 pin function control register	P93PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C190h	MPC	PA0 pin function control register	PA0PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C191h	MPC	PA1 pin function control register	PA1PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C192h	MPC	PA2 pin function control register	PA2PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C193h	MPC	PA3 pin function control register	PA3PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C194h	MPC	PA4 pin function control register	PA4PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C195h	MPC	PA5 pin function control register	PA5PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C196h	MPC	PA6 pin function control register	PA6PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C197h	MPC	PA7 pin function control register	PA7PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C198h	MPC	PB0 pin function control register	PB0PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C199h	MPC	PB1 pin function control register	PB1PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C19Ah	MPC	PB2 pin function control register	PB2PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C19Bh	MPC	PB3 pin function control register	PB3PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C19Ch	MPC	PB4 pin function control register	PB4PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C19Dh	MPC	PB5 pin function control register	PB5PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C19Eh	MPC	PB6 pin function control register	PB6PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C19Fh	MPC	PB7 pin function control register	PB7PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C1A0h	MPC	PC0 pin function control register	PC0PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C1A1h	MPC	PC1 pin function control register	PC1PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C1A2h	MPC	PC2 pin function control register	PC2PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C1A3h	MPC	PC3 pin function control register	PC3PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C1A4h	MPC	PC4 pin function control register	PC4PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C1A5h	MPC	PC5 pin function control register	PC5PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C1A6h	MPC	PC6 pin function control register	PC6PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C1A7h	MPC	PC7 pin function control register	PC7PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C1A8h	MPC	PD0 pin function control register	PD0PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C1A9h	MPC	PD1 pin function control register	PD1PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C1AAh	MPC	PD2 pin function control register	PD2PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C1ABh	MPC	PD3 pin function control register	PD3PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C1ACh	MPC	PD4 pin function control register	PD4PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C1ADh	MPC	PD5 pin function control register	PD5PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C1AEh	MPC	PD6 pin function control register	PD6PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C1AFh	MPC	PD7 pin function control register	PD7PFS	8	8	2, 3 PCLKB	2 ICLK



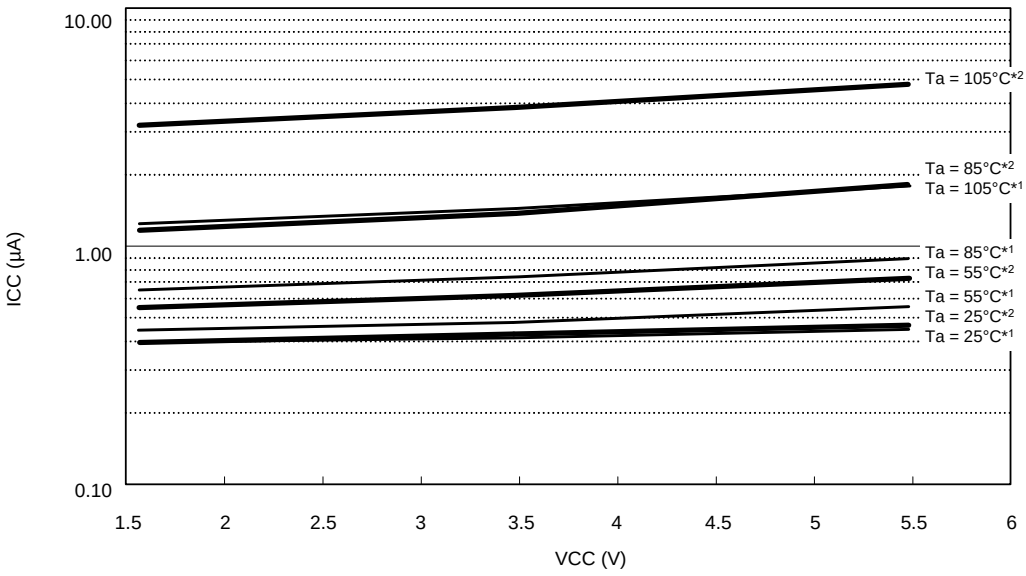
Note 1. Average value of the tested middle samples during product evaluation.
Note 2. Average value of the tested upper-limit samples during product evaluation.

Figure 5.13 Voltage Dependency in Software Standby Mode (SOFTCUT[2:0] Bits = 111b) (Reference Data) for Chip Version C



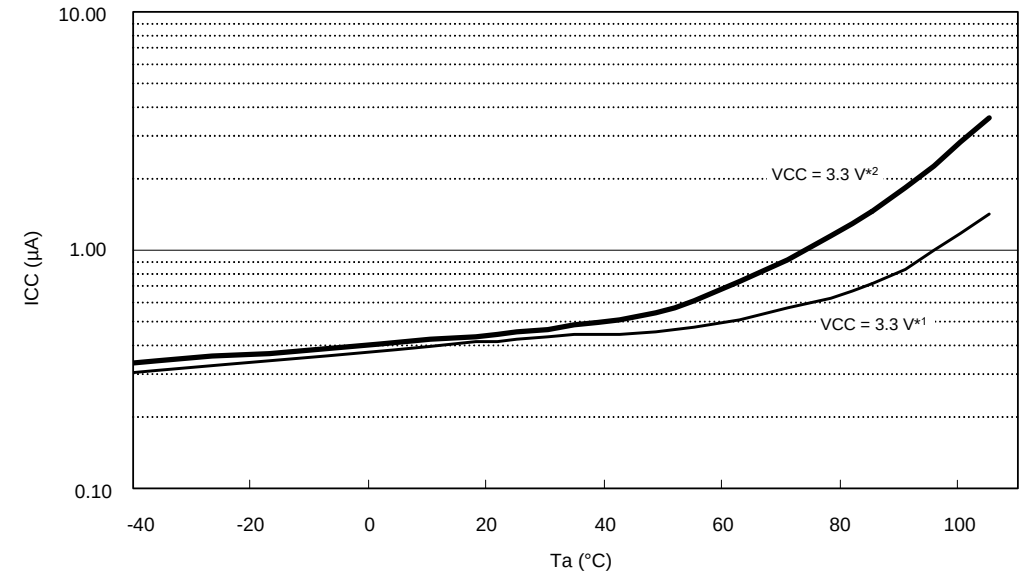
Note 1. Average value of the tested middle samples during product evaluation.
Note 2. Average value of the tested upper-limit samples during product evaluation.

Figure 5.14 Temperature Dependency in Software Standby Mode (SOFTCUT[2:0] Bits = 111b) (Reference Data) for Chip Version C



Note 1. Average value of the tested middle samples during product evaluation.
Note 2. Average value of the tested upper-limit samples during product evaluation.

Figure 5.33 Voltage Dependency in Deep Software Standby Mode (DEEPCUT1 Bit = 1) (Reference Data) for Chip Version B with 768 Kbytes/1 Mbyte of Flash Memory and 100 to 145 Pins



Note 1. Average value of the tested middle samples during product evaluation.
Note 2. Average value of the tested upper-limit samples during product evaluation.

Figure 5.34 Temperature Dependency in Deep Software Standby Mode (DEEPCUT1 Bit = 1) (Reference Data) for Chip Version B with 768 Kbytes/1 Mbyte of Flash Memory and 100 to 145 Pins

[Chip version B]

Table 5.36 Operation Frequency Value (Middle-Speed Operating Mode 2A)

Conditions: VCC = AVCC0 = 1.62 to 5.5 V, VSS = AVSS0 = VREFL = VREFL0 = 0 V, T_a = –40 to +105°C

Item		Symbol	VCC			Unit
			1.62 to 1.8 V	1.8 to 2.7 V	2.7 to 5.5 V	
Maximum operating frequency	System clock (ICLK)	f_{max}	8	16	32	MHz
	FlashIF clock (FCLK)*1		8	16	32	
	Peripheral module clock (PCLKB)		8	16	32	
	Peripheral module clock (PCLKD)*2		8	16	32	
	External bus clock (BCLK)		8	16	25	
	BCLK pin output		8	8	12.5	

Note 1. The VCC is 2.7 to 5.5 V and the lower-limit frequency of FCLK is 4 MHz during programming or erasing of the flash memory.
Note 2. The lower-limit frequency of PCLKD is 1 MHz when the A/D converter is in use.

[Chip version B]

Table 5.37 Operation Frequency Value (Middle-Speed Operating Mode 2B)

Conditions: VCC = AVCC0 = 1.62 to 5.5 V, VSS = AVSS0 = VREFL = VREFL0 = 0 V, T_a = –40 to +105°C

Item		Symbol	VCC			Unit
			1.62 to 1.8 V	1.8 to 2.7 V	2.7 to 5.5 V	
Maximum operating frequency	System clock (ICLK)	f_{max}	8	16	32	MHz
	FlashIF clock (FCLK)*1		8	16	32	
	Peripheral module clock (PCLKB)		8	16	32	
	Peripheral module clock (PCLKD)*2		8	16	32	
	External bus clock (BCLK)		8	16	25	
	BCLK pin output		8	8	12.5	

Note 1. The VCC is 1.62 to 3.6 V and the lower-limit frequency of FCLK is 4 MHz during programming or erasing of the flash memory.
Note 2. The lower-limit frequency of PCLKD is 1 MHz when the A/D converter is in use.

[Chip versions A and C]

Table 5.38 Operation Frequency Value (Low-Speed Operating Mode 1)

Conditions: VCC = AVCC0 = 1.62 to 5.5 V, VSS = AVSS0 = VREFL = VREFL0 = 0 V, T_a = –40 to +105°C

Item		Symbol	VCC			Unit
			1.62 to 1.8 V	1.8 to 2.7 V	2.7 to 5.5 V	
Maximum operating frequency	System clock (ICLK)	f_{max}	1	1	1	MHz
	FlashIF clock (FCLK)*1		1	1	1	
	Peripheral module clock (PCLKB)		1	1	1	
	Peripheral module clock (PCLKD)*2		1	1	1	
	External bus clock (BCLK)		1	1	1	
	BCLK pin output		1	1	1	

Note 1. Programming and erasing the flash memory is impossible.
Note 2. The lower-limit frequency of PCLKD is 1 MHz when the A/D converter is in use.

Table 5.52 Bus Timing (Multiplexed Bus) (1)

Conditions: VCC = AVCC0 = 2.7 to 5.5 V, VSS = AVSS0 = VREFL = VREFL0 = 0 V,
fBCLK ≤ 25 MHz (BCLK pin output frequency ≤ 12.5 MHz), T_a = –40 to +105°C, V_{OH} = VCC × 0.5,
V_{OL} = VCC × 0.5, I_{OH} = –1.0 mA, I_{OL} = 1.0 mA, C_L = 30 pF
When normal output is selected by the drive capacity register

Item	Symbol	Min.	Typ.	Max.	Unit
Address delay time	t_{AD}	—	60	ns	Figure 5.81 and Figure 5.82
Byte control delay time	t_{BCD}	—	60	ns	
CS# delay time	t_{CSD}	—	60	ns	
RD# delay time	t_{RSD}	—	60	ns	
ALE delay time	t_{ALED}	—	60	ns	
Read data setup time	t_{RDS}	40	—	ns	
Read data hold time	t_{RDH}	0	—	ns	
WR# delay time	t_{WRD}	—	60	ns	
Write data delay time	t_{WDD}	—	60	ns	
Write data hold time	t_{WDH}	0	—	ns	
WAIT# setup time	t_{WTS}	40	—	ns	Figure 5.80
WAIT# hold time	t_{WTH}	0	—	ns	

Table 5.53 Bus Timing (Multiplexed Bus) (2)

Conditions: VCC = AVCC0 = 1.8 to 2.7 V, VSS = AVSS0 = VREFL = VREFL0 = 0 V,
fBCLK ≤ 16 MHz (BCLK pin output frequency ≤ 8 MHz), T_a = –40 to +105°C, V_{OH} = VCC × 0.5,
V_{OL} = VCC × 0.5, I_{OH} = –1.0 mA, I_{OL} = 1.0 mA, C_L = 30 pF
When normal output is selected by the drive capacity register

Item	Symbol	Min.	Typ.	Max.	Unit
Address delay time	t_{AD}	—	90	ns	Figure 5.81 and Figure 5.82
Byte control delay time	t_{BCD}	—	90	ns	
CS# delay time	t_{CSD}	—	90	ns	
RD# delay time	t_{RSD}	—	90	ns	
ALE delay time	t_{ALED}	—	90	ns	
Read data setup time	t_{RDS}	60	—	ns	
Read data hold time	t_{RDH}	0	—	ns	
WR# delay time	t_{WRD}	—	90	ns	
Write data delay time	t_{WDD}	—	90	ns	
Write data hold time	t_{WDH}	0	—	ns	
WAIT# setup time	t_{WTS}	60	—	ns	Figure 5.80
WAIT# hold time	t_{WTH}	0	—	ns	

[512 Kbytes or less of flash memory and 48 to 100 pins]

Table 5.56 Timing of On-Chip Peripheral Modules (2)

Conditions: VCC = AVCC0 = 1.62 to 5.5 V, VSS = AVSS0 = VREFL = VREFL0 = 0 V, T_a = –40 to +105°C
When high-drive output is selected by the drive capacity register

Item				Symbol	Min.	Max.	Unit*1	Test Conditions
RSPI	RSPCK clock cycle	Master		t_{SPcyc}	2	4096	t_{Pcyc}	C = 30 pF Figure 5.91
					125	—	ns	
		Slave			8	4096	t_{Pcyc}	
	RSPCK clock high pulse width	Master	2.7 V ≤ VCC ≤ 5.5 V	t_{SPCKWH}	$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf})/2 - 3$	—	ns	
			1.8 V ≤ VCC < 2.7 V		$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf})/2 - 3$	—		
			1.62 V ≤ VCC < 1.8 V		$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf})/2 - 10$	—		
		Slave			$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf})/2$	—		
	RSPCK clock low pulse width	Master	2.7 V ≤ VCC ≤ 5.5 V	t_{SPCKWL}	$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf})/2 - 3$	—	ns	
			1.8 V ≤ VCC < 2.7 V		$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf})/2 - 3$	—		
			1.62 V ≤ VCC < 1.8 V		$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf})/2 - 10$	—		
		Slave			$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf})/2$	—		
	RSPCK clock rise/fall time	Output	2.7 V ≤ VCC ≤ 5.5 V	t_{SPCKr}, t_{SPCKf}	—	10	ns	
			1.8 V ≤ VCC < 2.7 V		—	15		
			1.62 V ≤ VCC < 1.8 V		—	20		
		Input			—	1	µs	
	Data input setup time	Master	2.7 V ≤ VCC ≤ 5.5 V	t_{SU}	50	—	ns	C = 30 pF Figure 5.92 to Figure 5.97
			1.8 V ≤ VCC < 2.7 V		65	—		
			1.62 V ≤ VCC < 1.8 V		75	—		
		Slave			$25 - t_{Pcyc}$	—		
	Data input hold time	Master		t_H	t_{Pcyc}	—	ns	
		Slave			$20 + 2 \times t_{Pcyc}$	—		
	SSL setup time	Master		t_{LEAD}	1	8	t_{SPcyc}	
		Slave			4	—	t_{Pcyc}	
	SSL hold time	Master		t_{LAG}	1	8	t_{SPcyc}	
		Slave			4	—	t_{Pcyc}	
	Data output delay time	Master	2.7 V ≤ VCC ≤ 5.5 V	t_{OD}	—	50	ns	
			1.8 V ≤ VCC < 2.7 V		—	55		
			1.62 V ≤ VCC < 1.8 V		—	60		
		Slave	2.7 V ≤ VCC ≤ 5.5 V		—	$3 \times t_{Pcyc} + 65$		
			1.8 V ≤ VCC < 2.7 V		—	$3 \times t_{Pcyc} + 85$		
			1.62 V ≤ VCC < 1.8 V		—	$3 \times t_{Pcyc} + 95$		
	Data output hold time	Master		t_{OH}	0	—	ns	
		Slave			0	—		
	Successive transmission delay time	Master		t_{TD}	$t_{SPcyc} + 2 \times t_{Pcyc}$	$8 \times t_{SPcyc} + 2 \times t_{Pcyc}$	ns	
		Slave			$4 \times t_{Pcyc}$	—		

Item				Symbol	Min.	Max.	Unit*1	Test Conditions
RSPI	MOSI and MISO rise/fall time	Output		t_{Dr}, t_{Df}	—	20	ns	C = 30 pF Figure 5.92 to Figure 5.97
		Input			—	1	μs	
	SSL rise/fall time	Output		t_{SSLr}, t_{SSLf}	—	20	ns	
		Input			—	1	μs	
	Slave access time		2.7 V ≤ VCC ≤ 5.5 V	t_{SA}	—	6	t_{Pcyc}	C = 30 pF Figure 5.96 and Figure 5.97
			1.8 V ≤ VCC < 2.7 V		—	7		
			1.62 V ≤ VCC < 1.8 V		—	7		
	Slave output release time		2.7 V ≤ VCC ≤ 5.5 V	t_{REL}	—	5	t_{Pcyc}	
			1.8 V ≤ VCC < 2.7 V		—	6		
			1.62 V ≤ VCC < 1.8 V		—	6		

Note 1. t_{Pcyc}: PCLK cycle

[768 Kbytes/1 Mbyte of flash memory or 144/145 pins]

Table 5.57 Timing of On-Chip Peripheral Modules (3)

Conditions: VCC = AVCC0 = 1.62 to 5.5 V, VSS = AVSS0 = VREFL = VREFL0 = 0 V, T_a = –40 to +105°C
When high-drive output is selected by the drive capacity register

Item				Symbol	Min.	Max.	Unit*1	Test Conditions
RSPI	RSPCK clock cycle	Master		t_{SPcyc}	2	4096	t_{Pcyc}	C = 30pF Figure 5.91
		Slave			8	4096		
	RSPCK clock high pulse width	Master	2.7 V ≤ VCC ≤ 5.5 V	t_{SPCKWH}	$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf})/2 - 3$	—	ns	
			1.8 V ≤ VCC < 2.7 V		$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf})/2 - 3$	—		
			1.62 V ≤ VCC < 1.8 V		$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf})/2 - 10$	—		
		Slave			$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf})/2$	—		
	RSPCK clock low pulse width	Master	2.7 V ≤ VCC ≤ 5.5 V	t_{SPCKWL}	$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf})/2 - 3$	—	ns	
			1.8 V ≤ VCC < 2.7 V		$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf})/2 - 3$	—		
			1.62 V ≤ VCC < 1.8 V		$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf})/2 - 10$	—		
		Slave			$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf})/2$	—		
	RSPCK clock rise/fall time	Output	2.7 V ≤ VCC ≤ 5.5 V	t_{SPCKr}, t_{SPCKf}	—	10	ns	
			1.8 V ≤ VCC < 2.7 V		—	15		
			1.62 V ≤ VCC < 1.8 V		—	20		
		Input			—	1	μs	

Table 5.60 Timing of On-Chip Peripheral Modules (6)

Conditions: VCC = AVCC0 = 2.7 to 5.5 V, VSS = AVSS0 = VREFL = VREFL0 = 0 V, fPCLKB = up to 32 MHz,
T_a = –40 to +105°C
When high-drive output is selected by the drive capacity register

Item		Symbol	Min.*1	Max.	Unit	Test Conditions
Simple IIC (Standard mode)	SDA input rise time	t_{Sr}	—	1000	ns	Figure 5.98
	SDA input fall time	t_{Sf}	—	300	ns	
	SDA input spike pulse removal time	t_{SP}	0	$4 \times t_{pcyc}$*2	ns	
	Data input setup time	t_{SDAS}	250	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b	—	400	pF	
Simple IIC (Fast mode)	SCL, SDA input rise time	t_{Sr}	$20 + 0.1C_b$	300	ns	Figure 5.98
	SCL, SDA input fall time	t_{Sf}	$20 + 0.1C_b$	300	ns	
	SCL, SDA input spike pulse removal time	t_{SP}	0	$4 \times t_{pcyc}$*2	ns	
	Data input setup time	t_{SDAS}	100	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b	—	400	pF	

Note: • t_{Pcyc}: PCLK cycle
Note 1. C_b indicates the total capacity of the bus line.
Note 2. This applies when the SMR.CKS[1:0] bits = 00b and the SNFR.NFCS[2:0] bits = 010b while the SNFR.NFE bit = 1 and the digital filter is enabled.

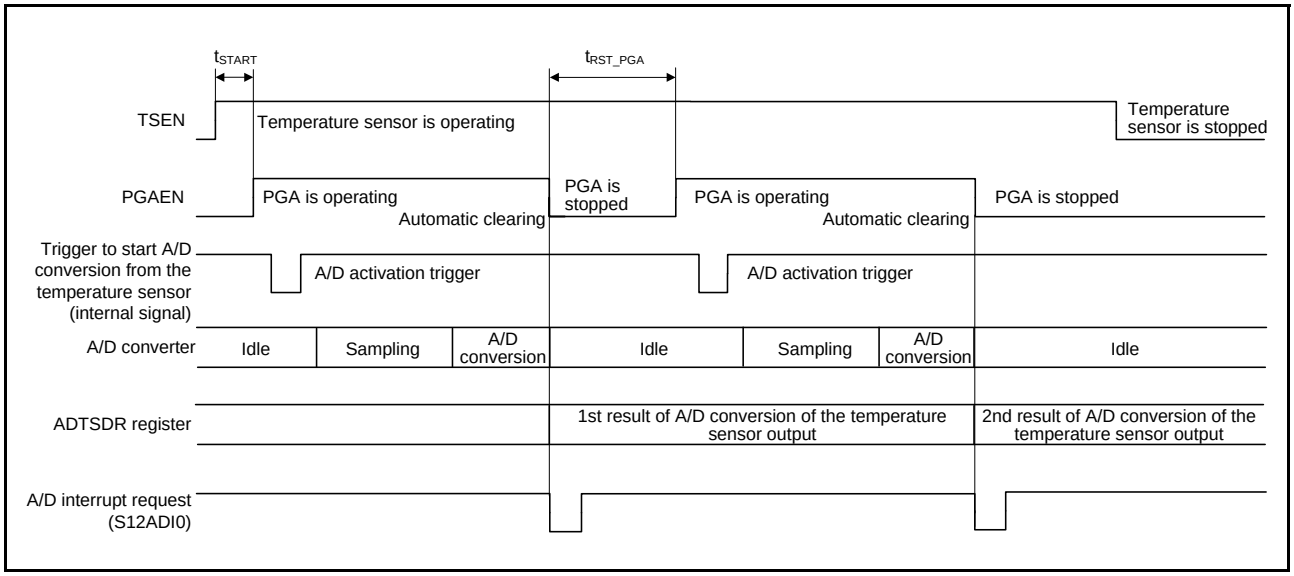


Figure 5.102 A/D Conversion Timing Example of the Temperature Sensor (Two Conversions Performed)

5.7 Comparator Characteristics

Table 5.70 Comparator Characteristics

Conditions: VCC = AVCC0 = 1.62 to 5.5 V, VSS = AVSS0 = VREFL = VREFL0 = 0 V, T_a = –40 to +105°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Comparator A	External reference voltage input range	LVREF	1.4	—	VCC	V	
	External comparison voltage (CMPA1, CMPA2) input range	VI	–0.3	—	VCC + 0.3	V	
	Offset	—	—	±50	±150	mV	
	Comparator output delay time*1	—	—	3	—	µs	At falling edge VI = LVREF – 110 mV
			—	2	—	µs	At falling edge VI < LVREF – 1 V
			—	3	—	µs	At rising edge VI = LVREF + 160 mV
			—	1.5	—	µs	At rising edge VI > LVREF + 1 V
	Comparator operating current	ICMPA	—	0.5	—	µA	VCC = 5.0 V
Comparator B	Input reference voltage for CVREFB0, CVREFB1	VREF	0	—	VCC – 1.4	V	
	Input voltage for CMPB0, CMPB1	VI	–0.3	—	VCC + 0.3	V	
	Offset	—	—	±10	±100	mV	
	Comparator output delay time	t_d	—	—	1	µs	VI = VREF + 100 mV
	Comparator operating current	ICMPB	—	75	150	µA	VCC = 5.0 V For total two channels

Note 1. When the digital filter is disabled.

5.8 Power-on Reset Circuit and Voltage Detection Circuit Characteristics

Table 5.71 Power-on Reset Circuit and Voltage Detection Circuit Characteristics (1)

Conditions: VCC = AVCC0, VSS = AVSS0 = VREFL = VREFL0 = 0 V, T_a = –40 to +105°C

Item			Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Voltage detection level	Power-on reset (POR)	Low power consumption function disabled*1	V_{POR}	1.30	1.40	1.55	V	Figure 5.103 and Figure 5.104
		Low power consumption function enabled*2		1.00	1.20	1.45		
	Voltage detection circuit (LVD0)*3		V_{det0_0}	3.65	3.80	3.95	V	Figure 5.105
			V_{det0_1}	2.70	2.80	2.90		
			V_{det0_2}	1.80	1.90	2.00		
			V_{det0_3}	1.62	1.72	1.82		
	Voltage detection circuit (LVD1)*4		V_{det1_0}	4.00	4.15	4.30	V	Figure 5.106
			V_{det1_1}	3.85	4.00	4.15		
			V_{det1_2}	3.70	3.85	4.00		At falling edge VCC
			V_{det1_3}	3.55	3.70	3.85		
			V_{det1_4}	3.40	3.55	3.70		
			V_{det1_5}	3.25	3.40	3.55		
			V_{det1_6}	3.10	3.25	3.40		
			V_{det1_7}	2.95	3.10	3.25		
			V_{det1_8}	2.85	2.95	3.05		
			V_{det1_9}	2.70	2.80	2.90		
			V_{det1_A}	2.55	2.65	2.75		
			V_{det1_B}	2.40	2.50	2.60		
			V_{det1_C}	2.25	2.35	2.45		
			V_{det1_D}	2.10	2.20	2.30		
			V_{det1_E}	1.95	2.05	2.15		
			V_{det1_F}	1.80	1.90	2.00		

Note: • These characteristics apply when noise is not superimposed on the power supply.

Note 1. When the CPU is in a mode other than software standby and deep software standby modes, when the CPU transits to software standby mode with the FHSSBYCR.SOFTCUT[2] bit set to 0, or when the CPU transits to deep software standby mode with the DPSBYCR.DEEPCUT1 bit set to 0.

Note 2. When the CPU transits to software standby mode with the FHSSBYCR.SOFTCUT[2] bit set to 1 or when the CPU transits to deep software standby mode with the DPSBYCR.DEEPCUT1 bit set to 1.

Note 3. # in the symbol Vdet0_# denotes the value of the LDSEL[1:0] bits.

Note 4. # in the symbol Vdet1_# denotes the value of the LVDLVLR.LVD1LVL[3:0] bits.

5.9 Oscillation Stop Detection Timing

Table 5.73 Oscillation Stop Detection Circuit Characteristics

Conditions: VCC = AVCC0 = 1.62 to 5.5 V, VSS = AVSS0 = VREFL = VREFL0 = 0 V, T_a = –40 to +105°C

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Detection time	t_{dr}	—	—	1	ms	Figure 5.108

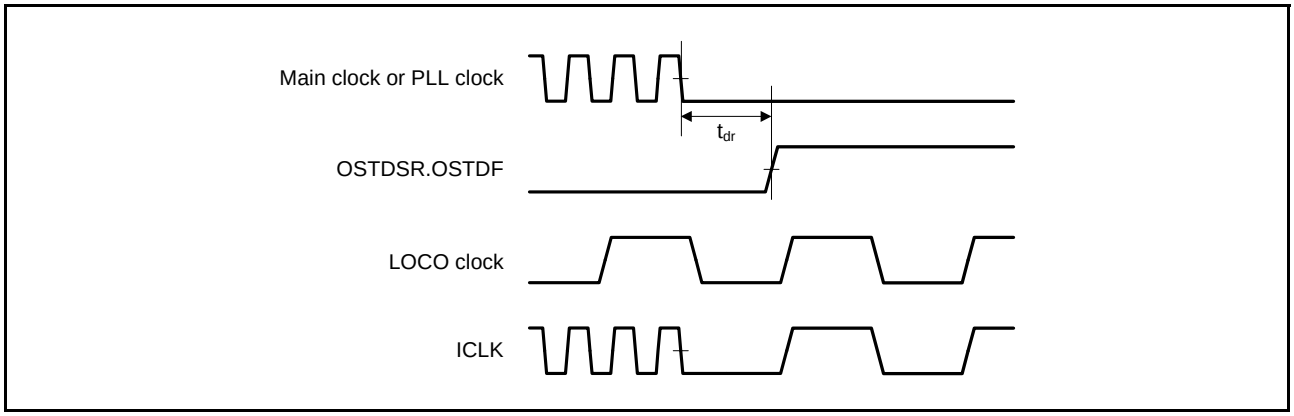


Figure 5.108 Oscillation Stop Detection Timing

5.10 ROM (Flash Memory for Code Storage) Characteristics

[Chip version A]

Table 5.74 ROM (Flash Memory for Code Storage) Characteristics (1)

Item	Symbol	Min.	Typ.	Max.	Unit	Conditions
Reprogramming/erasure cycle*1	N_{PEC}	1000	—	—	Times	
Data hold time	t_{DRP}	10*2	—	—	Year	

Note 1. Definition of reprogram/erase cycle: The reprogram/erase cycle is the number of erasing for each block. When the reprogram/erase cycle is n times (n = 1000), erasing can be performed n times for each block. For instance, when 128-byte programming is performed 16 times for different addresses in 2-Kbyte block and then the entire block is erased, the reprogram/erase cycle is counted as one. However, programming the same address for several times as one erasing is not enabled (overwriting is prohibited).

Note 2. This result is obtained from reliability testing.

[Chip versions B and C]

Table 5.75 ROM (Flash Memory for Code Storage) Characteristics (2)

Item		Symbol	Min.	Typ.	Max.	Unit	Conditions
Reprogramming/erasure cycle*1		N_{PEC}	10000	—	—	Times	
Data hold time	After 1000 times of N_{PEC}	t_{DRP}	30*2	—	—	Year	Ta = +85°C
	After 10000 times of N_{PEC}		1*2	—	—	Year	

Note 1. Definition of reprogram/erase cycle: The reprogram/erase cycle is the number of erasing for each block. When the reprogram/erase cycle is n times (n = 1000), erasing can be performed n times for each block. For instance, when 128-byte programming is performed 16 times for different addresses in 2-Kbyte block and then the entire block is erased, the reprogram/erase cycle is counted as one. However, programming the same address for several times as one erasing is not enabled (overwriting is prohibited).

Note 2. This result is obtained from reliability testing.

[Chip versions A and C]

Table 5.77 ROM (Flash Memory for Code Storage) Characteristics (4) : middle-speed operating mode 1B

Conditions: VCC = AVCC0 = 1.62 to 3.6 V, VREFH = VREFH0 = AVCC0, VSS = AVSS0 = VREFL = VREFL0 = 0 V
Temperature range for the programming/erasure operation: T_a = –40 to +105°C

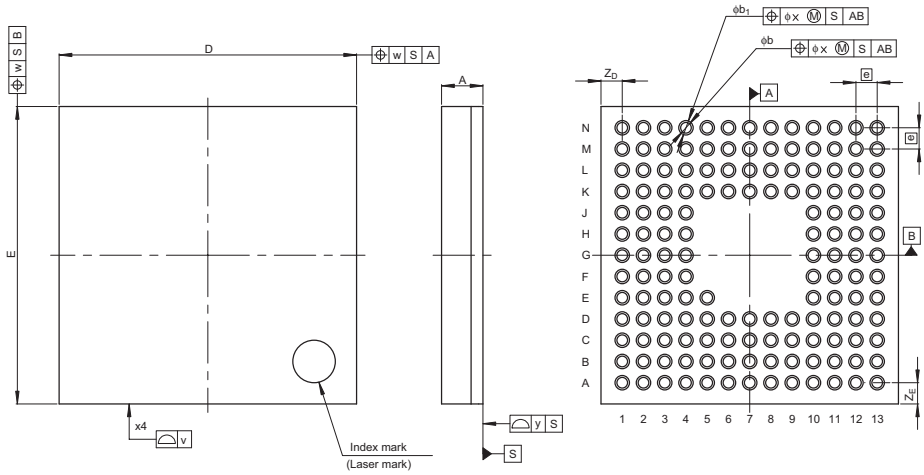
Item		Symbol	FCLK = 4 MHz			FCLK = 32 MHz*1			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Programming time when N_{PEC} ≤ 100 times	2 bytes	t_{P2}	—	0.69	6.0	—	0.30	3.5	ms
	8 bytes	t_{P8}	—	0.69	6.0	—	0.30	3.5	
	128 bytes	t_{P128}	—	1.76	14.2	—	0.85	8.3	
Programming time when N_{PEC} > 100 times	2 bytes	t_{P2}	—	0.81	7.1	—	0.35	4.2	ms
	8 bytes	t_{P8}	—	0.81	7.6	—	0.35	4.5	
	128 bytes	t_{P128}	—	1.99	17.5	—	0.96	10	
Erasure time when N_{PEC} ≤ 100 times	2 Kbytes	t_{E2K}	—	24.5	113.7	—	19.0	46	ms
Erasure time when N_{PEC} > 100 times	2 Kbytes	t_{E2K}	—	29.8	225.8	—	23.2	90 (1000 times ≥ N_{PEC} > 100 times), 98 (10000 times ≥ N_{PEC} > 1000 times)	ms
Suspend delay time during programming (in programming/erasure priority mode)		t_{SPD}	—	—	1.7	—	—	1.6	ms
First suspend delay time during programming (in suspend priority mode)		t_{SPSD1}	—	—	220	—	—	120	µs
Second suspend delay time during programming (in suspend priority mode)		t_{SPSD2}	—	—	1.7	—	—	1.6	ms
Suspend delay time during erasing (in programming/erasure priority mode)		t_{SED}	—	—	1.7	—	—	1.6	ms
First suspend delay time during erasing (in suspend priority mode)		t_{SESD1}	—	—	220	—	—	120	µs
Second suspend delay time during erasing (in suspend priority mode)		t_{SESD2}	—	—	1.7	—	—	1.6	ms
FCU reset time		t_{FCUR}	20 µs or longer and FCLK × 6 or greater	—	—	20 µs or longer and FCLK × 6 or greater	—	—	µs

Note 1. The operating frequency is 20 MHz (max.) when the voltage is in the range from 1.62 V to less than 1.8 V.

Appendix 1. Package Dimensions

Information on the latest version of the package dimensions or mountings has been displayed in “Packages” on Renesas Electronics Corporation website.

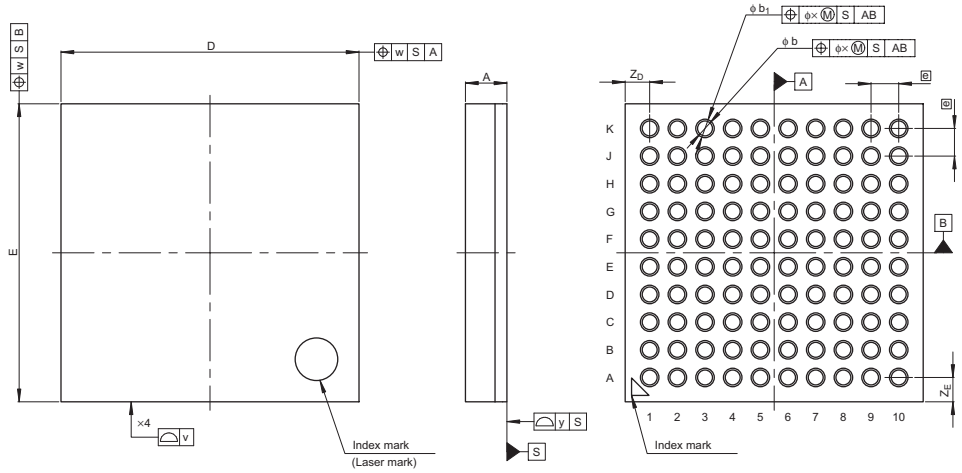
JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-TFLGA145-7x7-0.50	PTLG0145KA-A	145F0G	0.1g



Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	—	7.0	—
E	—	7.0	—
v	—	—	0.15
w	—	—	0.20
A	—	—	1.05
e	—	0.5	—
b	0.21	0.25	0.29
b_1	0.29	0.34	0.39
x	—	—	0.08
y	—	—	0.08
Z_D	—	0.5	—
Z_E	—	0.5	—

Figure A 145-Pin TFLGA (PTLG0145KA-A)

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-TFLGA100-7x7-0.65	PTLG0100JA-A	100F0G	0.1g



Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	—	7.0	—
E	—	7.0	—
v	—	—	0.15
w	—	—	0.20
A	—	—	1.05
e	—	0.65	—
b	0.31	0.35	0.39
b_1	0.385	0.435	0.485
x	—	—	0.08
y	—	—	0.10
Z_D	—	0.575	—
Z_E	—	0.575	—

Figure C 100-Pin TFLGA (PTLG0100JA-A)