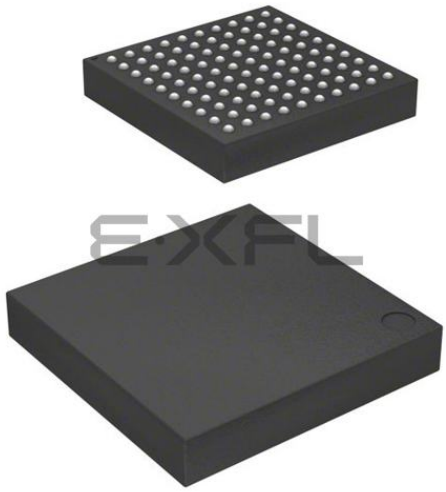

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	RX
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	EBI/EMI, I²C, SCI, SPI
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	84
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	8K x 8
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	1.62V ~ 5.5V
Data Converters	A/D 16x12b; D/A 2x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TFLGA
Supplier Device Package	100-TFLGA (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f52108cdlj-u0

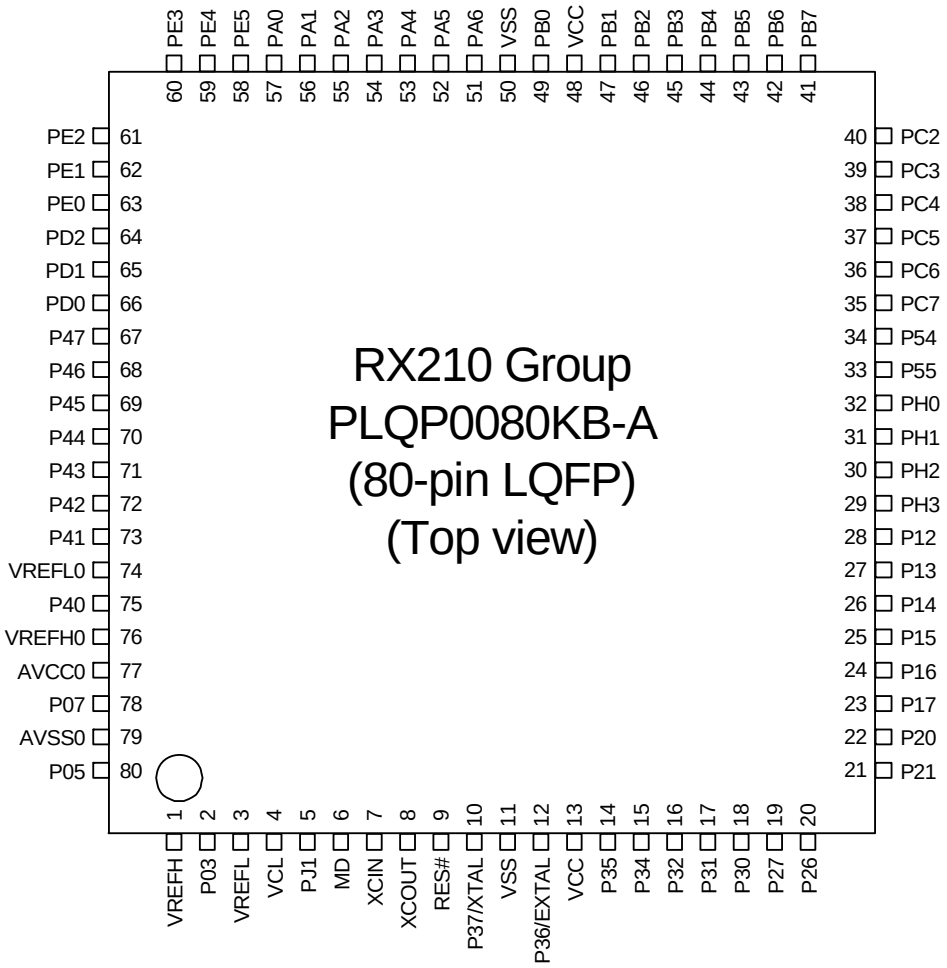
1.2 List of Products

Table 1.3 to Table 1.7 are a list of products, and Figure 1.1 shows how to read the product part no., memory capacity, and package type.

Table 1.3 List of Products Chip Version A: D Version (Ta = –40 to +85°C)

Group	Part No.	Orderable Part No.	Package	ROM Capacity	RAM Capacity	E2 DataFlash	Operating Frequency (Max.)	Operating Temperature
RX210	R5F52108ADFP	R5F52108ADFP#V0	PLQP0100KB-A	512 Kbytes	64 Kbytes	8 Kbytes	50 MHz	–40 to +85°C
	R5F52108ADFN	R5F52108ADFN#V0	PLQP0080KB-A					
	R5F52108ADFM	R5F52108ADFM#V0	PLQP0064KB-A					
	R5F52108ADLJ	R5F52108ADLJ#U0	PTLG0100JA-A					
	R5F52107ADFP	R5F52107ADFP#V0	PLQP0100KB-A	384 Kbytes				
	R5F52107ADFN	R5F52107ADFN#V0	PLQP0080KB-A					
	R5F52107ADFM	R5F52107ADFM#V0	PLQP0064KB-A					
	R5F52107ADLJ	R5F52107ADLJ#U0	PTLG0100JA-A					
	R5F52106ADFP	R5F52106ADFP#V0	PLQP0100KB-A	256 Kbytes	32 Kbytes			
	R5F52106ADFN	R5F52106ADFN#V0	PLQP0080KB-A					
	R5F52106ADFM	R5F52106ADFM#V0	PLQP0064KB-A					
	R5F52106ADLJ	R5F52106ADLJ#U0	PTLG0100JA-A					
	R5F52105ADFP	R5F52105ADFP#V0	PLQP0100KB-A	128 Kbytes	20 Kbytes			
	R5F52105ADFN	R5F52105ADFN#V0	PLQP0080KB-A					
	R5F52105ADFM	R5F52105ADFM#V0	PLQP0064KB-A					
	R5F52105ADLJ	R5F52105ADLJ#U0	PTLG0100JA-A					

Note: • Orderable part numbers are current as of when this manual was published. Please make sure to refer to the relevant product page on the Renesas website for the latest part numbers.



Note: • This figure indicates the power supply pins and I/O port pins. For the pin configuration, see the table “List of Pins and Pin Functions (80-Pin LQFP)”.

Figure 1.7 Pin Assignments of the 80-Pin LQFP

Table 1.10 List of Pins and Pin Functions (144-Pin LQFP) (4 / 4)

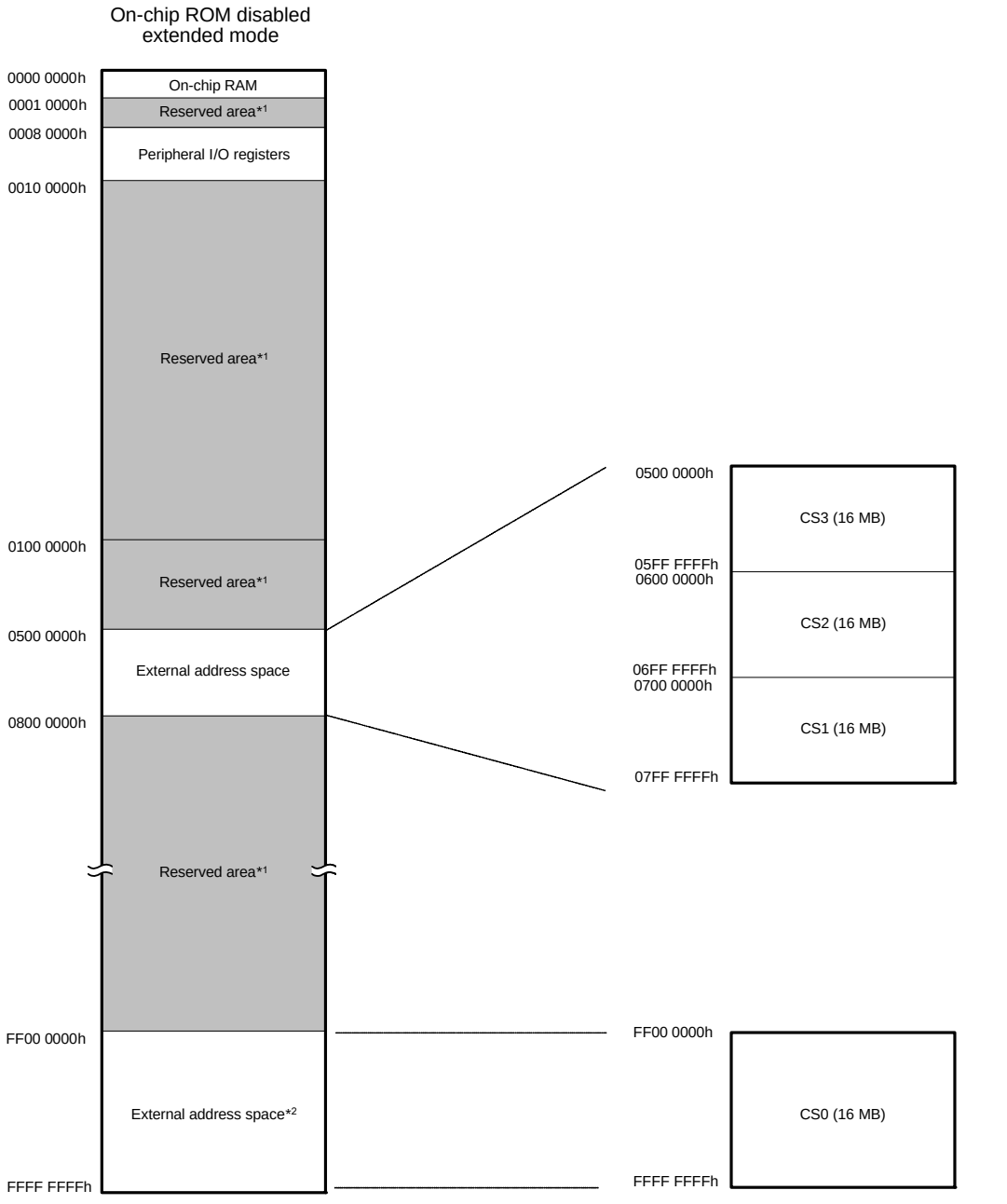
Pin No.	Power Supply, Clock, System Control	I/O Port	External Bus	Timers (MTU, TMR, POE)	Communications (SCIc, SCId, RSPI, RIIC)	Others
122		PD4	D4[A4/D4]	POE3#		IRQ4
123		PD3	D3[A3/D3]	POE8#		IRQ3
124		PD2	D2[A2/D2]	MTIOC4D		IRQ2
125		PD1	D1[A1/D1]	MTIOC4B		IRQ1
126		PD0	D0[A0/D0]			IRQ0
127		P93			CTS7#/RTS7#/SS7#	
128		P92			RXD7/SMISO7/SSCL7	
129		P91			SCK7	
130	VSS					
131		P90			TXD7/SMOSI7/SSDA7	
132	VCC					
133		P47				AN007
134		P46				AN006
135		P45				AN005
136		P44				AN004
137		P43				AN003
138		P42				AN002
139		P41				AN001
140	VREFL0					
141		P40				AN000
142	VREFH0					
143	AVCC0					
144		P07				ADTRG0#

Note: • Pin names to which –DS is appended are for pins that can be used to trigger release from deep software standby mode.
Note: • Leave the NC pin open.

3.2 External Address Space

The external address space is divided into up to four CS areas (CS0 to CS3), each corresponding to the CSn# signal output from a CSn# (n = 0 to 3) pin.

Figure 3.2 shows the address ranges corresponding to the individual CS areas (CS0 to CS3) in on-chip ROM disabled extended mode.



Note 1. Reserved areas should not be accessed.

Note 2. The CS0 area is disabled in on-chip ROM enabled extended mode. In this mode, the address space for addresses above 0800 0000h is as shown in figure on this section “Memory Map in Each Operating Mode”.

Figure 3.2 Correspondence between External Address Spaces and CS Areas (In On-Chip ROM Disabled Extended Mode)

Table 4.1 List of I/O Registers (Address Order) (2 / 29)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles ICLK ≥ PCLK	Number of Access Cycles ICLK < PCLK
0008 201Dh	DMAC0	DMA software start register	DMREQ	8	8	2 ICLK	
0008 201Eh	DMAC0	DMA status register	DMSTS	8	8	2 ICLK	
0008 201Fh	DMAC0	DMA activation source flag control register	DMCSL	8	8	2 ICLK	
0008 2040h	DMAC1	DMA source address register	DMSAR	32	32	2 ICLK	
0008 2044h	DMAC1	DMA destination address register	DMDAR	32	32	2 ICLK	
0008 2048h	DMAC1	DMA transfer count register	DMCRA	32	32	2 ICLK	
0008 204Ch	DMAC1	DMA block transfer count register	DMCRB	16	16	2 ICLK	
0008 2050h	DMAC1	DMA transfer mode register	DMTMD	16	16	2 ICLK	
0008 2053h	DMAC1	DMA interrupt setting register	DMINT	8	8	2 ICLK	
0008 2054h	DMAC1	DMA address mode register	DMAMD	16	16	2 ICLK	
0008 205Ch	DMAC1	DMA transfer enable register	DMCNT	8	8	2 ICLK	
0008 205Dh	DMAC1	DMA software start register	DMREQ	8	8	2 ICLK	
0008 205Eh	DMAC1	DMA status register	DMSTS	8	8	2 ICLK	
0008 205Fh	DMAC1	DMA activation source flag control register	DMCSL	8	8	2 ICLK	
0008 2080h	DMAC2	DMA source address register	DMSAR	32	32	2 ICLK	
0008 2084h	DMAC2	DMA destination address register	DMDAR	32	32	2 ICLK	
0008 2088h	DMAC2	DMA transfer count register	DMCRA	32	32	2 ICLK	
0008 208Ch	DMAC2	DMA block transfer count register	DMCRB	16	16	2 ICLK	
0008 2090h	DMAC2	DMA transfer mode register	DMTMD	16	16	2 ICLK	
0008 2093h	DMAC2	DMA interrupt setting register	DMINT	8	8	2 ICLK	
0008 2094h	DMAC2	DMA address mode register	DMAMD	16	16	2 ICLK	
0008 209Ch	DMAC2	DMA transfer enable register	DMCNT	8	8	2 ICLK	
0008 209Dh	DMAC2	DMA software start register	DMREQ	8	8	2 ICLK	
0008 209Eh	DMAC2	DMA status register	DMSTS	8	8	2 ICLK	
0008 209Fh	DMAC2	DMA activation source flag control register	DMCSL	8	8	2 ICLK	
0008 20C0h	DMAC3	DMA source address register	DMSAR	32	32	2 ICLK	
0008 20C4h	DMAC3	DMA destination address register	DMDAR	32	32	2 ICLK	
0008 20C8h	DMAC3	DMA transfer count register	DMCRA	32	32	2 ICLK	
0008 20CCh	DMAC3	DMA block transfer count register	DMCRB	16	16	2 ICLK	
0008 20D0h	DMAC3	DMA transfer mode register	DMTMD	16	16	2 ICLK	
0008 20D3h	DMAC3	DMA interrupt setting register	DMINT	8	8	2 ICLK	
0008 20D4h	DMAC3	DMA address mode register	DMAMD	16	16	2 ICLK	
0008 20DCh	DMAC3	DMA transfer enable register	DMCNT	8	8	2 ICLK	
0008 20DDh	DMAC3	DMA software start register	DMREQ	8	8	2 ICLK	
0008 20DEh	DMAC3	DMA status register	DMSTS	8	8	2 ICLK	
0008 20DFh	DMAC3	DMA activation source flag control register	DMCSL	8	8	2 ICLK	
0008 2200h	DMAC	DMA module activation register	DMAST	8	8	2 ICLK	
0008 2400h	DTC	DTC control register	DTCCR	8	8	2 ICLK	
0008 2404h	DTC	DTC vector base register	DTCVBR	32	32	2 ICLK	
0008 2408h	DTC	DTC address mode register	DTCADMOD	8	8	2 ICLK	
0008 240Ch	DTC	DTC module start register	DTCST	8	8	2 ICLK	
0008 240Eh	DTC	DTC status register	DTCSTS	16	16	2 ICLK	
0008 3002h	BSC	CS0 mode register	CS0MOD	16	16	1, 2 BCLK	
0008 3004h	BSC	CS0 wait control register 1	CS0WCR1	32	32	1, 2 BCLK	
0008 3008h	BSC	CS0 wait control register 2	CS0WCR2	32	32	1, 2 BCLK	
0008 3012h	BSC	CS1 mode register	CS1MOD	16	16	1, 2 BCLK	
0008 3014h	BSC	CS1 wait control register 1	CS1WCR1	32	32	1, 2 BCLK	
0008 3018h	BSC	CS1 wait control register 2	CS1WCR2	32	32	1, 2 BCLK	
0008 3022h	BSC	CS2 mode register	CS2MOD	16	16	1, 2 BCLK	
0008 3024h	BSC	CS2 wait control register 1	CS2WCR1	32	32	1, 2 BCLK	
0008 3028h	BSC	CS2 wait control register 2	CS2WCR2	32	32	1, 2 BCLK	

Table 4.1 List of I/O Registers (Address Order) (5 / 29)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles ICLK ≥ PCLK	Number of Access Cycles ICLK < PCLK
0008 70ABh	ICU	Interrupt request register 171	IR171	8	8		2 ICLK
0008 70AEh	ICU	Interrupt request register 174	IR174	8	8		2 ICLK
0008 70AFh	ICU	Interrupt request register 175	IR175	8	8		2 ICLK
0008 70B0h	ICU	Interrupt request register 176	IR176	8	8		2 ICLK
0008 70B1h	ICU	Interrupt request register 177	IR177	8	8		2 ICLK
0008 70B2h	ICU	Interrupt request register 178	IR178	8	8		2 ICLK
0008 70B3h	ICU	Interrupt request register 179	IR179	8	8		2 ICLK
0008 70B4h	ICU	Interrupt request register 180	IR180	8	8		2 ICLK
0008 70B5h	ICU	Interrupt request register 181	IR181	8	8		2 ICLK
0008 70B6h	ICU	Interrupt request register 182	IR182	8	8		2 ICLK
0008 70B7h	ICU	Interrupt request register 183	IR183	8	8		2 ICLK
0008 70B8h	ICU	Interrupt request register 184	IR184	8	8		2 ICLK
0008 70B9h	ICU	Interrupt request register 185	IR185	8	8		2 ICLK
0008 70BAh	ICU	Interrupt request register 186	IR186	8	8		2 ICLK
0008 70BBh	ICU	Interrupt request register 187	IR187	8	8		2 ICLK
0008 70BCh	ICU	Interrupt request register 188	IR188	8	8		2 ICLK
0008 70BDh	ICU	Interrupt request register 189	IR189	8	8		2 ICLK
0008 70BEh	ICU	Interrupt request register 190	IR190	8	8		2 ICLK
0008 70BFh	ICU	Interrupt request register 191	IR191	8	8		2 ICLK
0008 70C0h	ICU	Interrupt request register 192	IR192	8	8		2 ICLK
0008 70C1h	ICU	Interrupt request register 193	IR193	8	8		2 ICLK
0008 70C2h	ICU	Interrupt request register 194	IR194	8	8		2 ICLK
0008 70C3h	ICU	Interrupt request register 195	IR195	8	8		2 ICLK
0008 70C4h	ICU	Interrupt request register 196	IR196	8	8		2 ICLK
0008 70C5h	ICU	Interrupt request register 197	IR197	8	8		2 ICLK
0008 70C6h	ICU	Interrupt request register 198	IR198	8	8		2 ICLK
0008 70C7h	ICU	Interrupt request register 199	IR199	8	8		2 ICLK
0008 70C8h	ICU	Interrupt request register 200	IR200	8	8		2 ICLK
0008 70C9h	ICU	Interrupt request register 201	IR201	8	8		2 ICLK
0008 70CEh	ICU	Interrupt request register 206	IR206	8	8		2 ICLK
0008 70CFh	ICU	Interrupt request register 207	IR207	8	8		2 ICLK
0008 70D0h	ICU	Interrupt request register 208	IR208	8	8		2 ICLK
0008 70D1h	ICU	Interrupt request register 209	IR209	8	8		2 ICLK
0008 70D2h	ICU	Interrupt request register 210	IR210	8	8		2 ICLK
0008 70D3h	ICU	Interrupt request register 211	IR211	8	8		2 ICLK
0008 70D4h	ICU	Interrupt request register 212	IR212	8	8		2 ICLK
0008 70D5h	ICU	Interrupt request register 213	IR213	8	8		2 ICLK
0008 70D6h	ICU	Interrupt request register 214	IR214	8	8		2 ICLK
0008 70D7h	ICU	Interrupt request register 215	IR215	8	8		2 ICLK
0008 70D8h	ICU	Interrupt request register 216	IR216	8	8		2 ICLK
0008 70D9h	ICU	Interrupt request register 217	IR217	8	8		2 ICLK
0008 70DAh	ICU	Interrupt request register 218	IR218	8	8		2 ICLK
0008 70DBh	ICU	Interrupt request register 219	IR219	8	8		2 ICLK
0008 70DCh	ICU	Interrupt request register 220	IR220	8	8		2 ICLK
0008 70DDh	ICU	Interrupt request register 221	IR221	8	8		2 ICLK
0008 70DEh	ICU	Interrupt request register 222	IR222	8	8		2 ICLK
0008 70DFh	ICU	Interrupt request register 223	IR223	8	8		2 ICLK
0008 70E0h	ICU	Interrupt request register 224	IR224	8	8		2 ICLK
0008 70E1h	ICU	Interrupt request register 225	IR225	8	8		2 ICLK
0008 70E2h	ICU	Interrupt request register 226	IR226	8	8		2 ICLK
0008 70E3h	ICU	Interrupt request register 227	IR227	8	8		2 ICLK

[Chip version A]

Table 5.7 DC Characteristics (6)

Conditions: VCC = AVCC0 = 1.62 to 5.5 V, VSS = AVSS0 = VREFL = VREFL0 = 0 V, T_a = –40 to +105°C

Item					Symbol	Typ.	Max.	Unit	Test Conditions
Supply current*1	Middle-speed operating modes 1A and 1B	Normal operating mode	No peripheral operation	ICLK = 32 MHz*2	I_{CC}	7.0	—	mA	
				ICLK = 20 MHz*3		6.0	—		
			All peripheral operation: Normal	ICLK = 32 MHz*4		26	—		
				ICLK = 20 MHz*5		18.5	—		
			All peripheral operation: Max.	ICLK = 32 MHz*4		—	40		
				ICLK = 20 MHz*5		—	30		
		Sleep mode	No peripheral operation	ICLK = 32 MHz		5.0	—		
				ICLK = 20 MHz		4.6	—		
			All peripheral operation: Normal	ICLK = 32 MHz		15.5	—		
				ICLK = 20 MHz		12	—		
		All-module clock stop mode		ICLK = 32 MHz		4.5	—		
				ICLK = 20 MHz		4.3	—		
		Increase during BGO operation*6	Middle-speed operating mode 1A			25	—		
			Middle-speed operating mode 1B			20	—		
	Low-speed operating mode 1	Normal operating mode	No peripheral operation*7	ICLK = 1 MHz		0.68	—		
			All peripheral operation: Normal*8	ICLK = 1 MHz		2.4	—		
			All peripheral operation: Max.*8	ICLK = 1 MHz		—	7		
		Sleep mode	No peripheral operation	ICLK = 1 MHz		0.6	—		
			All peripheral operation: Normal	ICLK = 1 MHz		2	—		
		All-module clock stop mode				0.58	—		
	Low-speed operating mode 2	Normal operating mode	No peripheral operation*9	ICLK = 32 kHz		0.024	—		
			All peripheral operation: Normal*10	ICLK = 32 kHz		0.05	—		
			All peripheral operation: Max.*10	ICLK = 32 kHz		—	3*11		
		Sleep mode	No peripheral operation	ICLK = 32 kHz		0.02	—		
			All peripheral operation: Normal	ICLK = 32 kHz		0.04	—		
		All-module clock stop mode				0.018	—		

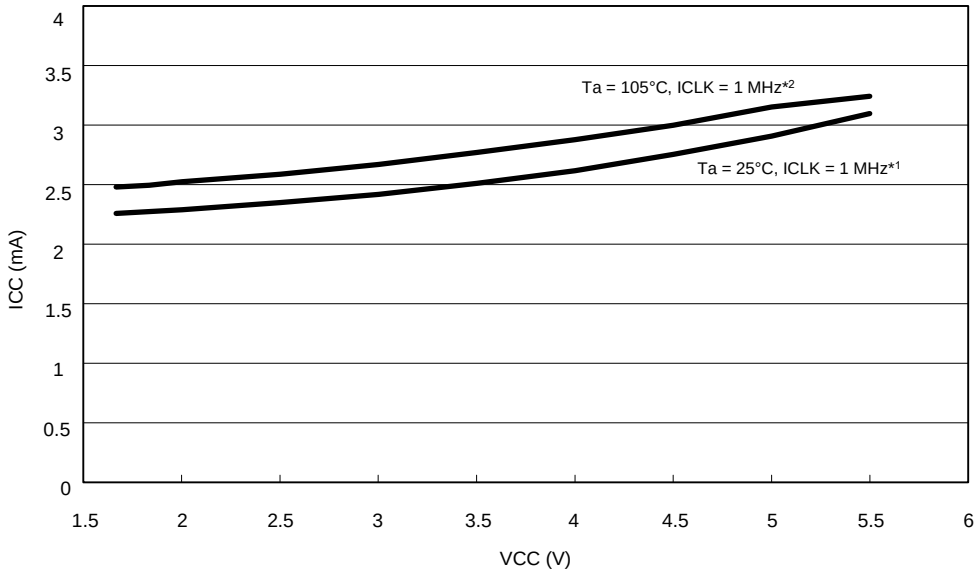
Note 1. Supply current values do not include output charge/discharge current from all pins. The values apply when internal pull-up MOSs are in the off state.

Note 2. Clock supply to the peripheral functions is stopped. This does not include BGO operation. The clock source is PLL and the VCO oscillation frequency is 64 MHz. BCLK, FCLK, and PCLK are set to divided by 64.

Note 3. Clock supply to the peripheral functions is stopped. This does not include BGO operation. The clock source is HOCO and the oscillation frequency is 40 MHz. BCLK, FCLK, and PCLK are set to divided by 64.

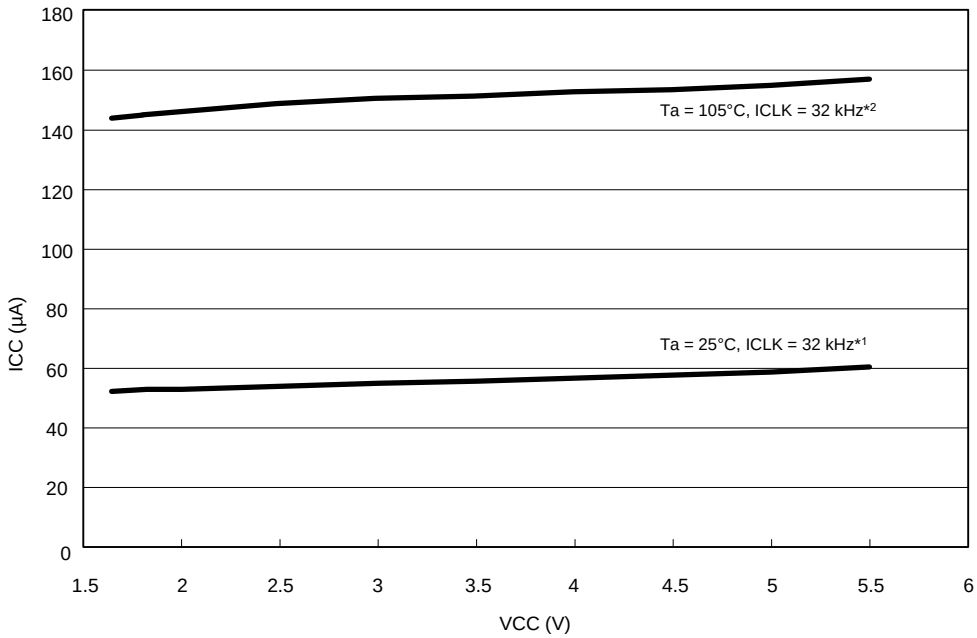
Note 4. Clocks are supplied to the peripheral functions. This does not include BGO operation. The clock source is PLL and the VCO oscillation frequency is 64 MHz. BCLK, FCLK, and PCLK are ICLK divided by 1.

Note 5. Clocks are supplied to the peripheral functions. This does not include BGO operation. The clock source is HOCO and the oscillation frequency is 40 MHz. BCLK, FCLK, and PCLK are ICLK divided by 1.
Note 6. This is the increase if data is programmed to or erasing from the ROM or E2 DataFlash during program execution.
Note 7. Clock supply to the peripheral functions is stopped. This does not include BGO operation. The clock source is HOCO and the oscillation frequency is 32 MHz. BCLK, FCLK, and PCLK are set to divided by 64.
Note 8. Clocks are supplied to the peripheral functions. This does not include BGO operation. The clock source is HOCO and the oscillation frequency is 32 MHz. BCLK, FCLK, and PCLK are ICLK divided by 1.
Note 9. Clock supply to the peripheral functions is stopped. This does not include BGO operation. The clock source is the sub oscillation circuit. BCLK, FCLK, and PCLK are set to divided by 64.
Note 10. Clocks are supplied to the peripheral functions. This does not include BGO operation. The clock source is the sub oscillation circuit. BCLK, FCLK, and PCLK are ICLK divided by 1.
Note 11. Value when the main clock continues oscillating at 12.5 MHz.



Note 1. All peripheral operation is normal.
Average value of the tested middle samples during product evaluation.
Note 2. All peripheral operation is maximum.
Average value of the tested upper-limit samples during product evaluation.

Figure 5.3 Voltage Dependency in Low-Speed Operating Mode 1 (Reference Data) for Chip Version A



Note 1. All peripheral operation is normal.
Average value of the tested middle samples during product evaluation.
Note 2. All peripheral operation is maximum.
Average value of the tested upper-limit samples during product evaluation.

Figure 5.4 Voltage Dependency in Low-Speed Operating Mode 2 (Reference Data) for Chip Version A

[Chip version B with 768 Kbytes/1 Mbyte of flash memory and 100 to 145 pins]

Table 5.15 DC Characteristics (14)

Conditions: VCC = AVCC0 = 2.7 to 5.5 V, VSS = AVSS0 = VREFL = VREFL0 = 0 V, T_a = –40 to +105°C

Item					Symbol	Typ.	Max.	Unit	Test Conditions
Supply current*1	High-speed operating mode	Normal operating mode	No peripheral operation*2	ICLK = 50 MHz	I_{CC}	7.8	—	mA	
			All peripheral operation: Normal*3	ICLK = 50 MHz		29.8	—		
			All peripheral operation: Max.*3	ICLK = 50 MHz		—	45		
		Sleep mode	No peripheral operation	ICLK = 50 MHz		4.3	—		
			All peripheral operation: Normal	ICLK = 50 MHz		13.5	—		
		All-module clock stop mode				3.7	—		
		Increase during BGO operation*4				23	—		

Note 1. Supply current values do not include output charge/discharge current from all pins. The values apply when internal pull-up MOSs are in the off state.

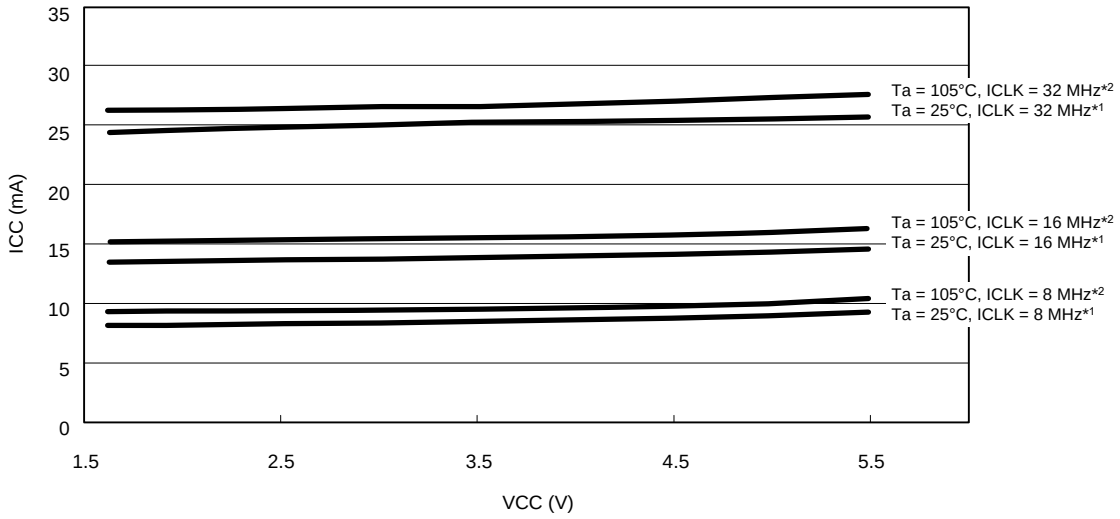
Note 2. Clock supply to the peripheral functions is stopped. This does not include BGO operation. The clock source is PLL and the VCO oscillation frequency is 100 MHz. BCLK, FCLK, and PCLK are set to divided by 64.

Note 3. Clocks are supplied to the peripheral functions. This does not include BGO operation. The clock source is PLL and the VCO oscillation frequency is 100 MHz. BCLK, FCLK, and PCLK are ICLK divided by 2.

Note 4. This is the increase if data is programmed to or erasing from the ROM or E2 DataFlash during program execution.

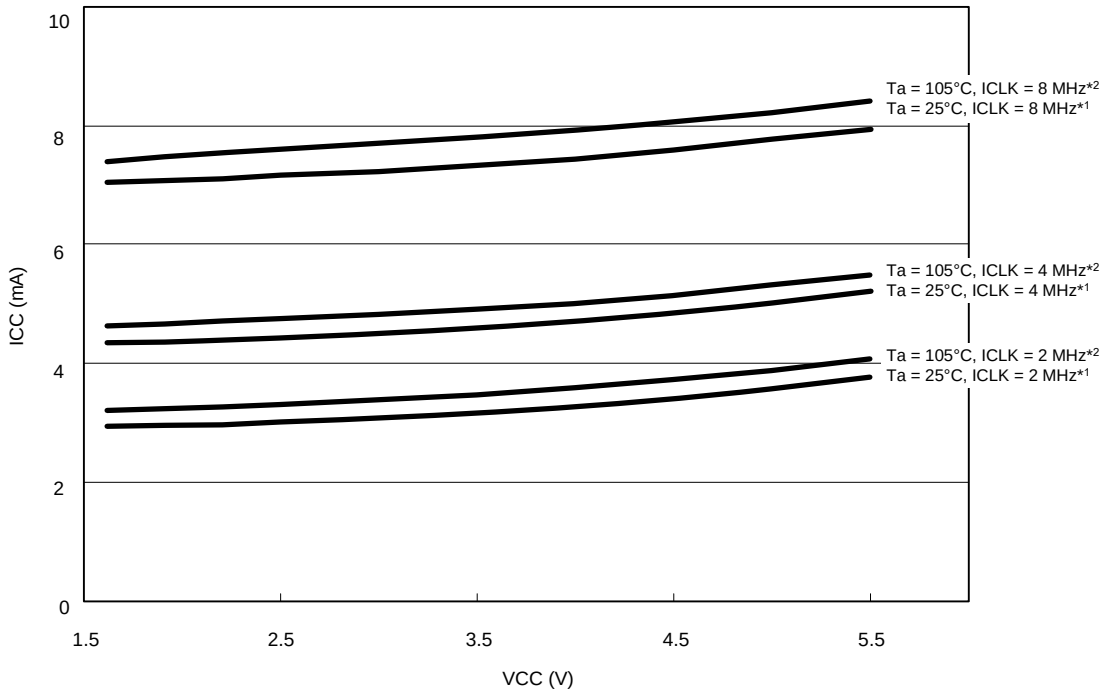
Item					Symbol	Typ.	Max.	Unit	Test Conditions
Supply current*1	Low-speed operating mode 1	Normal operating mode	No peripheral operation*7	ICLK = 8 MHz	I_{CC}	2.1	—	mA	
				ICLK = 4 MHz		1.7	—		
				ICLK = 2 MHz		1.5	—		
			All peripheral operation: Normal*8	ICLK = 8 MHz		7.3	—		
				ICLK = 4 MHz		4.5	—		
				ICLK = 2 MHz		3.1	—		
			All peripheral operation: Max.*7	ICLK = 8 MHz		—	12		
				ICLK = 4 MHz		—	—		
				ICLK = 2 MHz		—	—		
		Sleep mode	No peripheral operation	ICLK = 8 MHz		1.5	—		
				ICLK = 4 MHz		1.4	—		
				ICLK = 2 MHz		1.3	—		
			All peripheral operation: Normal	ICLK = 8 MHz		4.1	—		
				ICLK = 4 MHz		3.0	—		
				ICLK = 2 MHz		2.3	—		
		All-module clock stop mode		ICLK = 8 MHz		1.4	—		
				ICLK = 4 MHz		1.3	—		
				ICLK = 2 MHz		1.2	—		
	Low-speed operating mode 2	Normal operating mode	No peripheral operation*9	ICLK = 32 kHz		0.022	—		
			All peripheral operation: Normal*10	ICLK = 32 kHz		0.06	—		
			All peripheral operation: Max.*10	ICLK = 32 kHz		—	3*11		
		Sleep mode	No peripheral operation	ICLK = 32 kHz		0.017	—		
			All peripheral operation: Normal	ICLK = 32 kHz		0.036	—		
		All-module clock stop mode				0.017	—		

Note 1. Supply current values do not include output charge/discharge current from all pins. The values apply when internal pull-up MOSs are in the off state.
Note 2. Clock supply to the peripheral functions is stopped. This does not include BGO operation. The clock source is PLL and the VCO oscillation frequency is 64 MHz. BCLK, FCLK, and PCLK are set to divided by 64.
Note 3. Clock supply to the peripheral functions is stopped. This does not include BGO operation. The clock source is HOCO and the oscillation frequency is 40 MHz. BCLK, FCLK, and PCLK are set to divided by 64.
Note 4. Clocks are supplied to the peripheral functions. This does not include BGO operation. The clock source is PLL and the VCO oscillation frequency is 64 MHz. BCLK, FCLK, and PCLK are ICLK divided by 1.
Note 5. Clocks are supplied to the peripheral functions. This does not include BGO operation. The clock source is HOCO and the oscillation frequency is 40 MHz. BCLK, FCLK, and PCLK are ICLK divided by 1.
Note 6. This is the increase if data is programmed to or erasing from the ROM or E2 DataFlash during program execution.
Note 7. Clock supply to the peripheral functions is stopped. This does not include BGO operation. The clock source is HOCO and the oscillation frequency is 32 MHz. BCLK, FCLK, and PCLK are set to divided by 64.
Note 8. Clocks are supplied to the peripheral functions. This does not include BGO operation. The clock source is HOCO and the oscillation frequency is 32 MHz. BCLK, FCLK, and PCLK are ICLK divided by 1.
Note 9. Clock supply to the peripheral functions is stopped. This does not include BGO operation. The clock source is the sub oscillation circuit. BCLK, FCLK, and PCLK are set to divided by 64.
Note 10. Clocks are supplied to the peripheral functions. This does not include BGO operation. The clock source is the sub oscillation circuit. BCLK, FCLK, and PCLK are ICLK divided by 1.
Note 11. Value when the main clock continues oscillating at 12.5 MHz.



Note 1. All peripheral operation is normal. This does not include BGO operation.
Average value of the tested middle samples during product evaluation
Note 2. All peripheral operation is maximum. This does not include BGO operation.
Average value of the tested upper-limit samples during product evaluation.

Figure 5.28 Voltage Dependency in Middle-Speed Operating Modes 2A and 2B (Reference Data) for Chip Version B with 768 Kbytes/1 Mbyte of Flash Memory and 100 to 145 Pins



Note 1. All peripheral operation is normal.
Average value of the tested middle samples during product evaluation.
Note 2. All peripheral operation is maximum.
Average value of the tested upper-limit samples during product evaluation.

Figure 5.29 Voltage Dependency in Low-Speed Operating Mode 1 (Reference Data) for Chip Version B with 768 Kbytes/1 Mbyte of Flash Memory and 100 to 145 Pins

[Chip versions B and C]

Table 5.31 Output Values of Voltage (4)

Conditions: VCC = AVCC0 = 2.7 to 4.0 V, VSS = AVSS0 = VREFL = VREFL0 = 0 V, T_a = –40 to +105°C

Item			Symbol	Min.	Max.	Unit	Test Conditions
Output low	All output pins (other than RIIC)	Normal output mode	V_{OL}	—	0.5	V	I_{OL} = 1.0 mA
		High-drive output mode		—	0.5		I_{OL} = 2.0 mA
	RIIC pins			—	0.4		I_{OL} = 3.0 mA
				—	0.6		I_{OL} = 6.0 mA
Output high	All output pins	Normal output mode	V_{OH}	VCC – 0.5	—	V	I_{OH} = –1.0 mA
		High-drive output mode		VCC – 0.5	—		I_{OH} = –2.0 mA

[Chip versions B and C]

Table 5.32 Output Values of Voltage (5)

Conditions: VCC = AVCC0 = 4.0 to 5.5 V, VSS = AVSS0 = VREFL = VREFL0 = 0 V, T_a = –40 to +105°C

Item			Symbol	Min.	Max.	Unit	Test Conditions
Output low	All output pins (other than RIIC)	Normal output mode	V_{OL}	—	0.8	V	I_{OL} = 2.0 mA
		High-drive output mode		—	0.8		I_{OL} = 4.0 mA
	RIIC pins			—	0.4		I_{OL} = 3.0 mA
				—	0.6		I_{OL} = 6.0 mA
Output high	All output pins	Normal output mode	V_{OH}	VCC – 0.8	—	V	I_{OH} = –2.0 mA
		High-drive output mode		VCC – 0.8	—		I_{OH} = –4.0 mA

5.2.1 Standard I/O Pin Output Characteristics (1)

Figure 5.45 to Figure 5.49 show the characteristics when normal output is selected by the drive capacity control register.

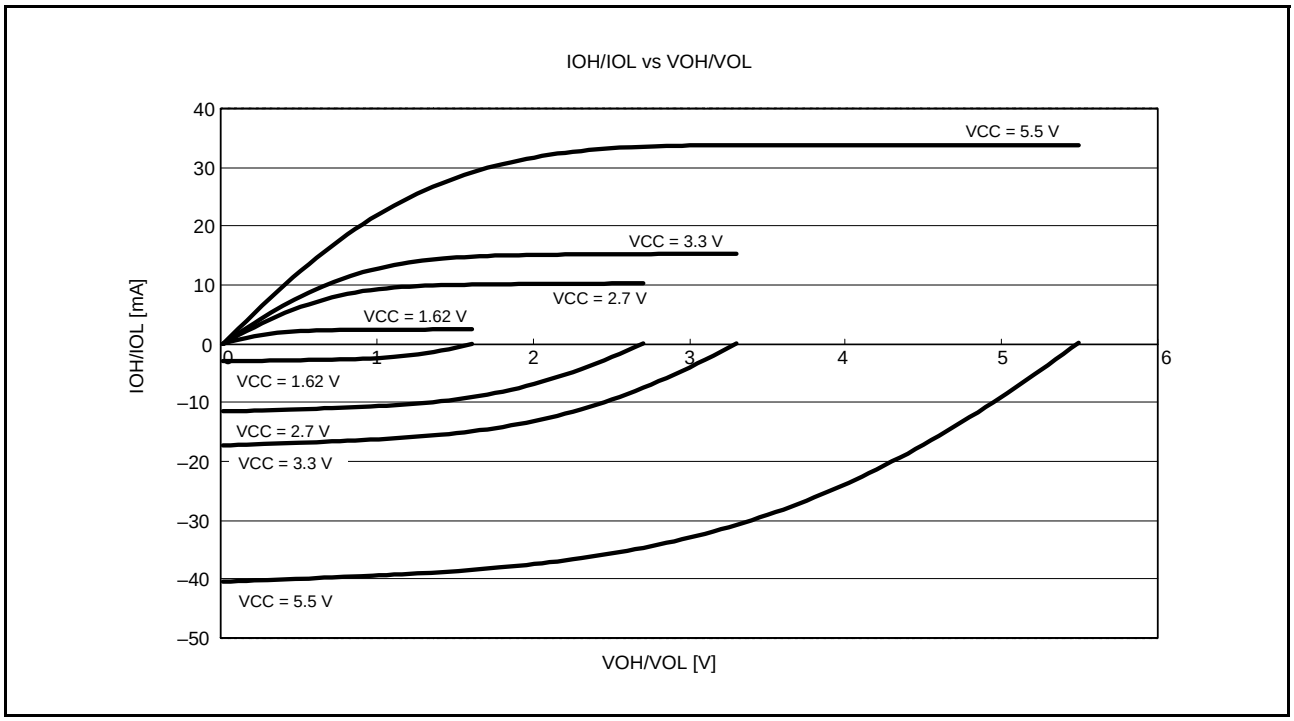


Figure 5.45 VOH/VOL and IOH/IOL Voltage Characteristics at Ta = 25°C when Normal Output is Selected (Reference Data)

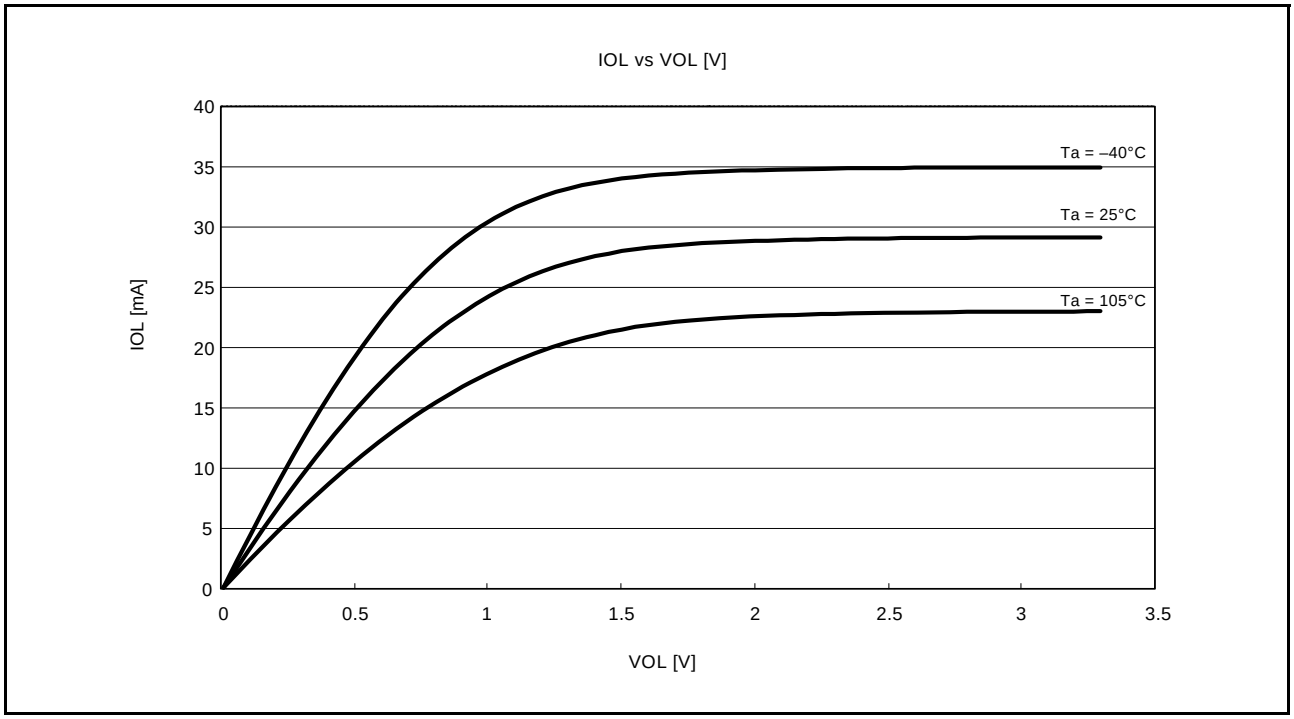


Figure 5.57 VOL and IOL Temperature Characteristics of RIIC Output Pin at VCC = 3.3 V (Reference Data)

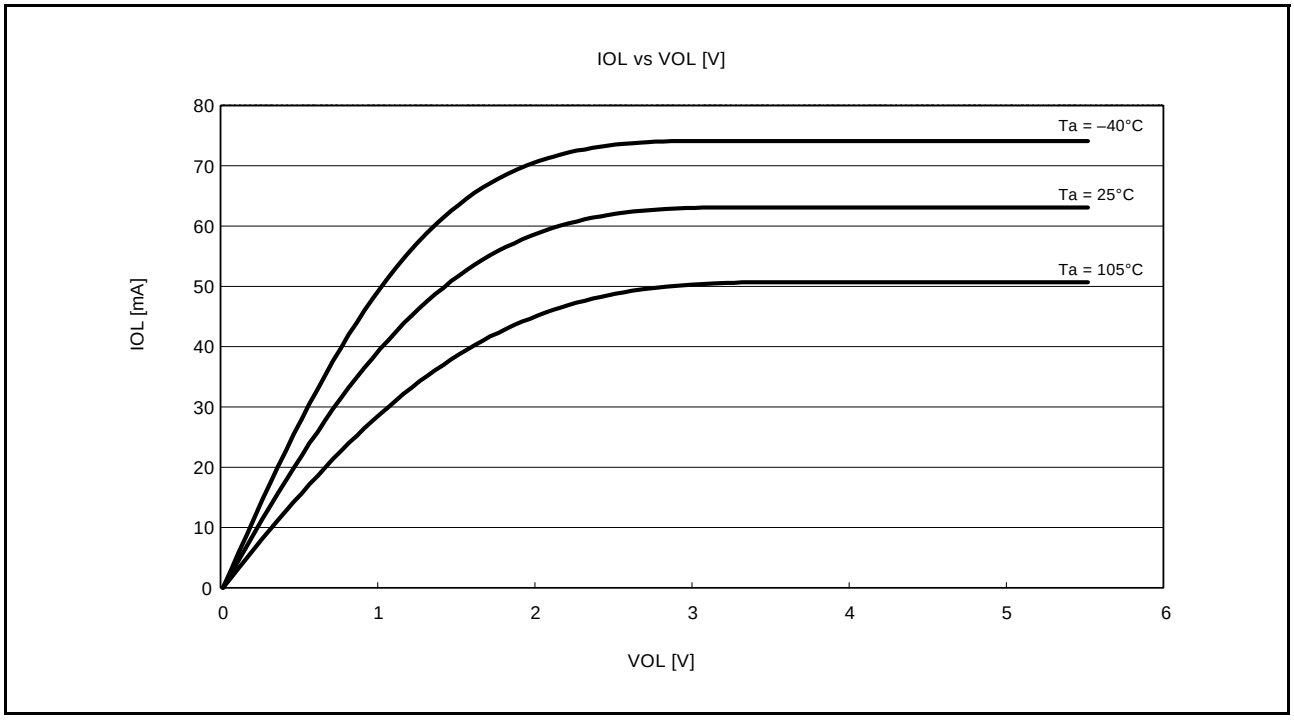


Figure 5.58 VOL and IOL Temperature Characteristics of RIIC Output Pin at VCC = 5.5 V (Reference Data)

Item				Symbol	Min.	Max.	Unit*1	Test Conditions
RSPI	Data input setup time	Master	2.7 V ≤ VCC ≤ 5.5 V	t_{SU}	10	—	ns	C = 30pF Figure 5.92 to Figure 5.97
			1.8 V ≤ VCC < 2.7 V		25	—		
			1.62 V ≤ VCC < 1.8 V		30	—		
		Slave			25 – t_{Pcyc}	—		
	Data input hold time	Master	PCLKB set to a division ratio other than divided by 2	t_H	t_{Pcyc}	—	ns	
			PCLKB set to divided by 2*2	t_{HF}	0	—		
		Slave		t_H	20 + 2 × t_{Pcyc}	—		
	SSL setup time	Master		t_{LEAD}	1	8	t_{SPcyc}	
		Slave			4	—	t_{Pcyc}	
	SSL hold time	Master		t_{LAG}	1	8	t_{SPcyc}	
		Slave			4	—	t_{Pcyc}	
	Data output delay time	Master	2.7 V ≤ VCC ≤ 5.5 V	t_{OD}	—	14	ns	
			1.8 V ≤ VCC < 2.7 V		—	20		
			1.62 V ≤ VCC < 1.8 V		—	25		
		Slave	2.7 V ≤ VCC ≤ 5.5 V		—	3 × t_{Pcyc} + 65		
			1.8 V ≤ VCC < 2.7 V		—	3 × tPcyc +85		
			1.62 V ≤ VCC < 1.8 V		—	3 × tPcyc +95		
	Data output hold time	Master		t_{OH}	0	—	ns	
		Slave			0	—		
	Successive transmission delay time	Master		t_{TD}	t_{SPcyc} + 2 × t_{Pcyc}	8 × t_{SPcyc} + 2 × t_{Pcyc}	ns	
		Slave			4 × t_{Pcyc}	—		
	MOSI and MISO rise/fall time	Output	2.7 V ≤ VCC ≤ 5.5 V	t_{Dr}, t_{Df}	—	10	ns	
			1.8 V ≤ VCC < 2.7 V		—	15		
			1.62 V ≤ VCC < 1.8 V		—	20		
		Input			—	1	µs	
	SSL rise/fall time	Output	2.7 V ≤ VCC ≤ 5.5 V	t_{SSLr}, t_{SSLf}	—	10	ns	
			1.8 V ≤ VCC < 2.7 V		—	15		
			1.62 V ≤ VCC < 1.8 V		—	20		
		Input			—	1	µs	
	Slave access time		2.7 V ≤ VCC ≤ 5.5 V	t_{SA}	—	6	t_{Pcyc}	C = 30pF Figure 5.96 and Figure 5.97
			1.8 V ≤ VCC < 2.7 V		—	7		
			1.62 V ≤ VCC < 1.8 V		—	7		
	Slave output release time		2.7 V ≤ VCC ≤ 5.5 V	t_{REL}	—	5	t_{Pcyc}	
			1.8 V ≤ VCC < 2.7 V		—	6		
			1.62 V ≤ VCC < 1.8 V		—	6		

Note 1. t_{Pcyc}: PCLK cycle
Note 2. Divided by 2 can be set only in packages with 768 Kbytes/1 Mbyte of flash memory or 144/145 pins.

Table 5.66 Sampling Time

Conditions: VCC = AVCC0 = 1.62 to 5.5 V, VSS = AVSS0 = VREFL = VREFL0 = 0 V, T_a = –40 to +105°C

Item		Symbol	Typ.	Unit	Test Conditions
Sampling time	High-precision channel	Ts	0.2 + 0.14 × R0 (KΩ)	µs	Figure 5.100
	Normal-precision channel		0.35 + 0.14 × R0 (KΩ)		

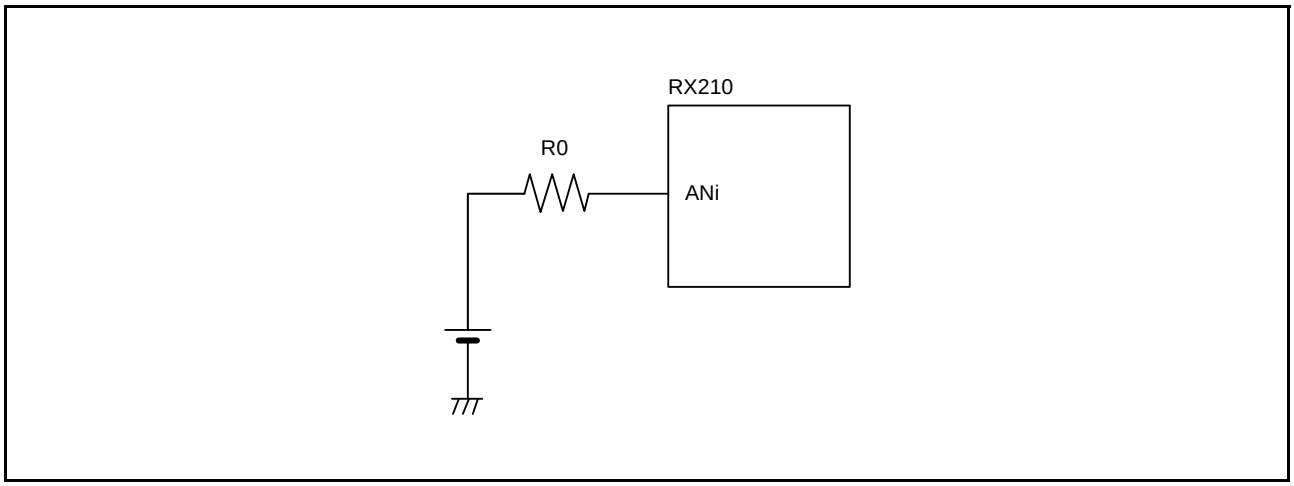


Figure 5.100 Internal Equivalent Circuit of Analog Input Pin

[Chip version B]

Table 5.79 ROM (Flash Memory for Code Storage) Characteristics (6) : middle-speed operating modes 1B and 2B

Conditions: VCC = AVCC0 = 1.62 to 3.6 V, VREFH = VREFH0 = AVCC0, VSS = AVSS0 = VREFL = VREFL0 = 0 V
Temperature range for the programming/erasure operation: T_a = –40 to +105°C

Item		Symbol	FCLK = 4 MHz			FCLK = 32 MHz*1			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Programming time when N_{PEC} ≤ 100 times	2 bytes	t_{P2}	—	0.25	5.0	—	0.21	2.8	ms
	8 bytes	t_{P8}	—	0.25	5.3	—	0.21	3.0	
	128 bytes	t_{P128}	—	0.92	14.0	—	0.65	8.3	
Programming time when N_{PEC} > 100 times	2 bytes	t_{P2}	—	0.31	6.2	—	0.26	3.5	ms
	8 bytes	t_{P8}	—	0.31	6.6	—	0.26	3.7	
	128 bytes	t_{P128}	—	1.09	17.5	—	0.77	10.0	
Erasure time when N_{PEC} ≤ 100 times	2 Kbytes	t_{E2K}	—	21.0	113.7	—	18.5	46	ms
Erasure time when N_{PEC} > 100 times	2 Kbytes	t_{E2K}	—	25.6	220.6	—	22.5	90 (1000 times ≥ N_{PEC} > 100 times), 98 (10000 times ≥ N_{PEC} > 1000 times)	ms
Suspend delay time during programming (in programming/erasure priority mode)		t_{SPD}	—	—	1.7	—	—	1.6	ms
First suspend delay time during programming (in suspend priority mode)		t_{SPSD1}	—	—	220	—	—	120	µs
Second suspend delay time during programming (in suspend priority mode)		t_{SPSD2}	—	—	1.7	—	—	1.6	ms
Suspend delay time during erasing (in programming/erasure priority mode)		t_{SED}	—	—	1.7	—	—	1.6	ms
First suspend delay time during erasing (in suspend priority mode)		t_{SESD1}	—	—	220	—	—	120	µs
Second suspend delay time during erasing (in suspend priority mode)		t_{SESD2}	—	—	1.7	—	—	1.6	ms
FCU reset time		t_{FCUR}	20 µs or longer and FCLK × 6 or greater	—	—	20 µs or longer and FCLK × 6 or greater	—	—	µs

Note 1. The operating frequency is 20 MHz (max.) when the voltage is in the range from 1.62 V to less than 1.8 V.

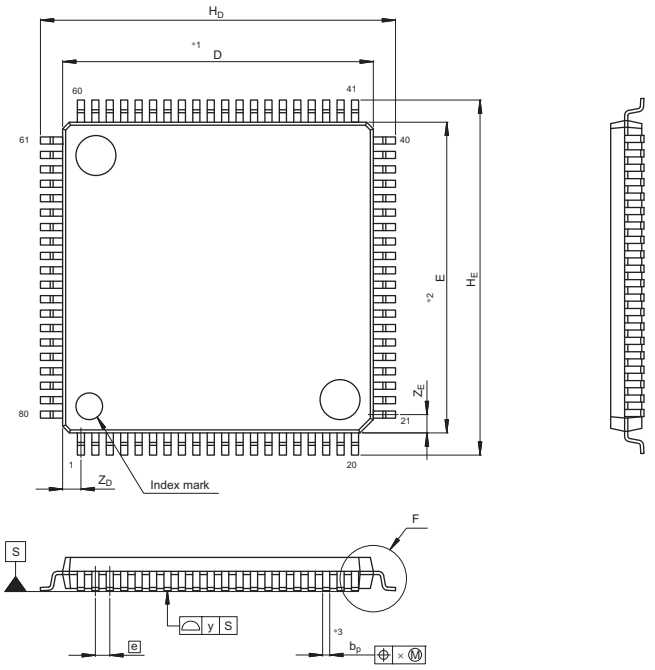
[Chip version B]

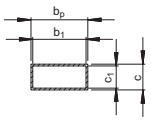
Table 5.84 E2 DataFlash Characteristics (5)
: high-speed operating mode, middle-speed operating modes 1A and 2A

Conditions: VCC = AVCC0 = 2.7 to 5.5 V, VREFH = VREFH0 = AVCC0, VSS = AVSS0 = VREFL = VREFL0 = 0 V
Temperature range for the programming/erasure operation: T_a = –40 to +105°C

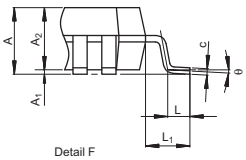
Item		Symbol	FCLK = 4 MHz			FCLK = 32 MHz			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Programming time when N_{DPEC} ≤ 100 times	2 bytes	t_{DP2}	—	0.19	4.4	—	0.13	2.0	ms
	8 bytes	t_{DP8}	—	0.24	5.1	—	0.13	2.2	
Programming time when N_{DPEC} > 100 times	2 bytes	t_{DP2}	—	0.25	6.4	—	0.17	3.0	ms
	8 bytes	t_{DP8}	—	0.32	7.5	—	0.18	3.2	
Erasure time when N_{DPEC} ≤ 100 times	128 bytes	t_{DE128}	—	3.3	27.1	—	2.5	8	ms
Erasure time when N_{DPEC} > 100 times	128 bytes	t_{DE128}	—	4.0	45.1	—	3.0	12	ms
Blank check time	2 bytes	t_{DBC2}	—	—	98	—	—	35	µs
	2 Kbytes	t_{DBC2K}	—	—	16	—	—	2.5	ms
Suspend delay time during programming (in programming/erasure priority mode)		t_{DSPD}	—	—	0.9	—	—	0.8	ms
First suspend delay time during programming (in suspend priority mode)		t_{DSPSD1}	—	—	220	—	—	120	µs
Second suspend delay time during programming (in suspend priority mode)		t_{DSPSD2}	—	—	0.9	—	—	0.8	ms
Suspend delay time during erasing (in programming/erasure priority mode)		t_{DSED}	—	—	0.9	—	—	0.8	ms
First suspend delay time during erasing (in suspend priority mode)		t_{DSESD1}	—	—	220	—	—	120	µs
Second suspend delay time during erasing (in suspend priority mode)		t_{DSESD2}	—	—	0.9	—	—	0.8	ms

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LQFP80-14x14-0.65	PLQP0080JA-A	FP-80W / FP-80WV	0.6g





Terminal cross section



Detail F

NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	13.9	14.0	14.1
E	13.9	14.0	14.1
A_2	—	1.4	—
H_D	15.8	16.0	16.2
H_E	15.8	16.0	16.2
A	—	—	1.7
A_1	0.05	0.1	0.15
b_p	0.27	0.32	0.37
b_1	—	0.30	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	8°
e	—	0.65	—
x	—	—	0.13
y	—	—	0.10
Z_D	—	0.825	—
Z_E	—	0.825	—
L	0.35	0.5	0.65
L_1	—	1.0	—

Figure I 80-Pin LQFP (PLQP0080JA-A)

REVISION HISTORY	RX210 Group Datasheet

Rev.	Date	Description	
		Page	Summary
0.50	Apr.15, 2011	—	First edition, issued
0.90	Aug.10, 2011	1. Overview	
		4	Table 1.1 Outline of Specifications: Power supply voltage/ Operating frequency, changed
		17, 21, 24, 26	Table 1.5 to Table 1.8 List of Pins and Pin Functions (Pin name: LVCMP2 → CMPA2), changed
		2. CPU	
		51	Table 2.14 Instructions that are Converted into Multiple Micro-Operations (multiplier: 32 × 32 → 64 bits), (memory source operand), added
		4. I/O Registers	
		63	Table 5.1 List of I/O Registers (Address Order), SOSCWTCR, LOCOWTCR2, HOCOWTCR2, added
		114 to 116	Table 5.1 List of I/O Registers (Address Order): Interrupt source priority register, changed
		5. Electrical Characteristics	
		85 to 137	Newly added
1.20	Nov 28, 2012	All	Information on chip versions A, B, and C, corresponding descriptions and notes, added 48-pin products added, PLQP0080JA-A 14 × 14 mm, 0.65-mm pitch, package deleted
		Features	
		1	Description changed
		1. Overview	
		2	1.1 Outline of Specifications: Description, changed
		2 to 5	Table 1.1 Outline of Specifications, changed Note 1, added
		6	Table 1.2 Comparison of Functions for Different Packages, changed
		7	Table 1.3 List of Products, changed
		8 to 10	Tables 1.4 to 1.7 List of Products, added
		11	Figure 1.1 How to Read the Product Part No., Memory Capacity, and Package Type: G item added
		12	Figure 1.2 Block Diagram, changed
		13	Table 1.8 Pin Functions: Power supply and On-chip emulator, changed
		13	Table 1.8 Pin Functions: Multiplexed bus, added
		18	Figure 1.4 Pin Assignments of the 100-Pin LQFP, changed
		21	Figure 1.7 Pin Assignments of the 48-Pin LQFP, added
		23	Table 1.9 List of Pins and Pin Functions (100-Pin TFLGA): Pin No. G4, changed
		25	Table 1.10 List of Pins and Pin Functions (100-Pin LQFP): Pin No. 21, changed
		28	Table 1.11 List of Pins and Pin Functions (80-Pin LQFP): Pin No. 19, changed
		30	Table 1.12 List of Pins and Pin Functions (64-Pin LQFP): Pin No. 15, changed
		3. Address Space	
		37	Figure 3.1 Memory Map in Each Operating Mode: Note 2, changed
		4. I/O Registers	
		41 to 63	Table 4.1 List of I/O Registers (Address Order): Number of Access, changed Voltage regulator control register, Timeout internal counter L, Timeout internal counter U, and PLL power control register, added
		63	Table 4.1 List of I/O Registers (Address Order): Notes 1 and 2, added
		—	Table 4.1 List of I/O Registers (Address Order): LOCO Wait Control Register 2 (LOCOWTCR2), deleted
		5. Electrical Characteristics	
		64 to 152	Description added
1.30	Jan 22, 2013	Features	
		1	On-chip flash memory for code, no wait states, On-chip SRAM, no wait states, Real-time clock, Up to 15 communications channels, Up to 20 extended-function timers, changed
		1.Overview	
		2 to 6	Table 1.1 Outline of Specifications, changed
		7	Table 1.2 Comparison of Functions for Different Packages, changed
		9	Table 1.4 List of Products Chip Version B: D Version (Ta = -40 to +85°C), changed
		10	Table 1.5 List of Products Chip Version B: G Version (Ta = -40 to +105°C), changed