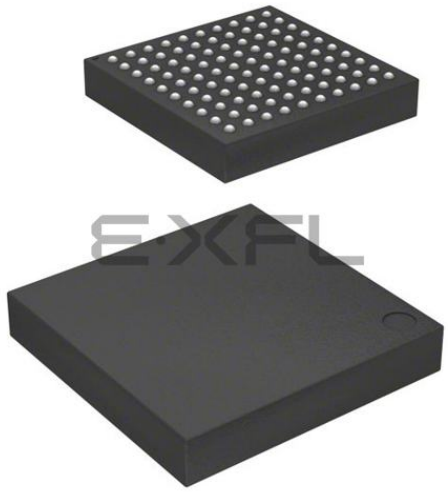


**Welcome to E-XFL.COM**

## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Not For New Designs |
| Core Processor | RX |
| Core Size | 32-Bit Single-Core |
| Speed | 50MHz |
| Connectivity | EBI/EMI, I²C, SCI, SPI |
| Peripherals | DMA, LVD, POR, PWM, WDT |
| Number of I/O | 84 |
| Program Memory Size | 768KB (768K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | 8K x 8 |
| RAM Size | 96K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.62V ~ 5.5V |
| Data Converters | A/D 16x12b; D/A 2x10b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 100-TFLGA |
| Supplier Device Package | 100-TFLGA (7x7) |
| Purchase URL | https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f5210abdlj-u0 |

**Table 1.5 List of Products Chip Version B: G Version (Ta = –40 to +105°C)**

| Group | Part No. | Orderable Part No. | Package | ROM Capacity | RAM Capacity | E2 DataFlash | Operating Frequency (Max.) | Operating Temperature |
|---|---|---|---|---|---|---|---|---|
| RX210 | R5F5210BBGFB | R5F5210BBGFB#30 | PLQP0144KA-A | 1 Mbytes | 96 Kbytes | 8 Kbytes | 50 MHz | –40 to +105°C |
| | R5F5210BBGFP | R5F5210BBGFP#30 | PLQP0100KB-A | | | | | |
| | R5F5210ABGFB | R5F5210ABGFB#30 | PLQP0144KA-A | 768 Kbytes | | | | |
| | R5F5210ABGFP | R5F5210ABGFP#30 | PLQP0100KB-A | | | | | |
| | R5F52108BGFB | R5F52108BGFB#30 | PLQP0144KA-A | 512 Kbytes | 64 Kbytes | | | |
| | R5F52107BGFB | R5F52107BGFB#30 | PLQP0144KA-A | 384 Kbytes | | | | |
| | R5F52106BGFB | R5F52106BGFB#30 | PLQP0144KA-A | 256 Kbytes | 32 Kbytes | | | |
| | R5F52106BGFP | R5F52106BGFP#30 | PLQP0100KB-A | | | | | |
| | R5F52106BGFN | R5F52106BGFN#30 | PLQP0080KB-A | | | | | |
| | R5F52106BGFM | R5F52106BGFM#30 | PLQP0064KB-A | | | | | |
| | R5F52106BGFL | R5F52106BGFL#30 | PLQP0048KB-A | | | | | |
| | R5F52106BGFF | R5F52106BGFF#V0 | PTLG0100JA-A | | | | | |
| | R5F52106BGFK | R5F52106BGFK#30 | PLQP0064GA-A | | | | | |
| | R5F52105BGFB | R5F52105BGFB#30 | PLQP0144KA-A | 128 Kbytes | 20 Kbytes | | | |
| | R5F52105BGFP | R5F52105BGFP#30 | PLQP0100KB-A | | | | | |
| | R5F52105BGFN | R5F52105BGFN#30 | PLQP0080KB-A | | | | | |
| | R5F52105BGFM | R5F52105BGFM#30 | PLQP0064KB-A | | | | | |
| | R5F52105BGFL | R5F52105BGFL#30 | PLQP0048KB-A | | | | | |
| | R5F52105BGFF | R5F52105BGFF#V0 | PLQP0080JA-A | | | | | |
| | R5F52105BGFK | R5F52105BGFK#30 | PLQP0064GA-A | | | | | |
| | R5F52104BGFM | R5F52104BGFM#30 | PLQP0064KB-A | 96 Kbytes | 16 Kbytes | | | |
| | R5F52104BGFL | R5F52104BGFL#30 | PLQP0048KB-A | | | | | |
| | R5F52104BGFF | R5F52104BGFF#V0 | PLQP0080JA-A | | | | | |
| | R5F52103BGFM | R5F52103BGFM#30 | PLQP0064KB-A | 64 Kbytes | 12 Kbytes | | | |
| | R5F52103BGFL | R5F52103BGFL#30 | PLQP0048KB-A | | | | | |
| | R5F52103BGFF | R5F52103BGFF#V0 | PLQP0080JA-A | | | | | |

Note: • Please contact Renesas Electronics sales office for derating of operation under Ta = +85°C to +105°C. Derating is the systematic reduction of load for the sake of improved reliability.

Note: • Orderable part numbers are current as of when this manual was published. Please make sure to refer to the relevant product page on the Renesas website for the latest part numbers.

**Table 1.6 List of Products Chip Version C: D Version (Ta = –40 to +85°C)**

| Group | Part No. | Orderable Part No. | Package | ROM Capacity | RAM Capacity | E2 DataFlash | Operating Frequency (Max.) | Operating Temperature |
|---|---|---|---|---|---|---|---|---|
| RX210 | R5F52108CDFP | R5F52108CDFP#30 | PLQP0100KB-A | 512 Kbytes | 64 Kbytes | 8 Kbytes | 50 MHz | –40 to +85°C |
| | R5F52108CDFN | R5F52108CDFN#30 | PLQP0080KB-A | | | | | |
| | R5F52108CDFM | R5F52108CDFM#30 | PLQP0064KB-A | | | | | |
| | R5F52108CDLJ | R5F52108CDLJ#U0 | PTLG0100JA-A | | | | | |
| | R5F52108CDFF | R5F52108CDFF#V0 | PLQP0080JA-A | | | | | |
| | R5F52108CDFK | R5F52108CDFK#30 | PLQP0064GA-A | | | | | |
| | R5F52107CDFP | R5F52107CDFP#30 | PLQP0100KB-A | 384 Kbytes | | | | |
| | R5F52107CDFN | R5F52107CDFN#30 | PLQP0080KB-A | | | | | |
| | R5F52107CDFM | R5F52107CDFM#30 | PLQP0064KB-A | | | | | |
| | R5F52107CDLJ | R5F52107CDLJ#U0 | PTLG0100JA-A | | | | | |
| | R5F52107CDFF | R5F52107CDFF#V0 | PLQP0080JA-A | | | | | |
| | R5F52107CDFK | R5F52107CDFK#30 | PLQP0064GA-A | | | | | |

Note: • Orderable part numbers are current as of when this manual was published. Please make sure to refer to the relevant product page on the Renesas website for the latest part numbers.

**Table 1.7 List of Products Chip Version C: G Version (Ta = –40 to +105°C)**

| Group | Part No. | Orderable Part No. | Package | ROM Capacity | RAM Capacity | E2 DataFlash | Operating Frequency (Max.) | Operating Temperature |
|---|---|---|---|---|---|---|---|---|
| RX210 | R5F52108CGFP | R5F52108CGFP#30 | PLQP0100KB-A | 512 Kbytes | 64 Kbytes | 8 Kbytes | 50 MHz | –40 to +105°C |
| | R5F52108CGFN | R5F52108CGFN#30 | PLQP0080KB-A | | | | | |
| | R5F52108CGFM | R5F52108CGFM#30 | PLQP0064KB-A | | | | | |
| | R5F52108CGFF | R5F52108CGFF#V0 | PLQP0080JA-A | | | | | |
| | R5F52108CGFK | R5F52108CGFK#30 | PLQP0064GA-A | | | | | |
| | R5F52107CGFP | R5F52107CGFP#30 | PLQP0100KB-A | 384 Kbytes | | | | |
| | R5F52107CGFN | R5F52107CGFN#30 | PLQP0080KB-A | | | | | |
| | R5F52107CGFM | R5F52107CGFM#30 | PLQP0064KB-A | | | | | |
| | R5F52107CGFF | R5F52107CGFF#V0 | PLQP0080JA-A | | | | | |
| | R5F52107CGFK | R5F52107CGFK#30 | PLQP0064GA-A | | | | | |

Note: • Please contact Renesas Electronics sales office for derating of operation under Ta = +85°C to +105°C. Derating is the systematic reduction of load for the sake of improved reliability.

Note: • Orderable part numbers are current as of when this manual was published. Please make sure to refer to the relevant product page on the Renesas website for the latest part numbers.

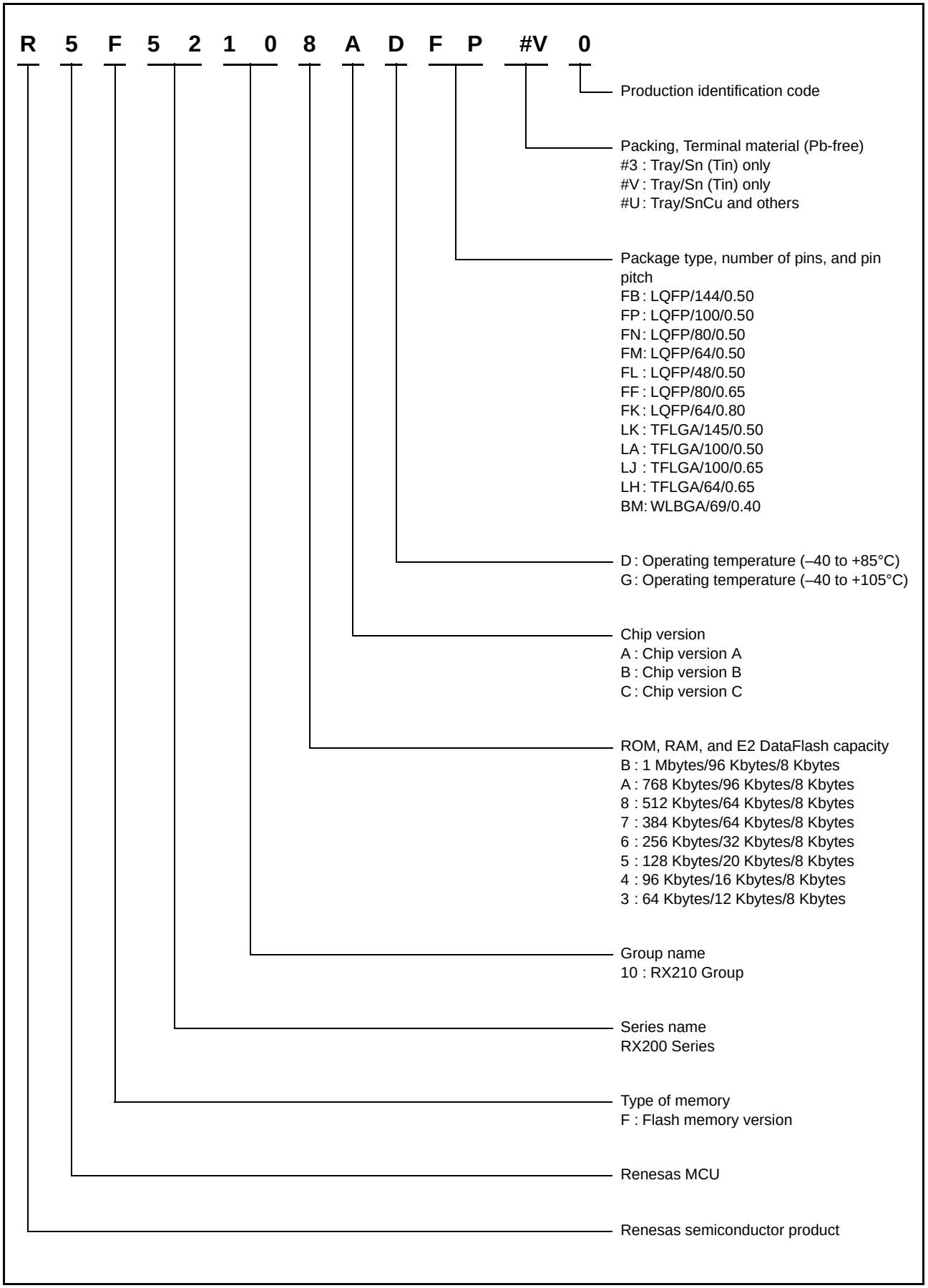
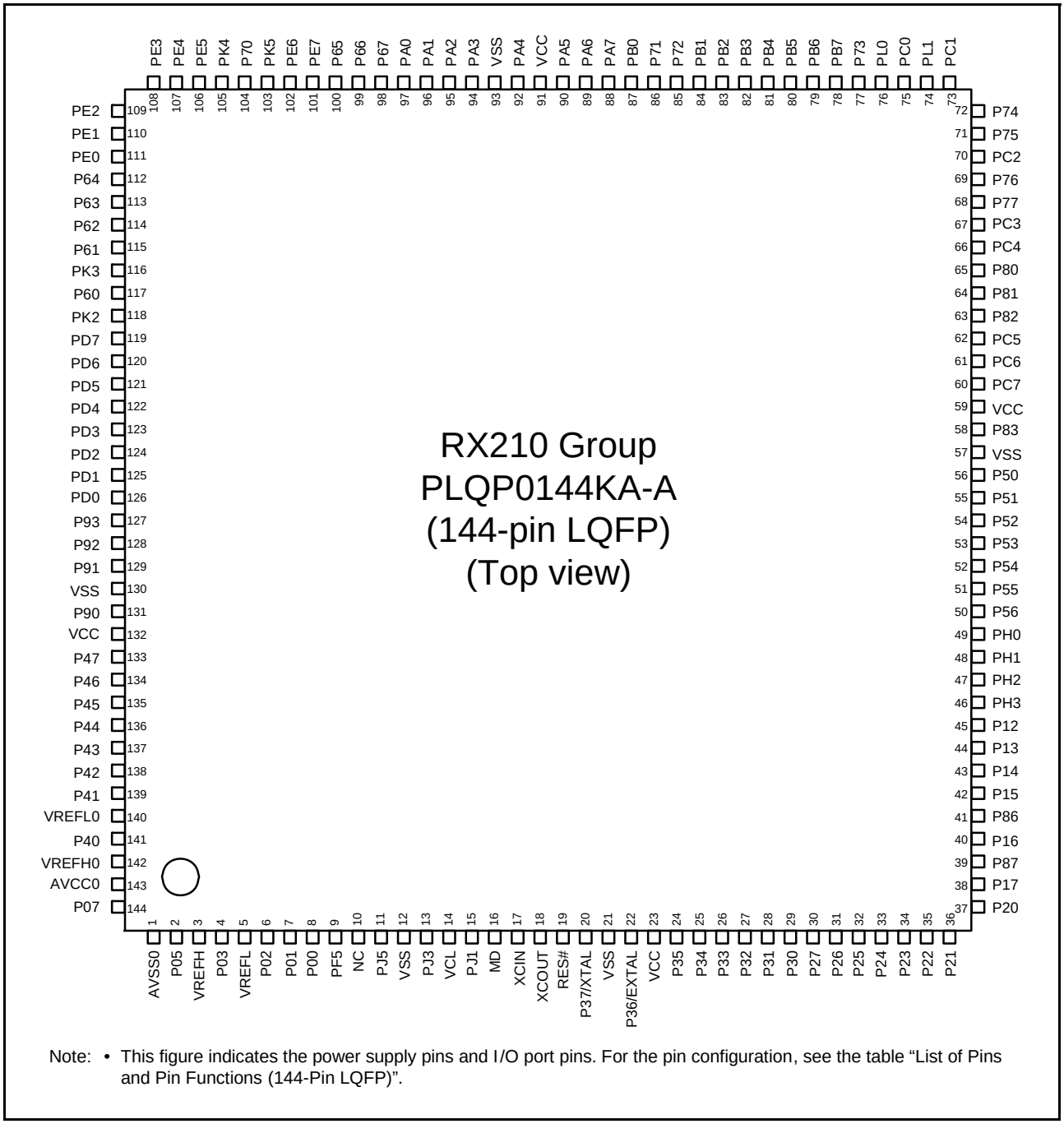



**Figure 1.1 How to Read the Product Part No., Memory Capacity, and Package Type**




Note: • This figure indicates the power supply pins and I/O port pins. For the pin configuration, see the table “List of Pins and Pin Functions (144-Pin LQFP)”.

**Figure 1.4 Pin Assignments of the 144-Pin LQFP**

**Table 1.10 List of Pins and Pin Functions (144-Pin LQFP) (3 / 4)**

| Pin No. | Power Supply, Clock, System Control | I/O Port | External Bus | Timers (MTU, TMR, POE) | Communications (SCIc, SCId, RSPI, RIIC) | Others |
|---|---|---|---|---|---|---|
| 81 | | PB4 | A12 | TIOCA4 | CTS9#/RTS9#/SS9# | |
| 82 | | PB3 | A11 | MTIOC0A/MTIOC4A/ TMO0/POE3#/ TIOCD3/TCLKD | SCK4/SCK6 | |
| 83 | | PB2 | A10 | TIOCC3/TCLKC | CTS4#/RTS4#/SS4#/ CTS6#/RTS6#/SS6# | |
| 84 | | PB1 | A9 | MTIOC0C/MTIOC4C/ TMCI0/TIOCB3 | TXD4/SMOSI4/SSDA4/ TXD6/SMOSI6/SSDA6 | IRQ4-DS |
| 85 | | P72 | | | | |
| 86 | | P71 | | | | |
| 87 | | PB0 | A8 | MTIC5W/TIOCA3 | RXD4/SMISO4/SSCL4/ RXD6/SMISO6/SSCL6/ RSPCKA | |
| 88 | | PA7 | A7 | TIOCB2 | MISOA | |
| 89 | | PA6 | A6 | MTIC5V/MTCLKB/ TMCI3/POE2#/TIOCA2 | CTS5#/RTS5#/SS5#/ MOSIA/ | |
| 90 | | PA5 | A5 | TIOCB1 | RSPCKA | |
| 91 | VCC | | | | | |
| 92 | | PA4 | A4 | MTIC5U/MTCLKA/ TMRI0/TIOCA1 | TXD5/SMOSI5/SSDA5/ SSLA0 | IRQ5-DS/CVREFB1 |
| 93 | VSS | | | | | |
| 94 | | PA3 | A3 | MTIOC0D/MTCLKD/ TIOCD0/TCLKB | RXD5/SMISO5/SSCL5 | IRQ6-DS/CMPB1 |
| 95 | | PA2 | A2 | | RXD5/SMISO5/SSCL5/ SSLA3 | |
| 96 | | PA1 | A1 | MTIOC0B/MTCLKC/ TIOCB0 | SCK5/SSLA2 | CVREFA |
| 97 | | PA0 | A0/BC0# | MTIOC4A/TIOCA0 | SSLA1 | CACREF |
| 98 | | P67 | | | | |
| 99 | | P66 | | | | |
| 100 | | P65 | | | | |
| 101 | | PE7 | D15[A15/D15] | | | IRQ7/AN015 |
| 102 | | PE6 | D14[A14/D14] | | CTS4#/RTS4#/SS4# | IRQ6/AN014 |
| 103 | | PK5 | | | TXD4/SMOSI4/SSDA4 | |
| 104 | | P70 | | | SCK4 | |
| 105 | | PK4 | | | RXD4/SMISO4/SSCL4 | |
| 106 | | PE5 | D13[A13/D13] | MTIOC4C/MTIOC2B | | IRQ5/AN013 |
| 107 | | PE4 | D12[A12/D12] | MTIOC4D/MTIOC1A | | AN012/CMPA2 |
| 108 | | PE3 | D11[A11/D11] | MTIOC4B/POE8# | CTS12#/RTS12#/SS12# | AN011/CMPA1 |
| 109 | | PE2 | D10[A10/D10] | MTIOC4A | RXD12/RXDX12/ SMISO12/SSCL12 | IRQ7-DS/AN010/ CVREFB0 |
| 110 | | PE1 | D9[A9/D9] | MTIOC4C | TXD12/TXDX12/SIOX12/ SMOSI12/SSDA12 | AN009/CMPB0 |
| 111 | | PE0 | D8[A8/D8] | | SCK12 | AN008 |
| 112 | | P64 | | | | |
| 113 | | P63 | | | | |
| 114 | | P62 | | | | |
| 115 | | P61 | | | CTS9#/RTS9#/SS9# | |
| 116 | | PK3 | | | RXD9/SMISO9/SSCL9 | |
| 117 | | P60 | | | SCK9 | |
| 118 | | PK2 | | | TXD9/SMOSI9/SSDA9 | |
| 119 | | PD7 | D7[A7/D7] | MTIC5U/POE0# | | IRQ7 |
| 120 | | PD6 | D6[A6/D6] | MTIC5V/POE1# | | IRQ6 |
| 121 | | PD5 | D5[A5/D5] | MTIC5W/POE2# | | IRQ5 |

**Table 1.12 List of Pins and Pin Functions (100-Pin LQFP) (2 / 3)**

| Pin No. | Power Supply, Clock, System Control | I/O Port | External Bus | Timers (MTU, TMR, POE) | Communications (SCIc, SCId, RSPI, RIIC) | Others |
|---|---|---|---|---|---|---|
| 42 | | P52 | RD# | | | |
| 43 | | P51 | WR1#/BC1#/WAIT# | | | |
| 44 | | P50 | WR0#/WR# | | | |
| 45 | | PC7 | A23/CS0# | MTIOC3A/TMO2/ MTCLKB | TXD8/SMOSI8/SSDA8/ MISOA | CACREF |
| 46 | | PC6 | A22/CS1# | MTIOC3C/MTCLKA/ TMCI2 | RXD8/SMISO8/SSCL8/ MOSIA | |
| 47 | | PC5 | A21/CS2#/WAIT# | MTIOC3B/MTCLKD/ TMRI2 | SCK8/RSPCKA | |
| 48 | | PC4 | A20/CS3# | MTIOC3D/MTCLKC/ TMCI1/POE0# | SCK5/CTS8#/RTS8#/ SS8#/SSLA0 | |
| 49 | | PC3 | A19 | MTIOC4D | TXD5/SMOSI5/SSDA5 | |
| 50 | | PC2 | A18 | MTIOC4B | RXD5/SMISO5/SSCL5/ SSLA3 | |
| 51 | | PC1 | A17 | MTIOC3A | SCK5/SSLA2 | |
| 52 | | PC0 | A16 | MTIOC3C | CTS5#/RTS5#/SS5#/ SSLA1 | |
| 53 | | PB7 | A15 | MTIOC3B | TXD9/SMOSI9/SSDA9 | |
| 54 | | PB6 | A14 | MTIOC3D | RXD9/SMISO9/SSCL9 | |
| 55 | | PB5 | A13 | MTIOC2A/MTIOC1B/ TMRI1/POE1# | SCK9 | |
| 56 | | PB4 | A12 | | CTS9#/RTS9#/SS9# | |
| 57 | | PB3 | A11 | MTIOC0A/MTIOC4A/ TMO0/POE3# | SCK6 | |
| 58 | | PB2 | A10 | | CTS6#/RTS6#/SS6# | |
| 59 | | PB1 | A9 | MTIOC0C/MTIOC4C/ TMCI0 | TXD6/SMOSI6/SSDA6 | IRQ4-DS |
| 60 | VCC | | | | | |
| 61 | | PB0 | A8 | MTIC5W | RXD6/SMISO6/SSCL6/ RSPCKA | |
| 62 | VSS | | | | | |
| 63 | | PA7 | A7 | | MISOA | |
| 64 | | PA6 | A6 | MTIC5V/MTCLKB/ TMCI3/POE2# | CTS5#/RTS5#/SS5#/ MOSIA | |
| 65 | | PA5 | A5 | | RSPCKA | |
| 66 | | PA4 | A4 | MTIC5U/MTCLKA/ TMRI0 | TXD5/SMOSI5/SSDA5/ SSLA0 | IRQ5-DS/CVREFB1 |
| 67 | | PA3 | A3 | MTIOC0D/MTCLKD | RXD5/SMISO5/SSCL5 | IRQ6-DS/CMPB1 |
| 68 | | PA2 | A2 | | RXD5/SMISO5/SSCL5/ SSLA3 | |
| 69 | | PA1 | A1 | MTIOC0B/MTCLKC | SCK5/SSLA2 | CVREFA |
| 70 | | PA0 | A0/BC0# | MTIOC4A | SSLA1 | CACREF |
| 71 | | PE7 | D15[A15/D15] | | | IRQ7/AN015 |
| 72 | | PE6 | D14[A14/D14] | | | IRQ6/AN014 |
| 73 | | PE5 | D13[A13/D13] | MTIOC4C/MTIOC2B | | IRQ5/AN013 |
| 74 | | PE4 | D12[A12/D12] | MTIOC4D/MTIOC1A | | AN012/CMPA2 |
| 75 | | PE3 | D11[A11/D11] | MTIOC4B/POE8# | CTS12#/RTS12#/SS12# | AN011/CMPA1 |
| 76 | | PE2 | D10[A10/D10] | MTIOC4A | RXD12/RXDX12/ SMISO12/SSCL12 | IRQ7-DS/AN010/ CVREFB0 |
| 77 | | PE1 | D9[A9/D9] | MTIOC4C | TXD12/TXDX12/SIOX12/ SMOSI12/SSDA12 | AN009/CMPB0 |
| 78 | | PE0 | D8[A8/D8] | | SCK12 | AN008 |
| 79 | | PD7 | D7[A7/D7] | MTIC5U/POE0# | | IRQ7 |

**Table 1.13 List of Pins and Pin Functions (80-Pin LQFP) (1 / 2)**

| Pin No. | Power Supply, Clock, System Control | I/O Port | Timers (MTU, TMR, POE) | Communications (SCIc, SCId, RSPI, RIIC) | Others |
|---|---|---|---|---|---|
| 1 | VREFH | | | | |
| 2 | | P03 | | | DA0 |
| 3 | VREFL | | | | |
| 4 | VCL | | | | |
| 5 | | PJ1 | MTIOC3A | | |
| 6 | MD | | | | FINED |
| 7 | XCIN | | | | |
| 8 | XCOUT | | | | |
| 9 | RES# | | | | |
| 10 | XTAL | P37 | | | |
| 11 | VSS | | | | |
| 12 | EXTAL | P36 | | | |
| 13 | VCC | | | | |
| 14 | | P35 | | | NMI |
| 15 | | P34 | MTIOC0A/TMCI3/POE2# | SCK6 | IRQ4 |
| 16 | | P32 | MTIOC0C/TMO3 | TXD6/SMOSI6/SSDA6 | IRQ2-DS/RTCOUT/ RTCIC2 |
| 17 | | P31 | MTIOC4D/TMCI2 | CTS1#/RTS1#/SS1# | IRQ1-DS/RTCIC1 |
| 18 | | P30 | MTIOC4B/TMRI3/POE8# | RXD1/SMISO1/SSCL1 | IRQ0-DS/RTCIC0 |
| 19 | | P27 | MTIOC2B/TMCI3 | SCK1 | |
| 20 | | P26 | MTIOC2A/TMO1 | TXD1/SMOSI1/SSDA1 | |
| 21 | | P21 | MTIOC1B/TMCI0 | RXD0/SSCL0 | |
| 22 | | P20 | MTIOC1A/TMRI0 | TXD0/SSDA0 | |
| 23 | | P17 | MTIOC3A/MTIOC3B/TMO1/ POE8# | SCK1/MISOA/ SDA-DS | IRQ7 |
| 24 | | P16 | MTIOC3C/MTIOC3D/TMO2 | TXD1/SMOSI1/SSDA1/MOSIA/ SCL-DS | IRQ6/RTCOUT/ ADTRG0# |
| 25 | | P15 | MTIOC0B/MTCLKB/TMCI2 | RXD1/SMISO1/SSCL1 | IRQ5 |
| 26 | | P14 | MTIOC3A/MTCLKA/TMRI2 | CTS1#/RTS1#/SS1# | IRQ4 |
| 27 | | P13 | MTIOC0B/TMO3 | SDA | IRQ3 |
| 28 | | P12 | TMCI1 | SCL | IRQ2 |
| 29 | | PH3 | TMCI0 | | |
| 30 | | PH2 | TMRI0 | | IRQ1 |
| 31 | | PH1 | TMO0 | | IRQ0 |
| 32 | | PH0 | | | CACREF |
| 33 | | P55 | MTIOC4D/TMO3 | | |
| 34 | | P54 | MTIOC4B/TMCI1 | | |
| 35 | | PC7 | MTIOC3A/TMO2/MTCLKB | TXD8/SMOSI8/SSDA8/MISOA | CACREF |
| 36 | | PC6 | MTIOC3C/MTCLKA/TMCI2 | RXD8/SMISO8/SSCL8/MOSIA | |
| 37 | | PC5 | MTIOC3B/MTCLKD/TMRI2 | SCK8/RSPCKA | |
| 38 | | PC4 | MTIOC3D/MTCLKC/TMCI1/ POE0# | SCK5/CTS8#/RTS8#/SS8#/ SSLA0 | |
| 39 | | PC3 | MTIOC4D | TXD5/SMOSI5/SSDA5 | |
| 40 | | PC2 | MTIOC4B | RXD5/SMISO5/SSCL5/SSLA3 | |
| 41 | | PB7 | MTIOC3B | TXD9/SMOSI9/SSDA9 | |
| 42 | | PB6 | MTIOC3D | RXD9/SMISO9/SSCL9 | |
| 43 | | PB5 | MTIOC2A/MTIOC1B/TMRI1/ POE1# | SCK9 | |
| 44 | | PB4 | | CTS9#/RTS9#/SS9# | |

**Table 1.14 List of Pins and Pin Functions (69-Pin WLBGA) (2 / 2)**

| Pin No. | Power Supply, Clock, System Control | I/O Port | Timers (MTU, TMR, POE) | Communications (SCIc, SCId, RSPI, RIIC) | Others |
|---|---|---|---|---|---|
| G3 | NC | | | | |
| G4 | | P54 | MTIOC4B/TMCI1 | | |
| G5 | | PH1 | TMO0 | | IRQ0 |
| G6 | | P14 | MTIOC3A/MTCLKA/TMRI2 | CTS1#/RTS1#/SS1# | IRQ4 |
| G7 | | P27 | MTIOC2B/TMCI3 | SCK1 | |
| G8 | | P32 | MTIOC0C/TMO3 | TXD6/SMOSI6/SSDA6 | IRQ2-DS/RTCOUT/ RTCIC2 |
| G9 | | P35 | | | NMI |
| H1 | | PB7 | MTIOC3B | TXD9/SMOSI9/SSDA9 | |
| H2 | | PC3 | MTIOC4D | TXD5/SMOSI5/SSDA5 | |
| H3 | | PC5 | MTIOC3B/MTCLKD/TMRI2 | SCK8/RSPCKA | |
| H4 | | PC6 | MTIOC3C/MTCLKA/TMCI2 | RXD8/SMISO8/SSCL8/MOSIA | |
| H5 | | P55 | MTIOC4D/TMO3 | | |
| H6 | | PH3 | TMCI0 | | |
| H7 | | P17 | MTIOC3A/MTIOC3B/TMO1/ POE8# | SCK1/MISOA/SDA-DS | IRQ7 |
| H8 | | P26 | MTIOC2A/TMO1 | TXD1/SMOSI1/SSDA1 | |
| H9 | | P30 | MTIOC4B/TMRI3/POE8# | RXD1/SMISO1/SSCL1 | IRQ0-DS/RTCIC0 |
| J1 | NC | | | | |
| J2 | | PC2 | MTIOC4B | RXD5/SMISO5/SSCL5/SSLA3 | |
| J3 | | PC4 | MTIOC3D/MTCLKC/TMCI1/ POE0# | SCK5/CTS8#/RTS8#/SS8#/ SSLA0 | |
| J4 | | PC7 | MTIOC3A/TMO2/MTCLKB | TXD8/SMOSI8/SSDA8/MISOA | CACREF |
| J5 | | PH0 | | | CACREF |
| J6 | | PH2 | TMRI0 | | IRQ1 |
| J7 | | P15 | MTIOC0B/MTCLKB/TMCI2 | RXD1/SMISO1/SSCL1 | IRQ5 |
| J8 | | P16 | MTIOC3C/MTIOC3D/TMO2 | TXD1/SMOSI1/SSDA1/ MOSIA/SCL-DS | IRQ6/RTCOUT/ ADTRG0# |
| J9 | NC | | | | |

Note: • Pin names to which –DS is appended are for pins that can be used to trigger release from deep software standby mode.
Note: • Leave the NC pin open.

**Table 1.15 List of Pins and Pin Functions (64-Pin TFLGA) (2 / 2)**

| Pin No. | Power Supply, Clock, System Control | I/O Port | Timers (MTU, TMR, POE) | Communication (SCIc, SCId, RSPI, RIIC) | Others |
|---|---|---|---|---|---|
| F5 | | P15 | MTIOC0B/MTCLKB/TMCI2 | RXD1/SMISO1/SSCL1 | IRQ5 |
| F6 | | PB1 | MTIOC0C/MTIOC4C/TMCI0 | TXD6/SMOSI6/SSDA6 | IRQ4-DS |
| F7 | | PB5 | MTIOC2A/MTIOC1B/TMRI1/ POE1# | SCK9 | |
| F8 | | PB3 | MTIOC0A/MTIOC4A/TMO0/ POE3# | SCK6 | |
| G1 | EXTAL | P36 | | | |
| G2 | | P26 | MTIOC2A/TMO1 | TXD1/SMOSI1/SSDA1 | |
| G3 | | PH3 | TMCI0 | | |
| G4 | | PH0 | | | CACREF |
| G5 | | PC7 | MTIOC3A/TMO2/MTCLKB | TXD8/SMOSI8/SSDA8/MISOA | CACREF |
| G6 | | PC6 | MTIOC3C/MTCLKA/TMCI2 | RXD8/SMISO8/SSCL8/MOSIA | |
| G7 | | PC3 | MTIOC4D | TXD5/SMOSI5/SSDA5 | |
| G8 | | PB6 | MTIOC3D | RXD9/SMISO9/SSCL9 | |
| H1 | XTAL | P37 | | | |
| H2 | | P17 | MTIOC3A/MTIOC3B/TMO1/ POE8# | SCK1/MISOA/SDA-DS | IRQ7 |
| H3 | | PH2 | TMRI0 | | IRQ1 |
| H4 | | PH1 | TMO0 | | IRQ0 |
| H5 | | P55 | MTIOC4D/TMO3 | | |
| H6 | | P54 | MTIOC4B/TMCI1 | | |
| H7 | | PC2 | MTIOC4B | RXD5/SMISO5/SSCL5/SSLA3 | |
| H8 | | PB7 | MTIOC3B | TXD9/SMOSI9/SSDA9 | |

Note: • Pin names to which -DS is appended are for pins that can be used to trigger release from deep software standby mode.

**Table 1.17 List of Pins and Pin Functions (48-Pin LQFP) (2 / 2)**

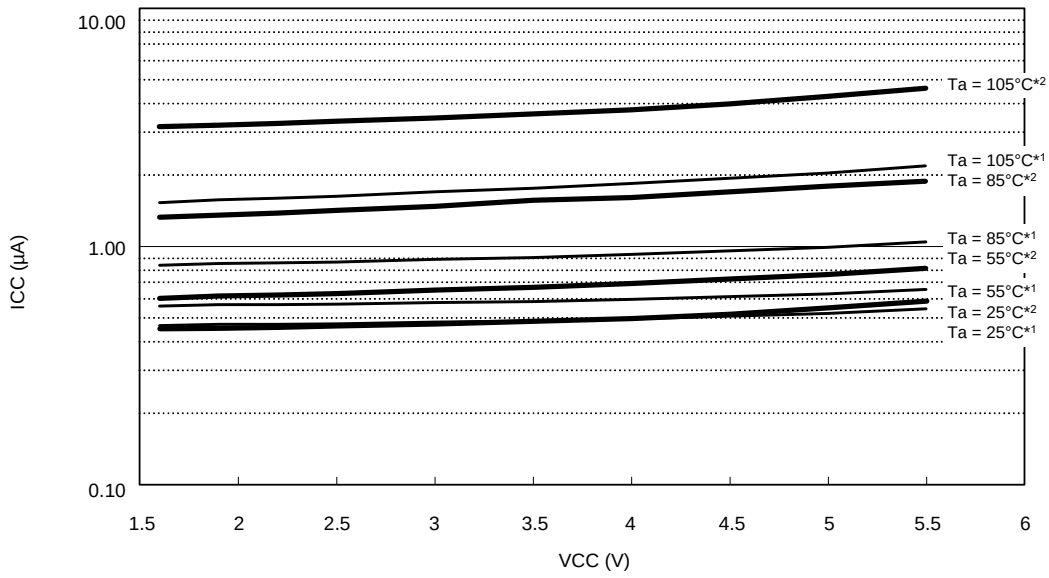
| Pin No. | Power Supply, Clock, System Control | I/O Port | Timers (MTU, TMR, POE) | Communication (SCIc, SCId, RSPI, RIIC) | Others |
|---|---|---|---|---|---|
| 44 | VREFL0 | | | | |
| 45 | | P40 | | | AN000 |
| 46 | VREFH0 | | | | |
| 47 | AVCC0 | | | | |
| 48 | AVSS0 | | | | |

Note: • Pin names to which –DS is appended are for pins that can be used to trigger release from deep software standby mode.

**Table 4.1 List of I/O Registers (Address Order) (8 / 29)**

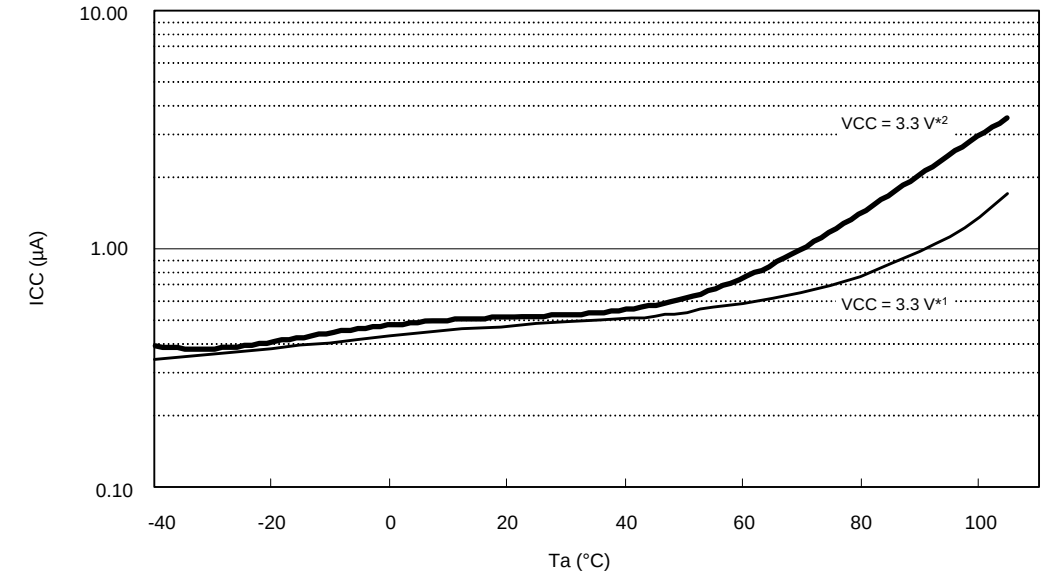
| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access Cycles | |
|---|---|---|---|---|---|---|---|
| | | | | | | ICLK ≥ PCLK | ICLK < PCLK |
| 0008 71D0h | ICU | DTC activation enable register 208 | DTCER208 | 8 | 8 | 2 ICLK | |
| 0008 71D3h | ICU | DTC activation enable register 211 | DTCER211 | 8 | 8 | 2 ICLK | |
| 0008 71D4h | ICU | DTC activation enable register 212 | DTCER212 | 8 | 8 | 2 ICLK | |
| 0008 71D7h | ICU | DTC activation enable register 215 | DTCER215 | 8 | 8 | 2 ICLK | |
| 0008 71D8h | ICU | DTC activation enable register 216 | DTCER216 | 8 | 8 | 2 ICLK | |
| 0008 71DBh | ICU | DTC activation enable register 219 | DTCER219 | 8 | 8 | 2 ICLK | |
| 0008 71DCh | ICU | DTC activation enable register 220 | DTCER220 | 8 | 8 | 2 ICLK | |
| 0008 71DFh | ICU | DTC activation enable register 223 | DTCER223 | 8 | 8 | 2 ICLK | |
| 0008 71E0h | ICU | DTC activation enable register 224 | DTCER224 | 8 | 8 | 2 ICLK | |
| 0008 71E3h | ICU | DTC activation enable register 227 | DTCER227 | 8 | 8 | 2 ICLK | |
| 0008 71E4h | ICU | DTC activation enable register 228 | DTCER228 | 8 | 8 | 2 ICLK | |
| 0008 71E7h | ICU | DTC activation enable register 231 | DTCER231 | 8 | 8 | 2 ICLK | |
| 0008 71E8h | ICU | DTC activation enable register 232 | DTCER232 | 8 | 8 | 2 ICLK | |
| 0008 71EBh | ICU | DTC activation enable register 235 | DTCER235 | 8 | 8 | 2 ICLK | |
| 0008 71ECh | ICU | DTC activation enable register 236 | DTCER236 | 8 | 8 | 2 ICLK | |
| 0008 71EFh | ICU | DTC activation enable register 239 | DTCER239 | 8 | 8 | 2 ICLK | |
| 0008 71F0h | ICU | DTC activation enable register 240 | DTCER240 | 8 | 8 | 2 ICLK | |
| 0008 71F7h | ICU | DTC activation enable register 247 | DTCER247 | 8 | 8 | 2 ICLK | |
| 0008 71F8h | ICU | DTC activation enable register 248 | DTCER248 | 8 | 8 | 2 ICLK | |
| 0008 71FBh | ICU | DTC activation enable register 251 | DTCER251 | 8 | 8 | 2 ICLK | |
| 0008 71FCh | ICU | DTC activation enable register 252 | DTCER252 | 8 | 8 | 2 ICLK | |
| 0008 7202h | ICU | Interrupt request enable register 02 | IER02 | 8 | 8 | 2 ICLK | |
| 0008 7203h | ICU | Interrupt request enable register 03 | IER03 | 8 | 8 | 2 ICLK | |
| 0008 7204h | ICU | Interrupt request enable register 04 | IER04 | 8 | 8 | 2 ICLK | |
| 0008 7205h | ICU | Interrupt request enable register 05 | IER05 | 8 | 8 | 2 ICLK | |
| 0008 7207h | ICU | Interrupt request enable register 07 | IER07 | 8 | 8 | 2 ICLK | |
| 0008 7208h | ICU | Interrupt request enable register 08 | IER08 | 8 | 8 | 2 ICLK | |
| 0008 720Bh | ICU | Interrupt request enable register 0B | IER0B | 8 | 8 | 2 ICLK | |
| 0008 720Ch | ICU | Interrupt request enable register 0C | IER0C | 8 | 8 | 2 ICLK | |
| 0008 720Dh | ICU | Interrupt request enable register 0D | IER0D | 8 | 8 | 2 ICLK | |
| 0008 720Eh | ICU | Interrupt request enable register 0E | IER0E | 8 | 8 | 2 ICLK | |
| 0008 720Fh | ICU | Interrupt request enable register 0F | IER0F | 8 | 8 | 2 ICLK | |
| 0008 7210h | ICU | Interrupt request enable register 10 | IER10 | 8 | 8 | 2 ICLK | |
| 0008 7211h | ICU | Interrupt request enable register 11 | IER11 | 8 | 8 | 2 ICLK | |
| 0008 7212h | ICU | Interrupt request enable register 12 | IER12 | 8 | 8 | 2 ICLK | |
| 0008 7213h | ICU | Interrupt request enable register 13 | IER13 | 8 | 8 | 2 ICLK | |
| 0008 7214h | ICU | Interrupt request enable register 14 | IER14 | 8 | 8 | 2 ICLK | |
| 0008 7215h | ICU | Interrupt request enable register 15 | IER15 | 8 | 8 | 2 ICLK | |
| 0008 7216h | ICU | Interrupt request enable register 16 | IER16 | 8 | 8 | 2 ICLK | |
| 0008 7217h | ICU | Interrupt request enable register 17 | IER17 | 8 | 8 | 2 ICLK | |
| 0008 7218h | ICU | Interrupt request enable register 18 | IER18 | 8 | 8 | 2 ICLK | |
| 0008 7219h | ICU | Interrupt request enable register 19 | IER19 | 8 | 8 | 2 ICLK | |
| 0008 721Ah | ICU | Interrupt request enable register 1A | IER1A | 8 | 8 | 2 ICLK | |
| 0008 721Bh | ICU | Interrupt request enable register 1B | IER1B | 8 | 8 | 2 ICLK | |
| 0008 721Ch | ICU | Interrupt request enable register 1C | IER1C | 8 | 8 | 2 ICLK | |
| 0008 721Dh | ICU | Interrupt request enable register 1D | IER1D | 8 | 8 | 2 ICLK | |
| 0008 721Eh | ICU | Interrupt request enable register 1E | IER1E | 8 | 8 | 2 ICLK | |
| 0008 721Fh | ICU | Interrupt request enable register 1F | IER1F | 8 | 8 | 2 ICLK | |
| 0008 72E0h | ICU | Software interrupt activation register | SWINTR | 8 | 8 | 2 ICLK | |
| 0008 72F0h | ICU | Fast interrupt set register | FIR | 16 | 16 | 2 ICLK | |
| 0008 7300h | ICU | Interrupt source priority register 000 | IPR000 | 8 | 8 | 2 ICLK | |

Note 5. Clocks are supplied to the peripheral functions. This does not include BGO operation. The clock source is HOCO and the oscillation frequency is 40 MHz. BCLK, FCLK, and PCLK are ICLK divided by 1.
Note 6. This is the increase if data is programmed to or erasing from the ROM or E2 DataFlash during program execution.
Note 7. Clock supply to the peripheral functions is stopped. This does not include BGO operation. The clock source is HOCO and the oscillation frequency is 32 MHz. BCLK, FCLK, and PCLK are set to divided by 64.
Note 8. Clocks are supplied to the peripheral functions. This does not include BGO operation. The clock source is HOCO and the oscillation frequency is 32 MHz. BCLK, FCLK, and PCLK are ICLK divided by 1.
Note 9. Clock supply to the peripheral functions is stopped. This does not include BGO operation. The clock source is the sub oscillation circuit. BCLK, FCLK, and PCLK are set to divided by 64.
Note 10. Clocks are supplied to the peripheral functions. This does not include BGO operation. The clock source is the sub oscillation circuit. BCLK, FCLK, and PCLK are ICLK divided by 1.
Note 11. Value when the main clock continues oscillating at 12.5 MHz.




Note 1. Average value of the tested middle samples during product evaluation.
Note 2. Average value of the tested upper-limit samples during product evaluation.

**Figure 5.15 Voltage Dependency in Deep Software Standby Mode (DEEPCUT1 Bit = 1) (Reference Data) for Chip Version C**




Note 1. Average value of the tested middle samples during product evaluation
Note 2. Average value of the tested upper-limit samples during product evaluation.

**Figure 5.16 Temperature Dependency in Deep Software Standby Mode (DEEPCUT1 Bit = 1) (Reference Data) for Chip Version C**

[Chip version B with 256 Kbytes or less of flash memory and 48 to 100 pins]

**Table 5.13 DC Characteristics (12)**

Conditions: VCC = AVCC0 = 1.62 to 5.5 V, VSS = AVSS0 = VREFL = VREFL0 = 0 V, $T_a$ = –40 to +105°C

| Item | | | | | Symbol | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|---|---|
| Supply current*1 | Middle-speed operating modes 1A and 1B | Normal operating mode | No peripheral operation | ICLK = 32 MHz*2 | $I_{CC}$ | 5.3 | — | mA | |
| | | | | ICLK = 20 MHz*3 | | 4.6 | — | | |
| | | | All peripheral operation: Normal | ICLK = 32 MHz*4 | | 20.1 | — | | |
| | | | | ICLK = 20 MHz*5 | | 14.3 | — | | |
| | | | All peripheral operation: Max. | ICLK = 32 MHz*4 | | — | 35 | | |
| | | | | ICLK = 20 MHz*5 | | — | — | | |
| | | Sleep mode | No peripheral operation | ICLK = 32 MHz | | 3.4 | — | | |
| | | | | ICLK = 20 MHz | | 3.3 | — | | |
| | | | All peripheral operation: Normal | ICLK = 32 MHz | | 11.5 | — | | |
| | | | | ICLK = 20 MHz | | 9 | — | | |
| | | All-module clock stop mode | | ICLK = 32 MHz | | 3 | — | | |
| | | | | ICLK = 20 MHz | | 3 | — | | |
| | | Increase during BGO operation*6 | Middle-speed operating mode 1A | | | 17 | — | | |
| | | | Middle-speed operating mode 1B | | | 17 | — | | |
| | Middle-speed operating modes 2A and 2B | Normal operating mode | No peripheral operation*2 | ICLK = 32 MHz | | 4.7 | — | | |
| | | | | ICLK = 16 MHz | | 3.4 | — | | |
| | | | | ICLK = 8 MHz | | 2.7 | — | | |
| | | | All peripheral operation: Normal*4 | ICLK = 32 MHz | | 19.6 | — | | |
| | | | | ICLK =16 MHz | | 11.3 | — | | |
| | | | | ICLK = 8 MHz | | 7.2 | — | | |
| | | | All peripheral operation: Max.*4 | ICLK = 32 MHz | | — | 34 | | |
| | | | | ICLK = 16 MHz | | — | — | | |
| | | | | ICLK = 8 MHz | | — | — | | |
| | | Sleep mode | No peripheral operation | ICLK = 32 MHz | | 2.8 | — | | |
| | | | | ICLK = 16 MHz | | 2.5 | — | | |
| | | | | ICLK = 8 MHz | | 2.2 | — | | |
| | | | All peripheral operation: Normal | ICLK = 32 MHz | | 11 | — | | |
| | | | | ICLK = 16 MHz | | 7.2 | — | | |
| | | | | ICLK = 8 MHz | | 5.3 | — | | |
| | | All-module clock stop mode | | ICLK = 32 MHz | | 2.4 | — | | |
| | | | | ICLK = 16 MHz | | 2.2 | — | | |
| | | | | ICLK = 8 MHz | | 2.1 | — | | |
| | | Increase during BGO operation*6 | Middle-speed operating mode 1A | | | 17 | — | | |
| | | | Middle-speed operating mode 1B | | | 17 | — | | |

## 5.3.5 Bus Timing

**Table 5.49 Bus Timing (1)**

Conditions: VCC = AVCC0 = 2.7 to 5.5 V, VSS = AVSS0 = VREFL = VREFL0 = 0 V,
fBCLK ≤ 25 MHz (BCLK pin output frequency ≤ 12.5 MHz), $T_a$ = –40 to +105°C, $V_{OH}$ = VCC × 0.5,
$V_{OL}$ = VCC × 0.5, $I_{OH}$ = –1.0 mA, $I_{OL}$ = 1.0 mA, $C_L$ = 30 pF
When normal output is selected by the drive capacity register

| Item | Symbol | Min. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|
| Address delay time | $t_{AD}$ | — | 60 | ns | Figure 5.76 to Figure 5.79 |
| Byte control delay time | $t_{BCD}$ | — | 60 | ns | |
| CS# delay time | $t_{CSD}$ | — | 60 | ns | |
| RD# delay time | $t_{RSD}$ | — | 60 | ns | |
| Read data setup time | $t_{RDS}$ | 40 | — | ns | |
| Read data hold time | $t_{RDH}$ | 0 | — | ns | |
| WR# delay time | $t_{WRD}$ | — | 60 | ns | |
| Write data delay time | $t_{WDD}$ | — | 60 | ns | |
| Write data hold time | $t_{WDH}$ | 0 | — | ns | |
| WAIT# setup time | $t_{WTS}$ | 40 | — | ns | Figure 5.80 |
| WAIT# hold time | $t_{WTH}$ | 0 | — | ns | |

**Table 5.50 Bus Timing (2)**

Conditions: VCC = AVCC0 = 1.8 to 2.7 V, VSS = AVSS0 = VREFL = VREFL0 = 0 V,
fBCLK ≤ 16 MHz (BCLK pin output frequency ≤ 8 MHz), $T_a$ = –40 to +105°C, $V_{OH}$ = VCC × 0.5,
$V_{OL}$ = VCC × 0.5, $I_{OH}$ = –1.0 mA, $I_{OL}$ = 1.0 mA, $C_L$ = 30 pF
When normal output is selected by the drive capacity register

| Item | Symbol | Min. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|
| Address delay time | $t_{AD}$ | — | 90 | ns | Figure 5.76 to Figure 5.79 |
| Byte control delay time | $t_{BCD}$ | — | 90 | ns | |
| CS# delay time | $t_{CSD}$ | — | 90 | ns | |
| RD# delay time | $t_{RSD}$ | — | 90 | ns | |
| Read data setup time | $t_{RDS}$ | 60 | — | ns | |
| Read data hold time | $t_{RDH}$ | 0 | — | ns | |
| WR# delay time | $t_{WRD}$ | — | 90 | ns | |
| Write data delay time | $t_{WDD}$ | — | 90 | ns | |
| Write data hold time | $t_{WDH}$ | 0 | — | ns | |
| WAIT# setup time | $t_{WTS}$ | 60 | — | ns | Figure 5.80 |
| WAIT# hold time | $t_{WTH}$ | 0 | — | ns | |

**Table 5.51 Bus Timing (3)**

Conditions: VCC = AVCC0 = 1.62 to 1.8 V, VSS = AVSS0 = VREFL = VREFL0 = 0 V,
fBCLK ≤ 12 MHz (BCLK pin output frequency ≤ 6 MHz), $T_a$ = –40 to +105°C, $V_{OH}$ = VCC × 0.5,
$V_{OL}$ = VCC × 0.5, $I_{OH}$ = –0.5 mA, $I_{OL}$ = 0.5 mA, $C_L$ = 30 pF
When normal output is selected by the drive capacity register

| Item | Symbol | Min. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|
| Address delay time | $t_{AD}$ | — | 125 | ns | Figure 5.76 to Figure 5.79 |
| Byte control delay time | $t_{BCD}$ | — | 125 | ns | |
| CS# delay time | $t_{CSD}$ | — | 125 | ns | |
| RD# delay time | $t_{RSD}$ | — | 125 | ns | |
| Read data setup time | $t_{RDS}$ | 85 | — | ns | |
| Read data hold time | $t_{RDH}$ | 0 | — | ns | |
| WR# delay time | $t_{WRD}$ | — | 125 | ns | |
| Write data delay time | $t_{WDD}$ | — | 125 | ns | |
| Write data hold time | $t_{WDH}$ | 0 | — | ns | |
| WAIT# setup time | $t_{WTS}$ | 85 | — | ns | Figure 5.80 |
| WAIT# hold time | $t_{WTH}$ | 0 | — | ns | |

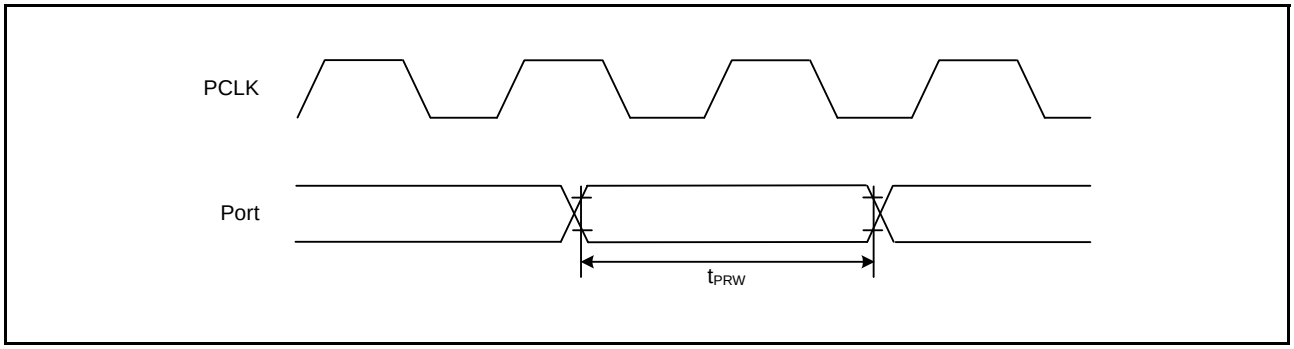



**Figure 5.83 I/O Port Input Timing**

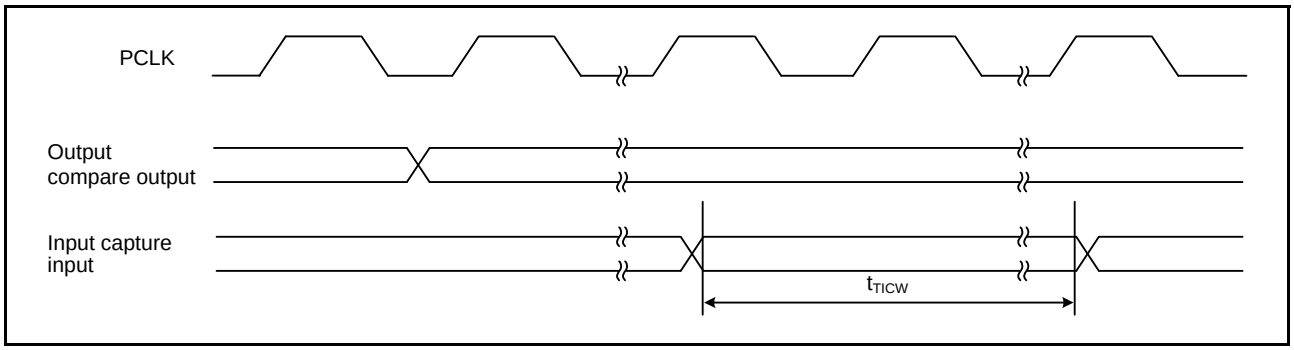



**Figure 5.84 MTU/TPU Input/Output Timing**

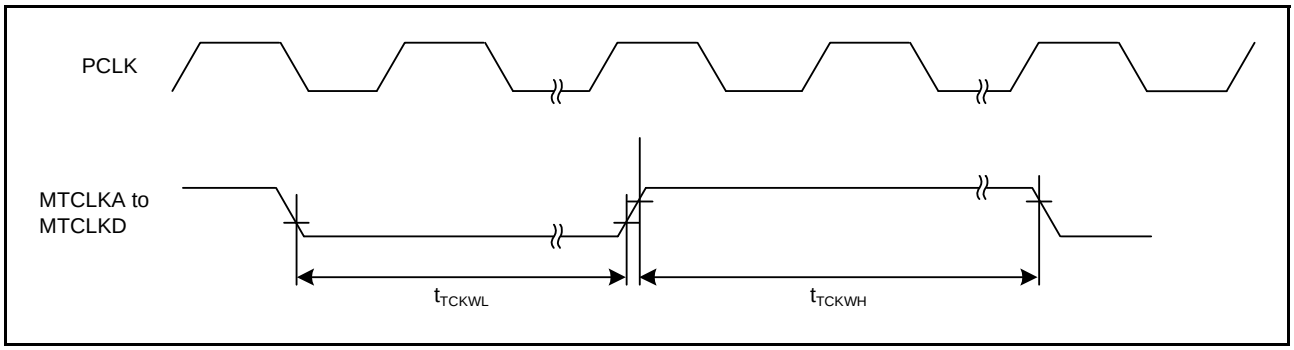



**Figure 5.85 MTU/TPU Clock Input Timing**

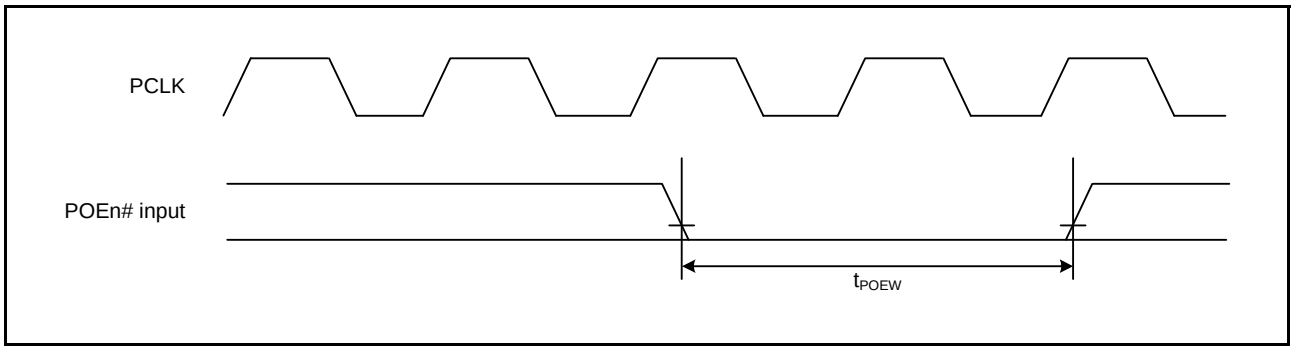



**Figure 5.86 POE# Input Timing**

## 5.9 Oscillation Stop Detection Timing

**Table 5.73 Oscillation Stop Detection Circuit Characteristics**

Conditions: VCC = AVCC0 = 1.62 to 5.5 V, VSS = AVSS0 = VREFL = VREFL0 = 0 V, $T_a$ = –40 to +105°C

| Item | Symbol | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| Detection time | $t_{dr}$ | — | — | 1 | ms | Figure 5.108 |

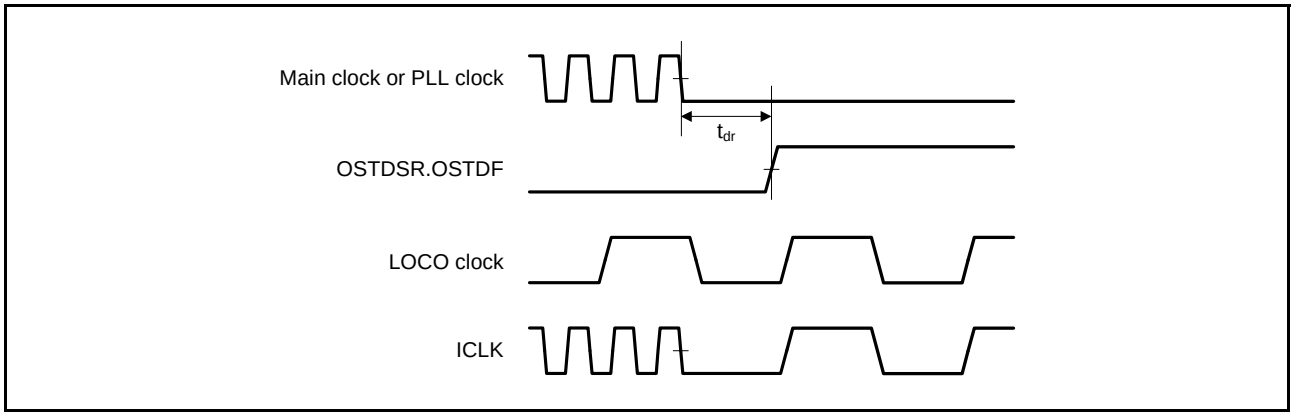



**Figure 5.108 Oscillation Stop Detection Timing**

[Chip versions A and C]

**Table 5.77 ROM (Flash Memory for Code Storage) Characteristics (4) : middle-speed operating mode 1B**

Conditions: VCC = AVCC0 = 1.62 to 3.6 V, VREFH = VREFH0 = AVCC0, VSS = AVSS0 = VREFL = VREFL0 = 0 V
Temperature range for the programming/erasure operation: $T_a$ = –40 to +105°C

| Item | | Symbol | FCLK = 4 MHz | | | FCLK = 32 MHz*1 | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | Min. | Typ. | Max. | |
| Programming time when $N_{PEC}$ ≤ 100 times | 2 bytes | $t_{P2}$ | — | 0.69 | 6.0 | — | 0.30 | 3.5 | ms |
| | 8 bytes | $t_{P8}$ | — | 0.69 | 6.0 | — | 0.30 | 3.5 | |
| | 128 bytes | $t_{P128}$ | — | 1.76 | 14.2 | — | 0.85 | 8.3 | |
| Programming time when $N_{PEC}$ > 100 times | 2 bytes | $t_{P2}$ | — | 0.81 | 7.1 | — | 0.35 | 4.2 | ms |
| | 8 bytes | $t_{P8}$ | — | 0.81 | 7.6 | — | 0.35 | 4.5 | |
| | 128 bytes | $t_{P128}$ | — | 1.99 | 17.5 | — | 0.96 | 10 | |
| Erasure time when $N_{PEC}$ ≤ 100 times | 2 Kbytes | $t_{E2K}$ | — | 24.5 | 113.7 | — | 19.0 | 46 | ms |
| Erasure time when $N_{PEC}$ > 100 times | 2 Kbytes | $t_{E2K}$ | — | 29.8 | 225.8 | — | 23.2 | 90 (1000 times ≥ $N_{PEC}$ > 100 times), 98 (10000 times ≥ $N_{PEC}$ > 1000 times) | ms |
| Suspend delay time during programming (in programming/erasure priority mode) | | $t_{SPD}$ | — | — | 1.7 | — | — | 1.6 | ms |
| First suspend delay time during programming (in suspend priority mode) | | $t_{SPSD1}$ | — | — | 220 | — | — | 120 | µs |
| Second suspend delay time during programming (in suspend priority mode) | | $t_{SPSD2}$ | — | — | 1.7 | — | — | 1.6 | ms |
| Suspend delay time during erasing (in programming/erasure priority mode) | | $t_{SED}$ | — | — | 1.7 | — | — | 1.6 | ms |
| First suspend delay time during erasing (in suspend priority mode) | | $t_{SESD1}$ | — | — | 220 | — | — | 120 | µs |
| Second suspend delay time during erasing (in suspend priority mode) | | $t_{SESD2}$ | — | — | 1.7 | — | — | 1.6 | ms |
| FCU reset time | | $t_{FCUR}$ | 20 µs or longer and FCLK × 6 or greater | — | — | 20 µs or longer and FCLK × 6 or greater | — | — | µs |

Note 1. The operating frequency is 20 MHz (max.) when the voltage is in the range from 1.62 V to less than 1.8 V.

## 5.11 E2 DataFlash Characteristics

[Chip version A]

**Table 5.80 E2 DataFlash Characteristics (1)**

| Item | Symbol | Min. | Typ. | Max. | Unit | Conditions |
|---|---|---|---|---|---|---|
| Reprogramming/erasure cycle*1 | $N_{DPEC}$ | 100000 | — | — | Times | |
| Data hold time | $t_{DRP}$ | 10*2 | — | — | Year | |

Note 1. The reprogram/erase cycle is the number of erasing for each block. When the reprogram/erase cycle is n times (n = 100000), erasing can be performed n times for each block. For instance, when 8-byte programming is performed 16 times for different addresses in 128-byte block and then the entire block is erased, the reprogram/erase cycle is counted as one. However, programming the same address for several times as one erasing is not enabled (overwriting is prohibited).

Note 2. This result is obtained from reliability testing.

[Chip versions B and C]

**Table 5.81 E2 DataFlash Characteristics (2)**

| Item | | Symbol | Min. | Typ. | Max. | Unit | Conditions |
|---|---|---|---|---|---|---|---|
| Reprogramming/erasure cycle*1 | | $N_{DPEC}$ | 100000 | — | — | Times | |
| Data hold time | After 100000 times of $N_{DPEC}$ | $t_{DRP}$ | 30*2 | — | — | Year | Ta = +85°C |

Note 1. The reprogram/erase cycle is the number of erasing for each block. When the reprogram/erase cycle is n times (n = 100000), erasing can be performed n times for each block. For instance, when 8-byte programming is performed 16 times for different addresses in 128-byte block and then the entire block is erased, the reprogram/erase cycle is counted as one. However, programming the same address for several times as one erasing is not enabled (overwriting is prohibited).

Note 2. This result is obtained from reliability testing.