Renesas Electronics America Inc - R5F5210BBDFB#30 Datasheet

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	RX
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	EBI/EMI, I²C, SCI, SPI
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	122
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	8K x 8
RAM Size	96K x 8
Voltage - Supply (Vcc/Vdd)	1.62V ~ 5.5V
Data Converters	A/D 16x12b; D/A 2x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LFQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f5210bbdfb-30

1.Overview

1.1 Outline of Specifications

Table 1.1 lists the specifications in outline, and Table 1.2 gives a comparison of the functions of products in different packages.
Table 1.1 is for products with the greatest number of functions, so numbers of peripheral modules and channels will differ in accord with the package. For details, see Table 1.2, Comparison of Functions for Different Packages.
This product includes chip version A (part no.: R5F5210xAxxx), chip version B (part no.: R5F5210xBxxx), and chip version C (part no: R5F5210xCxxx).
For the specification differences between chip versions A, B, and C, see Table 1, Specification Differences Depending on Chip Versions.

Table 1.1 Outline of Specifications (1 / 5)

Classification	Module/Function	Description
CPU	CPU	• Maximum operating frequency: 50 MHz • 32-bit RX CPU • Minimum instruction execution time: One instruction per state (cycle of the system clock) • Address space: 4-Gbyte linear • Register General purpose: Sixteen 32-bit registers Control: Eight 32-bit registers Accumulator: One 64-bit register • Basic instructions: 73 • DSP instructions: 9 • Addressing modes: 10 • Data arrangement Instructions: Little endian Data: Selectable as little endian or big endian • On-chip 32-bit multiplier: 32 × 32 → 64 bits • On-chip divider: 32 / 32 → 32 bits • Barrel shifter: 32 bits
Memory	ROM	• Capacity: 64 K/96 K/128 K/256 K/384 K/512 K/768 Kbytes/1 Mbyte • 50 MHz, no-wait memory access • On-board programming: 3 types Off-board programming
	RAM	• Capacity: 12 K/16 K/20 K/32 K/64 K/96 Kbytes • 50 MHz, no-wait memory access
	E2 DataFlash	• Capacity: 8 Kbytes • Number of times for programming/erasing: 100,000
MCU operating mode		Single-chip mode, on-chip ROM enabled expansion mode, and on-chip ROM disabled expansion mode (software switching)
Clock	Clock generation circuit	• Main clock oscillator, sub-clock oscillator, low-speed on-chip oscillator, high-speed on-chip oscillator, PLL frequency synthesizer, and IWDT-dedicated on-chip oscillator • Oscillation stop detection • Measuring circuit for accuracy of clock frequency (clock-accuracy check: CAC) • Independent settings for the system clock (ICLK), peripheral module clock (PCLK), external bus clock (BCLK), and FlashIF clock (FCLK) The CPU and system sections such as other bus masters run in synchronization with the system clock (ICLK): 50 MHz (at max.) Peripheral modules run in synchronization with the peripheral module clock (PCLK): 32 MHz (at max.) Devices connected to the external bus run in synchronization with the external bus clock (BCLK): 12.5 MHz (at max.) The flash peripheral circuit runs in synchronization with the FlashIF clock (FCLK): 32 MHz (at max.)
Reset		RES# pin reset, power-on reset, voltage monitoring reset, watchdog timer reset, independent watchdog timer reset, deep software standby reset, and software reset
Voltage detection	Voltage detection circuit (LVDAa)	• When the voltage on VCC falls below the voltage detection level, an internal reset or internal interrupt is generated. Voltage detection circuit 0 is capable of selecting the detection voltage from 4 levels Voltage detection circuit 1 is capable of selecting the detection voltage from 16 levels Voltage detection circuit 2 is capable of selecting the detection voltage from 16 levels

Table 1.1 Outline of Specifications (2 / 5)

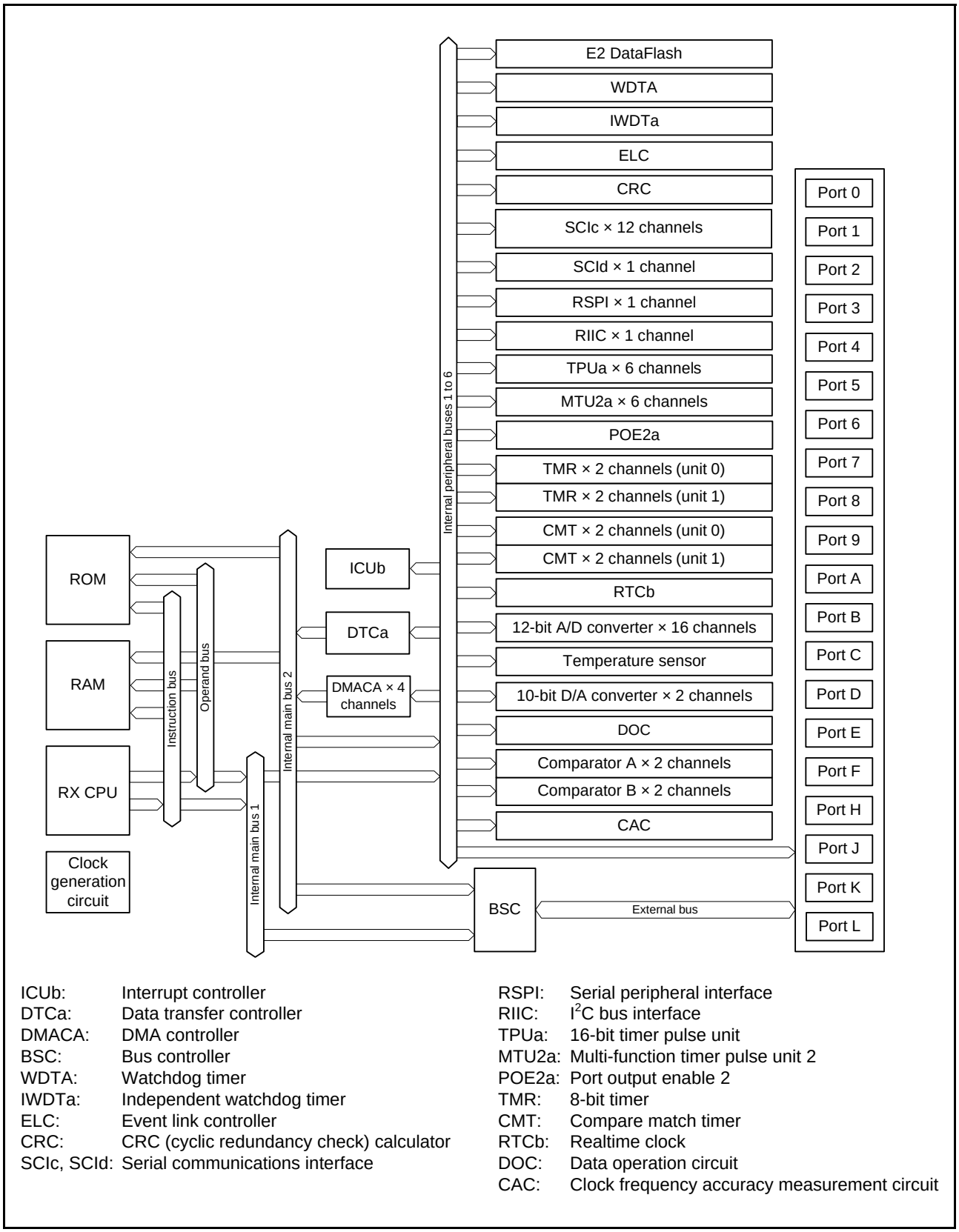
Classification	Module/Function	Description
Low power consumption	Low power consumption facilities	• Module stop function • Four low power consumption modes Sleep mode, all-module clock stop mode, software standby mode, and deep software standby mode
	Function for lower operating power consumption	• Operating power control modes [Chip versions A and C] High-speed operating mode, middle-speed operating mode 1A, middle-speed operating mode 1B, low-speed operating mode 1, low-speed operating mode 2 [Chip version B] High-speed operating mode, middle-speed operating mode 1A, middle-speed operating mode 1B, middle-speed operating mode 2A, middle-speed operating mode 2B, low-speed operating mode 1, low-speed operating mode 2
Interrupt	Interrupt controller (ICUb)	• Interrupt vectors: 167 • External interrupts: 9 (NMI, IRQ0 to IRQ7 pins) • Non-maskable interrupts: 6 (the NMI pin, oscillation stop detection interrupt, voltage monitoring 1 interrupt, voltage monitoring 2 interrupt, WDT interrupt, and IWDT interrupt) • 16 levels specifiable for the order of priority
External bus extension		• The external address space can be divided into four areas (CS0 to CS3), each with independent control of access settings. Capacity of each area: 16 Mbytes (CS0 to CS3) A chip-select signal (CS0# to CS3#) can be output for each area. Each area is specifiable as an 8-bit or 16-bit bus space The data arrangement in each area is selectable as little or big endian (only for data). Bus format: Separate bus, multiplex bus • Wait control • Write buffer facility
DMA	DMA controller (DMACA)	• 4 channels • Three transfer modes: Normal transfer, repeat transfer, and block transfer • Activation sources: Software trigger, external interrupts, and interrupt requests from peripheral functions
	Data transfer controller (DTCa)	• Three transfer modes: Normal transfer, repeat transfer, and block transfer • Activation sources: Interrupts • Chain transfer function
I/O ports	General I/O ports	145-pin/144-pin/100-pin/80-pin/69-pin/64-pin/48-pin • I/O: 122/122/84/64/48/48/34 • Input: 1/1/1/1/1/1/1 • Pull-up resistors: 122/122/84/64/48/48/34 • Open-drain outputs: 76/76/54/44/35/35/26 • 5-V tolerance:4/4/4/4/2/2*1/2
Event link controller (ELC)		• Event signals of 59 types can be directly connected to the module • Operations of timer modules are selectable at event input • Capable of event link operation for ports B and E
Multi-function pin controller (MPC)		• Capable of selecting input/output function from multiple pins

Table 1.1 Outline of Specifications (4 / 5)

Classification	Module/Function	Description
Communication functions	Serial communications interfaces (SCIc, SCId)	• 13 channels (channel 0 to 11: SCIc, channel 12: SCId) • Serial communications modes: Asynchronous, clock synchronous, and smart-card interface • On-chip baud rate generator allows selection of the desired bit rate • Choice of LSB-first or MSB-first transfer • Average transfer rate clock can be input from TMR timers (SCI5, SCI6, and SCI12) • Simple IIC • Simple SPI • Master/slave mode supported (SCId only) • Start frame and information frame are included (SCId only)
	I^2C bus interface (RIIC)	• 1 channel • Communications formats: I^2C bus format/SMBus format • Master/slave selectable • Supports the fast mode
	Serial peripheral interface (RSPI)	• 1 channel • Transfer facility Using the MOSI (master out, slave in), MISO (master in, slave out), SSL (slave select), and RSPI clock (RSPCK) signals enables serial transfer through SPI operation (four lines) or clock-synchronous operation (three lines) • Capable of handling serial transfer as a master or slave • Data formats • Choice of LSB-first or MSB-first transfer The number of bits in each transfer can be changed to any number of bits from 8 to 16, 20, 24, or 32 bits. 128-bit buffers for transmission and reception Up to four frames can be transmitted or received in a single transfer operation (with each frame having up to 32 bits) • Double buffers for both transmission and reception
12-bit A/D converter (S12ADb)		• 12 bits (16 channels × 1 unit) • 12-bit resolution • Minimum conversion time: 1.0 μs per channel (in operation with ADCLK at 50 MHz) • Operating modes Scan mode (single scan mode, continuous scan mode, and group scan mode) • Sample-and-hold function • Self-diagnosis for the A/D converter • Assistance in detecting disconnected analog inputs • Double-trigger mode (duplication of A/D conversion data) • A/D conversion start conditions A software trigger, a trigger from a timer (MTU), an external trigger signal, or ELC
Temperature sensor (TEMPSa)		• Outputs the voltage that changes depending on the temperature • PGA gain switchable: Four levels according to the voltage range
D/A converter (DA)		• 2 channels • 10-bit resolution • Output voltage: 0 V to VREFH
CRC calculator (CRC)		• CRC code generation for arbitrary amounts of data in 8-bit units • Select any of three generating polynomials: $X^8 + X^2 + X + 1$, $X^{16} + X^{15} + X^2 + 1$, or $X^{16} + X^{12} + X^5 + 1$ • Generation of CRC codes for use with LSB-first or MSB-first communications is selectable.
Comparator A (CMPA)		• 2 channels • Comparison of reference voltage and analog input voltage
Comparator B (CMPB)		• 2 channels • Comparison of reference voltage and analog input voltage
Data Operation Circuit (DOC)		Comparison, addition, and subtraction of 16-bit data
Power supply voltage/Operating frequency		VCC = 1.62 to 1.8 V: 20 MHz, VCC = 1.8 to 2.7 V: 32 MHz, VCC = 2.7 to 5.5 V: 50 MHz
Operating temperature		D version: −40 to +85°C, G version: −40 to +105°C*2

1.3 Block Diagram

Figure 1.2 shows a block diagram.



ICUb: Interrupt controller
DTCa: Data transfer controller
DMACA: DMA controller
BSC: Bus controller
WDTA: Watchdog timer
IWDTa: Independent watchdog timer
ELC: Event link controller
CRC: CRC (cyclic redundancy check) calculator
SCIc, SCId: Serial communications interface
RSPI: Serial peripheral interface
RIIC: I^2C bus interface
TPUa: 16-bit timer pulse unit
MTU2a: Multi-function timer pulse unit 2
POE2a: Port output enable 2
TMR: 8-bit timer
CMT: Compare match timer
RTCb: Realtime clock
DOC: Data operation circuit
CAC: Clock frequency accuracy measurement circuit

Figure 1.2 Block Diagram

Table 1.9 List of Pins and Pin Functions (145-Pin TFLGA) (3 / 4)

Pin No.	Power Supply, Clock, System Control	I/O Port	External Bus	Timers (MTU, TMR, POE)	Communications (SCIc, SCId, RSPI, RIIC)	Others
J12		PB2	A10	TIOCC3/TCLKC	CTS4#/RTS4#/SS4#/ CTS6#/RTS6#/SS6#	
J13		PB1	A9	MTIOC0C/MTIOC4C/ TMCI0/TIOCB3	TXD4/SMOSI4/SSDA4/ TXD6/SMOSI6/SSDA6	IRQ4-DS
K1		P27	CS3#	MTIOC2B/TMCI3	SCK1	
K2		P26	CS2#	MTIOC2A/TMO1	TXD1/SMOSI1/SSDA1/ CTS3#/RTS3#/SS3#	
K3		P31		MTIOC4D/TMCI2	CTS1#/RTS1#/SS1#	IRQ1-DS/RTCIC1
K4		P15		MTIOC0B/MTCLKB/ TMCI2/TIOCB2/TCLKB	RXD1/SMISO1/SSCL1/ SCK3	IRQ5
K5		P54	ALE	MTIOC4B/TMCI1	CTS2#/RTS2#/SS2#	
K6	BCLK	P53				
K7		P51	WR1#/BC1#/WAIT#		SCK2	
K8	VCC					
K9		P80		MTIOC3B	SCK10	
K10		P76			RXD11/SMISO11/SSCL11	
K11		PB7	A15	MTIOC3B/TIOCB5	TXD9/SMOSI9/SSDA9	
K12		PB6	A14	MTIOC3D/TIOCA5	RXD9/SMISO9/SSCL9	
K13		PB5	A13	MTIOC2A/MTIOC1B/ TMRI1/POE1#/TIOCB4	SCK9	
L1		P25	CS1#	MTIOC4C/MTCLKB/ TIOCA4	RXD3/SMISO3/SSCL3	ADTRG0#
L2		P23		MTIOC3D/MTCLKD/ TIOCD3	CTS0#/RTS0#/SS0#/ TXD3/SMOSI3/SSDA3	
L3		P16		MTIOC3C/MTIOC3D/ TMO2/TIOCB1/TCLKC	TXD1/SMOSI1/SSDA1/ MOSIA/SCL-DS/RXD3/ SMISO3/SSCL3	IRQ6/RTCOUT/ ADTRG0#
L4		P24	CS0#	MTIOC4A/MTCLKA/ TMRI1/TIOCB4	SCK3	
L5		P13		MTIOC0B/TMO3/ TIOCA5	SDA/TXD2/SMOSI2/ SSDA2	IRQ3
L6		P56		MTIOC3C/TIOCA1		
L7		P52	RD#		RXD2/SMISO2/SSCL2	
L8		P83		MTIOC4C	CTS10#/RTS10#	
L9		PC5	A21/CS2#/WAIT#	MTIOC3B/MTCLKD/ TMRI2	SCK8/RSPCKA	
L10		PC4	A20/CS3#	MTIOC3D/MTCLKC/ TMCI1/POE0#	SCK5/CTS8#/RTS8#/ SS8#/SSLA0	
L11		PC2	A18	MTIOC4B/TCLKA	RXD5/SMISO5/SSCL5/ SSLA3	
L12		P73				
L13		PL0				
M1		P22		MTIOC3B/MTCLKC/ TMO0/TIOCC3	SCK0	
M2		P17		MTIOC3A/MTIOC3B/ TMO1/POE8#/TIOCB0/ TCLKD	SCK1/MISOA/SDA-DS/ TXD3/SMOSI3/SSDA3	IRQ7
M3		P86		TIOCA0		
M4		P12		TMCI1	SCL/RXD2/SMISO2/ SSCL2	IRQ2
M5		PH3		TMCI0		
M6		PH0				CACREF
M7		P50	WR0#/WR#		TXD2/SMOSI2/SSDA2	
M8		PC6	A22/CS1#	MTIOC3C/MTCLKA/ TMCI2	RXD8/SMISO8/SSCL8/ MOSIA	
M9		P81		MTIOC3D	RXD10/SMISO10/SSCL10	
M10		P77			TXD11/SMOSI11/SSDA11	

Table 1.15 List of Pins and Pin Functions (64-Pin TFLGA) (1 / 2)

Pin No.	Power Supply, Clock, System Control	I/O Port	Timers (MTU, TMR, POE)	Communication (SCIc, SCId, RSPI, RIIC)	Others
A1		P05			DA1
A2	AVCC0				
A3	VREFH0				
A4	VREFL0				
A5	VREFH				
A6	VREFL				
A7		PE2	MTIOC4A	RXD12/RXDX12/SMISO12/ SSCL12	IRQ7-DS/AN010/ CVREFB0
A8		PE3	MTIOC4B/POE8#	CTS12#/RTS12#/SS12#	AN011/CMPA1
B1	VCL				
B2	AVSS0				
B3		P40			AN000
B4		P42			AN002
B5		P44			AN004
B6		P46			AN006
B7		PE1	MTIOC4C	TXD12/TXDX12/SIOX12/ SMOSI12/SSDA12	AN009/CMPB0
B8		PE4	MTIOC4D/MTIOC1A		AN012/CMPA2
C1	XCIN				
C2	MD				FINED
C3		P03			DA0
C4		P41			AN001
C5		P43			AN003
C6		PE0		SCK12	AN008
C7		PE5	MTIOC4C/MTIOC2B		IRQ5/AN013
C8		PA0	MTIOC4A	SSLA1	CACREF
D1	XCOUT				
D2	RES#				
D3		P27	MTIOC2B/TMCI3	SCK1	
D4		P14	MTIOC3A/MTCLKA/TMRI2	CTS1#/RTS1#/SS1#	IRQ4
D5		PA6	MTIC5V/MTCLKB/TMCI3/ POE2#	CTS5#/RTS5#/SS5#/MOSIA	
D6		PA4	MTIC5U/MTCLKA/TMRI0	TXD5/SMOSI5/SSDA5/SSLA0	IRQ5-DS/CVREFB1
D7		PA1	MTIOC0B/MTCLKC	SCK5/SSLA2	CVREFA
D8		PA3	MTIOC0D/MTCLKD	RXD5/SMISO5/SSCL5	IRQ6-DS/CMPB1
E1	VSS				
E2		P32	MTIOC0C/TMO3	TXD6/SMOSI6/SSDA6	IRQ2-DS/RTCOUT/ RTCIC2
E3		P30	MTIOC4B/TMRI3/POE8#	RXD1/SMISO1/SSCL1	IRQ0-DS/RTCIC0
E4		P16	MTIOC3C/MTIOC3D/TMO2	TXD1/SMOSI1/SSDA1/MOSIA/ SCL-DS	IRQ6/RTCOUT/ ADTRG0#
E5		PC4	MTIOC3D/MTCLKC/TMCI1/ POE0#	SCK5/CTS8#/RTS8#/SS8#/ SSLA0	
E6	VCC				
E7	VSS				
E8		PB0	MTIC5W	RXD6/SMISO6/SSCL6/RSPCKA	
F1	VCC				
F2		P35			NMI
F3		P31	MTIOC4D/TMCI2	CTS1#/RTS1#/SS1#	IRQ1-DS/RTCIC1
F4		PC5	MTIOC3B/MTCLKD/TMRI2	SCK8/RSPCKA	

4.1 I/O Register Addresses (Address Order)

Table 4.1 List of I/O Registers (Address Order) (1 / 29)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles: ICLK ≥ PCLK	Number of Access Cycles: ICLK < PCLK
0008 0000h	SYSTEM	Mode monitor register	MDMONR	16	16		3 ICLK
0008 0002h	SYSTEM	Mode status register	MDSR	16	16		3 ICLK
0008 0006h	SYSTEM	System control register 0	SYSCR0	16	16		3 ICLK
0008 0008h	SYSTEM	System control register 1	SYSCR1	16	16		3 ICLK
0008 000Ch	SYSTEM	Standby control register	SBYCR	16	16		3 ICLK
0008 0010h	SYSTEM	Module stop control register A	MSTPCRA	32	32		3 ICLK
0008 0014h	SYSTEM	Module stop control register B	MSTPCRB	32	32		3 ICLK
0008 0018h	SYSTEM	Module stop control register C	MSTPCRC	32	32		3 ICLK
0008 0020h	SYSTEM	System clock control register	SCKCR	32	32		3 ICLK
0008 0026h	SYSTEM	System clock control register 3	SCKCR3	16	16		3 ICLK
0008 0028h	SYSTEM	PLL control register	PLLCR	16	16		3 ICLK
0008 002Ah	SYSTEM	PLL control register 2	PLLCR2	8	8		3 ICLK
0008 0030h	SYSTEM	External bus clock control register	BCKCR	8	8		3 ICLK
0008 0032h	SYSTEM	Main clock oscillator control register	MOSCCR	8	8		3 ICLK
0008 0033h	SYSTEM	Sub-clock oscillator control register	SOSCCR	8	8		3 ICLK
0008 0034h	SYSTEM	Low-speed on-chip oscillator control register	LOCOCR	8	8		3 ICLK
0008 0035h	SYSTEM	IWDT-dedicated on-chip oscillator control register	ILOCOCR	8	8		3 ICLK
0008 0036h	SYSTEM	High-speed on-chip oscillator control register	HOCOCR	8	8		3 ICLK
0008 0037h	SYSTEM	High-speed on-chip oscillator control register 2	HOCOCR2	8	8		3 ICLK
0008 0040h	SYSTEM	Oscillation stop detection control register	OSTDCR	8	8		3 ICLK
0008 0041h	SYSTEM	Oscillation stop detection status register	OSTDSR	8	8		3 ICLK
0008 00A0h	SYSTEM	Operating power control register	OPCCR	8	8		3 ICLK
0008 00A1h	SYSTEM	Sleep mode return clock source switching register	RSTCKCR	8	8		3 ICLK
0008 00A2h	SYSTEM	Main clock oscillator wait control register	MOSCWTCR	8	8		3 ICLK
0008 00A3h	SYSTEM	Sub-clock oscillator wait control register	SOSCWTCR	8	8		3 ICLK
0008 00A6h	SYSTEM	PLL wait control register	PLLWTCR	8	8		3 ICLK
0008 00A9h	SYSTEM	HOCO wait control register 2	HOCOWTCR2	8	8		3 ICLK
0008 00C0h	SYSTEM	Reset status register 2	RSTSR2	8	8		3 ICLK
0008 00C2h	SYSTEM	Software reset register	SWRR	16	16		3 ICLK
0008 00E0h	SYSTEM	Voltage monitoring 1 circuit/comparator A1 control register 1	LVD1CR1	8	8		3 ICLK
0008 00E1h	SYSTEM	Voltage monitoring 1 circuit/comparator A1 status register	LVD1SR	8	8		3 ICLK
0008 00E2h	SYSTEM	Voltage monitoring 2 circuit/comparator A2 control register 1	LVD2CR1	8	8		3 ICLK
0008 00E3h	SYSTEM	Voltage monitoring 2 circuit/comparator A2 status register	LVD2SR	8	8		3 ICLK
0008 0200h	SYSTEM	Voltage regulator control register	VRCR	8	8		3 ICLK
0008 03FEh	SYSTEM	Protect register	PRCR	16	16		3 ICLK
0008 1300h	BSC	Bus error status clear register	BERCLR	8	8		2 ICLK
0008 1304h	BSC	Bus error monitoring enable register	BEREN	8	8		2 ICLK
0008 1308h	BSC	Bus error status register 1	BERSR1	8	8		2 ICLK
0008 130Ah	BSC	Bus error status register 2	BERSR2	16	16		2 ICLK
0008 1310h	BSC	Bus priority control register	BUSPRI	16	16		2 ICLK
0008 2000h	DMAC0	DMA source address register	DMSAR	32	32		2 ICLK
0008 2004h	DMAC0	DMA destination address register	DMDAR	32	32		2 ICLK
0008 2008h	DMAC0	DMA transfer count register	DMCRA	32	32		2 ICLK
0008 200Ch	DMAC0	DMA block transfer count register	DMCRB	16	16		2 ICLK
0008 2010h	DMAC0	DMA transfer mode register	DMTMD	16	16		2 ICLK
0008 2013h	DMAC0	DMA interrupt setting register	DMINT	8	8		2 ICLK
0008 2014h	DMAC0	DMA address mode register	DMAMD	16	16		2 ICLK
0008 2018h	DMAC0	DMA offset register	DMOFR	32	32		2 ICLK
0008 201Ch	DMAC0	DMA transfer enable register	DMCNT	8	8		2 ICLK

Table 4.1 List of I/O Registers (Address Order) (5 / 29)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles ICLK ≥ PCLK	Number of Access Cycles ICLK < PCLK
0008 70ABh	ICU	Interrupt request register 171	IR171	8	8		2 ICLK
0008 70AEh	ICU	Interrupt request register 174	IR174	8	8		2 ICLK
0008 70AFh	ICU	Interrupt request register 175	IR175	8	8		2 ICLK
0008 70B0h	ICU	Interrupt request register 176	IR176	8	8		2 ICLK
0008 70B1h	ICU	Interrupt request register 177	IR177	8	8		2 ICLK
0008 70B2h	ICU	Interrupt request register 178	IR178	8	8		2 ICLK
0008 70B3h	ICU	Interrupt request register 179	IR179	8	8		2 ICLK
0008 70B4h	ICU	Interrupt request register 180	IR180	8	8		2 ICLK
0008 70B5h	ICU	Interrupt request register 181	IR181	8	8		2 ICLK
0008 70B6h	ICU	Interrupt request register 182	IR182	8	8		2 ICLK
0008 70B7h	ICU	Interrupt request register 183	IR183	8	8		2 ICLK
0008 70B8h	ICU	Interrupt request register 184	IR184	8	8		2 ICLK
0008 70B9h	ICU	Interrupt request register 185	IR185	8	8		2 ICLK
0008 70BAh	ICU	Interrupt request register 186	IR186	8	8		2 ICLK
0008 70BBh	ICU	Interrupt request register 187	IR187	8	8		2 ICLK
0008 70BCh	ICU	Interrupt request register 188	IR188	8	8		2 ICLK
0008 70BDh	ICU	Interrupt request register 189	IR189	8	8		2 ICLK
0008 70BEh	ICU	Interrupt request register 190	IR190	8	8		2 ICLK
0008 70BFh	ICU	Interrupt request register 191	IR191	8	8		2 ICLK
0008 70C0h	ICU	Interrupt request register 192	IR192	8	8		2 ICLK
0008 70C1h	ICU	Interrupt request register 193	IR193	8	8		2 ICLK
0008 70C2h	ICU	Interrupt request register 194	IR194	8	8		2 ICLK
0008 70C3h	ICU	Interrupt request register 195	IR195	8	8		2 ICLK
0008 70C4h	ICU	Interrupt request register 196	IR196	8	8		2 ICLK
0008 70C5h	ICU	Interrupt request register 197	IR197	8	8		2 ICLK
0008 70C6h	ICU	Interrupt request register 198	IR198	8	8		2 ICLK
0008 70C7h	ICU	Interrupt request register 199	IR199	8	8		2 ICLK
0008 70C8h	ICU	Interrupt request register 200	IR200	8	8		2 ICLK
0008 70C9h	ICU	Interrupt request register 201	IR201	8	8		2 ICLK
0008 70CEh	ICU	Interrupt request register 206	IR206	8	8		2 ICLK
0008 70CFh	ICU	Interrupt request register 207	IR207	8	8		2 ICLK
0008 70D0h	ICU	Interrupt request register 208	IR208	8	8		2 ICLK
0008 70D1h	ICU	Interrupt request register 209	IR209	8	8		2 ICLK
0008 70D2h	ICU	Interrupt request register 210	IR210	8	8		2 ICLK
0008 70D3h	ICU	Interrupt request register 211	IR211	8	8		2 ICLK
0008 70D4h	ICU	Interrupt request register 212	IR212	8	8		2 ICLK
0008 70D5h	ICU	Interrupt request register 213	IR213	8	8		2 ICLK
0008 70D6h	ICU	Interrupt request register 214	IR214	8	8		2 ICLK
0008 70D7h	ICU	Interrupt request register 215	IR215	8	8		2 ICLK
0008 70D8h	ICU	Interrupt request register 216	IR216	8	8		2 ICLK
0008 70D9h	ICU	Interrupt request register 217	IR217	8	8		2 ICLK
0008 70DAh	ICU	Interrupt request register 218	IR218	8	8		2 ICLK
0008 70DBh	ICU	Interrupt request register 219	IR219	8	8		2 ICLK
0008 70DCh	ICU	Interrupt request register 220	IR220	8	8		2 ICLK
0008 70DDh	ICU	Interrupt request register 221	IR221	8	8		2 ICLK
0008 70DEh	ICU	Interrupt request register 222	IR222	8	8		2 ICLK
0008 70DFh	ICU	Interrupt request register 223	IR223	8	8		2 ICLK
0008 70E0h	ICU	Interrupt request register 224	IR224	8	8		2 ICLK
0008 70E1h	ICU	Interrupt request register 225	IR225	8	8		2 ICLK
0008 70E2h	ICU	Interrupt request register 226	IR226	8	8		2 ICLK
0008 70E3h	ICU	Interrupt request register 227	IR227	8	8		2 ICLK

Table 4.1 List of I/O Registers (Address Order) (18 / 29)

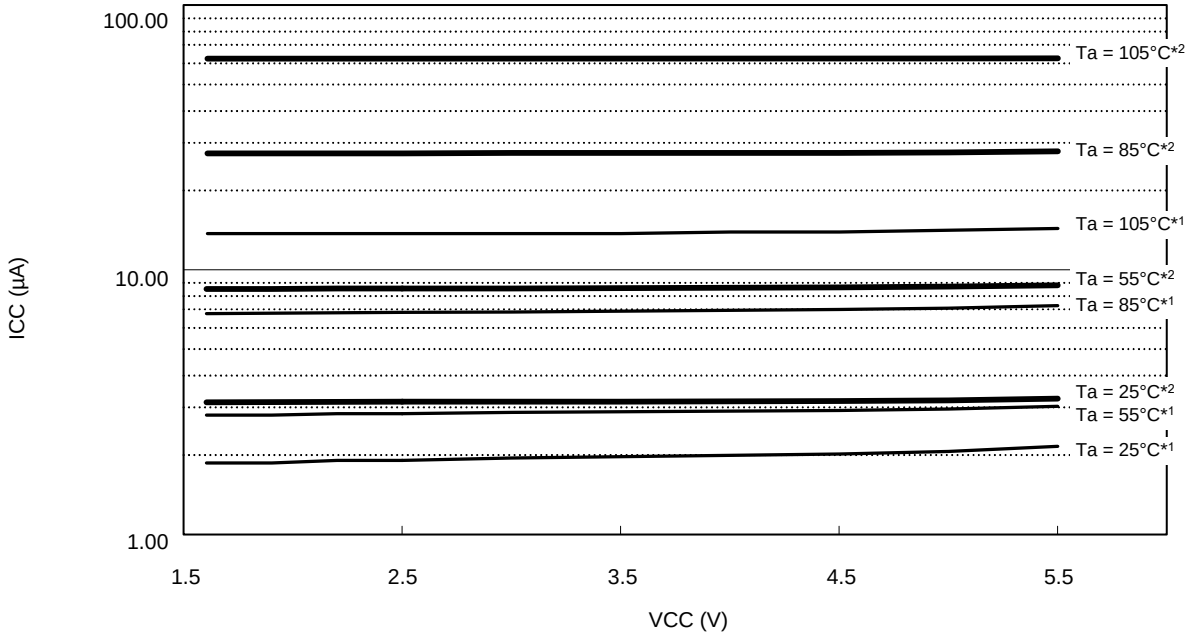
Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles: ICLK ≥ PCLK	Number of Access Cycles: ICLK < PCLK
0008 A064h	SCI3	Serial status register	SSR	8	8	2, 3 PCLKB	2 ICLK
0008 A065h	SCI3	Receive data register	RDR	8	8	2, 3 PCLKB	2 ICLK
0008 A066h	SCI3	Smart card mode register	SCMR	8	8	2, 3 PCLKB	2 ICLK
0008 A067h	SCI3	Serial extended mode register	SEMR	8	8	2, 3 PCLKB	2 ICLK
0008 A068h	SCI3	Noise filter setting register	SNFR	8	8	2, 3 PCLKB	2 ICLK
0008 A069h	SCI3	I^2C mode register 1	SIMR1	8	8	2, 3 PCLKB	2 ICLK
0008 A06Ah	SCI3	I^2C mode register 2	SIMR2	8	8	2, 3 PCLKB	2 ICLK
0008 A06Bh	SCI3	I^2C mode register 3	SIMR3	8	8	2, 3 PCLKB	2 ICLK
0008 A06Ch	SCI3	I^2C status register	SISR	8	8	2, 3 PCLKB	2 ICLK
0008 A06Dh	SCI3	SPI mode register	SPMR	8	8	2, 3 PCLKB	2 ICLK
0008 A080h	SCI4	Serial mode register	SMR	8	8	2, 3 PCLKB	2 ICLK
0008 A081h	SCI4	Bit rate register	BRR	8	8	2, 3 PCLKB	2 ICLK
0008 A082h	SCI4	Serial control register	SCR	8	8	2, 3 PCLKB	2 ICLK
0008 A083h	SCI4	Transmit data register	TDR	8	8	2, 3 PCLKB	2 ICLK
0008 A084h	SCI4	Serial status register	SSR	8	8	2, 3 PCLKB	2 ICLK
0008 A085h	SCI4	Receive data register	RDR	8	8	2, 3 PCLKB	2 ICLK
0008 A086h	SCI4	Smart card mode register	SCMR	8	8	2, 3 PCLKB	2 ICLK
0008 A087h	SCI4	Serial extended mode register	SEMR	8	8	2, 3 PCLKB	2 ICLK
0008 A088h	SCI4	Noise filter setting register	SNFR	8	8	2, 3 PCLKB	2 ICLK
0008 A089h	SCI4	I^2C mode register 1	SIMR1	8	8	2, 3 PCLKB	2 ICLK
0008 A08Ah	SCI4	I^2C mode register 2	SIMR2	8	8	2, 3 PCLKB	2 ICLK
0008 A08Bh	SCI4	I^2C mode register 3	SIMR3	8	8	2, 3 PCLKB	2 ICLK
0008 A08Ch	SCI4	I^2C status register	SISR	8	8	2, 3 PCLKB	2 ICLK
0008 A08Dh	SCI4	SPI mode register	SPMR	8	8	2, 3 PCLKB	2 ICLK
0008 A0A0h	SCI5	Serial mode register	SMR	8	8	2, 3 PCLKB	2 ICLK
0008 A0A1h	SCI5	Bit rate register	BRR	8	8	2, 3 PCLKB	2 ICLK
0008 A0A2h	SCI5	Serial control register	SCR	8	8	2, 3 PCLKB	2 ICLK
0008 A0A3h	SCI5	Transmit data register	TDR	8	8	2, 3 PCLKB	2 ICLK
0008 A0A4h	SCI5	Serial status register	SSR	8	8	2, 3 PCLKB	2 ICLK
0008 A0A5h	SCI5	Receive data register	RDR	8	8	2, 3 PCLKB	2 ICLK
0008 A0A6h	SCI5	Smart card mode register	SCMR	8	8	2, 3 PCLKB	2 ICLK
0008 A0A7h	SCI5	Serial extended mode register	SEMR	8	8	2, 3 PCLKB	2 ICLK
0008 A0A8h	SCI5	Noise filter setting register	SNFR	8	8	2, 3 PCLKB	2 ICLK
0008 A0A9h	SCI5	I^2C mode register 1	SIMR1	8	8	2, 3 PCLKB	2 ICLK
0008 A0AAh	SCI5	I^2C mode register 2	SIMR2	8	8	2, 3 PCLKB	2 ICLK
0008 A0ABh	SCI5	I^2C mode register 3	SIMR3	8	8	2, 3 PCLKB	2 ICLK
0008 A0ACh	SCI5	I^2C status register	SISR	8	8	2, 3 PCLKB	2 ICLK
0008 A0ADh	SCI5	SPI mode register	SPMR	8	8	2, 3 PCLKB	2 ICLK
0008 A0C0h	SCI6	Serial mode register	SMR	8	8	2, 3 PCLKB	2 ICLK
0008 A0C1h	SCI6	Bit rate register	BRR	8	8	2, 3 PCLKB	2 ICLK
0008 A0C2h	SCI6	Serial control register	SCR	8	8	2, 3 PCLKB	2 ICLK
0008 A0C3h	SCI6	Transmit data register	TDR	8	8	2, 3 PCLKB	2 ICLK
0008 A0C4h	SCI6	Serial status register	SSR	8	8	2, 3 PCLKB	2 ICLK
0008 A0C5h	SCI6	Receive data register	RDR	8	8	2, 3 PCLKB	2 ICLK
0008 A0C6h	SCI6	Smart card mode register	SCMR	8	8	2, 3 PCLKB	2 ICLK
0008 A0C7h	SCI6	Serial extended mode register	SEMR	8	8	2, 3 PCLKB	2 ICLK
0008 A0C8h	SCI6	Noise filter setting register	SNFR	8	8	2, 3 PCLKB	2 ICLK
0008 A0C9h	SCI6	I^2C mode register 1	SIMR1	8	8	2, 3 PCLKB	2 ICLK
0008 A0CAh	SCI6	I^2C mode register 2	SIMR2	8	8	2, 3 PCLKB	2 ICLK
0008 A0CBh	SCI6	I^2C mode register 3	SIMR3	8	8	2, 3 PCLKB	2 ICLK
0008 A0CCh	SCI6	I^2C status register	SISR	8	8	2, 3 PCLKB	2 ICLK

Table 4.1 List of I/O Registers (Address Order) (24 / 29)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles: ICLK ≥ PCLK	Number of Access Cycles: ICLK < PCLK
0008 C04Ch	PORTC	Port input data register	PIDR	8	8	3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing	3 ICLK cycles when reading, 2 ICLK cycles when writing
0008 C04Dh	PORTD	Port input data register	PIDR	8	8	3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing	3 ICLK cycles when reading, 2 ICLK cycles when writing
0008 C04Eh	PORTE	Port input data register	PIDR	8	8	3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing	3 ICLK cycles when reading, 2 ICLK cycles when writing
0008 C04Fh	PORTF	Port input data register	PIDR	8	8	3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing	3 ICLK cycles when reading, 2 ICLK cycles when writing
0008 C051h	PORTH	Port input data register	PIDR	8	8	3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing	3 ICLK cycles when reading, 2 ICLK cycles when writing
0008 C052h	PORTJ	Port input data register	PIDR	8	8	3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing	3 ICLK cycles when reading, 2 ICLK cycles when writing
0008 C053h	PORTK	Port input data register	PIDR	8	8	2, 3 PCLKB	2 ICLK
0008 C054h	PORTL	Port input data register	PIDR	8	8	2, 3 PCLKB	2 ICLK
0008 C060h	PORT0	Port mode register	PMR	8	8	2, 3 PCLKB	2 ICLK
0008 C061h	PORT1	Port mode register	PMR	8	8	2, 3 PCLKB	2 ICLK
0008 C062h	PORT2	Port mode register	PMR	8	8	2, 3 PCLKB	2 ICLK
0008 C063h	PORT3	Port mode register	PMR	8	8	2, 3 PCLKB	2 ICLK
0008 C064h	PORT4	Port mode register	PMR	8	8	2, 3 PCLKB	2 ICLK
0008 C065h	PORT5	Port mode register	PMR	8	8	2, 3 PCLKB	2 ICLK
0008 C066h	PORT6	Port mode register	PMR	8	8	2, 3 PCLKB	2 ICLK
0008 C067h	PORT7	Port mode register	PMR	8	8	2, 3 PCLKB	2 ICLK
0008 C068h	PORT8	Port mode register	PMR	8	8	2, 3 PCLKB	2 ICLK
0008 C069h	PORT9	Port mode register	PMR	8	8	2, 3 PCLKB	2 ICLK
0008 C06Ah	PORTA	Port mode register	PMR	8	8	2, 3 PCLKB	2 ICLK
0008 C06Bh	PORTB	Port mode register	PMR	8	8	2, 3 PCLKB	2 ICLK
0008 C06Ch	PORTC	Port mode register	PMR	8	8	2, 3 PCLKB	2 ICLK
0008 C06Dh	PORTD	Port mode register	PMR	8	8	2, 3 PCLKB	2 ICLK
0008 C06Eh	PORTE	Port mode register	PMR	8	8	2, 3 PCLKB	2 ICLK
0008 C06Fh	PORTF	Port mode register	PMR	8	8	2, 3 PCLKB	2 ICLK
0008 C071h	PORTH	Port mode register	PMR	8	8	2, 3 PCLKB	2 ICLK
0008 C072h	PORTJ	Port mode register	PMR	8	8	2, 3 PCLKB	2 ICLK
0008 C073h	PORTK	Port mode register	PMR	8	8	2, 3 PCLKB	2 ICLK
0008 C074h	PORTL	Port mode register	PMR	8	8	2, 3 PCLKB	2 ICLK

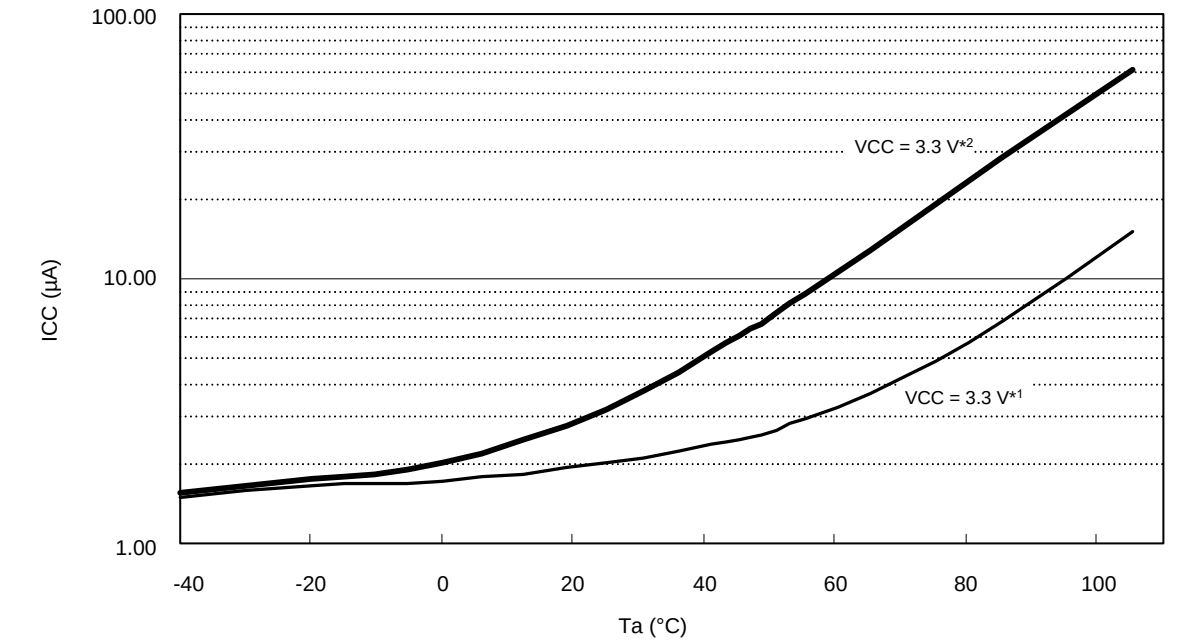
Table 4.1 List of I/O Registers (Address Order) (27 / 29)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles: ICLK ≥ PCLK	Number of Access Cycles: ICLK < PCLK
0008 C16Dh	MPC	P55 pin function control register	P55PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C16Eh	MPC	P56 pin function control register	P56PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C170h	MPC	P60 pin function control register	P60PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C171h	MPC	P61 pin function control register	P61PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C178h	MPC	P70 pin function control register	P70PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C17Ch	MPC	P74 pin function control register	P74PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C17Dh	MPC	P75 pin function control register	P75PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C17Eh	MPC	P76 pin function control register	P76PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C17Fh	MPC	P77 pin function control register	P77PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C180h	MPC	P80 pin function control register	P80PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C181h	MPC	P81 pin function control register	P81PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C182h	MPC	P82 pin function control register	P82PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C183h	MPC	P83 pin function control register	P83PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C186h	MPC	P86 pin function control register	P865PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C187h	MPC	P87 pin function control register	P87PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C188h	MPC	P90 pin function control register	P90PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C189h	MPC	P91 pin function control register	P91PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C18Ah	MPC	P92 pin function control register	P92PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C18Bh	MPC	P93 pin function control register	P93PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C190h	MPC	PA0 pin function control register	PA0PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C191h	MPC	PA1 pin function control register	PA1PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C192h	MPC	PA2 pin function control register	PA2PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C193h	MPC	PA3 pin function control register	PA3PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C194h	MPC	PA4 pin function control register	PA4PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C195h	MPC	PA5 pin function control register	PA5PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C196h	MPC	PA6 pin function control register	PA6PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C197h	MPC	PA7 pin function control register	PA7PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C198h	MPC	PB0 pin function control register	PB0PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C199h	MPC	PB1 pin function control register	PB1PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C19Ah	MPC	PB2 pin function control register	PB2PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C19Bh	MPC	PB3 pin function control register	PB3PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C19Ch	MPC	PB4 pin function control register	PB4PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C19Dh	MPC	PB5 pin function control register	PB5PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C19Eh	MPC	PB6 pin function control register	PB6PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C19Fh	MPC	PB7 pin function control register	PB7PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C1A0h	MPC	PC0 pin function control register	PC0PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C1A1h	MPC	PC1 pin function control register	PC1PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C1A2h	MPC	PC2 pin function control register	PC2PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C1A3h	MPC	PC3 pin function control register	PC3PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C1A4h	MPC	PC4 pin function control register	PC4PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C1A5h	MPC	PC5 pin function control register	PC5PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C1A6h	MPC	PC6 pin function control register	PC6PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C1A7h	MPC	PC7 pin function control register	PC7PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C1A8h	MPC	PD0 pin function control register	PD0PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C1A9h	MPC	PD1 pin function control register	PD1PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C1AAh	MPC	PD2 pin function control register	PD2PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C1ABh	MPC	PD3 pin function control register	PD3PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C1ACh	MPC	PD4 pin function control register	PD4PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C1ADh	MPC	PD5 pin function control register	PD5PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C1AEh	MPC	PD6 pin function control register	PD6PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C1AFh	MPC	PD7 pin function control register	PD7PFS	8	8	2, 3 PCLKB	2 ICLK



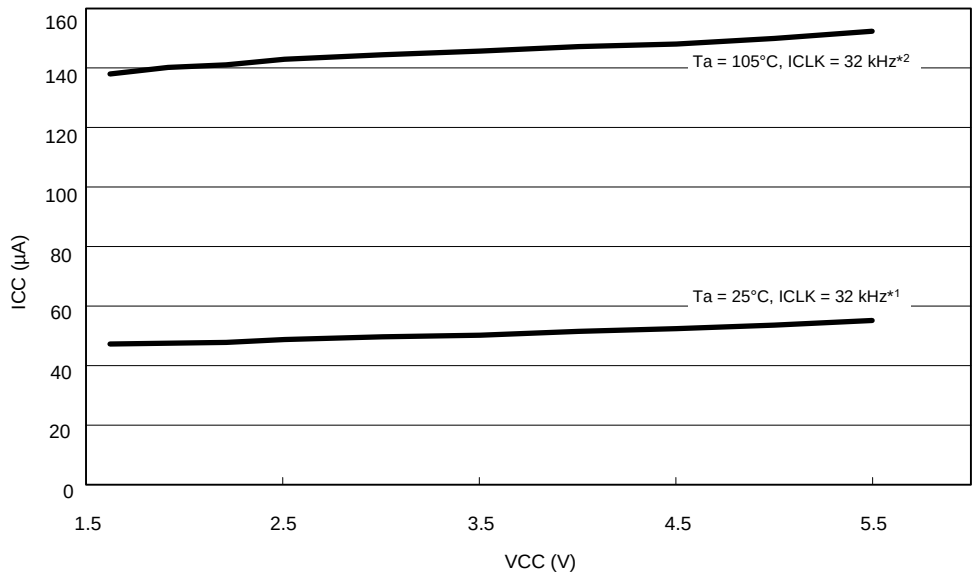
Note 1. Average value of the tested middle samples during product evaluation.
Note 2. Average value of the tested upper-limit samples during product evaluation.

Figure 5.5 Voltage Dependency in Software Standby Mode (SOFTCUT[2:0] Bits = 111b) (Reference Data) for Chip Version A



Note 1. Average value of the tested middle samples during product evaluation.
Note 2. Average value of the tested upper-limit samples during product evaluation.

Figure 5.6 Temperature Dependency in Software Standby Mode (SOFTCUT[2:0] Bits = 111b) (Reference Data) for Chip Version A



Note 1. All peripheral operation is normal.
Average value of the tested middle samples during product evaluation.
Note 2. All peripheral operation is maximum.
Average value of the tested upper-limit samples during product evaluation.

Figure 5.21 Voltage Dependency in Low-Speed Operating Mode 2 (Reference Data) for Chip Version B with 256 Kbytes or Less of Flash Memory and 48 to 100 Pins

5.2.2 Standard I/O Pin Output Characteristics (2)

Figure 5.50 to Figure 5.54 show the characteristics when high-drive output is selected by the drive capacity control register.

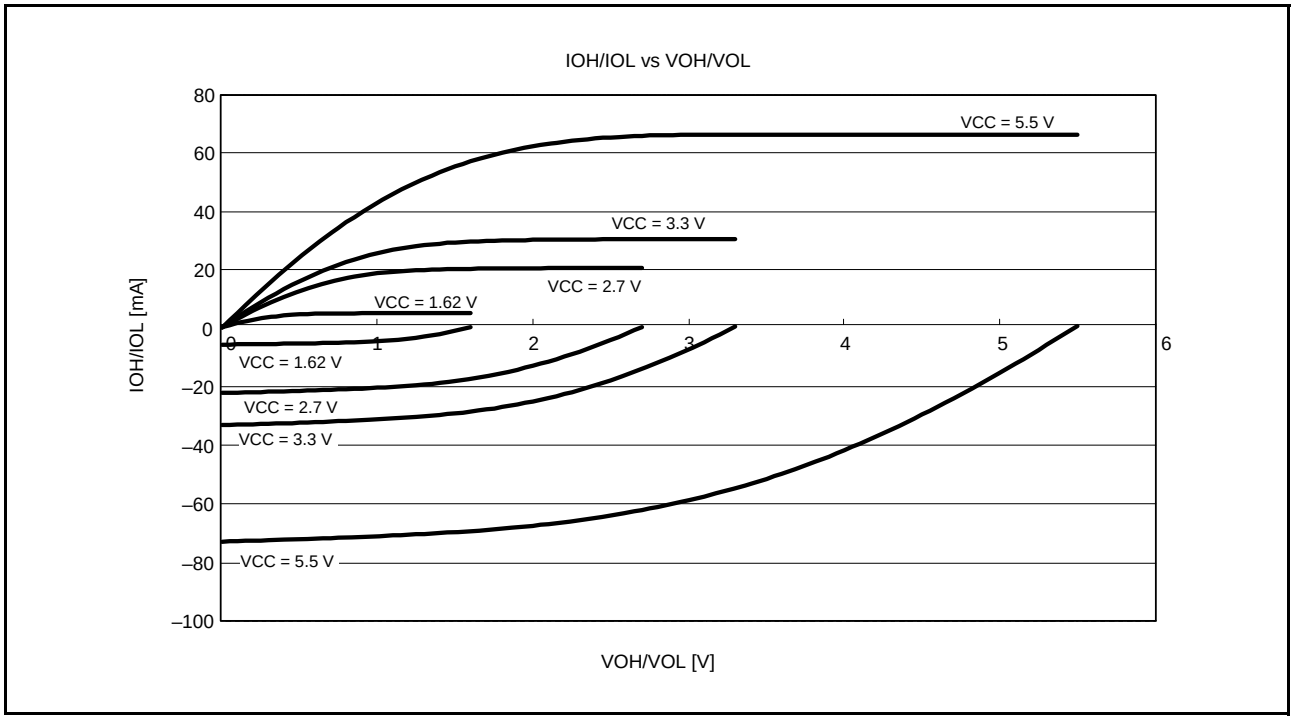


Figure 5.50 VOH/VOL and IOH/IOL Voltage Characteristics at Ta = 25°C when High-Drive Output is Selected (Reference Data)

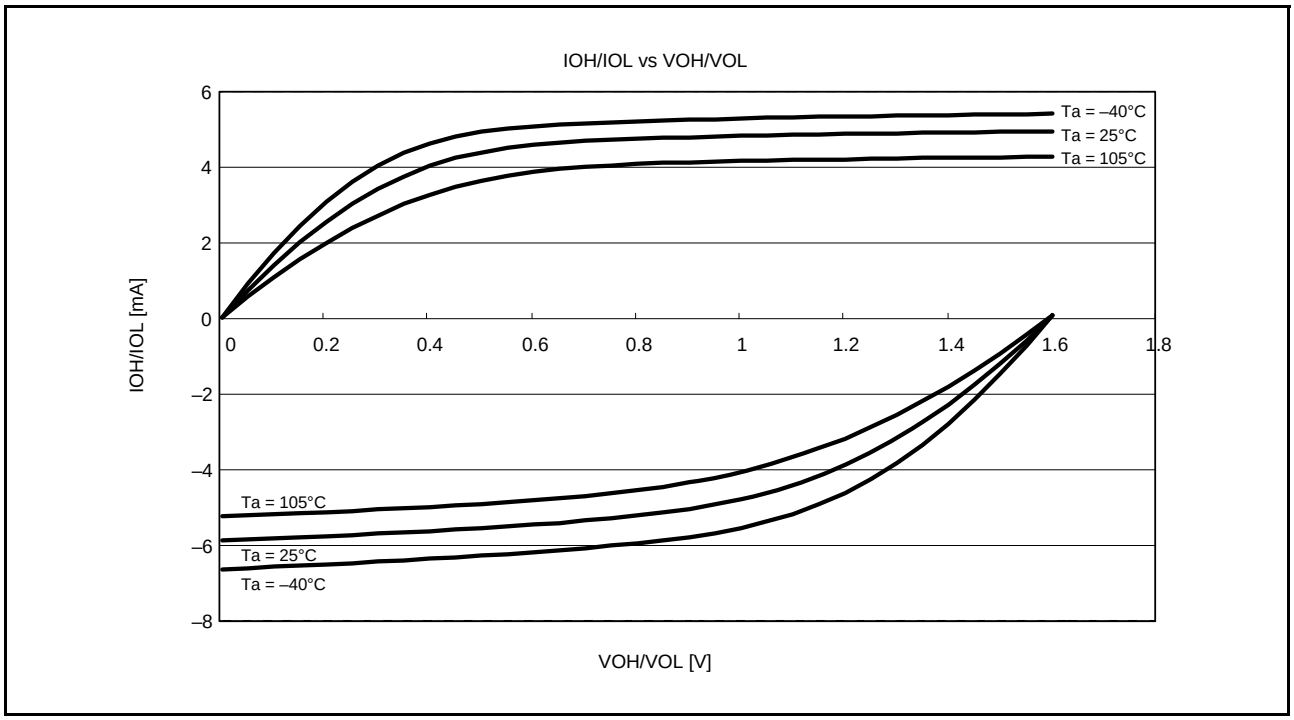


Figure 5.51 VOH/VOL and IOH/IOL Temperature Characteristics at VCC = 1.62 V when High-Drive Output is Selected (Reference Data)

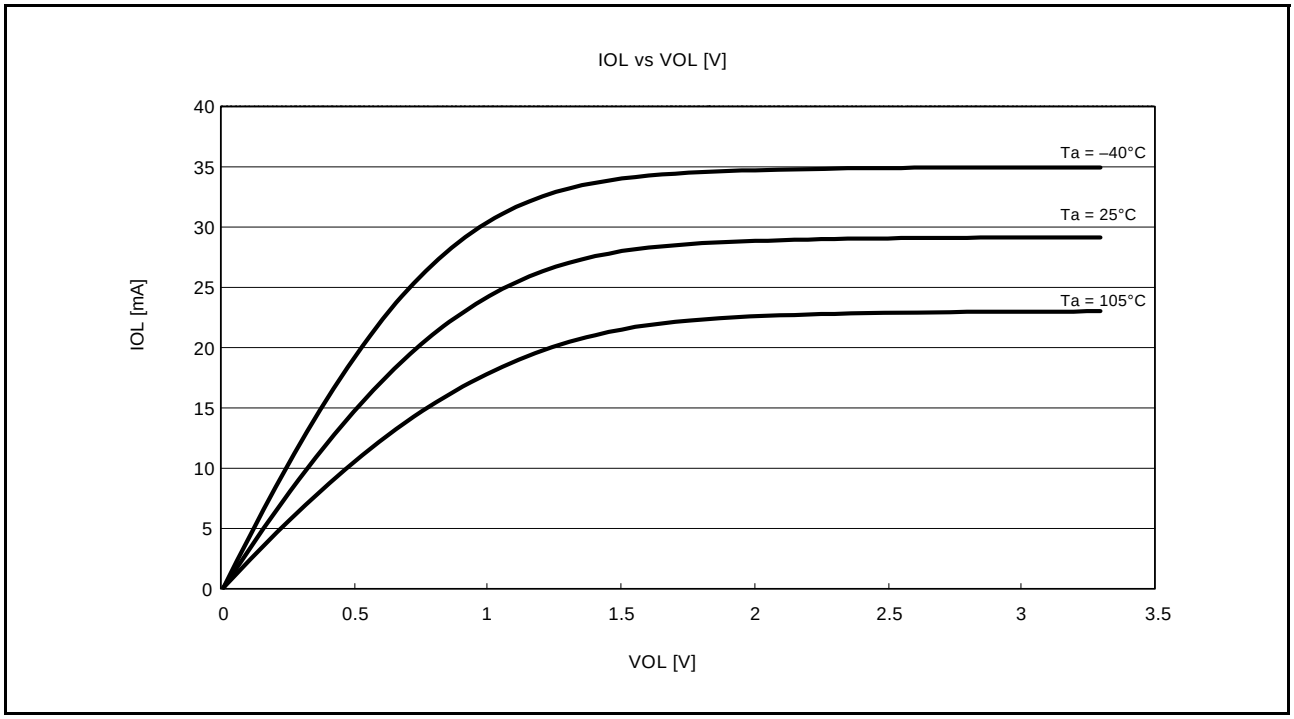


Figure 5.57 VOL and IOL Temperature Characteristics of RIIC Output Pin at VCC = 3.3 V (Reference Data)

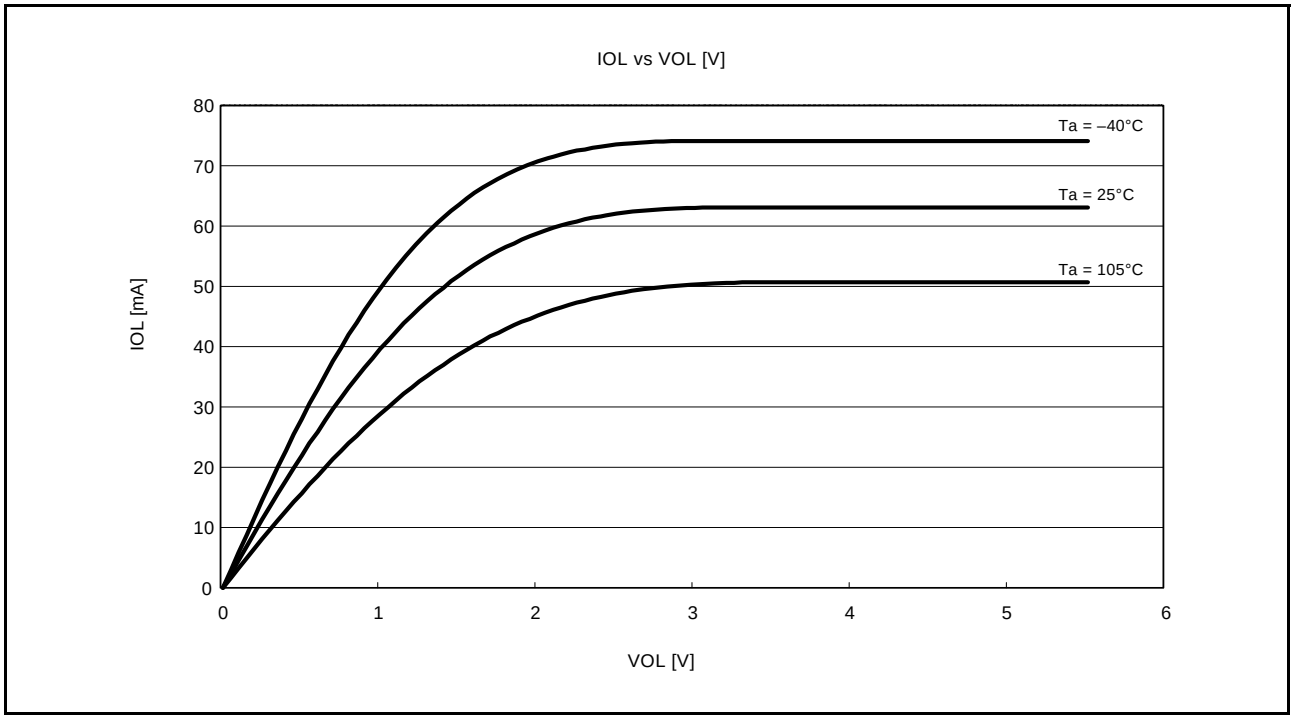


Figure 5.58 VOL and IOL Temperature Characteristics of RIIC Output Pin at VCC = 5.5 V (Reference Data)

[Chip version B]

Table 5.39 Operation Frequency Value (Low-Speed Operating Mode 1)

Conditions: VCC = AVCC0 = 1.62 to 5.5 V, VSS = AVSS0 = VREFL = VREFL0 = 0 V, T_a = –40 to +105°C

Item		Symbol	VCC			Unit
			1.62 to 1.8 V	1.8 to 2.7 V	2.7 to 5.5 V	
Maximum operating frequency	System clock (ICLK)	f_{max}	2	4	8	MHz
	FlashIF clock (FCLK)*1		2	4	8	
	Peripheral module clock (PCLKB)		2	4	8	
	Peripheral module clock (PCLKD)*2		2	4	8	
	External bus clock (BCLK)		2	4	8	
	BCLK pin output		2	4	8	

Note 1. Programming and erasing the flash memory is impossible.
Note 2. The lower-limit frequency of PCLKD is 1 MHz when the A/D converter is in use.

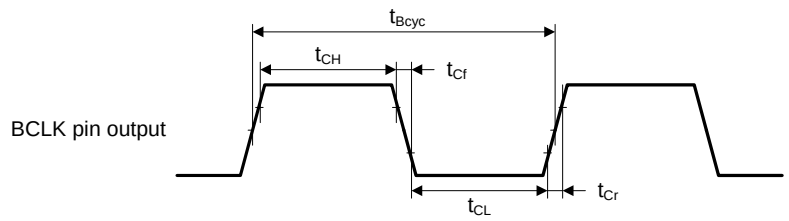
[Chip versions A, B, and C]

Table 5.40 Operation Frequency Value (Low-Speed Operating Mode 2)

Conditions: VCC = AVCC0 = 1.62 to 5.5 V, VSS = AVSS0 = VREFL=VREFL0 = 0 V, T_a = –40 to +105°C

Item		Symbol	VCC			Unit
			1.62 to 1.8 V	1.8 to 2.7 V	2.7 to 5.5 V	
Maximum operating frequency	System clock (ICLK)	f_{max}	32.768	32.768	32.768	kHz
	FlashIF clock (FCLK)*1		32.768	32.768	32.768	
	Peripheral module clock (PCLKB)		32.768	32.768	32.768	
	Peripheral module clock (PCLKD)*2		32.768	32.768	32.768	
	External bus clock (BCLK)		32.768	32.768	32.768	
	BCLK pin output		32.768	32.768	32.768	

Note 1. Programming and erasing the flash memory is impossible.
Note 2. The A/D converter cannot be used.



Test conditions: VOH = VCC × 0.7, VOL = VCC × 0.3, IOH = –1.0 mA, IOL = 1.0 mA, C = 30 pF

Figure 5.59 BCLK Pin Output Timing

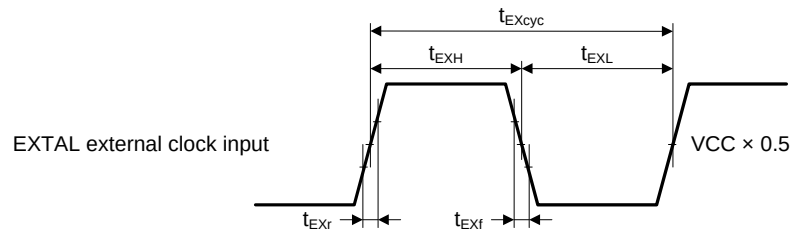


Figure 5.60 EXTAL External Clock Input Timing

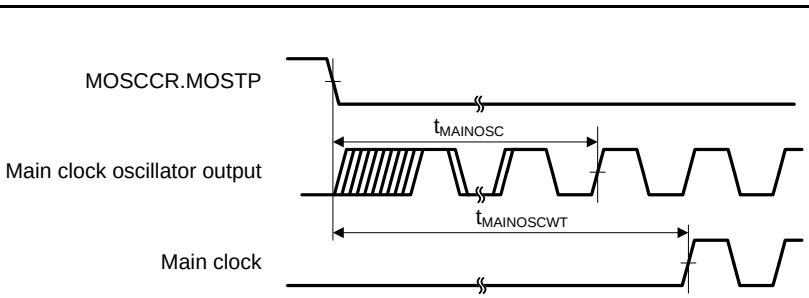


Figure 5.61 Main Clock Oscillation Start Timing

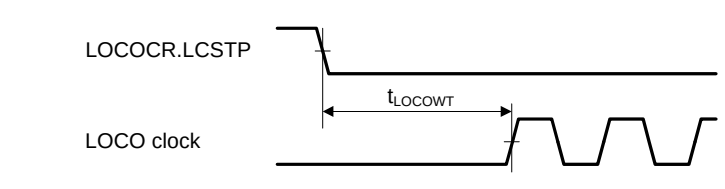


Figure 5.62 LOCO Clock Oscillation Start Timing

5.3.2 Reset Timing

Table 5.45 Reset Timing

Conditions: VCC = AVCC0 = 1.62 to 5.5 V, VSS = AVSS0 = VREFL = VREFL0 = 0 V, T_a = –40 to +105°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
RES# pulse width	Power-on	t_{RESWP}	8	—	—	ms	Figure 5.70
	Deep software standby mode	t_{RESWD}	8	—	—	ms	Figure 5.71
	Software standby mode, low-speed operating modes 1 and 2	t_{RESWS}	1	—	—	ms	
	Programming or erasure of the ROM or E2 DataFlash memory or blank checking of the E2 DataFlash memory	t_{RESWF}	200	—	—	µs	
	Other than above	t_{RESW}	200	—	—	µs	
Wait time after RES# cancellation		t_{RESWT}	—	—	912	µs	Figure 5.70
Internal reset time (independent watchdog timer reset, watchdog timer reset, software reset)		t_{RESW2}	—	—	1.4	ms	

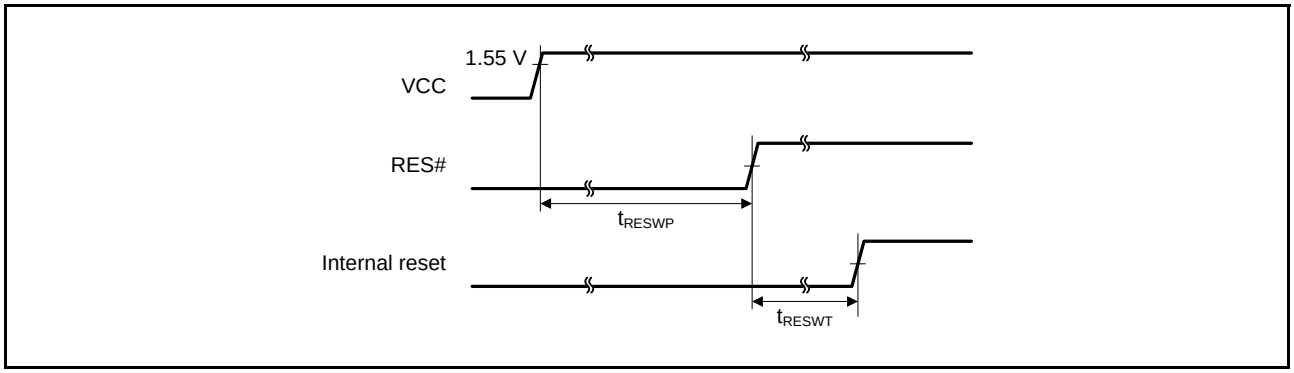


Figure 5.70 Reset Input Timing at Power-On

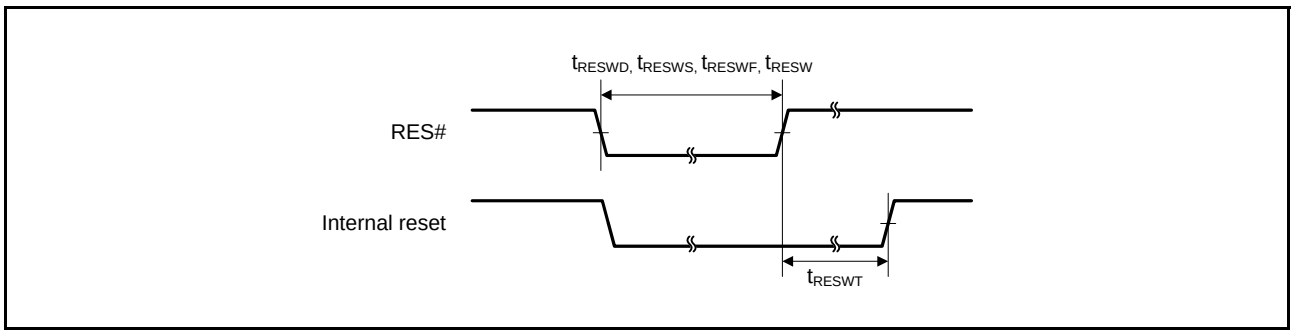


Figure 5.71 Reset Input Timing

Table 5.54 Bus Timing (Multiplexed Bus) (3)

Conditions: VCC = AVCC0 = 1.62 to 1.8 V, VSS = AVSS0 = VREFL = VREFL0 = 0 V,
fBCLK ≤ 12 MHz (BCLK pin output frequency ≤ 6 MHz), T_a = –40 to +105°C, V_{OH} = VCC × 0.5,
V_{OL} = VCC × 0.5, I_{OH} = –0.5 mA, I_{OL} = 0.5 mA, C_L = 30 pF
When normal output is selected by the drive capacity register

Item	Symbol	Min.	Typ.	Max.	Unit
Address delay time	t_{AD}	—	125	ns	Figure 5.81 and Figure 5.82
Byte control delay time	t_{BCD}	—	125	ns	
CS# delay time	t_{CSD}	—	125	ns	
RD# delay time	t_{RSD}	—	125	ns	
ALE delay time	t_{ALED}	—	125	ns	
Read data setup time	t_{RDS}	85	—	ns	
Read data hold time	t_{RDH}	0	—	ns	
WR# delay time	t_{WRD}	—	125	ns	
Write data delay time	t_{WDD}	—	125	ns	
Write data hold time	t_{WDH}	0	—	ns	
WAIT# setup time	t_{WTS}	85	—	ns	Figure 5.80
WAIT# hold time	t_{WTH}	0	—	ns	

[Chip versions A and C]

Table 5.76 ROM (Flash Memory for Code Storage) Characteristics (3) : high-speed operating mode, middle-speed operating mode 1A

Conditions: VCC = AVCC0 = 2.7 to 5.5 V, VREFH = VREFH0 = AVCC0, VSS = AVSS0 = VREFL = VREFL0 = 0 V
Temperature range for the programming/erasure operation: T_a = –40 to +105°C

Item		Symbol	FCLK = 4 MHz			FCLK = 32 MHz			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Programming time when N_{PEC} ≤ 100 times	2 bytes	t_{P2}	—	0.52	4.8	—	0.19	2.5	ms
	8 bytes	t_{P8}	—	0.52	4.9	—	0.19	2.5	
	128 bytes	t_{P128}	—	1.50	10.7	—	0.57	4.8	
Programming time when N_{PEC} > 100 times	2 bytes	t_{P2}	—	0.61	5.7	—	0.23	3.0	ms
	8 bytes	t_{P8}	—	0.61	6.2	—	0.23	3.2	
	128 bytes	t_{P128}	—	1.71	13.2	—	0.65	6.0	
Erasure time when N_{PEC} ≤ 100 times	2 Kbytes	t_{E2K}	—	17.0	92.9	—	11.0	29	ms
Erasure time when N_{PEC} > 100 times	2 Kbytes	t_{E2K}	—	20.8	195.8	—	13.5	60	ms
Suspend delay time during programming (in programming/erasure priority mode)		t_{SPD}	—	—	0.9	—	—	0.8	ms
First suspend delay time during programming (in suspend priority mode)		t_{SPSD1}	—	—	220	—	—	120	µs
Second suspend delay time during programming (in suspend priority mode)		t_{SPSD2}	—	—	0.9	—	—	0.8	ms
Suspend delay time during erasing (in programming/erasure priority mode)		t_{SED}	—	—	0.9	—	—	0.8	ms
First suspend delay time during erasing (in suspend priority mode)		t_{SESD1}	—	—	220	—	—	120	µs
Second suspend delay time during erasing (in suspend priority mode)		t_{SESD2}	—	—	0.9	—	—	0.8	ms
FCU reset time		t_{FCUR}	20 µs or longer and FCLK × 6 or greater	—	—	20 µs or longer and FCLK × 6 or greater	—	—	µs