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onsemi - LC88FC2H0BUTJ-2H Datasheet



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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

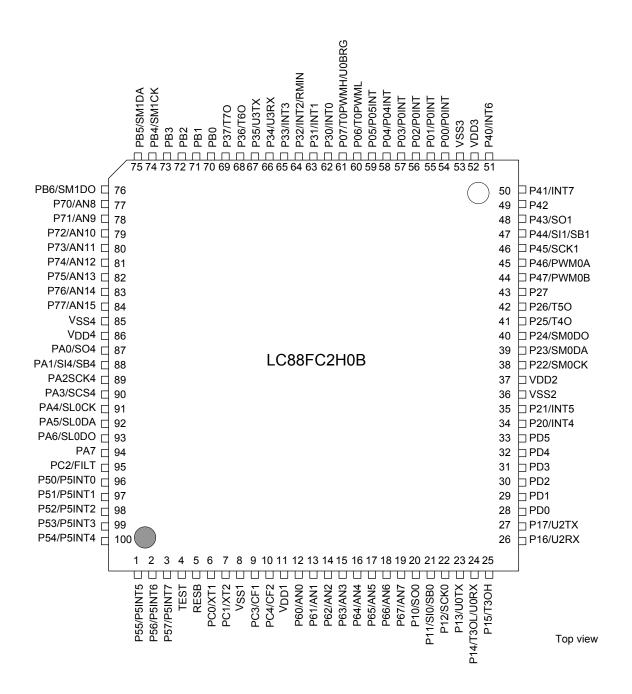
Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details	
Product Status	Not For New Designs
Core Processor	Xstormy16
Core Size	16-Bit
Speed	12MHz
Connectivity	I ² C, SIO, UART/USART
Peripherals	LVD, POR, PWM, WDT
Number of I/O	86
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	24K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 16x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/onsemi/lc88fc2h0butj-2h

Email: info@E-XFL.COM

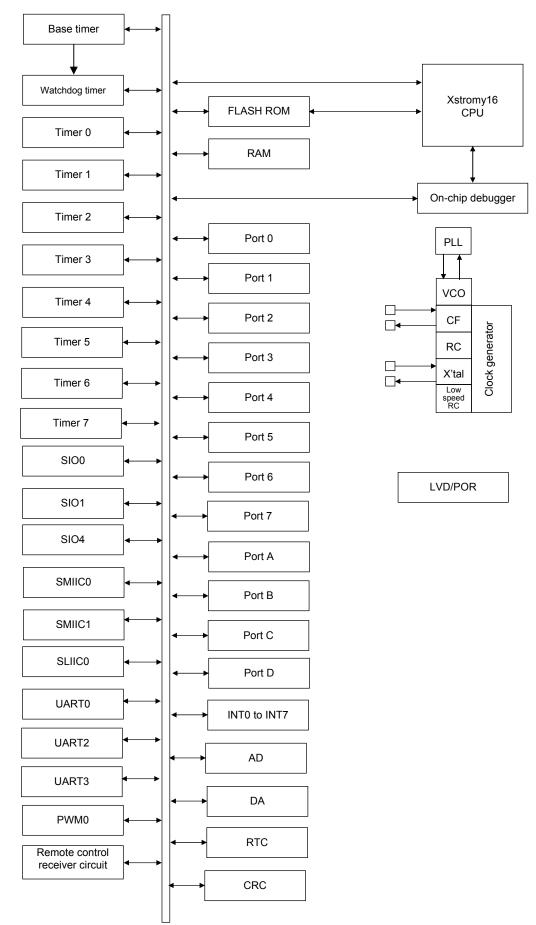
Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

Pin Assignment



TQFP100,14×14 (Pb-Free and Halogen Free type)

System Block Diagram



LC88FC2H0B

Pin Name	I/O	Description	
Port A	I/O	• 8-bit I/O port	
PA0 to PA7		• I/O specifiable in 1-bit units	
1110 10 1111		• Pull-up resistors can be turned on and off in 1 bit units	
		Multiplexed pin functions	
		PA0 : SIO4 data output	
		PA1 : SIO4 data input/pulse input/output	
		PA2 : SIO4 clock input/output	
		PA3 : SIO4 chip select input	
		PA4 : SLIIC0 clock input	
		PA5 : SLIIC0 bus input/output/data input	
		PA6 : SLIIC0 data output (used in 3-wire SIO mode)	
Port B	I/o	• 7-bit I/O port	
PB0 to PB6		• I/O specifiable in 1-bit units	
		• Pull-up resistors can be turned on and off in 1 bit units	
		• Multiplexed pin functions	
		PB4 : SMIIC1 clock input/output PB5 : SMIIC1 bus input/output/data input	
		PB6 : SMIIC1 data output (used in 3-wire SIO mode)	
Port C	I/O	Source 1 data output (used in 5-wire Sto mode) Source 1 data output (used in 5-wire Sto mode)	
	1/0	• I/O specifiable in 1-bit units	
PC0 to PC4		 Pull-up resistors can be turned on and off in 1 bit units(PC2) 	
		• Pin functions	
		PC0 : 32.768 kHz crystal oscillator input	
		PC1 : 32.768 kHz crystal oscillator output	
		PC2 : FILT of VCO	
		PC3 : Ceramic oscillator input	
		PC4 : Ceramic oscillator output/VCO output	
Port D	I/O	• 6-bit I/O port	
	1/0	• I/O specifiable in 1-bit units	
PD0 to PD5		• Pull-up resistors can be turned on and off in 1 bit units	
TEST	I/O	TEST pin	
	10	• Used to communicate with on-chip debugger.	
		• Connects an external 100 k Ω pull-down resistor.	
		Conneets un enternur 100 kas puir do wir resistor.	

	Demonster	Samah al	Applicable Pin	Conditions			Specifi	cation	
	Parameter	Symbol	/Remarks	Conditions	V _{DD} [V]	min	typ	max	unit
Max volt	ximum supply age	V _{DD} max	V _{DD} 1, V _{DD} 2, V _{DD} 3, V _{DD} 4	V _{SS} 1=V _{SS} 2=V _{SS} 3= V _{SS} 4		-0.3		+4.6	
Inpu	ut voltage	VI (1)	RESB			-0.3		V _{DD} +0.3	v
Inpu	ut/output voltage	VIO (1)	Ports 0, 1, 2 Ports 3, 4, 5 Ports 6, 7 Ports A, B, C, D			-0.3		VDD +0.3	
High level output current	Peak output current	IOPH (1)	Ports 0, 1, 2, 3 P40 to P45 Ports 7, A, D PB2 to PB6	CMOS output selected Per applicable pin		-7.5			
outpu		IOPH (2)	P46, P47 PB0, PB1	Per applicable pin		-12.5			
ıt curi		IOPH (3)	Port 5, 6 PC0 to PC4	Per applicable pin		-4.5			
ent	Average output current (Note 1-1)	IOMH (1)	Ports 0, 1, 2, 3 P40 to P45 Ports 5, 6, 7, A PB2 to PB6 Ports D	CMOS output selected Per applicable pin		-5			
		IOMH (2)	P46, P47 PB0, PB1	Per applicable pin		-10			
		IOMH (3)	Port 5, 6 PC0 to PC4	Per applicable pin		-3			
	Total output current	$\Sigma IOAH(1)$	Pprts 5 PC0 to PC4	Total of currents at applicable pins		-10			
		$\Sigma IOAH(2)$	Port 6	Total of currents at applicable pins		-10			mA
		$\Sigma IOAH(3)$	Port 5, 6 PC0 to PC4	Total of currents at applicable pins	-20				
		$\Sigma IOAH (4)$	Ports 1,D1 P20 to P21	Total of currents at applicable pins		-20			
		$\Sigma IOAH (5)$	P22 to P27	Total of currents at applicable pins		-20			
		Σ IOAH (6)	Ports 1, 2, D	Total of currents at applicable pins		-40			
		Σ IOAH (7)	Ports 4	Total of currents at applicable pins		-20			
		Σ IOAH (8)	Ports 0, 3	Total of currents at applicable pins		-20			
		ΣIOAH (9)	Ports 0, 3, 4	Total of currents at applicable pins		-40			
		ΣIOAH (10)	Ports B, 7	Total of currents at applicable pins		-20			1
		ΣIOAH (11)	Ports A	Total of currents at applicable pins		-20			
		ΣIOAH (12)	Ports 7, A, B	Total of currents at applicable pins		-40			1

■ Absolute Maximum Ratings at Ta=25°C, V_{SS}1=V_{SS}2=V_{SS}3= V_{SS}4=0V

Note 1-1 : Average output current refers to the average of output currents measured for a period of 100 ms.

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Demonstern	Secondard 1	Applicable Pin	Conditions			Specific	ation	
Parameter	Symbol	/Remarks	Conditions	V _{DD} [V]	min	typ	max	unit
Oscillation frequency range (Note 2-3)	FmCF (1)	PC3 (CF1), PC4 (CF2)	12 MHz ceramic oscillator mode See Fig. 1.	3.0 to 3.6		12		
(FmCF (2)	PC3(CF1), PC4(CF2)	10 MHz ceramic oscillator mode See Fig. 1.	2.7 to 3.6		10		MHz
	FmRC		Internal RC oscillation	2.7 to 3.6	0.5	1.0	2.0	
	FmSLRC		Internal low-speed RC oscillation	2.7 to 3.6	18	30	45	
	FsX'tal	XT1, XT2	32.768 kHz crystal oscillator mode See Fig. 2.	2.7 to 3.6		32.768		kHz
	FmVCO(1)		VCO oscillator When setting FRQSEL=0 See Fig. 9.	2.7 to 3.6	12		28	
	FmVCO(2)		VCO oscillator When setting FRQSEL=1 See Fig. 9.	2.7 to 3.6	38		70	MHz
	FmVCO(5)		VCO oscillator	2.7 to 3.6		Note 2-3		

Note 2-2 : See Tables 1 and 2 for oscillator constant values.

Note 2-3 : VCO oscillation frequency = Ceramic oscillator frequency × Setting point of SELREF

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

■ Electrical Characteristics at Ta=-40 to +85°C, V_{SS}1=V_{SS}2=V_{SS}3=V_{SS}4=0V

Parameter	Symbol	Applicable Pin	Conditions			Specific	ation	
Parameter	Symbol	/Remarks	Conditions	V _{DD} [V]	min	typ	max	unit
High level input current	IIH (1)	Ports 0, 1, 2 Ports 3, 4, 5 Ports 6, 7 Ports A, B,C, D RESB	Output disabled Pull-up resistor off VIN=VDD (including output Tr. off leakage current)	2.7 to 3.6			1	
Low level input current	IIL (1)	Ports 0, 1, 2 Ports 3, 4, 5 Ports 6, 7 Ports A, B, C, D RESB	Output disabled Pull-up resistor off VIN=VSS (including output Tr. off leakage current)	2.7 to 3.6	-1			μΑ
High level output voltage	VOH (1)	Ports 0, 1, 2, 3 Ports 5, 6	IOH=-0.4mA	3.0 to 3.6	V _{DD} -0.4			
	VOH (2)	Ports A, D, PC2 P40 to P45 PB2 to PB6	IOH=-0.2mA	2.7 to 3.6	V _{DD} -0.4			
	VOH (3)	P46, P47	IOH=-1.6mA	3.0 to 3.6	V _{DD} -0.4			
	VOH (4)	PB0, PB1	IOH=-1.0mA	2.7 to 3.6	V _{DD} -0.4			
	VOH (5)	PC0, PC1,	IOH=-1.0mA	3.0 to 3.6	V _{DD} -0.4			
	VOH (6)	PC3, PC4,	IOH=-0.4mA	2.7 to 3.6	V _{DD} -0.4			
Low level output voltage	VOL (1)	Ports 0, 1, 3 , 4 Ports 5, 6, 7, D PC2	IOL=1.6mA	3.0 to 3.6			0.4	v
	VOL (2)	P20 to P21, P24 to P27 PA0 to PA3 PA6 to PA7 PB0 to PB3, PB6	IOL=1.0mA	2.7 to 3.6			0.4	
	VOL (3)	P22, P23,	IOL=3.0mA	3.0 to 3.6			0.4	
	VOL (4)	PA4, PA5, PB4, PB5	IOL=1.3mA	2.7 to 3.6			0.4	
	VOL (5)	PC0, PC1,	IOL=1.0mA	3.0 to 3.6			0.4	
	VOL (6)	PC3, PC4,	IOL=0.4mA	2.7 to 3.6			0.4	
Pull-up resistor	Rpu (1)	Ports 0, 1, 2, 3 Ports 4, 5, 6, 7	VOH=0.9V _{DD}	3.0 to 3.6	15	35	80	kΩ
	Rpu (2)	Ports A, B, D, PC2		2.7 to 3.6	15	35	100	
Hysteresis voltage	VHYS	RESB When ports 1, 2, 3, 4, A, B PnFSAn=1		2.7 to 3.6		0.1V _{DD}		v
Pin capacitance	СР	All pins	Pins other than that under test V _{IN} =V _{SS} f=1 MHz Ta=25°C	2.7 to 3.6		10		pF

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

2-1. SIO1 Serial Input/Output Characteristics (Wakeup Function Disabled) (Note 4-3-1)

	г		Shl	Applicable	Conditions			Specif	ication	
	r	arameter	Symbol	Pin/Remarks	Conditions	V _{DD} [V]	min	typ	max	unit
Seri	Inpu	Period	tSCK (4)	SCK1 (P45)	• See Fig. 6.		4			
Serial clock	Input clock	Low level pulse width	tSCKL (4)				2			
		High level	tSCKH (4)				2			
		pulse width	tSCKHA (4)		 Automatic communication mode See Fig. 6. 	2.7 to 3.6	6			
			tSCKHBSY (4a)		 Automatic communication mode See Fig. 6. 		23			tCYC
			tSCKHBSY (4b)		 Mode other than automatic communication mode See Fig. 6. 		4			
	Output clock	Period	tSCK (5)	SCK1 (P45)	CMOS output selected See Fig. 6.		4			
	t clock	Low level pulse width	tSCKL (5)	_				1/2		4SCV
		High level pulse width	tSCKH (5)	_				1/2	1	tSCK
			tSCKHA (5)		 Automatic communication mode CMOS output selected See Fig. 6. 	2.7 to 3.6	6			
		tSCKHBS (5a)	tSCKHBSY (5a)		Automatic communication mode CMOS output selected See Fig. 6.		4		23	tCYC
			tSCKHBSY (5b)		 Mode other than automatic communication mode See Fig. 6. 		4			
Serial input	Dat	ta setup time	tsDI (3)	SI1 (P44), SB1 (P44)	 Specified with respect to rising edge of SIOCLK 		0.03			
input	Dat	ta hold time	thDI (3)		• See Fig. 6.	2.7 to 3.6	0.03			
Serial output	Input clock	Output delay time	tdD0 (4)	SO1 (P43), SB1 (P44)	• (Note 4-3-2)				1tCYC +0.05	μs
	Output clock		tdDO (5)	-	• (Note 4-3-2)	2.7 to 3.6			1tCYC +0.05	

Note 4-3-1 : These specifications are theoretical values. Add margin depending on its use.

Note 4-3-2 : Specified with respect to the falling edge of SIOCLK. Specified as the interval up to the time an output change begins in the open drain output mode. See Fig. 6.

2-2. SIO1 Serial Input/Output Characteristics (Wakeup Function Enabled) (Note 4-4-1)

	п	arameter	Symbol	Applicable	Conditions			Specif	ication	
	Г	arameter	Symbol	Pin/Remarks	Conditions	V _{DD} [V]	min	typ	max	unit
Seria	Inpu	Period	tSCK (6)	SCK1 (P45)	• See Fig. 6.		2			
Serial clock	Input clock	Low level pulse width	tSCKL (6)				1			
		High level	tSCKH (6)			2.7 to 3.6	1			tCYC
		pulse width	tSCKHBSY (6)				2			
Serial	Dat	ta setup time	tsDI (4)	SI1 (P44), SB1 (P44)	• Specified with respect to rising edge of SIOCLK		0.03			
input	Dat	ta hold time	thDI (4)		• See Fig. 6.	2.7 to 3.6	0.03			
Serial output	Input clock	Output delay time	tdD0 (6)	SO1 (P43), SB1 (P44)	• (Note 4-4-2)	2.7 to 3.6			1tCYC +0.05	μs

Note 4-4-1 : These specifications are theoretical values. Add margin depending on its use.

Note 4-4-2 : Specified with respect to the falling edge of SIOCLK. Specified as the interval up to the time an output change begins in the open drain output mode. See Fig. 6.

3-2. SIO4 Serial Input/Output Characteristics (Wakeup Function Enabled) (Note 4-6-1)

	п	arameter	Symbol	Applicable	Conditions			Specif	ication	
	Р	arameter	Symbol	Pin/Remarks	Conditions	V _{DD} [V]	min	typ	max	unit
Seria	Inpu	Period	tSCK (9)	SCK4 (P45)	• See Fig. 6.		2			
Serial clock	Input clock	Low level pulse width	tSCKL (9)				1			
		High level	tSCKH (9)			2.7 to 3.6	1			tCYC
		pulse width	tSCKHBSY (9)				2			
Serial	Dat	ta setup time	tsDI (6)	SI4 (P44), SB4 (P44)	• Specified with respect to rising edge of SIOCLK		0.03			
input	Dat	ta hold time	thDI (6)		• See Fig. 6.	2.7 to 3.6	0.03			
Serial output	Input clock	Output delay time	tdD0 (9)	SO4 (P43), SB4(P44)	• (Note 4-6-2)	2.7 to 3.6			1tCYC +0.05	μs

Note 4-6-1 : These specifications are theoretical values. Add margin depending on its use.

Note 4-6-2 : Specified with respect to the falling edge of SIOCLK. Specified as the interval up to the time an output change begins in the open drain output mode. See Fig. 6.

	г	arameter	Sympol	Applicable	Conditions			Specif	ication	
	P	rarameter	Symbol	Pin/Remarks	Conditions	V _{DD} [V]	min	typ	max	unit
Serial clock	Input clock	Period	tSCK (10)	SM0CK (P22)	See Fig. 6.		4			
clock	clock	Low level pulse width	tSCKL (10)			2.7 to 3.6	2			
		High level pulse width	tSCKH (10)				2			tCYC
	Outpu	Period	tSCK (11)	SM0CK (P22)	CMOS output selected See Fig. 6.		4			
	Period Low level pulse width High level pulse width	tSCKL (11)			2.7 to 3.6		1/2			
		tSCKH (11)					1/2		tSCK	
Serial input	Dat	ta setup time	tsDI (7)	SM0DA (P23),	• Specified with respect to rising edge of SIOCLK		0.03			
input	Dat	ta hold time	thDI (7)		• See Fig. 6.	2.7 to 3.6	0.03			
Serial output	Ou	tput delay time	tdD0 (10)	SM0DO (P24), SM0DA (P23)	 Specified with respect to falling edge of SIOCLK Specified as interval up to time when output state starts changing. See Fig. 6. 	2.7 to 3.6			1tCYC +0.05	μs

4-1. SMIIC0 Simple SIO Mode Input/Output Characteristics

Note 4-7-1 : These specifications are theoretical values. Add margin depending on its use.

4-2. SMIIC0 I²C Mode Input/Output Characteristics

	D	aramatar		Symbol	Applicable	Conditions			Specif	ication	_
	Pa	arameter		Symbol	Pin/Remarks	Conditions	V _{DD} [V]	min	typ	max	unit
Clock	Input clock	Period		tSCL	SM0CK (P22)	• See Fig. 8.		5			
	lock	Low level pulse widt	Ь	tSCLL			2.7 to 3.6	2.5			
		High level		tSCLH							Tfilt
		pulse widt						2			
	Output clock	Period		tSCLx	SM0CK (P22)	• Specified as interval up to time when output state starts		10			
	clock	Low level pulse widt	h	tSCLLx		changing.	2.7 to 3.6		1/2		49.01
		High level pulse widt		tSCLHx					1/2		tSCL
pin	s inp	C and SM0E out spike sion time)A	tsp	SM0CK (P22) SM0DA (P23)	• See Fig. 8.	2.7 to 3.6			1	Tfilt
			Input	tBUF	SM0CK (P22) SM0DA (P23)	• See Fig. 8.		2.5			Tfilt
	weer	ease time n start and	Ou	tBUFx	SM0CK (P22) SM0DA (P23)	 Standard clock mode Specified as interval up to time when output state starts changing. 	2.7 to 3.6	5.5			
	sop		Output			 High-speed clock mode Specified as interval up to time when output state starts changing. 		1.6			μs
			I	tHD;STA	SM0CK (P22) SM0DA (P23)	When SMIIC register control bit, I2CSHDS=0 · See Fig. 8.		2.0			
		restart			When SMIIC register control bit I2CSHDS=1 · See Fig. 8.		2.5			Tfilt	
cor tim		on hold	01	tHD;STAx	SM0CK (P22) SM0DA (P23)	 Standard clock mode Specified as interval up to time when output state starts changing. 	2.7 to 3.6	4.1			
			Output			 High-speed clock mode Specified as interval up to time when output state starts changing. 		1.0			μs
	_	_	Input	tSU;STA	SM0CK (P22) SM0DA (P23)	• See Fig. 8.		1.0			Tfilt
	start up tii	condition me	Out	tSU;STAx	SM0CK (P22) SM0DA (P23)	 Standard clock mode Specified as interval up to time when output state starts changing. 	2.7 to 3.6	5.5			
			Output			 High-speed clock mode Specified as interval up to time when output state starts changing. 		1.6			– μs

5-2. SMIIC1 I²C Mode Input/Output Characteristics

	D	arameter		Symbol	Applicable	Conditions			Specif	ication	_
	P	arameter		Symbol	Pin/Remarks	Conditions	V _{DD} [V]	Min	typ	max	unit
Clock	Input clock	Period		tSCL	SM1CK (PB4)	• See Fig. 8.		5			
	lock	Low level pulse widt	h	tSCLL			2.7 to 3.6	2.5			TCL
		High level pulse widt		tSCLH				2			Tfilt
	Outpu	Period		tSCLx	SM1CK (PB4)	• Specified as interval up to time when output state starts		10			
	Output clock	Low level pulse widt	h	tSCLLx		changing.	2.7 to 3.6		1/2		
		High level pulse widt		tSCLHx					1/2		tSCL
pin	s inp	C and SM0E out spike sion time	рА	tsp	SM1CK (PB4) SM1DA (PB5)	• See Fig. 8.	2.7 to 3.6			1	Tfilt
			Input	tBUF	SM1CK (PB4) SM1DA (PB5)	• See Fig. 8.		2.5			Tfilt
	weer	ease time n start and	Ou	tBUFx	SM1CK (PB4) SM1DA (PB5)	 Standard clock mode Specified as interval up to time when output state starts changing. 	2.7 to 3.6	5.5			
			Output			 High-speed clock mode Specified as interval up to time when output state starts changing. 		1.6			μsec
			In	tHD;STA	SM1CK (PB4) SM1DA (PB5)	 When SMIIC register control bit, I2CSHDS=0 See Fig. 8. 		2.0			
		estart	ıput			When SMIIC register control bit I2CSHDS=1 · See Fig. 8.		2.5			Tfilt
tim		on hold	Ou	tHD;STAx	SM1CK (PB4) SM1DA (PB5)	 Standard clock mode Specified as interval up to time when output state starts changing. 	2.7 to 3.6	4.1			
			Output			 High-speed clock mode Specified as interval up to time when output state starts changing. 		1.0			μsec
			Input	tSU;STA	SM1CK (PB4) SM1DA (PB5)	• See Fig. 8.		1.0			Tfilt
	start up tii	condition me	Out	tSU;STAx	SM1CK (PB4) SM1DA (PB5)	 Standard clock mode Specified as interval up to time when output state starts changing. 	2.7 to 3.6	5.5			11522
			Output			 High-speed clock mode Specified as interval up to time when output state starts changing. 		1.6			– μsec

Parameter		S-mak al	Applicable	Conditions			Specific	cation		
	1	Parameter	Symbol	Pin/Remarks	Conditions	V _{DD} [V]	min	typ	max	unit
Serial	Input clock	Period	Period tSCK (13) SLOCK See Fig. 6. (PA4)				4			
clock	clock	Low level pulse width	tSCKL (13)			2.7 to 3.6	2			tCYC
		High level pulse width	tSCKH (13)				2			
Serial	Data setup time		ta setup time tsDI (9) SL0DA (PA5),		• Specified with respect to rising edge of SIOCLK		0.03			
input	Da	ta hold time	thDI (9)		• See Fig. 6.	2.7 to 3.6	0.03			
Serial output	Output delay time		tdD0 (13)	SL0DO (PA6), SL0DA (PA5)	 Specified with respect to falling edge of SIOCLK Specified as interval up to time when output state starts changing. See Fig. 6. 	2.7 to 3.6			1tCYC +0.05	μs

6-1. SLIIC0 Simple SIO Mode Input/Output Characteristics

Note 4-11-1 : These specifications are theoretical values. Add margin depending on its use.

6-2. SLIIC1 I²C Mode Input/Output Characteristics

	р	arameter		Symbol	Applicable	Conditions			Specif	ïcation	
	P	arameter		Symbol	Pin/Remarks	Conditions	V _{DD} [V]	5 .6 2.5 .6 .6 2.5 .6 2.5 .6 2.5	unit		
Clock	Input clock	Period		tSCL	SLOCK (PA4)	• See Fig. 8.		5			
	clock	Low level pulse width	h	tSCLL			2.7 to 3.6	2.5			Tfilt
		High level pulse width		tSCLH				2			
SLOCK and SLODA pins input spike suppression time			tsp	SLOCK (PA4) SLODA (PA5)	• See Fig. 8.	2.7 to 3.6			1	Tfilt	
Bus release time between start and stop		Input	tBUF	SLOCK (PA4) SLODA (PA5)	• See Fig. 8.	2.7 to 3.6	2.5			Tfilt	
Start/restart condition hold		Input	tHD;STA	SLOCK (PA4) SLODA (PA5)	 When SMIIC register control bit, I2CSHDS=0 See Fig. 8. 	2.7 to 3.6	2.0			Tfilt	
tim	time		ut			When SMIIC register control bit I2CSHDS=1 · See Fig. 8.		2.5			
	Restart condition setup time		Input	tSU;STA	SLOCK (PA4) SLODA (PA5)	• See Fig. 8.	2.7 to 3.6	1.0			Tfilt
	op co up ti	ndition me	Input	tSU;STO	SLOCK (PA4) SLODA (PA5)	• See Fig. 8.	2.7 to 3.6	1.0			Tfilt
De			Input	tHD;DAT	SL0CK (PA4) SL0DA (PA5)	• See Fig. 8.	2.7 to 3.6	0			TOTA
Da	Data hold tin	sia time	Output	tHD;DATx	SL0CK (PA4) SL0DA (PA5)	 Specified as interval up to time when output state starts changing. 	2.7 10 3.6	1		1.5	Tfilt
Da	Data setup time		Input	tSU;DAT	SLOCK (PA4) SLODA (PA5)	• See Fig. 8.	2.7 to 3.6	1			T£14
Da			Output	tSU;DATx	SLOCK (PA4) SLODA (PA5)	 Specified as interval up to time when output state starts changing. 	2.7 10 5.0	1tSCL- 1.5Tfilt			Tfilt

■ AD Converter Characteristics at Ta=-40 to +85°C, V_{SS}1=V_{SS}2=V_{SS}3=V_{SS}4=0V 1. 12-bit AD Conversion Mode

	0 1 1	Applicable Pin	Q IV		Specification				
Parameter	Symbol	/Remarks	Conditions	V _{DD} [V]	min	typ	max	unit	
Resolution	NAD	AN0 (P60) to AN7 (P67),		2.7 to 3.6		12		bit	
Absolute accuracy	ETAD	AN8 (P70)	(Note 6-1)	2.7 to 3.6			±16	LSB	
Conversion time	TCAD12	to AN15 (P77)	Conversion time calculated	3.0 to 3.6	64		115		
				2.7 to 3.6	128		230	μs	
Analog input voltage range	VAIN			2.7 to 3.6	V _{SS}		V _{DD}	v	
Analog port input current	IAINH		VAIN=V _{DD}	2.7 to 3.6			1		
input current	IAINL		VAIN=V _{SS}	2.7 to 3.6	-1			μΑ	

- Conversion time calculation formula : TCAD12 = $(\frac{52}{\text{AD division ratio}} + 2) \times \text{tCYC}$

2. 8-bit AD Conversion Mode

Parameter	Course of	Applicable Pin	Conditions			Specif	ication	
Parameter	Symbol	/Remarks	Conditions	V _{DD} [V]	min	typ	max	unit
Resolution	NAD	AN0 (P60) to AN7 (P67),		2.7 to 3.6		8		bit
Absolute accuracy	ETAD	AN8 (P70)	(Note 6-1)	2.7 to 3.6			±1.5	LSB
Conversion time	TCAD8	to AN15 (P77) Conversion time calculate		3.0 to 3.6	39		71	
				2.7 to 3.6	79		140	μs
Analog input voltage range	VAIN			2.7 to 3.6	VSS		V _{DD}	V
Analog port input current	IAINH		VAIN=VDD	2.7 to 3.6			1	
input current	IAINL		VAIN=V _{SS}	2.7 to 3.6	-1			μA

- Conversion time calculation formula : TCAD8 = $\left(\frac{52}{\text{AD division ratio}} + 2\right) \times \text{tCYC}$

Note 6-1 : The quantization error ($\pm 1/2$ LSB) is excluded from the absolute accuracy.

Note 6-2 : The conversion time refers to the interval from the time a conversion starting instruction is issued till the time the complete digital value against the analog input value is loaded in the result register.

The conversion time is twice the normal value when one of the following conditions occurs:

- The first AD conversion is executed in the 12-bit AD conversion mode after a system reset.

- The first AD conversion is executed after the AD conversion mode is switched from 8-bit to 12-bit AD conversion mode.

Continued from	m preceding pa	ige.							
		Applicable Pin/Remarks			Specification				
r ai ailictei	Symbol	r III/ Keillaiks	Conditions	V _{DD} [V]	min	typ	max	unit	
HOLD mode consumption current	IDDHOLD (1)	V _{DD} 1	HOLD mode • CF1=VDD or open (external clock mode)	2.7 to 3.6		0.2	45		
	IDDHOLD (2)		HOLD mode • CF1=VDD or open (external clock mode) • LVD option selected	2.7 to 3.6		1.2	48		
HOLDX mode consumption current	IDDHOLD (3)		HOLDX mode • CF1=VDD or open (external clock mode) • FmX'tal=32.768 kHz crystal oscillator mode	2.7 to 3.6		4.6	60	μΑ	
	IDDHOLD (4) HOLDX mode • CF1=VDD or open (external clock mode)		2.7 to 3.6		5.6	63			

Note 7-1 : The consumption current value includes none of the currents that flow into the output transistor and internal pull-up resistors.

■ **F-ROM Programming Characteristics** at Ta=+10 to +55°C, V_{SS}1=V_{SS}2=V_{SS}3=V_{SS}4=0V

Parameter	Symbol	Applicable	Conditions		Specification				
Parameter	Symbol Pin/Remarks Conditions		V _{DD} [V]	min	typ	max	unit		
Onboard programming current	IDDFW (1)	V _{DD} 1	Microcontroller erase current current is excluded.	2.7 to 3.6			10	mA	
Onboard programming time	tFW (1)		• 2K-byte erase operation	2.7 to 3.6			25	ms	
	tFW (2)		2-byte programming operation	2.7 to 3.6			45	μs	

Characteristics of a Sample Main System Clock Oscillation Circuit

Given below are the characteristics of a sample main system clock oscillation circuit that are measured using a Our Company -designated oscillation characteristics evaluation board and external components with circuit constant values with which the oscillator vendor confirmed normal and stable oscillation.

Table 1 Characteristics of a Sample Main System Clock Oscillator Circuit with a Ceramic Resonator

Nominal	Vendor Name	Decemeter		Circuit	Constant		Operating Voltage	Oscillation Stabilization Time		Remarks	
Frequency	vendor Ivame	Resonator	C3 [pF]	C4 [pF]	Rf [Ω]	Rd2 [Ω]	Range [V]	typ [ms]	max [ms]	Kennarks	
12 MHz		CSTCE12M0G52-R0	(10)	(10)	OPEN	330	2.2 to 3.6	0.02	0.2	C1, C2 integrated type	
10 MHz	MURATA	CSTCE10M0G52-R0	(10)	(10)	OPEN	680	2.2 to 2.6	0.02	0.2	C1, C2 integrated type	
10 MHZ		CSTLS10M0G53-B0	(15)	(15)	OPEN	680	2.2 to 3.6	0.02	0.2	C1, C2 integrated type	

The oscillation stabilization time refers to the time interval that is required for the oscillation to get stabilized after V_{DD} goes above the lower limit level of the operating voltage range (see Figure 4)

■ Characteristics of a Sample Subsystem Clock Oscillator Circuit

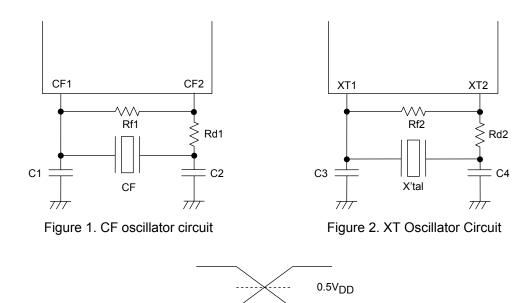
Given below are the characteristics of a sample subsystem clock oscillation circuit that are measured using a Our Company -designated oscillation characteristics evaluation board and external components with circuit constant values with which the oscillator vendor confirmed normal and stable oscillation.

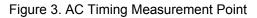
Table 2 Characteristics of a Sample Subsystem Clock Oscillator Circuit with a Crystal Resonator

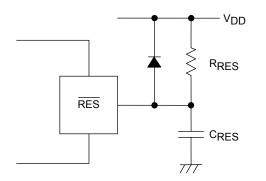
Nominal	Vendor Name	Resonator	Circuit Constant			t	Operating Voltage	Oscillation Stabilization Time		Remarks	
Frequency	vendor Name	Resolution	C3 [pF]	C4 [pF]	Rf2 [Ω]	Rd2 [Ω]	Range [V]	typ [s]	max [s]	Keinarks	
32.768 kHz	EPSON TOYOCOM	MC-306	10	10	Open	330K	2.2 to 3.6	1.0	3.0	CL=7.0pF	

The oscillation stabilization time refers to the time interval that is required for the oscillation to get stabilized after the instruction for starting the subclock oscillator circuit is executed plus the time interval that is required for the oscillation to get stabilized after the HOLD mode is released (see Figure 4).

Note : The traces to and from the components that are involved in oscillation should be kept as short as possible as the oscillation characteristics are affected by their trace pattern.





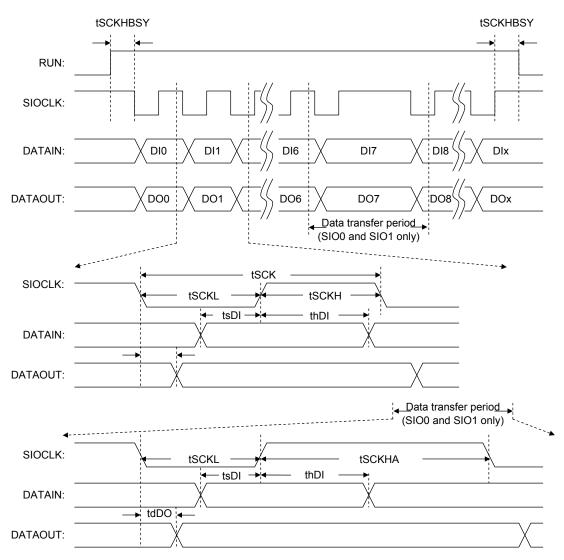


Note :

Reset signal must be present when power supply rises.

Determine the value of C_{RES} and R_{RES} so that the reset signal is present for 10 µs after the supply voltage gets stabilized.





* Remarks: DIx and DOx denote the last bits communicated; x=0 to 32768

Figure 6. Serial I/O Waveforms

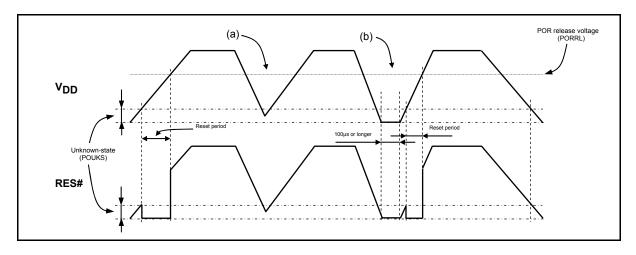


Figure 10. Waveform observed when only POR is used (LVD not used) (RESET pin : Pull-up resistor R_{RES} only)

- The POR function generates a reset only when power is turned on starting at the VSS level.
- <u>No stable reset will be generated if power is turned on again when the power level does not go</u> <u>down to the V_{SS} level as shown in (a). If such a case is anticipated, use the LVD function</u> <u>together with the POR function or implement an external reset circuit.</u>
- <u>A reset is generated only when the power level goes down to the VSS level as shown in (b) and power is turned on again after this condition continues for 100µs or longer.</u>

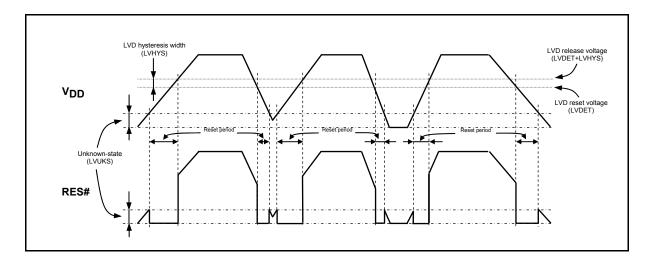
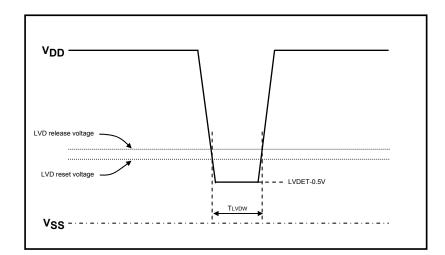
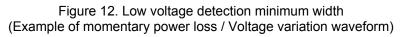


Figure 11. Waveform observed when both POR and LVD functions are used (RESET pin : Pull-up resistor R_{RES} only)

- Resets are generated both when power is turned on and when the power level lowers.
- <u>A hysteresis width (LVHYS) is provided to prevent the repetitions of reset release and entry cycles near the detection level.</u>





ORDERING INFORMATION

Device	Package	Shipping (Qty / Packing)			
LC88FC2H0BUTJ-2H	TQFP 100, 14x14 (Pb-Free / Halogen Free)	900 / Tray JEDEC			

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