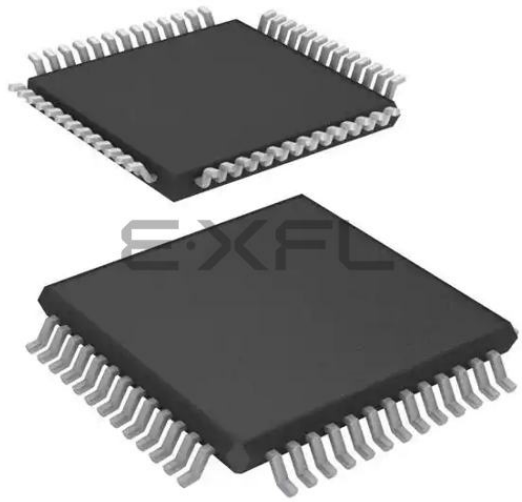

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	8032
Core Size	8-Bit
Speed	40MHz
Connectivity	I²C, IrDA, SPI, UART/USART
Peripherals	LVD, POR, PWM, WDT
Number of I/O	36
Program Memory Size	160KB (160K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	52-TQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/upsd3333d-40t6

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Table 2. Pin definitions (continued)

Port pin	Signal name	80-Pin num.	52-Pin num.(1)	In/Out	Function		
					Basic	Alternate 1	Alternate 2
P1.4	SPICLK ADC4	59	38	I/O	General I/O port pin	SPI Clock Out (SPICLK)	ADC Channel 4 input (ADC4)
P1.5	SPIRxD ADC6	60	39	I/O	General I/O port pin	SPI Receive (SPIRxD)	ADC Channel 5 input (ADC5)
P1.6	SPITXD ADC6	61	40	I/O	General I/O port pin	SPI Transmit (SPITxD)	ADC Channel 6 input (ADC6)
P1.7	SPISEL ADC7	64	41	I/O	General I/O port pin	SPI Slave Select ($\overline{\text{SPISEL}}$)	ADC Channel 7 input (ADC7)
P3.0	RxD0	75	23	I/O	General I/O port pin	UART0 Receive (RxD0)	
P3.1	TXD0	77	24	I/O	General I/O port pin	UART0 Transmit (TxD0)	
P3.2	EXINT0 TGO	79	25	I/O	General I/O port pin	Interrupt 0 input (EXTINT0)/Timer 0 gate control (TG0)	
P3.3	INT1	2	26	I/O	General I/O port pin	Interrupt 1 input (EXTINT1)/Timer 1 gate control (TG1)	
P3.4	C0	40	27	I/O	General I/O port pin	Counter 0 input (C0)	
P3.5	C1	42	28	I/O	General I/O port pin	Counter 1 input (C1)	
P3.6	SDA	44	29	I/O	General I/O port pin	I^2C Bus serial data (I^2CSDA)	
P3.7	SCL	46	30	I/O	General I/O port pin	I^2C Bus clock (I^2CSCL)	
P4.0	T2 TCM0	33	22	I/O	General I/O port pin	Program Counter Array0 PCA0-TCM0	Timer 2 Count input (T2)
P4.1	T2X TCM1	31	21	I/O	General I/O port pin	PCA0-TCM1	Timer 2 Trigger input (T2X)
P4.2	RXD1 TCM2	30	20	I/O	General I/O port pin	PCA0-TCM2	UART1 or IrDA Receive (RxD1)
P4.3	TXD1 PCACLK0	27	18	I/O	General I/O port pin	PCACLK0	UART1 or IrDA Transmit (TxD1)
P4.4	SPICLK TCM3	25	17	I/O	General I/O port pin	Program Counter Array1 PCA1-TCM3	SPI Clock Out (SPICLK)
P4.5	SPIRXD TCM4	23	16	I/O	General I/O port pin	PCA1-TCM4	SPI Receive (SPIRxD)

Figure 8. PFQ operation on multi-cycle instructions

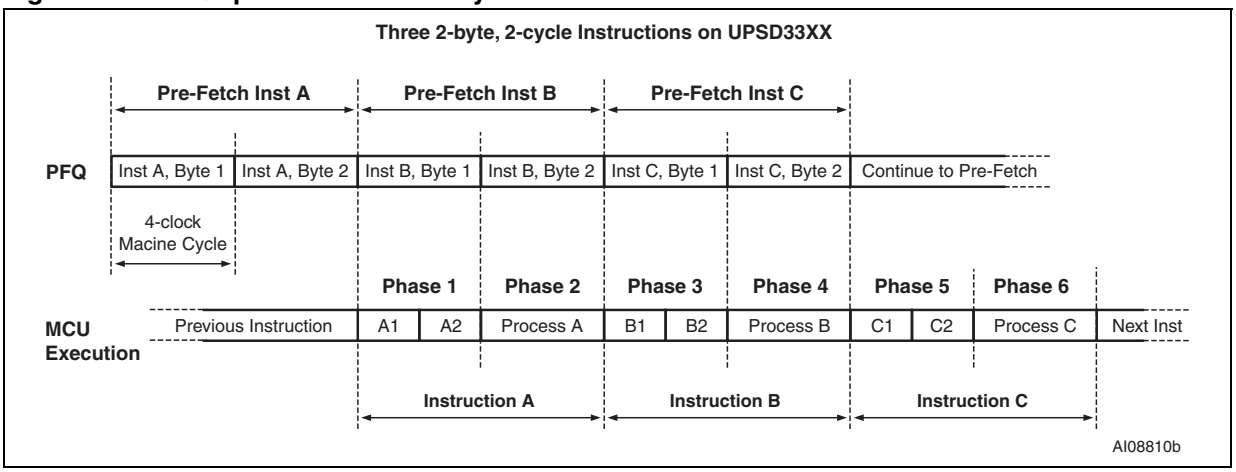


Figure 9. UPSD33xx multi-cycle instructions compared to standard 8032

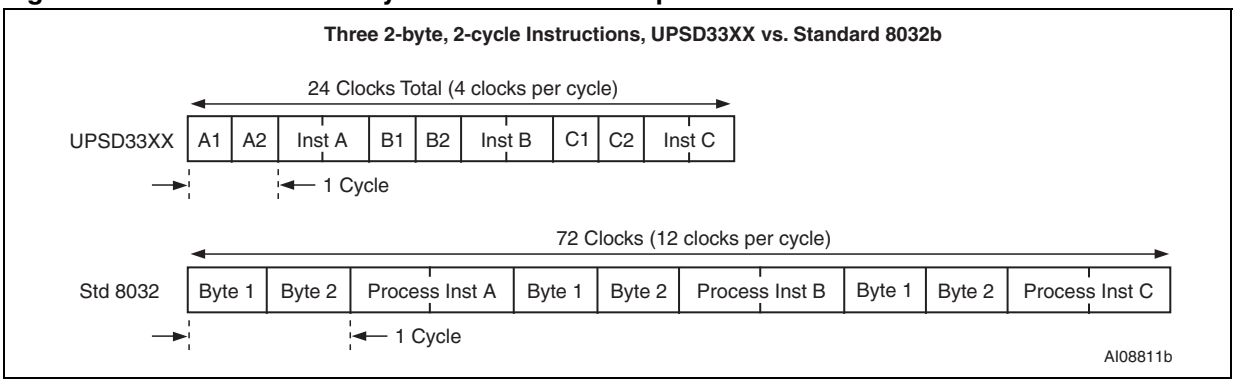


Figure 13. Clock generation logic

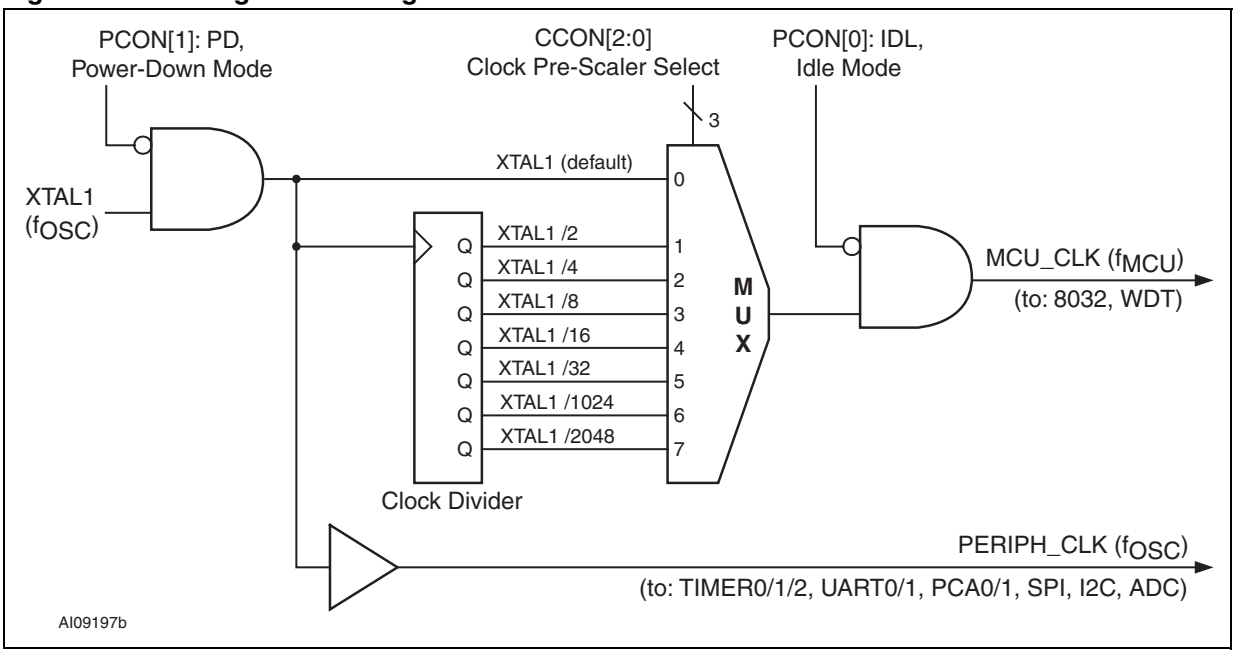


Table 27. CCON0: Clock Control register (SFR F9h, reset value 10h)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
–	–	–	DBGCE	CPUAR	CPUPS[2:0]		

Table 28. CCON0 register bit definition

Bit	Symbol	R/W	Definition
7	–	–	Reserved
6	–	–	Reserved
5	–	–	Reserved
4	DBGCE	R,W	**Debug Unit Breakpoint Comparator Enable** 0 = JTAG debug unit comparators are disabled 1 = JTAG debug unit comparators are enabled (Default condition after reset)
3	CPUAR	R,W	**Automatic MCU Clock Recovery** 0 = There is no change of CPUPS[2:0] when an interrupt occurs. 1 = Contents of CPUPS[2:0] automatically become 000b whenever any interrupt occurs.
2:0	CPUPS	R,W	**MCUCLK Pre-Scaler** 000b: $f_{MCU} = f_{OSC}$ (Default after reset) 001b: $f_{MCU} = f_{OSC}/2$ 010b: $f_{MCU} = f_{OSC}/4$ 011b: $f_{MCU} = f_{OSC}/8$ 100b: $f_{MCU} = f_{OSC}/16$ 101b: $f_{MCU} = f_{OSC}/32$ 110b: $f_{MCU} = f_{OSC}/1024$ 111b: $f_{MCU} = f_{OSC}/2048$

Table 61. Commonly used baud rates generated from Timer 2 (T2CON = 34h)

f_{OSC} MHz	Desired baud rate	Timer 2 SFRs		Resulting baud rate	Baud rate deviation
		RCAP2H (hex)	RCAP2L(hex)		
40.0	115200	FF	F5	113636	-1.36%
40.0	57600	FF	EA	56818	-1.36%
40.0	28800	FF	D5	29070	0.94%
40.0	19200	FF	BF	19231	0.16%
40.0	9600	FF	7E	9615	0.16%
36.864	115200	FF	F6	115200	0
36.864	57600	FF	EC	57600	0
36.864	28800	FF	D8	28800	0
36.864	19200	FF	C4	19200	0
36.864	9600	FF	88	9600	0
36.0	28800	FF	D9	28846	0.16%
36.0	19200	FF	C5	19067	-0.69%
36.0	9600	FF	8B	9615	0.16%
24.0	57600	FF	F3	57692	0.16%
24.0	28800	FF	E6	28846	0.16%
24.0	19200	FF	D9	19231	0.16%
24.0	9600	FF	B2	9615	0.16%
12.0	28800	FF	F3	28846	0.16%
12.0	9600	FF	D9	9615	0.16%
11.0592	115200	FF	FD	115200	0
11.0592	57600	FF	FA	57600	0
11.0592	28800	FF	F4	28800	0
11.0592	19200	FF	EE	19200	0
11.0592	9600	FF	DC	9600	0
3.6864	115200	FF	FF	115200	0
3.6864	57600	FF	FE	57600	0
3.6864	28800	FF	FC	28800	0
3.6864	19200	FF	FA	19200	0
3.6864	9600	FF	F4	9600	0
1.8432	19200	FF	FD	19200	0
1.8432	9600	FF	FA	9600	0

Figure 27. UART mode 0, block diagram

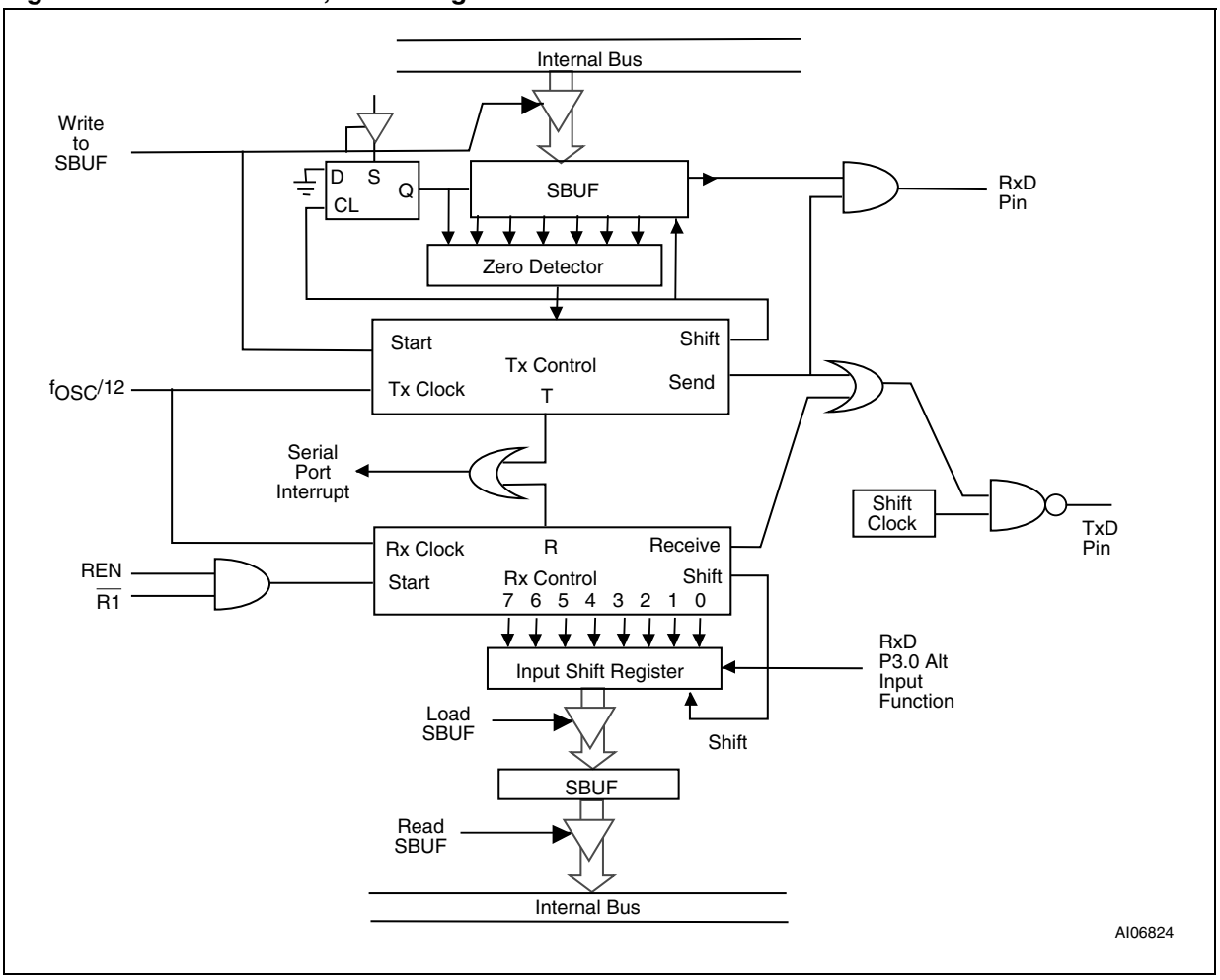


Figure 28. UART mode 0, timing diagram

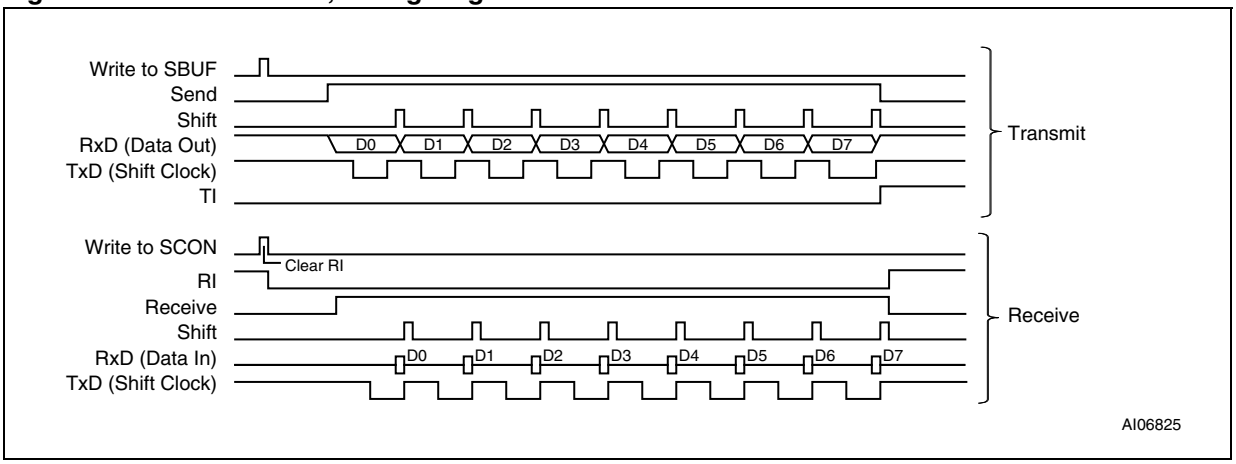


Table 81. S1SETUP register bit definition

Bit	Symbol	R/W	Function
7	EN_SS	R/W	**Enable Sample Setup** EN_SS = 1 will force the SIOE to sample(1) a START condition on the bus the number of times specified in SMPL_SET[6:0]. EN_SS = 0 means the SIOE will sample(1) a START condition only one time, regardless of the contents of SMPL_SET[6:0].
6:0	SMPL_SET [6:0]	–	**Sample Setting** Specifies the number of bus samples((1) taken during a START condition. See *Table 82 on page 133* for values.

1. Sampling SCL and SDA lines begins after '1'-to-'0' transition on SDA occurred while SCL is high. Time between samples is $1/f_{OSC}$.

Table 82. Number of I²C bus samples taken after 1-to-0 transition on SDA (START condition)

Contents of S1SETUP		Resulting value for S1SETUP	Resulting number of samples taken after 1-to-0 on SDA Line
SS_EN bit	SMPL_SET[6:0]		
0	XXXXXXXb	00h (default)	1
1	0000000b	80h	1
1	0000001b	81h	2
1	0000010b	82h	3
...	...	...	...
1	0001011b	8Bh	12
1	0010111b	97h	24
...	...	...	...
1	1111111b	FFh	128

Table 83. Start condition hold time

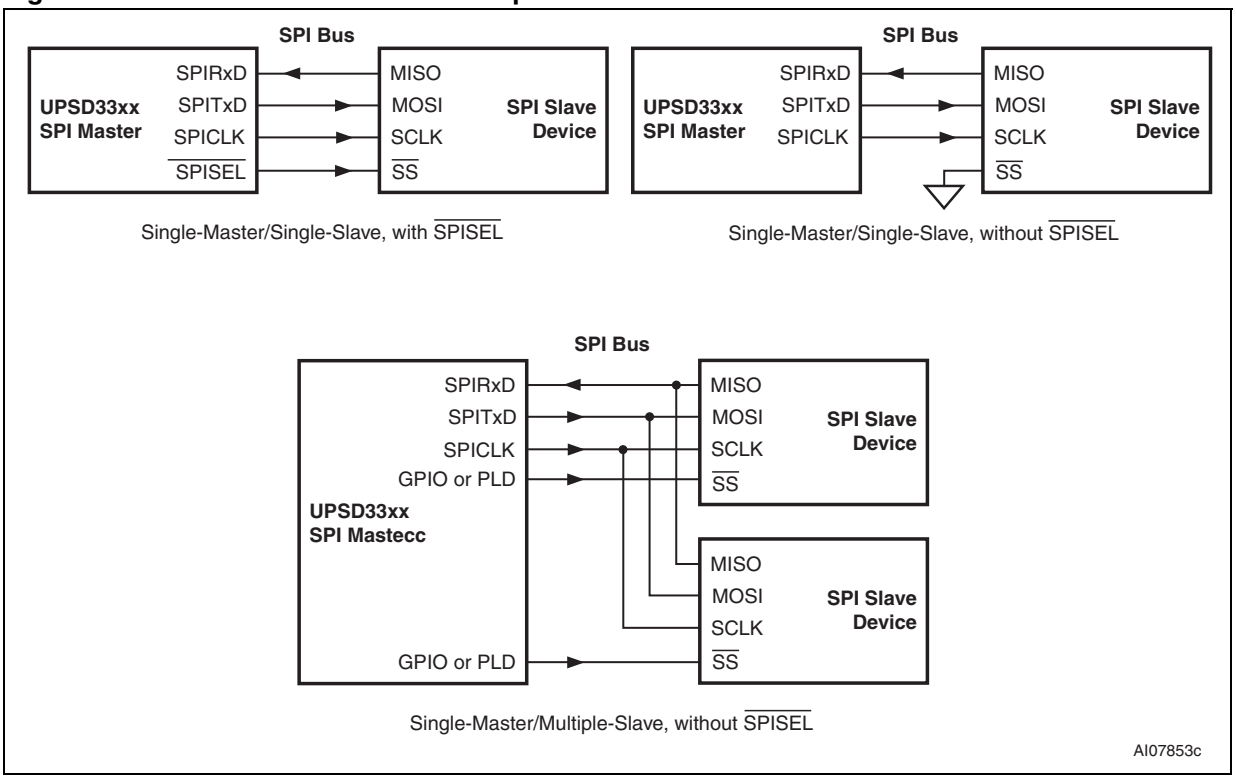
I²C bus speed	Range of I²C clock speed (f_{SCL})	Minimum START condition hold time (t_{HLDSTA})
Standard	Up to 100kHz	4000ns
Fast	101kHz to 400kHz	600ns
High	401kHz to 833kHz(1)	160ns

1. 833kHz is maximum for UPSD33xx devices.

Table 84 provides recommended settings for S1SETUP based on various combinations of f_{OSC} and f_{SCL}. Note that the “Total Sample Period” times in *Table 83* are typically slightly less than the minimum START condition hold time, t_{HLDSTA} for a given I²C bus speed.

Note: ***Important:*** *The SCL bit rate f_{SCL} must first be determined by bits CR[2:0] in the SFR S1CON before a value is chosen for SMPL_SET[6:0] in the SFR S1SETUP.*

Figure 40. SPI device connection examples



24.1 SPI bus features and communication flow

The SPICLK signal is a gated clock generated from the UPSD33xx (Master) and regulates the flow of data bits. The Master may transmit at a variety of baud rates, and the SPICLK signal will clock one period for each bit of transmitted data. Data is shifted on one edge of SPICLK and sampled on the opposite edge.

The SPITxD signal is generated by the Master and received by the Slave device. The SPIRxD signal is generated by the Slave device and received by the Master. There may be no more than one Slave device transmitting data on SPIRxD at any given time in a multi-Slave configuration. Slave selection is accomplished when a Slave's "Slave Select" (SS) input is permanently grounded or asserted active-low by a Master device. Slave devices that are not selected do not interfere with SPI activities. Slave devices ignore SPICLK and keep their MISO output pins in high-impedance state when not selected.

The SPI specification allows a selection of clock polarity and clock phase with respect to data. The UPSD33xx supports the choice of clock polarity, but it does not support the choice of clock phase (phase is fixed at what is typically known as CPHA = 1). See *Figure 42* and *Figure 43 on page 144* for SPI data and clock relationships.

Referring to these figures (*42* and *43*), when the phase mode is defined as such (fixed at CPHA =1), in a new SPI data frame, the Master device begins driving the first data bit on SPITxD at the very first edge of the first clock period of SPICLK.

The Slave device will use this first clock edge as a transmission start indicator, and therefore the Slave's Slave Select input signal may remain grounded in a single-Master/single-Slave

26.10 PWM mode - fixed frequency, 10-bit

The 10-bit PWM logic requires that all 3 TCMs in PCA0 or PCA1 operate in the same 10-bit PWM mode. The 10-bit PWM operates in a similar manner as the 16-bit PWM, except the PCACHm and PCACLm counters are reconfigured as 10-bit counters. The CAPCOMHn and CAPCOMLn registers become 10-bit registers.

PWM duty cycle of each TCM module can be specified in the 10-bit CAPCOMHn and CAPCOMLn registers. When the 10-bit PCA counter is equal or greater than the values in the 10-bit registers CAPCOMHn and CAPCOMLn, the PWM output switches to a high state. When the 10-bit PCA counter overflows, the PWM pin is switched to a logic low and starts the next PWM pulse.

The most-significant 6 bits in the PCACHm counter and CAPCOMH register are “Don’t cares” and have no effect on the PWM generation.

26.11 Writing to capture/compare registers

When writing a 16-bit value to the PCA Capture/Compare registers, the low byte should always be written first. Writing to CAPCOMLn clears the E_COMP Bit to '0'; writing to CAPCOMHn sets E_COMP to '1' the largest duty cycle is 100% (CAPCOMHn CAPCOMLn = 0x0000), and the smallest duty cycle is 0.0015% (CAPCOMHn CAPCOMLn = 0xFFFF). A 0% duty cycle may be generated by clearing the E_COMP Bit to ‘0’.

26.12 Control register bit definition

Each PCA has its own PCA_CONFIGn, and each module within the PCA block has its own TCM_Mode register which defines the operation of that module (see *Table 103 on page 159* through *Table 105 on page 160*). There is one PCA_STATUS register that covers both PCA0 and PCA1 (see *Table 107 on page 161*).

Table 103. PCA0 Control register PCACON0 (SFR 0A4h, Reset Value 00h)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
EN-ALL	EN_PCA	EOVFI	PCAIDLE	–	10B_PWM	CLK_SEL[1:0]	

Table 104. PCACON0 register bit definition

Bit	Symbol	Function
7	EN-ALL	0 = No impact on TCM modules 1 = Enable both PCA counters simultaneously (override the EN_PCA Bits) This bit is to start the two 16-bit counters in the PCA. For customers who want 5 PWM, for example, this bit can start all of the PWM outputs.
6	EN_PCA	0 = PCA counter is disabled 1 = PCA counter is enabled EN_PCA Counter Run Control Bit. Set with software to turn the PCA counter on. Must be cleared with software to turn the PCA counter off.

27.2 Memory mapping

There many different ways to place (or map) the address range of PSD module memory and I/O depending on system requirements. The DPLD provides complete mapping flexibility. *Figure 52* shows one possible system memory map. In this example, 128 Kbytes of main Flash memory for a UPSD3333 device is in 8032 program address space, and 32 Kbytes of secondary Flash memory, the SRAM, and csiop registers are all in 8032 XDATA space.

In *Figure 52*, the nomenclature fs0..fs7 are designators for the individual sectors of main Flash memory, 16 Kbytes each. CSBOOT0..CSBOOT3 are designators for the individual secondary Flash memory segments, 8 Kbytes each. *rs0* is the designator for SRAM, and csiop designates the PSD module control register set.

The designer may easily specify memory mapping in a point-and-click software environment using PSDsoft Express, creating a non-volatile configuration when the DPLD is programmed using JTAG.

27.2.1 8032 program address space

In the example of *Figure 52*, six sectors of main Flash memory (fs2.. fs7) are paged across three memory pages in the upper half of program address space, and the remaining two sectors of main Flash memory (fs0, fs1) reside in the lower half of program address space, and these two sectors are independent of paging (they reside in “common” program address space). This paged memory example is quite common and supported by many 8051 software compilers.

27.2.2 8032 data address space (XDATA)

Four sectors of secondary Flash memory reside in the upper half of 8032 XDATA space in the example of *Figure 52*. SRAM and csiop registers are in the lower half of XDATA space. The 8032 SFR registers and local SRAM inside the 8032 MCU module do not reside in XDATA space, so it is OK to place PSD module SRAM or csiop registers at an address that overlaps the address of internal 8032 MCU module SRAM and registers.

Figure 52. Typical system memory map

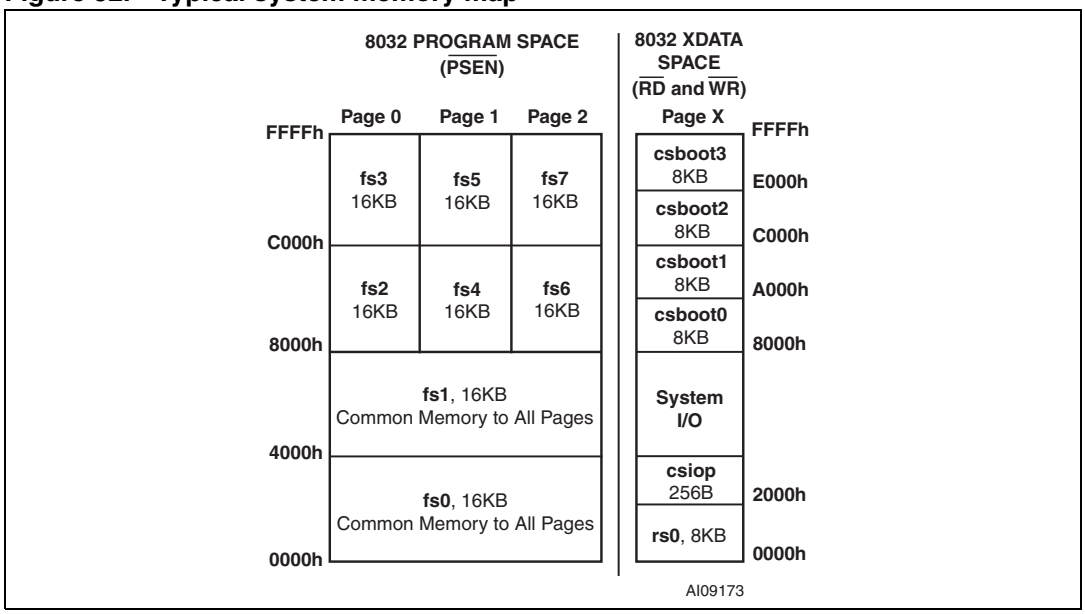
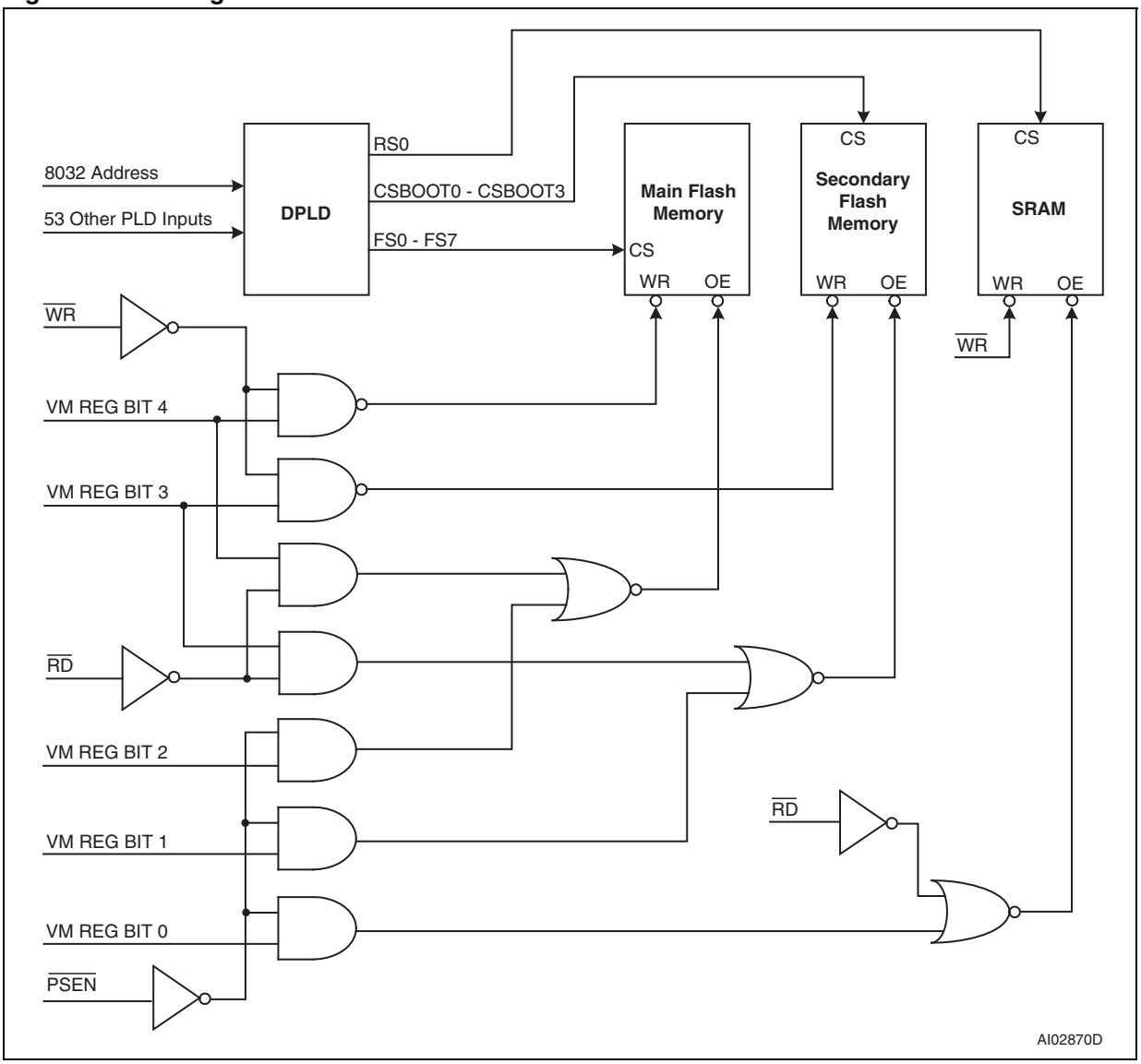


Figure 58. VM register control of memories



the PSD module with JTAG. When set, the security bit will block access of JTAG programming equipment from reading or modifying the PSD module Flash memory and PLD configuration. The security bit also blocks JTAG access to the MCU module for debugging. The only way to defeat the security bit is to erase the entire PSD module using JTAG (erase is the only JTAG operation allowed while security bit is set), after which the device is blank and may be used again. The 8032 MCU will always have access to Flash memory contents through its 8-bit data bus even while the security bit is set. The 8032 can read the status of the security bit at run-time (but it cannot change it) by reading the csiop register defined in *Table 120 on page 193*.

Table 119. Main Flash Memory Protection register definition (address = csiop + offset C0h)(1)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Sec7_Prot	Sec6_Prot	Sec5_Prot	Sec4_Prot	Sec3_Prot	Sec2_Prot	Sec1_Prot	Sec0_Prot

1. Bit definitions:
Sec<i>_Prot 1 = Flash memory sector <i> is write protected, 0 = Flash memory sector <i> is not write protected.

Table 120. Secondary Flash Memory Protection/Security register Definition (csiop+offset C2h)(1)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Security_Bit	not used	not used	not used	Sec3_Prot	Sec2_Prot	Sec1_Prot	Sec0_Prot

1. Security_Bit = 1, device is secured, 0 = not secured
Sec<i>_Prot 1 = Flash memory sector <i> is write protected, 0 = Flash memory sector <i> is not write protected.

27.4.24 PLDs

The PSD module contains two PLDs: the Decode PLD (DPLD), and the General PLD (GPLD), as shown in *Figure 62 on page 195*. Both PLDs are fed by a common PLD input signal bus, and additionally, the GPLD is connected to the 8032 data bus.

PLD logic is specified using PSDsoft Express and programmed into the PSD module using the JTAG ISP channel. PLD logic is non-volatile and available at power-up. PLDs may not be programmed by the 8032. The PLDs have selectable levels of performance and power consumption.

The DPLD performs address decoding, and generates select signals for internal and external components, such as memory, registers, and I/O ports. The DPLD can generate External Chip-Select (ECS1-ECS2) signals on Port D.

The GPLD can be used for logic functions, such as loadable counters and shift registers, state machines, encoding and decoding logic. These logic functions can be constructed from a combination of 16 Output Macrocells (OMC), 20 Input Macrocells (IMC), and the AND-OR Array.

Routing of the 16 OMCs outputs can be divided between pins on three Ports A, B, or C by the OMC Allocator as shown in *Figure 66 on page 202*. Eight of the 16 OMCs that can be routed to pins on Port A or Port B and are named MCELLAB0-MCELLAB7. The other eight OMCs to be routed to pins on Port B or Port C and are named MCELLBC0-MCELLBC7. This routing depends on the pin number assignments that are specified in PSDsoft Express for “PLD Outputs” in the Pin Definition section. OMC outputs can also be routed internally (not to pins) used as buried nodes to create shifters, counters, etc.

Table 131. Port configuration setting requirements

Port operating mode	Required action in PSDsoft Express to configure each pin	Value that 8032 writes to csiop Control register at run-time	Value that 8032 writes to csiop Direction register at run-time	Value that 8032 writes to bit 7 (PIO_EN) of csiop VM register at run-time
MCU I/O	Choose the MCU I/O function and declare the pin name	Logic '0' (default)	Logic 1 = Out of UPSD Logic 0 = Into UPSD	N/A
PLD I/O	Choose the PLD function type, declare pin name, and specify logic equation(s)	N/A	Direction register has no effect on a pin if pin is driven from OMC output	N/A
Latched Address Output	Choose Latched Address Out function, declare pin name	Logic '1'	Logic '1' Only	N/A
Peripheral I/O	Choose Peripheral I/O mode function and specify address range in DPLD for PSELx	N/A	N/A	PIO_EN Bit = Logic 1 (default is '0')
4-PIN JTAG ISP	No action required in PSDsoft to get 4-pin JTAG. By default TDO, TDI, TCK, TMS are dedicated JTAG functions.	N/A	N/A	N/A
6-PIN JTAG ISP (faster programming)	Choose JTAG TSTAT function for pin PC3 and JTAG $\overline{\text{TERR}}$ function for pin PC4.	N/A	N/A	N/A

27.4.37 MCU I/O mode

In MCU I/O mode, the 8032 on the MCU module expands its own I/O by using the I/O Ports on the PSD module. The 8032 can read PSD module I/O pins, set the direction of the I/O pins, and change the output state of I/O pins by accessing the Data In, Direction, and Data Out csiop registers respectively at run-time.

To implement MCU I/O mode, each desired pin is specified in PSDsoft Express as *MCU I/O* function and given a pin name. Then 8032 firmware is written to set the Direction bit for each corresponding pin during initialization routines (0 = In, 1 = Out of the chip), then the 8032 firmware simply reads the corresponding Data In register to determine the state of an I/O pin, or writes to a Data Out register to set the state of a pin. The Direction of each pin may be changed dynamically by the 8032 if desired. A mixture of input and output pins within a single port is allowed. *Figure 68 on page 208* shows the Data In, Data Out, and Direction signal paths.

The Data In registers are defined in *Table 132* to *Table 135 on page 210*. The Data Out registers are defined in *Table 136* to *Table 139 on page 211*. The Direction registers are defined in *Table 140* to *Table 27.4.38 on page 212*.

Table 145. Latched Address output, Port B Control register (address = csiop+offset 03h)(1)(2)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PB7 (addr A7 or A15)	PB6 (addr A6 or A14)	PB5 (addr A5 or A13)	PB4 (addr A4 or A12)	PB3 (addr A3 or A11)	PB2 (Addr A2 or A10)	PB1 (addr A1 or A9)	PB0 (addr A0 or A8)

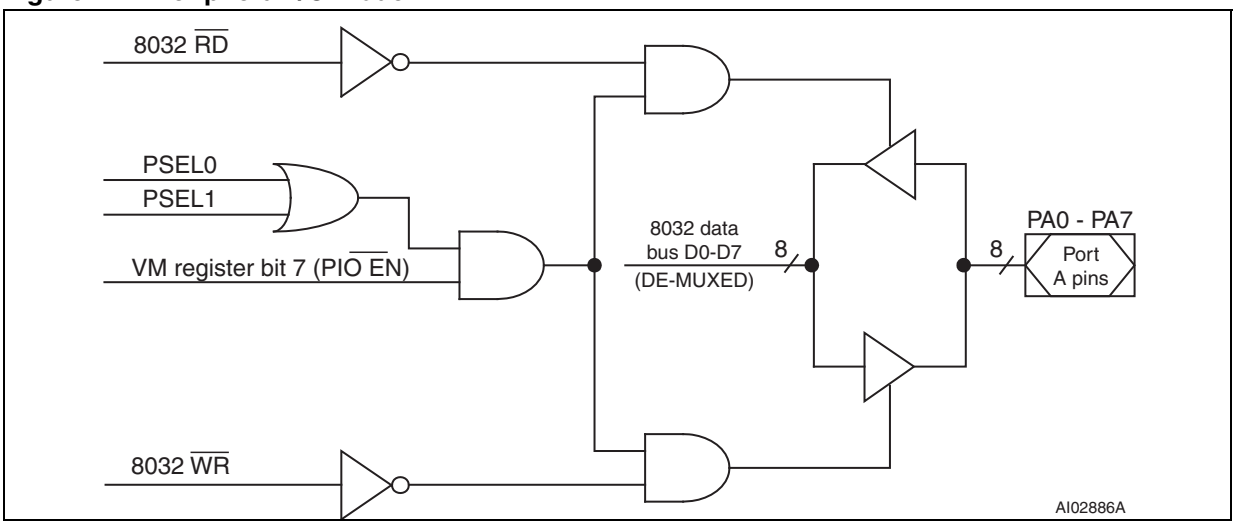
1. For each bit, 1 = drive demuxed 8032 address signal on pin, 0 = pin is default mode, MCU I/O
2. Default state for register is 00h after reset or power-up

27.4.40 Peripheral I/O mode

This mode will provide a data bus repeater function for the 8032 to interface with external parallel peripherals. The mode is only available on Port A (80-pin devices only) and the data bus signals, D0 - D7, are de-multiplexed (no address A0-A7). When active, this mode behaves like a bidirectional buffer, with the direction automatically controlled by the 8032 $\overline{RD}$ and $\overline{WR}$ signals for a specified address range. The DPLD signals PSEL0 and PSEL1 determine this address range. *Figure 68 on page 208* shows the action of Peripheral I/O mode on the Output Enable logic of the tri-state output driver for a single port pin. *Figure 72 on page 215* illustrates data repeater the operation. To activate this mode, choose the pin function “Peripheral I/O mode” in PSDsoft Express on any Port A pin (all eight pins of Port A will automatically change to this mode). Next in PSDsoft, specify an address range for the PSELx signals in the “Chip-Select” section of the “Design Assistant.” Specify an address range for either PSEL0 or PSEL1. Always qualify the PSELx equation with “$\overline{PSEN}$ is logic '1'” to ensure Peripheral I/O mode is only active during 8032 data cycles, not code cycles. Only one equation is needed since PSELx signals are OR’ed together (*Figure 72*). Then in the 8032 initialization firmware, a logic ’1’ is written to the csiop VM register, Bit 7 (PIO_EN) as shown in *Table 109 on page 162*. After this, Port A will automatically perform this repeater function whenever the 8032 presents an address (and memory page number, if paging is used) that is within the range specified by PSELx. Once Port A is designated as Peripheral I/O mode in PSDsoft Express, it cannot be used for other functions.

Note: The user can alternatively connect an external parallel peripheral to the standard 8032 AD0-AD7 pins on an 80-pin UPSD device (not Port A), but these pins have multiplexed address and data signals, with a weaker fanout drive capability.

Figure 72. Peripheral I/O mode



mode, making the pin suitable for input mode (read by the input buffer shown in *Figure 68 on page 208*). *Figure 68* shows the three sources that can control the pin output enable signal: a product term from AND-OR array; the csiop Direction register; or the Peripheral I/O Mode logic (Port A only). The csiop Enable Out registers represent the state of the final output enable signal for each port pin driver, and are defined in *Table 150* through *Table 153*.

Table 146. Port A Pin Drive Select register (address = csiop + offset 08h)(1)(2)(3)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PA7 Open Drain	PA6 Open Drain	PA5 Open Drain	PA4 Open Drain	PA3 Slew Rate	PA2 Slew Rate	PA1 Slew Rate	PA0 Slew Rate

1. Port A not available on 52-pin UPSD33xx devices
2. For each bit, 1 = pin drive type is selected, 0 = pin drive type is default mode, CMOS push/pull
3. Default state for register is 00h after reset or power-up

Table 147. Port B Pin Drive Select register (address = csiop + offset 09h)(1)(2)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PB7 Open Drain	PB6 Open Drain	PB5 Open Drain	PB4 Open Drain	PB3 Slew Rate	PB2 Slew Rate	PB1 Slew Rate	PB0 Slew Rate

1. For each bit, 1 = pin drive type is selected, 0 = pin drive type is default mode, CMOS push/pull
2. Default state for register is 00h after reset or power-up

Table 148. Port C Pin Drive Select register (address = csiop + offset 16h)(1)(2)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PC7 Open Drain	N/A (JTAG)	N/A (JTAG)	PC4 Open Drain	PC3 Open Drain	PC2 Open Drain	N/A (JTAG)	N/A (JTAG)

1. For each bit, 1 = pin drive type is selected, 0 = pin drive type is default mode, CMOS push/pull
2. Default state for register is 00h after reset or power-up

Table 149. Port D Pin Drive Select register (address = csiop + offset 17h)(1)(2)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
N/A	N/A	N/A	N/A	N/A	PD2(3) Slew Rate	PD1 Slew Rate	N/A

1. For each bit, 1 = pin drive type is selected, 0 = pin drive type is default mode, CMOS push/pull
2. Default state for register is 00h after reset or power-up
3. Pin is not available on 52-pin UPSD33xx devices

Table 150. Port A Enable Out register (address = csiop + offset 0Ch)(1)(2)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PA7 OE	PA6 OE	PA5 OE	PA4 OE	PA3 OE	PA2 OE	PA1 OE	PA0 OE

1. For each bit, 1 = pin drive is enabled as an output, 0 = pin drive is off (high-impedance, pin used as input)
2. Port A not available on 52-pin UPSD33xx devices

Table 167. PSD module DC characteristics (with 5 V V_{DD})

Symbol	Parameter		Test condition (in addition to *Table 166 on page 249*)	Min.	Typ.	Max.	Unit
V_{IH}	Input high voltage		4.5 V < V_{DD} < 5.5 V	2		V_{DD} +0.5	V
V_{IL}	Input low voltage		4.5 V < V_{DD} < 5.5 V	–0.5		0.8	V
V_{LKO}	VDD (min) for Flash Erase and Program			2.5		4.2	V
V_{OL}	Output low voltage		I_{OL} = 20 µA, V_{DD} = 4.5 V		0.01	0.1	V
			I_{OL} = 8 mA, V_{DD} = 4.5 V		0.25	0.45	V
V_{OH}	Output high voltage		I_{OH} = –20 µA, V_{DD} = 4.5 V	4.4	4.49		V
			I_{OH} = –2 mA, V_{DD} = 4.5 V	2.4	3.9		V
I_{SB}	Standby supply current for Power-down mode		CSI > V_{DD} – 0.3 V(1)(2)		120	250	µA
I_{LI}	Input leakage current		V_{SS} < V_{IN} < V_{DD}	–1	±0.1	1	µA
I_{LO}	Output leakage current		0.45 < V_{OUT} < V_{DD}	–10	±5	10	µA
I_{CC} (DC)(3)	Operating supply current	PLD only	PLD_TURBO = Off, f = 0 MHz(4)		0		µA/PT
			PLD_TURBO = On, f = 0 MHz		400	700	µA/PT
		Flash memory	During Flash memory WRITE/Erase only		15	30	mA
			Read only, f = 0 MHz		0	0	mA
		SRAM	f = 0 MHz		0	0	mA
I_{CC} (AC)(3)	PLD AC Adder					(4)	
	Flash memory AC Adder				1.5	2.5	mA/MHz
	SRAM AC Adder				1.5	3.0	mA/MHz

1. Internal Power-down mode is active.
2. PLD is in non-Turbo mode, and none of the inputs are switching.
3. I_{OUT} = 0 mA
4. Please see *Figure 84 on page 242* for the PLD current calculation.

Figure 89. Input to output disable / enable

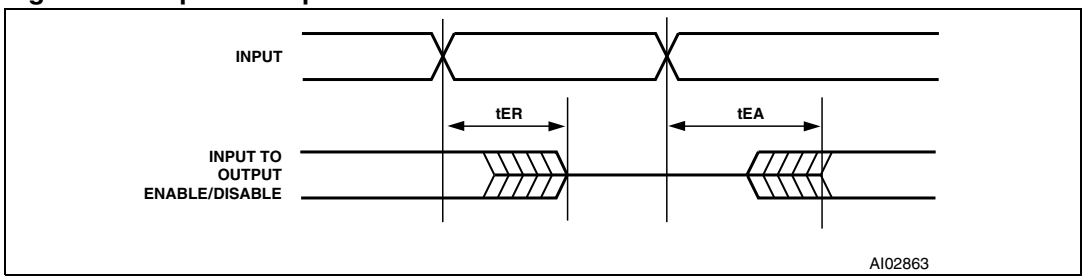


Table 174. CPLD combinatorial timing (5 V PSD module)

Symbol	Parameter	Conditions	Min	Max	PT Aloc	Turbo Off	Slew rate(1)	Unit
t_{PD}(2)	CPLD input pin/feedback to CPLD combinatorial output			20	+ 2	+ 10	– 2	ns
t_{EA}	CPLD input to CPLD Output Enable			21		+ 10	– 2	ns
t_{ER}	CPLD Input to CPLD Output Disable			21		+ 10	– 2	ns
t_{ARP}	CPLD register Clear or Preset delay			21		+ 10	– 2	ns
t_{ARPW}	CPLD register Clear or Preset pulse width		10			+ 10		ns
t_{ARD}	CPLD array delay	Any macrocell		11	+ 2			ns

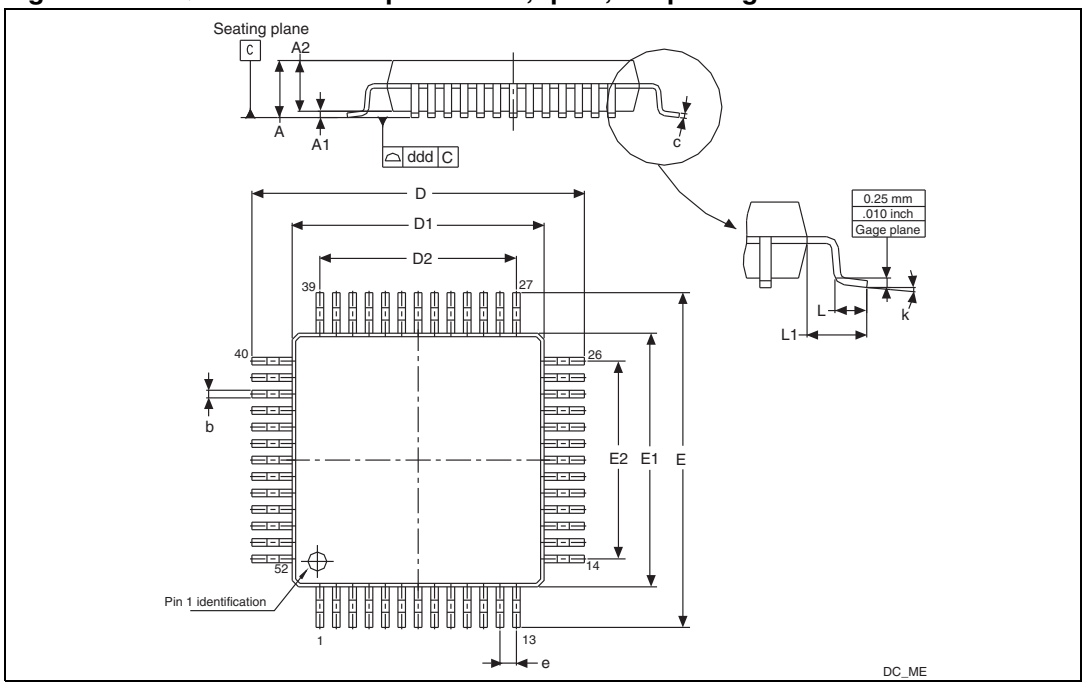
1. Fast Slew Rate output available on PA3-PA0, PB3-PB0, and PD2-PD1. Decrement times by given amount
2. t_{PD} for MCU address and control signals refers to delay from pins on Port 0, Port 2, $\overline{RD}$ $\overline{WR}$, $\overline{PSEN}$ and ALE to CPLD combinatorial output (80-pin package only)

Table 175. CPLD combinatorial timing (3 V PSD module)

Symbol	Parameter	Conditions	Min	Max	PT Aloc	Turbo Off	Slew rate (1)	Unit
t_{PD}(2)	CPLD input pin/feedback to CPLD combinatorial output			35	+ 4	+ 15	– 6	ns
t_{EA}	CPLD input to CPLD Output Enable			38		+15	– 6	ns
t_{ER}	CPLD input to CPLD Output Disable			38		+ 15	– 6	ns
t_{ARP}	CPLD register Clear or Preset delay			35		+ 15	– 6	ns
t_{ARPW}	CPLD register Clear or Preset pulse width		18			+ 15		ns
t_{ARD}	CPLD Array Delay	Any macrocell		20	+ 4			ns

1. Fast Slew Rate output available on PA3-PA0, PB3-PB0, and PD2-PD1. Decrement times by given amount
2. t_{PD} for MCU address and control signals refers to delay from pins on Port 0, Port 2, $\overline{RD}$ $\overline{WR}$, $\overline{PSEN}$ and ALE to CPLD combinatorial output (80-pin package only)

Figure 102. LQFP52 – 52-lead plastic thin, quad, flat package outline



1. Drawing not to scale.

Table 191. LQFP52 – 52-lead plastic thin, quad, flat package mechanical data

Symbol	millimeters			inches[1]		
	Typ	Min	Max	Typ	Min	Max
A			1.60			0.063
A1		0.05	0.15		0.002	0.0059
A2		1.35	1.45		0.0531	0.0571
b		0.22	0.38		0.0087	0.015
C		0.09	0.2		0.0035	0.0079
D	12			0.4724		
D1	10			0.3937		
D2	7.8			0.3071		
E	12			0.4724		
E1	10			0.3937		
E2	7.8			0.3071		
e	0.65			0.0256		
L		0.45	0.75		0.0177	0.0295
L1	1			0.0394		
k		0°	7°		0°	7°
ddd	0.100			0.0039		

1. Values in inches are converted from mm and rounded to 4 decimal digits.