Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	8032
Core Size	8-Bit
Speed	40MHz
Connectivity	I²C, IrDA, SPI, UART/USART
Peripherals	LVD, POR, PWM, WDT
Number of I/O	45
Program Memory Size	160KB (160K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/upsd3333dv-40u6t

The user can also block an input signal coming from pin PC7 to the PLD input bus if desired by writing to Bit 6 of PMMR2.

27.4.61 Blocking common clock, CLKIN

The input CLKIN (from pin PD1) can be blocked to reduce current consumption. CLKIN is used as a common clock input to all OMC flip-flips, it is a general input to the PLD input bus, and it is used to clock the APD counter. In PSDsoft Express, the function of pin PD1 must be specified as “Common Clock Input, CLKIN” before programming the device with JTAG to get the CLKIN function.

Bit 4 of PMMR0 can be set to logic ’1’ to block CLKIN from reaching the PLD input bus, but CLKIN will still reach the APD counter.

Bit 5 of PMMR0 can be set to logic ’1’ to block CLKIN from reaching the OMC flip-flops only, but CLKIN is still available to the PLD input bus and the APD counter.

See Table 154 on page 225 for details.

27.5 PSD module reset conditions

The PSD module receives a reset signal from the MCU module. This reset signal is referred to as the “$\overline{\text{RST}}$” input in PSD module documentation, and it is active-low when asserted. The character of the $\overline{\text{RST}}$ signal generated from the MCU module is described in Section 19: Supervisory functions on page 89.

Upon power-up, and while $\overline{\text{RST}}$ is asserted, the PSD module immediately loads its configuration from non-volatile bits to configure the PLDs and other items. PLD logic is operational and ready for use well before $\overline{\text{RST}}$ is de-asserted. The state of PLD outputs are determined by equations specified in PSDsoft Express.

The Flash memories are reset to Read Array mode after any assertion of $\overline{\text{RST}}$ (even if a program or erase operation is occurring).

Flash memory WRITE operations are automatically prevented while V_{DD} is ramping up until it rises above the V_{LKO} voltage threshold at which time Flash memory WRITE operations are allowed.

Once the UPSD33xx is up and running, any subsequent reset operation is referred to as a warm reset, until power is turned off again. Some PSD module functions are reset in different ways depending if the reset condition was caused from a power-up reset or a warm reset. Table 158 on page 233 summarizes how PSD module functions are affected by power-up and warm resets, as well as the affect of PSD module power-down mode (from APD).

The I/O pins of PSD module Ports A, B, C, and D do not have weak internal pull-ups.

In MCU I/O mode, Latched Address Out mode, and Peripheral I/O mode, the pins of Ports A, B, C, and D become standard CMOS inputs during a reset condition. If no external devices are driving these pins during reset, then these inputs may float and draw excessive current. If low power consumption is critical during reset, then these floating inputs should be pulled up externally to V_{DD} with a weak (100KΩ minimum) resistor.

In PLD I/O mode, pins of Ports A, B, C, and D may also float during reset if no external device is driving them, and if there is no equation specified for the DPLD or GPLD to make

27.5.5 6-pin JTAG ISP (optional)

The optional signals TSTAT and $\overline{\text{TERR}}$ are programming status flags that can reduce programming time by as much as 30% compared to 4-pin JTAG because this status information does not have to be scanned out of the device serially. TSTAT and $\overline{\text{TERR}}$ must be used as a pair for 6-pin JTAG operation.

TSTAT (pin PC3) indicates when programming of a single Flash location is complete. Logic 1 = Ready, Logic 0 = busy.

$\overline{\text{TERR}}$ (pin PC4) indicates if there was a Flash programming error. Logic 1 = no error, Logic 0 = error.

The pin functions for PC3 and PC4 must be selected as “Dedicated JTAG - TSTAT” and “Dedicated JTAG - $\overline{\text{TERR}}$” in PSDsoft Express to enable 6-pin JTAG ISP.

No 8032 firmware is needed to use 6-pin ISP because all ISP functions are controlled from the external JTAG program/test equipment.

TSTAT and $\overline{\text{TERR}}$ are functional only when JTAG ISP operations are occurring, which means they are non-functional during JTAG debugging of the 8032 on the MCU module.

Programming times vary depending on the number of locations to be programmed and the JTAG programming equipment, but typical JTAG ISP programming times are 10 to 25 seconds using 6-pin JTAG. The signals TSTAT and $\overline{\text{TERR}}$ are not included in the IEEE 1149.1 specification.

Figure 81 shows recommended connections on a circuit board to a JTAG program/test tool using 6-pin JTAG. It is required to connect the $\overline{\text{RST}}$ output signal from the JTAG program/test equipment to the $\overline{\text{RESET\_IN}}$ input on the UPSD33xx. The $\overline{\text{RST}}$ signal is driven by the equipment with an Open Drain driver, allowing other sources (like a push button) to drive $\overline{\text{RESET\_IN}}$ without conflict.

Note: The recommended pull-up resistors and decoupling capacitor are illustrated in Figure 81.

Table 165. Major parameters

Parameter	Test conditions/comments	5.0 V value	3.3 V value	Unit
Operating voltage	–	4.5 to 5.5 (PSD); 3.0 to 3.6 (MCU)	3.0 to 3.6 (PSD and MCU)	V
Operating temperature	–	–40 to 85	–40 to 85	°C
MCU frequency	8 MHz (min) for I^2C	1 Min, 40 Max	1 Min, 40 Max	MHz
Typical Active current (20% of PLD used; 25 °C operation)	40 MHz crystal, Turbo	50	40	mA
	40 MHz crystal, Non-Turbo	48	38	mA
	8 MHz crystal, Turbo	21	18	mA
	8 MHz crystal, Non-Turbo	10	8	mA
Typical Idle current (20% of PLD used; 25 °C operation)	40 MHz crystal divided by 2048 internally. All interfaces are disabled.	16	11	mA
Typical Standby current	Power-down mode needs reset to exit.	140	120	µA
I/O sink/source current, Ports A, B, C, and D	V_{OL} = 0.45 V (max); V_{OH} = 2.4 V (min)	I_{OL} = 8 (max); I_{OH} = –2 (min)	I_{OL} = 4 (max); I_{OH} = –1 (min)	mA
I/O sink/source current, Port 4	V_{OL} = 0.6 V (max); V_{OH} = 2.4 V (min)	I_{OL} = 10 (max); I_{OH} = –10 (min)	I_{OL} = 10 (max); I_{OH} = –10 (min)	mA
PLD macrocells	For registered or combinatorial logic	16	16	–
PLD inputs	Inputs from pins, feedback, or MCU addresses	69	69	–
PLD Outputs	Output to pins or internal feedback	18	18	–
Typical PLD propagation delay, Turbo mode	PLD input to output	15	22	ns