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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Discontinued at Digi-Key
Core Processor	ARM® Cortex®-M4/M0/M0
Core Size	32-Bit Tri-Core
Speed	204MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, IrDA, SD, SPI, SSC, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, I²S, LCD, POR, PWM, WDT
Number of I/O	49
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	282K x 8
Voltage - Supply (Vcc/Vdd)	2.2V ~ 3.6V
Data Converters	A/D 3x12b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TFBGA
Supplier Device Package	100-TFBGA (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc4370fet100e

Table 3. Pin description

LCD, Ethernet, USB0, and USB1 functions are not available on all parts. See Table 2.

Symbol	LBGA256	TFBGA100		Reset state [2]	Type	Description
Multiplexed digital pins						
P0_0	L3	G2	[3]	I; PU	I/O	**GPIO0[0] —** General purpose digital input/output pin.
					I/O	**SSP1_MISO —** Master In Slave Out for SSP1.
					I	**ENET_RXD1 —** Ethernet receive data 1 (RMII/MII interface).
					I/O	**SGPIO0 —** General purpose digital input/output pin.
					-	**R —** Function reserved.
					-	**R —** Function reserved.
					I/O	**I2S0_TX_WS —** Transmit Word Select. It is driven by the master and received by the slave. Corresponds to the signal WS in the *I^2S-bus specification*.
					I/O	**I2S1_TX_WS —** Transmit Word Select. It is driven by the master and received by the slave. Corresponds to the signal WS in the *I^2S-bus specification*.
P0_1	M2	G1	[3]	I; PU	I/O	**GPIO0[1] —** General purpose digital input/output pin.
					I/O	**SSP1_MOSI —** Master Out Slave in for SSP1.
					I	**ENET_COL —** Ethernet Collision detect (MII interface).
					I/O	**SGPIO1 —** General purpose digital input/output pin.
					-	**R —** Function reserved.
					-	**R —** Function reserved.
						ENET_TX_EN — Ethernet transmit enable (RMII/MII interface).
					I/O	**I2S1_TX_SDA —** I2S1 transmit data. It is driven by the transmitter and read by the receiver. Corresponds to the signal SD in the *I^2S-bus specification*.
P1_0	P2	H1	[3]	I; PU	I/O	**GPIO0[4] —** General purpose digital input/output pin.
					I	**CTIN_3 —** SCT input 3. Capture input 1 of timer 1.
					I/O	**EMC_A5 —** External memory address line 5.
					-	**R —** Function reserved.
					-	**R —** Function reserved.
					I/O	**SSP0_SSEL —** Slave Select for SSP0.
					I/O	**SGPIO7 —** General purpose digital input/output pin.
					-	**R —** Function reserved.
P1_1	R2	K2	[3]	I; PU	I/O	**GPIO0[8] —** General purpose digital input/output pin. Boot pin (see Table 5).
					O	**CTOUT_7 —** SCT output 7. Match output 3 of timer 1.
					I/O	**EMC_A6 —** External memory address line 6.
					I/O	**SGPIO8 —** General purpose digital input/output pin.
					-	**R —** Function reserved.
					I/O	**SSP0_MISO —** Master In Slave Out for SSP0.
					-	**R —** Function reserved.
					-	**R —** Function reserved.

Table 3. Pin description *…continued*

LCD, Ethernet, USB0, and USB1 functions are not available on all parts. See Table 2.

Symbol	LBGA256	TFBGA100		Reset state [2]	Type	Description
P4_2	D3	-	[3]	I; PU	I/O	**GPIO2[2] —** General purpose digital input/output pin.
					O	**CTOUT_0 —** SCT output 0. Match output 0 of timer 0.
					O	**LCD_VD3 —** LCD data.
					-	**R —** Function reserved.
					-	**R —** Function reserved.
					O	**LCD_VD12 —** LCD data.
					I	**U3_RXD —** Receiver input for USART3.
					I/O	**SGPIO8 —** General purpose digital input/output pin.
P4_3	C2	-	[6] [13]	I; PU	I/O	**GPIO2[3] —** General purpose digital input/output pin.
					O	**CTOUT_3 —** SCT output 3. Match output 3 of timer 0.
					O	**LCD_VD2 —** LCD data.
					-	**R —** Function reserved.
					-	**R —** Function reserved.
					O	**LCD_VD21 —** LCD data.
					I/O	**U3_BAUD —** Baud pin for USART3.
					I/O	**SGPIO9 —** General purpose digital input/output pin.
					AI	**ADC0_0 —** ADC0, input channel 0. Configure the pin as GPIO input and use the ADC function select register in the SCU to select the ADC.
P4_4	B1	-	[6]	I; PU	I/O	**GPIO2[4] —** General purpose digital input/output pin.
					O	**CTOUT_2 —** SCT output 2. Match output 2 of timer 0.
					O	**LCD_VD1 —** LCD data.
					-	**R —** Function reserved.
					-	**R —** Function reserved.
					O	**LCD_VD20 —** LCD data.
					I/O	**U3_DIR —** RS-485/EIA-485 output enable/direction control for USART3.
					I/O	**SGPIO10 —** General purpose digital input/output pin.
					O	**DAC —** DAC output. Configure the pin as GPIO input and use the analog function select register in the SCU to select the DAC.
P4_5	D2	-	[3]	I; PU	I/O	**GPIO2[5] —** General purpose digital input/output pin.
					O	**CTOUT_5 —** SCT output 5. Match output 1 of timer 1.
					O	**LCD_FP —** Frame pulse (STN). Vertical synchronization pulse (TFT).
					-	**R —** Function reserved.
					-	**R —** Function reserved.
					-	**R —** Function reserved.
					-	**R —** Function reserved.
					I/O	**SGPIO11 —** General purpose digital input/output pin.

Table 3. Pin description *…continued*

LCD, Ethernet, USB0, and USB1 functions are not available on all parts. See Table 2.

Symbol	LBGA256	TFBGA100		Reset state [2]	Type	Description
P4_6	C1	-	[3]	I; PU	I/O	**GPIO2[6] —** General purpose digital input/output pin.
					O	**CTOUT_4 —** SCT output 4. Match output 0 of timer 1.
					O	**LCD_ENAB/LCDM —** STN AC bias drive or TFT data enable input.
					-	**R —** Function reserved.
					-	**R —** Function reserved.
					-	**R —** Function reserved.
					-	**R —** Function reserved.
					I/O	**SGPIO12 —** General purpose digital input/output pin.
P4_7	H4	-	[3]	O; PU	O	**LCD_DCLK —** LCD panel clock.
					I	**GP_CLKIN —** General purpose clock input to the CGU.
					-	**R —** Function reserved.
					-	**R —** Function reserved.
					-	**R —** Function reserved.
					-	**R —** Function reserved.
					I/O	**I2S1_TX_SCK —** Transmit Clock. It is driven by the master and received by the slave. Corresponds to the signal SCK in the I^2S-bus specification.
					I/O	**I2S0_TX_SCK —** Transmit Clock. It is driven by the master and received by the slave. Corresponds to the signal SCK in the I^2S-bus specification.
P4_8	E2	-	[3]	I; PU	-	**R —** Function reserved.
					I	**CTIN_5 —** SCT input 5. Capture input 2 of timer 2.
					O	**LCD_VD9 —** LCD data.
					-	**R —** Function reserved.
					I/O	**GPIO5[12] —** General purpose digital input/output pin.
					O	**LCD_VD22 —** LCD data.
					O	**CAN1_TD —** CAN1 transmitter output.
					I/O	**SGPIO13 —** General purpose digital input/output pin.
P4_9	L2	-	[3]	I; PU	-	**R —** Function reserved.
					I	**CTIN_6 —** SCT input 6. Capture input 1 of timer 3.
					O	**LCD_VD11 —** LCD data.
					-	**R —** Function reserved.
					I/O	**GPIO5[13] —** General purpose digital input/output pin.
					O	**LCD_VD15 —** LCD data.
					I	**CAN1_RD —** CAN1 receiver input.
					I/O	**SGPIO14 —** General purpose digital input/output pin.

Table 3. Pin description *…continued*

LCD, Ethernet, USB0, and USB1 functions are not available on all parts. See Table 2.

Symbol	LBGA256	TFBGA100		Reset state [2]	Type	Description
P4_10	M3	-	[3]	I; PU	-	**R —** Function reserved.
					I	**CTIN_2 —** SCT input 2. Capture input 2 of timer 0.
					O	**LCD_VD10 —** LCD data.
					-	**R —** Function reserved.
					I/O	**GPIO5[14] —** General purpose digital input/output pin.
					O	**LCD_VD14 —** LCD data.
					-	**R —** Function reserved.
					I/O	**SGPIO15 —** General purpose digital input/output pin.
P5_0	N3	-	[3]	I; PU	I/O	**GPIO2[9] —** General purpose digital input/output pin.
					O	**MCOB2 —** Motor control PWM channel 2, output B.
					I/O	**EMC_D12 —** External memory data line 12.
					-	**R —** Function reserved.
					I	**U1_DSR —** Data Set Ready input for UART 1.
					I	**T1_CAP0 —** Capture input 0 of timer 1.
					-	**R —** Function reserved.
					-	**R —** Function reserved.
P5_1	P3	-	[3]	I; PU	I/O	**GPIO2[10] —** General purpose digital input/output pin.
					I	**MCI2 —** Motor control PWM channel 2, input.
					I/O	**EMC_D13 —** External memory data line 13.
					-	**R —** Function reserved.
					O	**U1_DTR —** Data Terminal Ready output for UART 1. Can also be configured to be an RS-485/EIA-485 output enable signal for UART 1.
					I	**T1_CAP1 —** Capture input 1 of timer 1.
					-	**R —** Function reserved.
					-	**R —** Function reserved.
P5_2	R4	-	[3]	I; PU	I/O	**GPIO2[11] —** General purpose digital input/output pin.
					I	**MCI1 —** Motor control PWM channel 1, input.
					I/O	**EMC_D14 —** External memory data line 14.
					-	**R —** Function reserved.
					O	**U1_RTS —** Request to Send output for UART 1. Can also be configured to be an RS-485/EIA-485 output enable signal for UART 1.
					I	**T1_CAP2 —** Capture input 2 of timer 1.
					-	**R —** Function reserved.
					-	**R —** Function reserved.

Table 3. Pin description *…continued*

LCD, Ethernet, USB0, and USB1 functions are not available on all parts. See Table 2.

Symbol	LBGA256	TFBGA100		Reset state [2]	Type	Description
PC_10	M5	-	[3]	I; PU	-	**R —** Function reserved.
					O	**USB1_ULPI_STP —** ULPI link STP signal. Asserted to end or interrupt transfers to the PHY.
					I	**U1_DSR —** Data Set Ready input for UART 1.
					-	**R —** Function reserved.
					I/O	**GPIO6[9] —** General purpose digital input/output pin.
					-	**R —** Function reserved.
					O	**T3_MAT3 —** Match output 3 of timer 3.
					I/O	**SD_CMD —** SD/MMC command signal.
PC_11	L5	-	[3]	I; PU	-	**R —** Function reserved.
					I	**USB1_ULPI_DIR —** ULPI link DIR signal. Controls the ULPI data line direction.
					I	**U1_DCD —** Data Carrier Detect input for UART 1.
					-	**R —** Function reserved.
					I/O	**GPIO6[10] —** General purpose digital input/output pin.
					-	**R —** Function reserved.
					-	**R —** Function reserved.
					I/O	**SD_DAT4 —** SD/MMC data bus line 4.
PC_12	L6	-	[3]	I; PU	-	**R —** Function reserved.
					-	**R —** Function reserved.
					O	**U1_DTR —** Data Terminal Ready output for UART 1. Can also be configured to be an RS-485/EIA-485 output enable signal for UART 1.
					-	**R —** Function reserved.
					I/O	**GPIO6[11] —** General purpose digital input/output pin.
					I/O	**SGPIO11 —** General purpose digital input/output pin.
					I/O	**I2S0_TX_SDA —** I2S transmit data. It is driven by the transmitter and read by the receiver. Corresponds to the signal SD in the *I^2S-bus specification*.
					I/O	**SD_DAT5 —** SD/MMC data bus line 5.
PC_13	M1	-	[3]	I; PU	-	**R —** Function reserved.
					-	**R —** Function reserved.
					O	**U1_TXD —** Transmitter output for UART 1.
					-	**R —** Function reserved.
					I/O	**GPIO6[12] —** General purpose digital input/output pin.
					I/O	**SGPIO12 —** General purpose digital input/output pin.
					I/O	**I2S0_TX_WS —** Transmit Word Select. It is driven by the master and received by the slave. Corresponds to the signal WS in the *I^2S-bus specification*.
					I/O	**SD_DAT6 —** SD/MMC data bus line 6.

Table 3. Pin description *…continued*

LCD, Ethernet, USB0, and USB1 functions are not available on all parts. See Table 2.

Symbol	LBGA256	TFBGA100		Reset state [2]	Type	Description
PC_14	N1	-	[3]	I; PU	-	**R —** Function reserved.
					-	**R —** Function reserved.
					I	**U1_RXD —** Receiver input for UART 1.
					-	**R —** Function reserved.
					I/O	**GPIO6[13] —** General purpose digital input/output pin.
					I/O	**SGPIO13 —** General purpose digital input/output pin.
					O	**ENET_TX_ER —** Ethernet Transmit Error (MII interface).
					I/O	**SD_DAT7 —** SD/MMC data bus line 7.
PD_0	N2	-	[3]	I; PU	-	**R —** Function reserved.
					O	**CTOUT_15 —** SCT output 15. Match output 3 of timer 3.
					O	**EMC_DQMOUT2 —** Data mask 2 used with SDRAM and static devices.
					-	**R —** Function reserved.
					I/O	**GPIO6[14] —** General purpose digital input/output pin.
					-	**R —** Function reserved.
					-	**R —** Function reserved.
					I/O	**SGPIO4 —** General purpose digital input/output pin.
PD_1	P1	-	[3]	I; PU	-	**R —** Function reserved.
					-	**R —** Function reserved.
					O	**EMC_CKEOUT2 —** SDRAM clock enable 2.
					-	**R —** Function reserved.
					I/O	**GPIO6[15] —** General purpose digital input/output pin.
					O	**SD_POW —** SD/MMC power monitor output.
					-	**R —** Function reserved.
					I/O	**SGPIO5 —** General purpose digital input/output pin.
PD_2	R1	-	[3]	I; PU	-	**R —** Function reserved.
					O	**CTOUT_7 —** SCT output 7. Match output 3 of timer 1.
					I/O	**EMC_D16 —** External memory data line 16.
					-	**R —** Function reserved.
					I/O	**GPIO6[16] —** General purpose digital input/output pin.
					-	**R —** Function reserved.
					-	**R —** Function reserved.
					I/O	**SGPIO6 —** General purpose digital input/output pin.

One of the two SRAM blocks connected to the subsystem AHB matrix is typically used for code running on the M0 subsystem and the other SRAM block for data. This allows other bus masters to access the data SRAM without interrupting the M0 processor instruction fetches and thereby stalling the M0 subsystem.

The M0 subsystem matrix runs at an asynchronous speed from the main matrix. This allows to operate the SGPIO at any desired frequency. The M0 subsystem can control the SGPIO in a deterministic way, without incurring latency that occurs when the M4 controls the SGPIO through a bridge.

7.4 Interprocessor communication

The ARM Cortex-M4 and ARM Cortex-M0 interprocessor communication is based on using shared SRAM as mailbox and one processor raising an interrupt on the other processor's NVIC, for example after it has delivered a new message in the mailbox. The receiving processor can reply by raising an interrupt on the sending processor's NVIC to acknowledge the message.

- Extended wait

- Four chip selects for synchronous memory and four chip selects for static memory devices.
- Power-saving modes dynamically control EMC_CKEOUT and EMC_CLK signals to SDRAMs.
- Dynamic memory self-refresh mode controlled by software.
- Controller supports 2048 (A0 to A10), 4096 (A0 to A11), and 8192 (A0 to A12) row address synchronous memory parts. That is typical 512 MB, 256 MB, and 128 MB parts, with 4, 8, 16, or 32 data bits per device.
- Separate reset domains allow the for auto-refresh through a chip reset if desired.
- SDRAM clock can run at full or half the Cortex-M4 core frequency.

Note: Synchronous static memory devices (synchronous burst mode) are not supported.

7.18.5 High-speed USB Host/Device/OTG interface (USB0)

The USB OTG module allows the LPC4370 to connect directly to a USB Host such as a PC (in device mode) or to a USB Device in host mode.

7.18.5.1 Features

- Contains UTMI+ compliant transceiver (PHY).
- Complies with *Universal Serial Bus specification 2.0*.
- Complies with *USB On-The-Go supplement*.
- Complies with *Enhanced Host Controller Interface Specification*.
- Supports auto USB 2.0 mode discovery.
- Supports all high-speed USB-compliant peripherals.
- Supports all full-speed USB-compliant peripherals.
- Supports software Host Negotiation Protocol (HNP) and Session Request Protocol (SRP) for OTG peripherals.
- Supports interrupts.
- This module has its own, integrated DMA engine.
- USB interface electrical test software included in ROM USB stack.

7.18.6 High-speed USB Host/Device interface with ULPI (USB1)

The USB1 interface can operate as a full-speed USB Host/Device interface or can connect to an external ULPI PHY for High-speed operation.

7.18.6.1 Features

- Complies with *Universal Serial Bus specification 2.0*.
- Complies with *Enhanced Host Controller Interface Specification*.
- Supports auto USB 2.0 mode discovery.
- Supports all high-speed USB-compliant peripherals if connected to external ULPI PHY.
- Supports all full-speed USB-compliant peripherals.

- Flag to indicate watchdog reset.
- Programmable 24-bit timer with internal prescaler.
- Selectable time period from ($T_{cy(WDCLK)} \times 256 \times 4$) to ($T_{cy(WDCLK)} \times 2^{24} \times 4$) in multiples of $T_{cy(WDCLK)} \times 4$.

7.21 Analog peripherals

7.21.1 12-bit high-speed Analog-to-Digital Converter (ADCHS)

7.21.1.1 Features

- 12-bit high-speed ADC.
- Six single-sided input channels or one differential input channel.
- Descriptor based conversion sequence for single or multiple inputs.
- Integrated 14-bit timer.
- Automatic high/low threshold detection.
- Power-down mode.
- Measurement range of 0 V to 1.2 V.
- 12-bit conversion rate of 80 MSamples/s.
- Conversion on transition on input pin or various internal signals.
- Output FIFO with DMA support.

7.21.2 10-bit Analog-to-Digital Converter (ADC0/1)

7.21.2.1 Features

- 10-bit successive approximation analog to digital converter.
- Input multiplexing among 8 pins per ADC for a total of 16 individual channels.
- Power-down mode.
- Measurement range 0 to VDDA.
- Sampling frequency up to 400 kSamples/s.
- Burst conversion mode for single or multiple inputs.
- Optional conversion on transition on ADCTRIG0 or ADCTRIG1 pins, combined timer outputs 8 or 15, or the PWM output MCOA2.
- Individual result registers for each A/D channel to reduce interrupt overhead.
- DMA support.

7.21.3 Digital-to-Analog Converter (DAC)

7.21.3.1 Features

- 10-bit resolution
- Monotonic by design (resistor string architecture)
- Controllable conversion speed
- Low power consumption

Wake-up from the Power-down modes, Deep-sleep, Power-down, and Deep power-down, is caused by an event on the WAKEUP pins or an event from the RTC or alarm timer.

When waking up from Deep power-down mode, the part resets and attempts to boot. After booting, the M4 core is in active mode and both M0 cores remain in the reset state until the reset is released by software.

7.24 Serial Wire Debug/JTAG

Debug and trace functions are integrated into the ARM Cortex-M4. Serial wire debug and trace functions are supported in addition to a standard JTAG debug and parallel trace functions. The ARM Cortex-M4 is configured to support up to eight breakpoints and four watch points.

The ARM Cortex-M0 coprocessors support JTAG boundary scan only.

10. Static characteristics

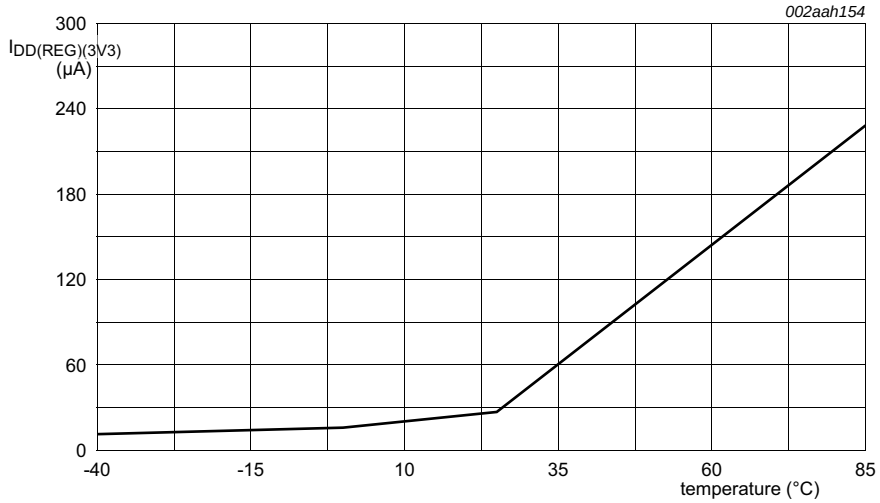
Table 10. Static characteristics

T_{amb} = −40 °C to +85 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
Supply pins							
$V_{DD(IO)}$	input/output supply voltage			2.2	-	3.6	V
$V_{DD(REG)(3V3)}$	regulator supply voltage (3.3 V)		[2]	2.2	-	3.6	V
$V_{DDA(3V3)}$	analog supply voltage (3.3 V)	on pin VDDA		2.2	-	3.6	V
		on pins USB0_VDDA3V3_ DRIVER and USB0_VDDA3V3		3.0	3.3	3.6	V
V_{BAT}	battery supply voltage		[2]	2.2	-	3.6	V
$V_{prog(pf)}$	polyfuse programming voltage	on pin VPP (for OTP)	[3]	2.7	-	3.6	V
$I_{prog(pf)}$	polyfuse programming current	on pin VPP; OTP programming time ≤ 1.6 ms		-	-	30	mA
$I_{DD(REG)(3V3)}$	regulator supply current (3.3 V)	Active mode; M0 cores in reset; code `while(1){}` executed from RAM; all peripherals disabled; PLL1 enabled					
		CCLK = 12 MHz	[4]	-	6.6	-	mA
		CCLK = 60 MHz	[4]		25.3	-	mA
		CCLK = 120 MHz	[4]	-	48.4	-	mA
		CCLK = 180 MHz	[4]	-	72.0	-	mA
		CCLK = 204 MHz	[4]	-	81.5	-	mA
$I_{DD(REG)(3V3)}$	regulator supply current (3.3 V)	after WFE/WFI instruction executed from RAM; all peripherals disabled;M0 cores in reset					
		sleep mode	[4][5]	-	5.0	-	mA
		deep-sleep mode	[4]	-	30	-	µA
		power-down mode	[4]	-	15	-	µA
		power-down mode with M0SUB SRAM retained	[4]	-	20	-	µA
		deep power-down mode	[4][6]	-	0.03	-	µA
		deep power-down mode; VBAT floating	[4]	-	2	-	µA
I_{BAT}	battery supply current	active mode; V_{BAT} = 3.2 V; $V_{DD(REG)(3V3)}$ = 3.6 V.	[7]	-	0	-	nA

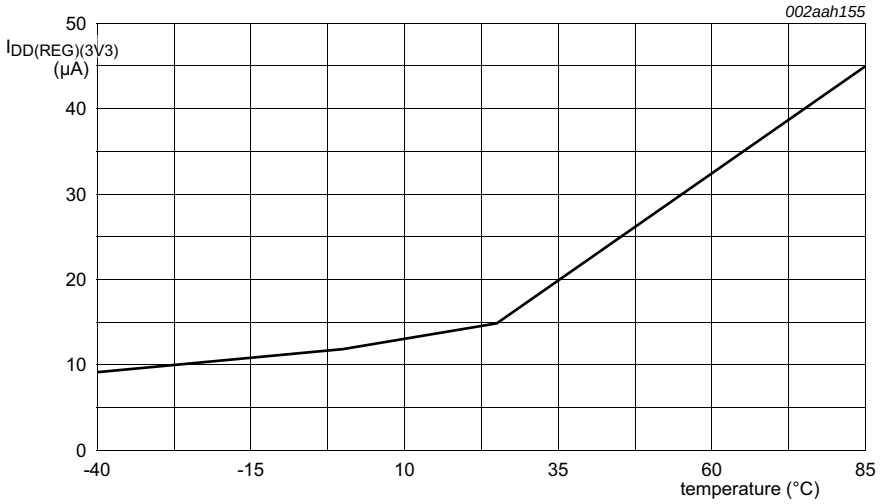
Table 10. Static characteristics *…continued*
T_{amb} = −40 °C to +85 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
V_{hys}	hysteresis voltage			0.1 × $V_{DD(IO)}$	-	-	V
V_{OL}	LOW-level output voltage	I_{OLS} = 3 mA		-	-	0.4	V
I_{LI}	input leakage current	$V_I = V_{DD(IO)}$	[13]	-	4.5	-	μA
		V_I = 5 V		-	-	10	μA
Oscillator pins							
$V_{i(XTAL1)}$	input voltage on pin XTAL1			−0.5	-	1.2	V
$V_{o(XTAL2)}$	output voltage on pin XTAL2			−0.5	-	1.2	V
C_{io}	input/output capacitance		[17]	-	-	0.8	pF
USB0 pins[18]							
V_I	input voltage	on pins USB0_DP; USB0_DM; USB0_VBUS					
		$V_{DD(IO)} \geq 2.2$ V		0	-	5.25	V
		$V_{DD(IO)}$ = 0 V		0	-	3.6	V
R_{pd}	pull-down resistance	on pin USB0_VBUS		48	64	80	kΩ
V_{IC}	common-mode input voltage	high-speed mode		−50	200	500	mV
		full-speed/low-speed mode		800	-	2500	mV
		chirp mode		−50	-	600	mV
$V_{i(dif)}$	differential input voltage			100	400	1100	mV
USB1 pins (USB1_DP/USB1_DM)[18]							
I_{OZ}	OFF-state output current	0 V < V_I < 3.3 V	[18]	-	-	±10	μA
V_{BUS}	bus supply voltage		[19]	-	-	5.25	V
V_{DI}	differential input sensitivity voltage	|(D+) − (D−)|		0.2	-	-	V
V_{CM}	differential common mode voltage range	includes V_{DI} range		0.8	-	2.5	V
$V_{th(rs)se}$	single-ended receiver switching threshold voltage			0.8	-	2.0	V
V_{OL}	LOW-level output voltage for low-/full-speed	R_L of 1.5 kΩ to 3.6 V		-	-	0.18	V



Conditions: $V_{DD(REG)(3V3)}$ = 3.3 V; V_{BAT} floating; $V_{DD(IO)}$ = 3.3 V.

Fig 12. Typical supply current versus temperature in Deep-sleep mode



Conditions: $V_{DD(REG)(3V3)}$ = 3.3 V; V_{BAT} floating; $V_{DD(IO)}$ = 3.3 V.

Fig 13. Typical supply current versus temperature in Power-down mode

11.10 USART interface

Table 24. USART dynamic characteristics

T_{amb} = −40 °C to 85 °C; 2.2 V ≤ $V_{DD(REG)(3V3)}$ ≤ 3.6 V; 2.7 V ≤ $V_{DD(IO)}$ ≤ 3.6 V; C_L = 20 pF. EHS = 1 for all pins. Simulated values.

Symbol	Parameter	Min	Max	Unit
USART master (in synchronous mode)				
$t_{su(D)}$	data input set-up time	26.6	-	ns
$t_{h(D)}$	data input hold time	0	-	ns
$t_{v(Q)}$	data output valid time	0	8.8	ns
USART slave (in synchronous mode)				
$t_{su(D)}$	data input set-up time	1.2	-	ns
$t_{h(D)}$	data input hold time	0.4	-	ns
$t_{v(Q)}$	data output valid time	5.5	24	ns

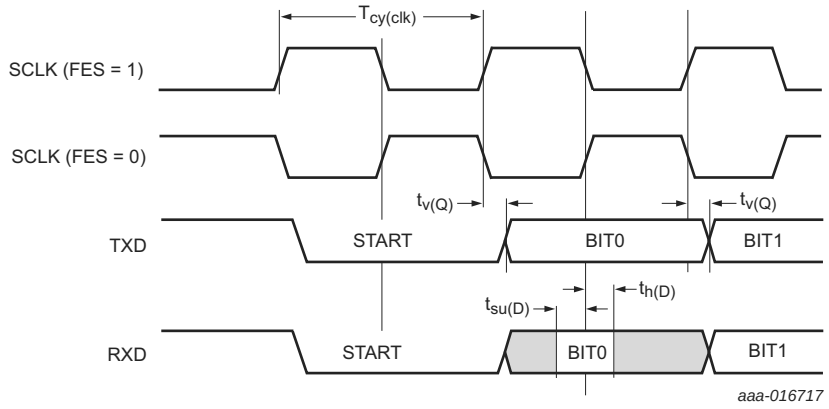


Fig 27. USART timing

11.12 SPI interface

Table 26. Dynamic characteristics: SPI

T_{amb} = −40 °C to +85 °C; 2.2 V ≤ $V_{DD(REG)(3V3)}$ ≤ 3.6 V; 2.7 V ≤ $V_{DD(IO)}$ ≤ 3.6 V. Simulated values.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$T_{cy(PCLK)}$	PCLK cycle time			5			ns
$T_{cy(clk)}$	clock cycle time		[1]	40	-	-	ns
Master							
t_{DS}	data set-up time			7.2	-	-	ns
t_{DH}	data hold time			0	-	-	ns
$t_{v(Q)}$	data output valid time			-	-	3.7	ns
$t_{h(Q)}$	data output hold time			-	-	1.2	ns
Slave							
t_{DS}	data set-up time			1.2	-	-	ns
t_{DH}	data hold time			$3 \times T_{cy(PCLK)} + 0.54$	-	-	ns
$t_{v(Q)}$	data output valid time			-	-	$3 \times T_{cy(PCLK)} + 9.7$	ns
$t_{h(Q)}$	data output hold time			-	-	$2 \times T_{cy(PCLK)} + 7.1$	ns

[1] $T_{cy(clk)}$ = 8/BASE_SPI_CLK. $T_{cy(PCLK)}$ = 1/BASE_SPI_CLK.

Table 33. Static characteristics: USB0 PHY pins[1]

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
High-speed mode							
P_{cons}	power consumption		[2]	-	68	-	mW
$I_{DDA(3V3)}$	analog supply current (3.3 V)	on pin USB0_VDDA3V3_DRIVER; total supply current	[3]	-	18	-	mA
		during transmit		-	31	-	mA
		during receive		-	14	-	mA
		with driver tri-stated		-	14	-	mA
I_{DDD}	digital supply current			-	7	-	mA
Full-speed/low-speed mode							
P_{cons}	power consumption		[2]	-	15	-	mW
$I_{DDA(3V3)}$	analog supply current (3.3 V)	on pin USB0_VDDA3V3_DRIVER; total supply current		-	3.5	-	mA
		during transmit		-	5	-	mA
		during receive		-	3	-	mA
		with driver tri-stated		-	3	-	mA
I_{DDD}	digital supply current			-	3	-	mA
Suspend mode							
$I_{DDA(3V3)}$	analog supply current (3.3 V)			-	24	-	μA
		with driver tri-stated		-	24	-	μA
		with OTG functionality enabled		-	3	-	mA
I_{DDD}	digital supply current			-	30	-	μA
VBUS detector outputs							
V_{th}	threshold voltage	for VBUS valid		4.4	-	-	V
		for session end		0.2	-	0.8	V
		for A valid		0.8	-	2	V
		for B valid		2	-	4	V
V_{hys}	hysteresis voltage	for session end		-	150	10	mV
		A valid		-	200	10	mV
		B valid		-	200	10	mV

[1] Characterized but not implemented as production test.

[2] Total average power consumption.

[3] The driver is active only 20 % of the time.

11.18 Ethernet

Remark: The timing characteristics of the ENET_MDC and ENET_MDIO signals comply with the *IEEE standard 802.3*.

13. Application information

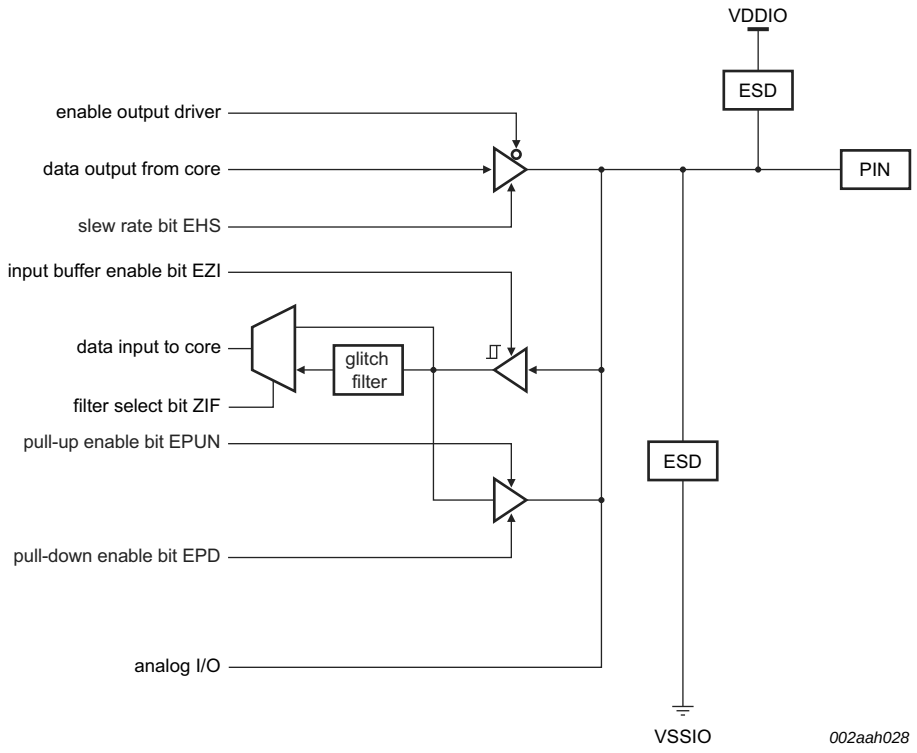
13.1 LCD panel signal usage

Table 40. LCD panel connections for STN single panel mode

External pin	4-bit mono STN single panel		8-bit mono STN single panel		Color STN single panel	
	LPC43xx pin used	LCD function	LPC43xx pin used	LCD function	LPC43xx pin used	LCD function
LCD_VD[23:8]	-	-	-	-	-	-
LCD_VD7	-	-	P8_4	UD[7]	P8_4	UD[7]
LCD_VD6	-	-	P8_5	UD[6]	P8_5	UD[6]
LCD_VD5	-	-	P8_6	UD[5]	P8_6	UD[5]
LCD_VD4	-	-	P8_7	UD[4]	P8_7	UD[4]
LCD_VD3	P4_2	UD[3]	P4_2	UD[3]	P4_2	UD[3]
LCD_VD2	P4_3	UD[2]	P4_3	UD[2]	P4_3	UD[2]
LCD_VD1	P4_4	UD[1]	P4_4	UD[1]	P4_4	UD[1]
LCD_VD0	P4_1	UD[0]	P4_1	UD[0]	P4_1	UD[0]
LCD_LP	P7_6	LCDLP	P7_6	LCDLP	P7_6	LCDLP
LCD_ENAB/ LCDM	P4_6	LCDENAB/ LCDM	P4_6	LCDENAB/ LCDM	P4_6	LCDENAB/ LCDM
LCD_FP	P4_5	LCDFP	P4_5	LCDFP	P4_5	LCDFP
LCD_DCLK	P4_7	LCDDCLK	P4_7	LCDDCLK	P4_7	LCDDCLK
LCD_LE	P7_0	LCDLE	P7_0	LCDLE	P7_0	LCDLE
LCD_PWR	P7_7	CDPWR	P7_7	LCDPWR	P7_7	LCDPWR
GP_CLKIN	PF_4	LCDCLKIN	PF_4	LCDCLKIN	PF_4	LCDCLKIN

Table 41. LCD panel connections for STN dual panel mode

External pin	4-bit mono STN dual panel		8-bit mono STN dual panel		Color STN dual panel	
	LPC43xx pin used	LCD function	LPC43xx pin used	LCD function	LPC43xx pin used	LCD function
LCD_VD[23:16]	-	-	-	-	-	-
LCD_VD15	-	-	PB_4	LD[7]	PB_4	LD[7]
LCD_VD14	-	-	PB_5	LD[6]	PB_5	LD[6]
LCD_VD13	-	-	PB_6	LD[5]	PB_6	LD[5]
LCD_VD12	-	-	P8_3	LD[4]	P8_3	LD[4]
LCD_VD11	P4_9	LD[3]	P4_9	LD[3]	P4_9	LD[3]
LCD_VD10	P4_10	LD[2]	P4_10	LD[2]	P4_10	LD[2]
LCD_VD9	P4_8	LD[1]	P4_8	LD[1]	P4_8	LD[1]
LCD_VD8	P7_5	LD[0]	P7_5	LD[0]	P7_5	LD[0]
LCD_VD7	-	-		UD[7]	P8_4	UD[7]
LCD_VD6	-	-	P8_5	UD[6]	P8_5	UD[6]
LCD_VD5	-	-	P8_6	UD[5]	P8_6	UD[5]
LCD_VD4	-	-	P8_7	UD[4]	P8_7	UD[4]
LCD_VD3	P4_2	UD[3]	P4_2	UD[3]	P4_2	UD[3]



The glitch filter rejects pulses of typical 12 ns width.

Fig 43. Standard I/O pin configuration with analog input

13.6 Reset pin configuration

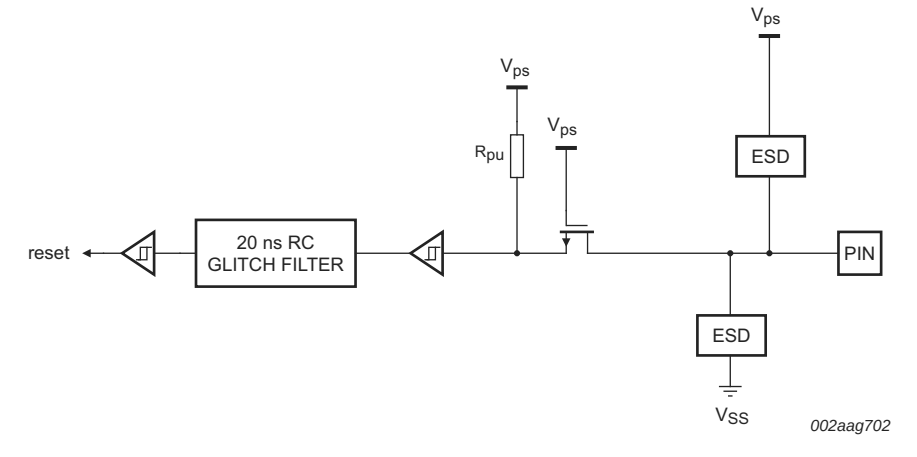


Fig 44. Reset pin configuration

13.7 Suggested USB interface solutions

The USB device can be connected to the USB as self-powered device (see Figure 45) or bus-powered device (see Figure 46).

13.9.3 Non-inverting single-ended circuit for input 0 V to 3.3 V

The advantage of having a non-inverting circuit comes at the cost of adding an additional op-amp for a high-impedance voltage reference to prevent the reference level being influenced by the input signal. This circuit is recommended for an input voltage from 0 V to 3.3 V using the internal negative reference voltage.

(4)

$$Vout = Vcom\frac{R1}{R1 + R2}$$

(5)

$$Vcom = (1.24\ \mathrm{V})\frac{R3}{R3 + R4}$$

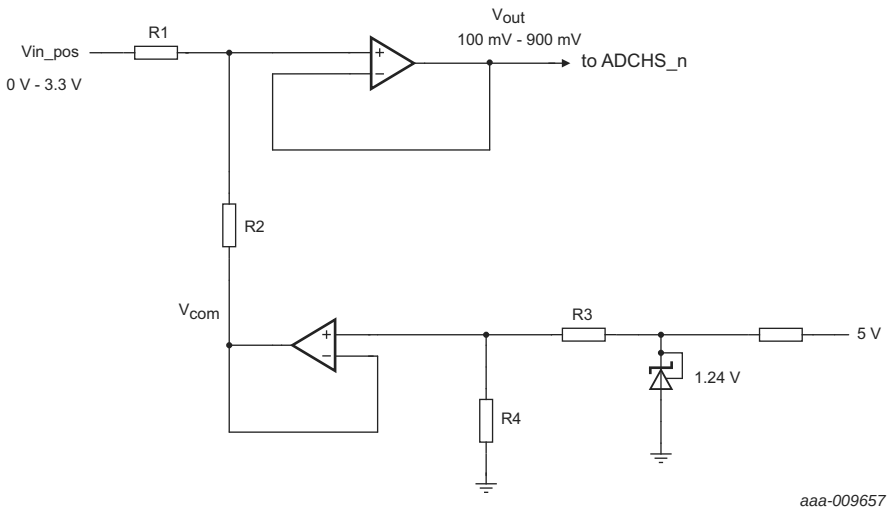
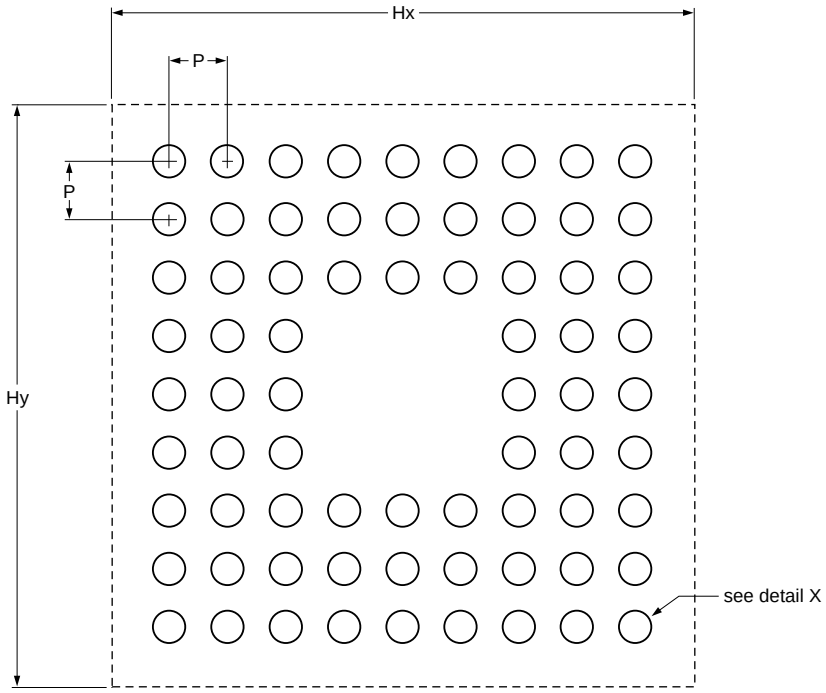


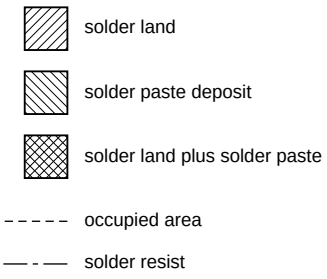
Fig 52. Non-inverting single-ended circuit for input 0 V to 3.3 V for 12-bit ADCHS input

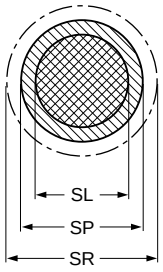
Footprint information for reflow soldering of TFBGA100 package **SOT926-1**



Generic footprint pattern

Refer to the package outline drawing for actual layout





detail X

DIMENSIONS in mm

P	SL	SP	SR	Hx	Hy
0.80	0.330	0.400	0.480	9.400	9.400

sot926-1_fr

Fig 56. Reflow soldering of the TFBGA100 package