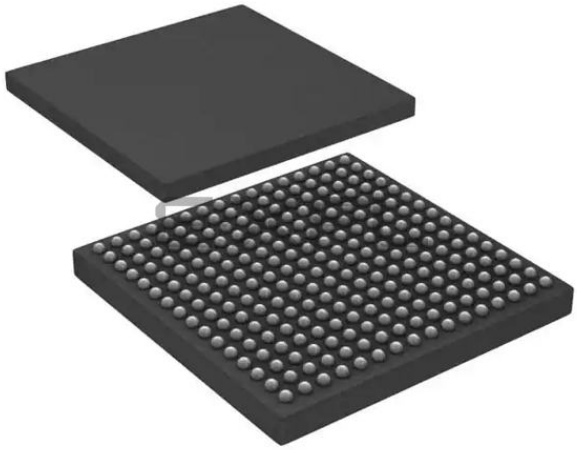


Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4/M0/M0
Core Size	32-Bit Tri-Core
Speed	204MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, IrDA, SD, SPI, SSC, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, I²S, LCD, POR, PWM, WDT
Number of I/O	164
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	282K x 8
Voltage - Supply (Vcc/Vdd)	2.2V ~ 3.6V
Data Converters	A/D 16x10b, 6x12b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	256-LBGA
Supplier Device Package	256-LBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc4370fet256e

Table 3. Pin description *…continued*

LCD, Ethernet, USB0, and USB1 functions are not available on all parts. See Table 2.

Symbol	LBGA256	TFBGA100		Reset state [2]	Type	Description
P1_2	R3	K1	[3]	I; PU	I/O	**GPIO0[9] —** General purpose digital input/output pin. Boot pin (see Table 5).
					O	**CTOUT_6 —** SCT output 6. Match output 2 of timer 1.
					I/O	**EMC_A7 —** External memory address line 7.
					I/O	**SGPIO9 —** General purpose digital input/output pin.
					-	**R —** Function reserved.
					I/O	**SSP0_MOSI —** Master Out Slave in for SSP0.
					-	**R —** Function reserved.
					-	**R —** Function reserved.
P1_3	P5	J1	[3]	I; PU	I/O	**GPIO0[10] —** General purpose digital input/output pin.
					O	**CTOUT_8 —** SCT output 8. Match output 0 of timer 2.
					I/O	**SGPIO10 —** General purpose digital input/output pin.
					O	**$\overline{\text{EMC\_OE}}$ —** LOW active Output Enable signal.
					O	**USB0_IND1 —** USB0 port indicator LED control output 1.
					I/O	**SSP1_MISO —** Master In Slave Out for SSP1.
					-	**R —** Function reserved.
					O	**SD_RST —** SD/MMC reset signal for MMC4.4 card.
P1_4	T3	J2	[3]	I; PU	I/O	**GPIO0[11] —** General purpose digital input/output pin.
					O	**CTOUT_9 —** SCT output 9. Match output 1 of timer 2.
					I/O	**SGPIO11 —** General purpose digital input/output pin.
					O	**$\overline{\text{EMC\_BLS0}}$ —** LOW active Byte Lane select signal 0.
					O	**USB0_IND0 —** USB0 port indicator LED control output 0.
					I/O	**SSP1_MOSI —** Master Out Slave in for SSP1.
					-	**R —** Function reserved.
					O	**SD_VOLT1 —** SD/MMC bus voltage select output 1.
P1_5	R5	J4	[3]	I; PU	I/O	**GPIO1[8] —** General purpose digital input/output pin.
					O	**CTOUT_10 —** SCT output 10. Match output 2 of timer 2.
					-	**R —** Function reserved.
					O	**$\overline{\text{EMC\_CS0}}$ —** LOW active Chip Select 0 signal.
					I	**USB0_PWR_FAULT —** Port power fault signal indicating overcurrent condition; this signal monitors over-current on the USB bus (external circuitry required to detect over-current condition).
					I/O	**SSP1_SSEL —** Slave Select for SSP1.
					I/O	**SGPIO15 —** General purpose digital input/output pin.
					O	**SD_POW —** SD/MMC power monitor output.

Table 3. Pin description *…continued*

LCD, Ethernet, USB0, and USB1 functions are not available on all parts. See Table 2.

Symbol	LBGA256	TFBGA100		Reset state [2]	Type	Description
P2_1	N15	G7	[3]	I; PU	I/O	**SGPIO5 —** General purpose digital input/output pin.
					I	**U0_RXD —** Receiver input for USART0.
					I/O	**EMC_A12 —** External memory address line 12.
					I	**USB0_PWR_FAULT —** Port power fault signal indicating overcurrent condition; this signal monitors over-current on the USB bus (external circuitry required to detect over-current condition).
					I/O	**GPIO5[1] —** General purpose digital input/output pin.
					-	**R —** Function reserved.
					I	**T3_CAP1 —** Capture input 1 of timer 3.
					-	**R —** Function reserved.
P2_2	M15	F5	[3]	I; PU	I/O	**SGPIO6 —** General purpose digital input/output pin.
					I/O	**U0_UCLK —** Serial clock input/output for USART0 in synchronous mode.
					I/O	**EMC_A11 —** External memory address line 11.
					O	**USB0_IND1 —** USB0 port indicator LED control output 1.
					I/O	**GPIO5[2] —** General purpose digital input/output pin.
					I	**CTIN_6 —** SCT input 6. Capture input 1 of timer 3.
					I	**T3_CAP2 —** Capture input 2 of timer 3.
					-	**R —** Function reserved.
P2_3	J12	D8	[4]	I; PU	I/O	**SGPIO12 —** General purpose digital input/output pin.
					I/O	**I2C1_SDA —** I^2C1 data input/output (this pin does not use a specialized I2C pad).
					O	**U3_TXD —** Transmitter output for USART3.
					I	**CTIN_1 —** SCT input 1. Capture input 1 of timer 0. Capture input 1 of timer 2.
					I/O	**GPIO5[3] —** General purpose digital input/output pin.
					-	**R —** Function reserved.
					O	**T3_MAT0 —** Match output 0 of timer 3.
					I	**USB0_PWR_EN —** VBUS drive signal (towards external charge pump or power management unit); indicates that Vbus must be driven (active HIGH).
P2_4	K11	D9	[4]	I; PU	I/O	**SGPIO13 —** General purpose digital input/output pin.
					I/O	**I2C1_SCL —** I^2C1 clock input/output (this pin does not use a specialized I2C pad).
					I	**U3_RXD —** Receiver input for USART3.
					I	**CTIN_0 —** SCT input 0. Capture input 0 of timer 0, 1, 2, 3.
					I/O	**GPIO5[4] —** General purpose digital input/output pin.
					-	**R —** Function reserved.
					O	**T3_MAT1 —** Match output 1 of timer 3.
					I	**USB0_PWR_FAULT —** Port power fault signal indicating overcurrent condition; this signal monitors over-current on the USB bus (external circuitry required to detect over-current condition).

Table 3. Pin description *…continued*

LCD, Ethernet, USB0, and USB1 functions are not available on all parts. See Table 2.

Symbol	LBGA256	TFBGA100		Reset state [2]	Type	Description
P4_2	D3	-	[3]	I; PU	I/O	**GPIO2[2] —** General purpose digital input/output pin.
					O	**CTOUT_0 —** SCT output 0. Match output 0 of timer 0.
					O	**LCD_VD3 —** LCD data.
					-	**R —** Function reserved.
					-	**R —** Function reserved.
					O	**LCD_VD12 —** LCD data.
					I	**U3_RXD —** Receiver input for USART3.
					I/O	**SGPIO8 —** General purpose digital input/output pin.
P4_3	C2	-	[6] [13]	I; PU	I/O	**GPIO2[3] —** General purpose digital input/output pin.
					O	**CTOUT_3 —** SCT output 3. Match output 3 of timer 0.
					O	**LCD_VD2 —** LCD data.
					-	**R —** Function reserved.
					-	**R —** Function reserved.
					O	**LCD_VD21 —** LCD data.
					I/O	**U3_BAUD —** Baud pin for USART3.
					I/O	**SGPIO9 —** General purpose digital input/output pin.
					AI	**ADC0_0 —** ADC0, input channel 0. Configure the pin as GPIO input and use the ADC function select register in the SCU to select the ADC.
P4_4	B1	-	[6]	I; PU	I/O	**GPIO2[4] —** General purpose digital input/output pin.
					O	**CTOUT_2 —** SCT output 2. Match output 2 of timer 0.
					O	**LCD_VD1 —** LCD data.
					-	**R —** Function reserved.
					-	**R —** Function reserved.
					O	**LCD_VD20 —** LCD data.
					I/O	**U3_DIR —** RS-485/EIA-485 output enable/direction control for USART3.
					I/O	**SGPIO10 —** General purpose digital input/output pin.
					O	**DAC —** DAC output. Configure the pin as GPIO input and use the analog function select register in the SCU to select the DAC.
P4_5	D2	-	[3]	I; PU	I/O	**GPIO2[5] —** General purpose digital input/output pin.
					O	**CTOUT_5 —** SCT output 5. Match output 1 of timer 1.
					O	**LCD_FP —** Frame pulse (STN). Vertical synchronization pulse (TFT).
					-	**R —** Function reserved.
					-	**R —** Function reserved.
					-	**R —** Function reserved.
					-	**R —** Function reserved.
					I/O	**SGPIO11 —** General purpose digital input/output pin.

Table 3. Pin description *…continued*

LCD, Ethernet, USB0, and USB1 functions are not available on all parts. See Table 2.

Symbol	LBGA256	TFBGA100		Reset state [2]	Type	Description
P6_3	P15	-	[3]	I; PU	I/O	**GPIO3[2] —** General purpose digital input/output pin.
					I	**USB0_PWR_EN —** VBUS drive signal (towards external charge pump or power management unit); indicates that the VBUS signal must be driven (active HIGH).
					I/O	**SGPIO4 —** General purpose digital input/output pin.
					O	**EMC_CS1 —** LOW active Chip Select 1 signal.
					-	**R —** Function reserved.
					I	**T2_CAP2 —** Capture input 2 of timer 2.
					-	**R —** Function reserved.
					-	**R —** Function reserved.
P6_4	R16	F6	[3]	I; PU	I/O	**GPIO3[3] —** General purpose digital input/output pin.
					I	**CTIN_6 —** SCT input 6. Capture input 1 of timer 3.
					O	**U0_TXD —** Transmitter output for USART0.
					O	**EMC_CAS —** LOW active SDRAM Column Address Strobe.
					-	**R —** Function reserved.
					-	**R —** Function reserved.
					-	**R —** Function reserved.
					-	**R —** Function reserved.
P6_5	P16	F9	[3]	I; PU	I/O	**GPIO3[4] —** General purpose digital input/output pin.
					O	**CTOUT_6 —** SCT output 6. Match output 2 of timer 1.
					I	**U0_RXD —** Receiver input for USART0.
					O	**EMC_RAS —** LOW active SDRAM Row Address Strobe.
					-	**R —** Function reserved.
					-	**R —** Function reserved.
					-	**R —** Function reserved.
					-	**R —** Function reserved.
P6_6	L14	-	[3]	I; PU	I/O	**GPIO0[5] —** General purpose digital input/output pin.
					O	**EMC_BLS1 —** LOW active Byte Lane select signal 1.
					I/O	**SGPIO5 —** General purpose digital input/output pin.
					I	**USB0_PWR_FAULT —** Port power fault signal indicating overcurrent condition; this signal monitors over-current on the USB bus (external circuitry required to detect over-current condition).
					-	**R —** Function reserved.
					I	**T2_CAP3 —** Capture input 3 of timer 2.
					-	**R —** Function reserved.
					-	**R —** Function reserved.

Table 3. Pin description *…continued*

LCD, Ethernet, USB0, and USB1 functions are not available on all parts. See Table 2.

Symbol	LBGA256	TFBGA100		Reset state [2]	Type	Description
PC_2	F6	-	[3]	I; PU	I/O	**USB1_ULPI_D6 —** ULPI link bidirectional data line 6.
					-	**R —** Function reserved.
					I	**U1_CTS —** Clear to Send input for UART 1.
					O	**ENET_TXD2 —** Ethernet transmit data 2 (MII interface).
					I/O	**GPIO6[1] —** General purpose digital input/output pin.
					-	**R —** Function reserved.
					-	**R —** Function reserved.
					O	**SD_RST —** SD/MMC reset signal for MMC4.4 card.
PC_3	F5	-	[6]	I; PU	I/O	**USB1_ULPI_D5 —** ULPI link bidirectional data line 5.
					-	**R —** Function reserved.
					O	**U1_RTS —** Request to Send output for UART 1. Can also be configured to be an RS-485/EIA-485 output enable signal for UART 1.
					O	**ENET_TXD3 —** Ethernet transmit data 3 (MII interface).
					I/O	**GPIO6[2] —** General purpose digital input/output pin.
					-	**R —** Function reserved.
					-	**R —** Function reserved.
					O	**SD_VOLT1 —** SD/MMC bus voltage select output 1.
					AI	**ADC1_0 —** ADC1, input channel 0. Configure the pin as GPIO input and use the ADC function select register in the SCU to select the ADC.
PC_4	F4	-	[3]	I; PU	-	**R —** Function reserved.
					I/O	**USB1_ULPI_D4 —** ULPI link bidirectional data line 4.
					-	**R —** Function reserved.
						ENET_TX_EN — Ethernet transmit enable (RMII/MII interface).
					I/O	**GPIO6[3] —** General purpose digital input/output pin.
					-	**R —** Function reserved.
					I	**T3_CAP1 —** Capture input 1 of timer 3.
					I/O	**SD_DAT0 —** SD/MMC data bus line 0.
PC_5	G4	-	[3]	I; PU	-	**R —** Function reserved.
					I/O	**USB1_ULPI_D3 —** ULPI link bidirectional data line 3.
					-	**R —** Function reserved.
					O	**ENET_TX_ER —** Ethernet Transmit Error (MII interface).
					I/O	**GPIO6[4] —** General purpose digital input/output pin.
					-	**R —** Function reserved.
					I	**T3_CAP2 —** Capture input 2 of timer 3.
					I/O	**SD_DAT1 —** SD/MMC data bus line 1.

Table 3. Pin description *…continued*

LCD, Ethernet, USB0, and USB1 functions are not available on all parts. See Table 2.

Symbol	LBGA256	TFBGA100		Reset state [2]	Type	Description
PD_11	N9	-	[3]	I; PU	-	**R —** Function reserved.
					-	**R —** Function reserved.
					O	**$\overline{\text{EMC\_CS3}}$ —** LOW active Chip Select 3 signal.
					-	**R —** Function reserved.
					I/O	**GPIO6[25] —** General purpose digital input/output pin.
					I/O	**USB1_ULPI_D0 —** ULPI link bidirectional data line 0.
					O	**CTOUT_14 —** SCT output 14. Match output 2 of timer 3.
					-	**R —** Function reserved.
PD_12	N11	-	[3]	I; PU	-	**R —** Function reserved.
					-	**R —** Function reserved.
					O	**$\overline{\text{EMC\_CS2}}$ —** LOW active Chip Select 2 signal.
					-	**R —** Function reserved.
					I/O	**GPIO6[26] —** General purpose digital input/output pin.
					-	**R —** Function reserved.
					O	**CTOUT_10 —** SCT output 10. Match output 2 of timer 2.
					-	**R —** Function reserved.
PD_13	T14	-	[3]	I; PU	-	**R —** Function reserved.
					I	**CTIN_0 —** SCT input 0. Capture input 0 of timer 0, 1, 2, 3.
					O	**$\overline{\text{EMC\_BLS2}}$ —** LOW active Byte Lane select signal 2.
					-	**R —** Function reserved.
					I/O	**GPIO6[27] —** General purpose digital input/output pin.
					-	**R —** Function reserved.
					O	**CTOUT_13 —** SCT output 13. Match output 1 of timer 3.
					-	**R —** Function reserved.
PD_14	R13	-	[3]	I; PU	-	**R —** Function reserved.
					-	**R —** Function reserved.
					O	**$\overline{\text{EMC\_DYCS2}}$ —** SDRAM chip select 2.
					-	**R —** Function reserved.
					I/O	**GPIO6[28] —** General purpose digital input/output pin.
					-	**R —** Function reserved.
					O	**CTOUT_11 —** SCT output 11. Match output 3 of timer 2.
					-	**R —** Function reserved.

Table 3. Pin description *…continued*

LCD, Ethernet, USB0, and USB1 functions are not available on all parts. See Table 2.

Symbol	LBGA256	TFBGA100		Reset state [2]	Type	Description
ADC pins						
ADCHS_0	E3	A2	[9]	I; IA	I	12-bit high-speed ADC input channel 0.
ADCHS_1	C3	A1	[9]	I; IA	I	12-bit high-speed ADC input channel 1.
ADCHS_2	A4	B3	[9]	I; IA	I	12-bit high-speed ADC input channel 2.
ADCHS_3	A5	-	[9]	I; IA	I	12-bit high-speed ADC input channel 3.
ADCHS_4	C6	-	[9]	I; IA	I	12-bit high-speed ADC input channel 4.
ADCHS_5	B3	-	[9]	I; IA	I	12-bit high-speed ADC input channel 5.
ADCHS_NEG	B5	A3	[9]	I; IA	I/O	12-bit high-speed ADC reference voltage output or negative differential input.
ADC0_7	C5	-	[9]	I; IA	I	10-bit ADC0 input channel 7.
RTC						
RTC_ALARM	A11	C3	[12]	-	O	RTC controlled output. This pin has an internal pull-up. The reset state of this pin is LOW after POR. For all other types of reset, the reset state depends on the state of the RTC alarm interrupt.
RTCX1	A8	A5	[9]	-	I	Input to the RTC 32 kHz ultra-low power oscillator circuit.
RTCX2	B8	B5	[9]	-	O	Output from the RTC 32 kHz ultra-low power oscillator circuit.
Crystal oscillator pins						
XTAL1	D1	B1	[9]	-	I	Input to the oscillator circuit and internal clock generator circuits.
XTAL2	E1	C1	[9]	-	O	Output from the oscillator amplifier.
Power and ground pins						
USB0_VDDA 3V3_DRIVER	F3	D1		-	-	Separate analog 3.3 V power supply for driver.
USB0 _VDDA3V3	G3	D2		-	-	USB 3.3 V separate power supply voltage.
USB0_VSSA _TERM	H3	D3		-	-	Dedicated analog ground for clean reference for termination resistors.
USB0_VSSA _REF	G1	F2		-	-	Dedicated clean analog ground for generation of reference currents and voltages.
VDDA	B4	B2		-	-	Analog power supply and 10-bit ADC reference voltage.
VBAT	B10	C5		-	-	RTC power supply: 3.3 V on this pin supplies power to the RTC.
VDDREG	F10, F9, L8, L7	E4, E5, F4			-	Main regulator power supply. Tie the VDDREG and VDDIO pins to a common power supply to ensure the same ramp-up time for both supply voltages.
VPP	E8	-		-	-	OTP programming voltage.

Table 3. Pin description *…continued*

LCD, Ethernet, USB0, and USB1 functions are not available on all parts. See Table 2.

Symbol	LBGA256	TFBGA100		Reset state [2]	Type	Description
VDDIO	D7, E12, F7, F8, G10, H10, J6, J7, K7, L9, L10, N7, N13	F10, K5		-	-	I/O power supply. Tie the VDDREG and VDDIO pins to a common power supply to ensure the same ramp-up time for both supply voltages.
VDD	-	-				Power supply for main regulator, I/O, and OTP.
VSS	G9, H7, J10, J11, K8	-		-	-	Ground.
VSSIO	C4, D13, G6, G7, G8, H8, H9, J8, J9, K9, K10, M13, P7, P13	C8, D4, D5, G8, J3, J6		-	-	Ground.
VSSA	B2	C2		-	-	Analog ground.
Not connected						
-	B9	-		-	-	n.c.

[1] - = not pinned out.

[2] I = input, O = output, AI/O analog input/output, IA = inactive; PU = pull-up enabled (weak pull-up resistor pulls up pin to $V_{DD(IO)}$); F = floating. Reset state reflects the pin state at reset without boot code operation.

[3] 5 V tolerant pad with 15 ns glitch filter (5 V tolerant if $V_{DD(IO)}$ present; if $V_{DD(IO)}$ not present, do not exceed 3.3 V); provides digital I/O functions with TTL levels and hysteresis; normal drive strength.

[4] 5 V tolerant pad with 15 ns glitch filter (5 V tolerant if $V_{DD(IO)}$ present; if $V_{DD(IO)}$ not present, do not exceed 3.3 V) providing digital I/O functions with TTL levels, and hysteresis; high drive strength.

[5] 5 V tolerant pad with 15 ns glitch filter (5 V tolerant if $V_{DD(IO)}$ present; if $V_{DD(IO)}$ not present, do not exceed 3.3 V) providing high-speed digital I/O functions with TTL levels and hysteresis.

7.9 Global Input Multiplexer Array (GIMA)

The GIMA allows to route signals to event-driven peripheral targets like the SCT, timers, event router, or the ADCs.

7.9.1 Features

- Single selection of a source.
- Signal inversion.
- Can capture a pulse if the input event source is faster than the target clock.
- Synchronization of input event and target clock.
- Single-cycle pulse generation for target.

7.10 System Tick timer (SysTick)

The ARM Cortex-M4 includes a system tick timer (SYSTICK) that is intended to generate a dedicated SYSTICK exception at a 10 ms interval.

7.11 On-chip static RAM

The LPC4370 support 200 kB local SRAM and an additional 64 kB AHB SRAM with separate bus master access for higher throughput and individual power control for low power operation. See Section 7.23.9.1 “Memory retention in Power-down modes”.

7.12 In-System Programming (ISP)

In-System programming (ISP) is programming or reprogramming the on-chip SRAM memory, using the boot loader software and the USART0 serial port. This can be done when the part resides in the end-user board. ISP allows to load data into on-chip SRAM and execute code from on-chip SRAM.

7.13 Boot ROM

The internal ROM memory is used to store the boot code of the LPC4370. After a reset, the ARM processor will start its code execution from this memory.

The boot ROM memory includes the following features:

- ROM memory size is 64 kB.
- Supports booting from UART interfaces and external static memory such as NOR flash, SPI flash, quad SPI flash.
- Includes APIs for OTP programming.
- Includes a flexible USB device stack that supports Human Interface Device (HID), Mass Storage Class (MSC), and Device Firmware Upgrade (DFU) drivers.

Several boot modes are available depending on the values of the OTP bits BOOT_SRC. If the OTP memory is not programmed or the BOOT_SRC bits are all zero, the boot mode is determined by the states of the boot pins P2_9, P2_8, P1_2, and P1_1.

- Supports interrupts.
- This module has its own, integrated DMA engine.
- USB interface electrical test software included in ROM USB stack.

7.18.7 LCD controller

Remark: The LCD controller is available on the LPC4370FET256 parts. See Table 2.

The LCD controller provides all of the necessary control signals to interface directly to a variety of color and monochrome LCD panels. Both STN (single and dual panel) and TFT panels can be operated. The display resolution is selectable and can be up to 1024 × 768 pixels. Several color modes are provided, up to a 24-bit true-color non-palettized mode. An on-chip 512-byte color palette allows reducing bus utilization (i.e. memory size of the displayed data) while still supporting a large number of colors.

The LCD interface includes its own DMA controller to allow it to operate independently of the CPU and other system functions. A built-in FIFO acts as a buffer for display data, providing flexibility for system timing. Hardware cursor support can further reduce the amount of CPU time needed to operate the display.

7.18.7.1 Features

- AHB master interface to access frame buffer.
- Setup and control via a separate AHB slave interface.
- Dual 16-deep programmable 64-bit wide FIFOs for buffering incoming display data.
- Supports single and dual-panel monochrome Super Twisted Nematic (STN) displays with 4-bit or 8-bit interfaces.
- Supports single and dual-panel color STN displays.
- Supports Thin Film Transistor (TFT) color displays.
- Programmable display resolution including, but not limited to: 320 × 200, 320 × 240, 640 × 200, 640 × 240, 640 × 480, 800 × 600, and 1024 × 768.
- Hardware cursor support for single-panel displays.
- 15 gray-level monochrome, 3375 color STN, and 32 K color palettized TFT support.
- 1, 2, or 4 bits-per-pixel (bpp) palettized displays for monochrome STN.
- 1, 2, 4, or 8 bpp palettized color displays for color STN and TFT.
- 16 bpp true-color non-palettized for color STN and TFT.
- 24 bpp true-color non-palettized for color TFT.
- Programmable timing for different display panels.
- 256 entry, 16-bit palette RAM, arranged as a 128 × 32-bit RAM.
- Frame, line, and pixel clock signals.
- AC bias signal for STN, data enable signal for TFT panels.
- Supports little and big-endian, and Windows CE data formats.
- LCD panel clock may be generated from the peripheral clock, or from a clock input pin.

9. Thermal characteristics

The average chip junction temperature, T_j (°C), can be calculated using the following equation:

$$T_j = T_{amb} + (P_D \times R_{th(j-a)}) \quad (1)$$

- T_{amb} = ambient temperature (°C),
- $R_{th(j-a)}$ = the package junction-to-ambient thermal resistance (°C/W)
- P_D = sum of internal and I/O power dissipation

The internal power dissipation is the product of I_{DD} and V_{DD}. The I/O power dissipation of the I/O pins is often small and many times can be negligible. However it can be significant in some applications.

Table 8. Thermal characteristics

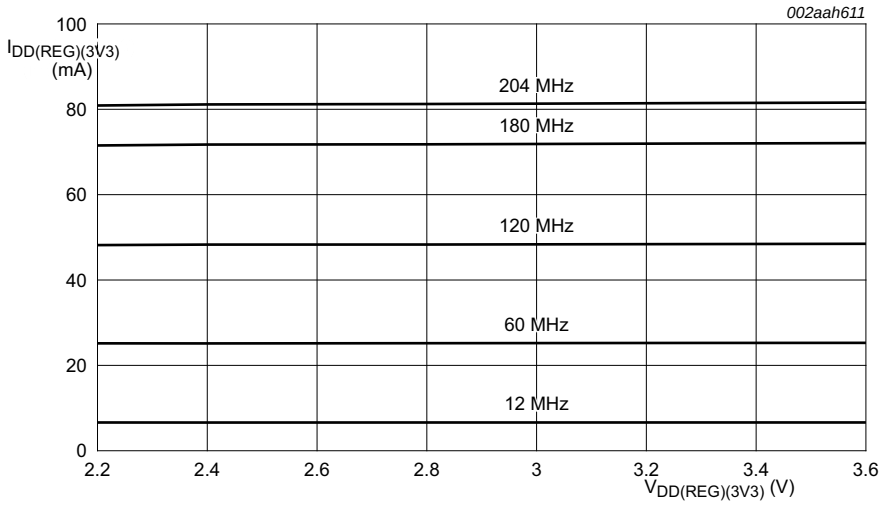
V_{DD} = 2.2 V to 3.6 V; T_{amb} = −40 °C to +85 °C unless otherwise specified;

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$T_{j(max)}$	maximum junction temperature			-	-	125	°C

Table 9. Thermal resistance value (BGA package)

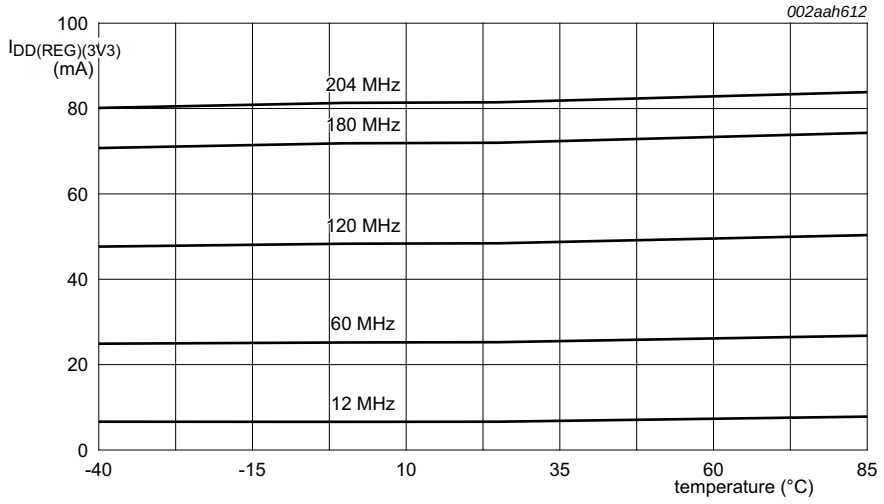
Symbol	Parameter	Conditions	Thermal resistance in °C/W ±15 %	
			LBGA256	TFBGA100
$R_{th(j-a)}$	thermal resistance from junction to ambient	JEDEC (4.5 in × 4 in); still air	29	46
		8-layer (4.5 in × 3 in); still air	24	37
$R_{th(j-c)}$	thermal resistance from junction to case		14	11

10.1 Power consumption



Conditions: T_{amb} = 25 °C; active mode entered executing code while(1){} from SRAM; M0 cores in reset; internal pull-up resistors disabled; PLL1 enabled; IRC enabled; all peripherals disabled; all peripheral clocks disabled.

Fig 8. Typical supply current versus regulator supply voltage $V_{DD(REG)(3V3)}$ in active mode



Conditions: $V_{DD(REG)(3V3)}$ = 3.3 V, Active mode entered executing code while(1){} from SRAM;M0 cores in reset; internal pull-up resistors disabled; PLL1 enabled; IRC enabled; all peripherals disabled; all peripheral clocks disabled.

Fig 9. Typical supply current versus temperature in Active mode

[2] Simulated using 10 cm of 50 Ω PCB trace with 5 pF receiver input. Rise and fall times measured between 80 % and 20 % of the full output signal level.

[3] The slew rate is configured in the system control block in the SFSP registers using the EHS bit. See the LPC43xx user manual.

[4] C_L = 20 pF. Rise and fall times measured between 90 % and 10 % of the full input signal level.

[5] The drive modes are configured in the system control block in the SFSP registers using the EHD bit. See the LPC43xx user manual.

11.7 RTC oscillator

Table 21. Dynamic characteristic: RTC oscillator

T_{amb} = −40 °C to +85 °C; 2.2 V ≤ $V_{DD(REG)(3V3)}$ ≤ 3.6 V or 2.2 V ≤ V_{BAT} ≤ 3.6 V[1]; typical $C_{RTCX1/2}$ = 20 pF; also see Section 13.3.

Symbol	Parameter	Conditions		Min	Typ[2]	Max	Unit
$f_{i(RTC)}$	RTC input frequency	-		-	32.768	-	kHz
$I_{DD(RTC)}$	RTC supply current				280	800	nA

[1] Parameters are valid over operating temperature range unless otherwise specified.

[2] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

11.8 I²C-bus

Table 22. Dynamic characteristic: I²C-bus pins

T_{amb} = −40 °C to +85 °C; 2.2 V ≤ $V_{DD(REG)(3V3)}$ ≤ 3.6 V.[1]

Symbol	Parameter		Conditions	Min	Max	Unit
f_{SCL}	SCL clock frequency		Standard-mode	0	100	kHz
			Fast-mode	0	400	kHz
			Fast-mode Plus	0	1	MHz
t_f	fall time	[3][4][5][6]	of both SDA and SCL signals Standard-mode	-	300	ns
			Fast-mode	20 + 0.1 × C_b	300	ns
			Fast-mode Plus	-	120	ns
t_{LOW}	LOW period of the SCL clock		Standard-mode	4.7	-	µs
			Fast-mode	1.3	-	µs
			Fast-mode Plus	0.5	-	µs
t_{HIGH}	HIGH period of the SCL clock		Standard-mode	4.0	-	µs
			Fast-mode	0.6	-	µs
			Fast-mode Plus	0.26	-	µs
$t_{HD;DAT}$	data hold time	[2][3][7]	Standard-mode	0	-	µs
			Fast-mode	0	-	µs
			Fast-mode Plus	0	-	µs
$t_{SU;DAT}$	data set-up time	[8][9]	Standard-mode	250	-	ns
			Fast-mode	100	-	ns
			Fast-mode Plus	50	-	ns

[1] Parameters are valid over operating temperature range unless otherwise specified. See the I²C-bus specification *UM10204* for details.

[2] tHD;DAT is the data hold time that is measured from the falling edge of SCL; applies to data in transmission and the acknowledge.

11.10 USART interface

Table 24. USART dynamic characteristics

T_{amb} = −40 °C to 85 °C; 2.2 V ≤ $V_{DD(REG)(3V3)}$ ≤ 3.6 V; 2.7 V ≤ $V_{DD(IO)}$ ≤ 3.6 V; C_L = 20 pF. EHS = 1 for all pins. Simulated values.

Symbol	Parameter	Min	Max	Unit
USART master (in synchronous mode)				
$t_{su(D)}$	data input set-up time	26.6	-	ns
$t_{h(D)}$	data input hold time	0	-	ns
$t_{v(Q)}$	data output valid time	0	8.8	ns
USART slave (in synchronous mode)				
$t_{su(D)}$	data input set-up time	1.2	-	ns
$t_{h(D)}$	data input hold time	0.4	-	ns
$t_{v(Q)}$	data output valid time	5.5	24	ns

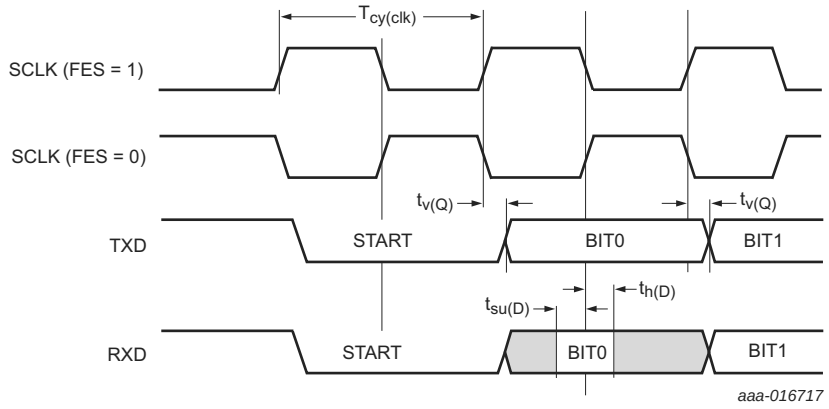


Fig 27. USART timing

Table 30. Dynamic characteristics: Dynamic external memory interface

Simulated data over temperature and process range; C_L = 10 pF for $\overline{EMC\_DYCSn}$, $\overline{EMC\_RAS}$, $\overline{EMC\_CAS}$, $\overline{EMC\_WE}$, EMC_An; C_L = 9 pF for EMC_Dn; C_L = 5 pF for EMC_DQMOUTn, EMC_CLKn, EMC_CKEOUTn; T_{amb} = −40 °C to 85 °C; 2.2 V ≤ $V_{DD(REG)(3V3)}$ ≤ 3.6 V; $V_{DD(IO)}$ = 3.3 V ± 10 %; RD = 1 (see LPC43xx User manual); EMC_CLKn delays CLK0_DELAY = CLK1_DELAY = CLK2_DELAY = CLK3_DELAY = 0.

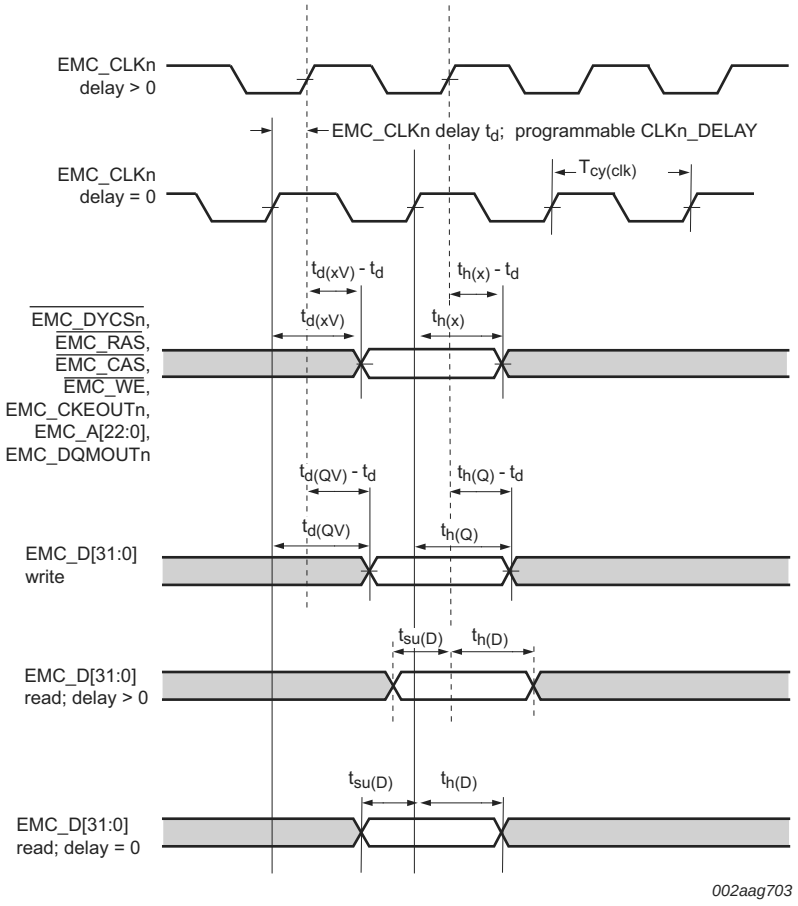
Symbol	Parameter	Min	Typ	Max	Unit
$T_{cy(clk)}$	clock cycle time	8.4	-	-	ns
Common to read and write cycles					
$t_{d(DYCSV)}$	DYCS delay time	-	3.1 + 0.5 × $T_{cy(clk)}$	5.1 + 0.5 × $T_{cy(clk)}$	ns
$t_{h(DYCS)}$	DYCS hold time	0.3 + 0.5 × $T_{cy(clk)}$	0.9 + 0.5 × $T_{cy(clk)}$	-	ns
$t_{d(RASV)}$	row address strobe valid delay time	-	3.1 + 0.5 × $T_{cy(clk)}$	4.9 + 0.5 × $T_{cy(clk)}$	ns
$t_{h(RAS)}$	row address strobe hold time	0.5 + 0.5 × $T_{cy(clk)}$	1.1 + 0.5 × $T_{cy(clk)}$	-	ns
$t_{d(CASV)}$	column address strobe valid delay time	-	2.9 + 0.5 × $T_{cy(clk)}$	4.6 + 0.5 × $T_{cy(clk)}$	ns
$t_{h(CAS)}$	column address strobe hold time	0.3 + 0.5 × $T_{cy(clk)}$	0.9 + 0.5 × $T_{cy(clk)}$	-	ns
$t_{d(WEV)}$	$\overline{WE}$ valid delay time	-	3.2 + 0.5 × $T_{cy(clk)}$	5.9 + 0.5 × $T_{cy(clk)}$	ns
$t_{h(WE)}$	$\overline{WE}$ hold time	1.3 + 0.5 × $T_{cy(clk)}$	1.4 + 0.5 × $T_{cy(clk)}$	-	ns
$t_{d(DQMOUTV)}$	DQMOUT valid delay time	-	3.1 + 0.5 × $T_{cy(clk)}$	5.0 + 0.5 × $T_{cy(clk)}$	ns
$t_{h(DQMOUT)}$	DQMOUT hold time	0.2 + 0.5 × $T_{cy(clk)}$	0.8 + 0.5 × $T_{cy(clk)}$	-	ns
$t_{d(AV)}$	address valid delay time	-	3.8 + 0.5 × $T_{cy(clk)}$	6.3 + 0.5 × $T_{cy(clk)}$	ns
$t_{h(A)}$	address hold time	0.3 + 0.5 × $T_{cy(clk)}$	0.9 + 0.5 × $T_{cy(clk)}$	-	ns
$t_{d(CKEOUTV)}$	CKEOUT valid delay time	-	3.1 + 0.5 × $T_{cy(clk)}$	5.1 + 0.5 × $T_{cy(clk)}$	ns
$t_{h(CKEOUT)}$	CKEOUT hold time	0.5 × $T_{cy(clk)}$	0.7 + 0.5 × $T_{cy(clk)}$	-	ns
Read cycle parameters					
$t_{su(D)}$	data input set-up time	−1.5	−0.5	-	ns
$t_{h(D)}$	data input hold time	2.2	0.8	-	ns
Write cycle parameters					
$t_{d(QV)}$	data output valid delay time	-	3.8 + 0.5 × $T_{cy(clk)}$	6.2 + 0.5 × $T_{cy(clk)}$	ns
$t_{h(Q)}$	data output hold time	0.5 × $T_{cy(clk)}$	0.7 + 0.5 × $T_{cy(clk)}$	-	ns

Table 31. Dynamic characteristics: Dynamic external memory interface; EMC_CLK[3:0] delay values

T_{amb} = −40 °C to 85 °C; $V_{DD(IO)}$ = 3.3 V ± 10 %; 2.2 V ≤ $V_{DD(REG)(3V3)}$ ≤ 3.6 V.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
t_d	delay time	delay value	[1]				
		CLKn_DELAY = 0		0.0	0.0	0.0	ns
		CLKn_DELAY = 1	[1]	0.4	0.5	0.8	ns
		CLKn_DELAY = 2	[1]	0.7	1.0	1.7	ns
		CLKn_DELAY = 3	[1]	1.1	1.6	2.5	ns
		CLKn_DELAY = 4	[1]	1.4	2.0	3.3	ns
		CLKn_DELAY = 5	[1]	1.7	2.6	4.1	ns
		CLKn_DELAY = 6	[1]	2.1	3.1	4.9	ns
		CLKn_DELAY = 7	[1]	2.5	3.6	5.8	ns

[1] Program the EMC_CLKn delay values in the EMCDELAYCLK register (see the *LPC43xx User manual*). The delay values must be the same for all SDRAM clocks EMC_CLKn: CLK0_DELAY = CLK1_DELAY = CLK2_DELAY = CLK3_DELAY.



For the programmable EMC_CLK[3:0] clock delays CLKn_DELAY, see Table 31.

Remark: For SDRAM operation, set CLK0_DELAY = CLK1_DELAY = CLK2_DELAY = CLK3_DELAY in the EMCDELAYCLK register.

Fig 34. SDRAM timing

Table 34. Dynamic characteristics: Ethernet

T_{amb} = −40 °C to 85 °C; 2.2 V ≤ $V_{DD(REG)(3V3)}$ ≤ 3.6 V; 2.7 V ≤ $V_{DD(IO)}$ ≤ 3.6 V. Values guaranteed by design.

Symbol	Parameter	Conditions		Min	Max	Unit
RMII mode						
f_{clk}	clock frequency	for ENET_RX_CLK	[1]	-	50	MHz
δ_{clk}	clock duty cycle		[1]	50	50	%
t_{su}	set-up time	for ENET_TXDn, ENET_TX_EN, ENET_RXDn, ENET_RX_ER, ENET_RX_DV	[1][2]	4	-	ns
t_h	hold time	for ENET_TXDn, ENET_TX_EN, ENET_RXDn, ENET_RX_ER, ENET_RX_DV	[1][2]	2	-	ns
MII mode						
f_{clk}	clock frequency	for ENET_TX_CLK	[1]	-	25	MHz
δ_{clk}	clock duty cycle		[1]	50	50	%
t_{su}	set-up time	for ENET_TXDn, ENET_TX_EN, ENET_TX_ER	[1][2]	4	-	ns
t_h	hold time	for ENET_TXDn, ENET_TX_EN, ENET_TX_ER	[1][2]	2	-	ns
f_{clk}	clock frequency	for ENET_RX_CLK	[1]	-	25	MHz
δ_{clk}	clock duty cycle		[1]	50	50	%
t_{su}	set-up time	for ENET_RXDn, ENET_RX_ER, ENET_RX_DV	[1][2]	4	-	ns
t_h	hold time	for ENET_RXDn, ENET_RX_ER, ENET_RX_DV	[1][2]	2	-	ns

[1] Output drivers can drive a load ≥ 25 pF accommodating over 12 inch of PCB trace and the input capacitance of the receiving device.

[2] Timing values are given from the point at which the clock signal waveform crosses 1.4 V to the valid input or output level.

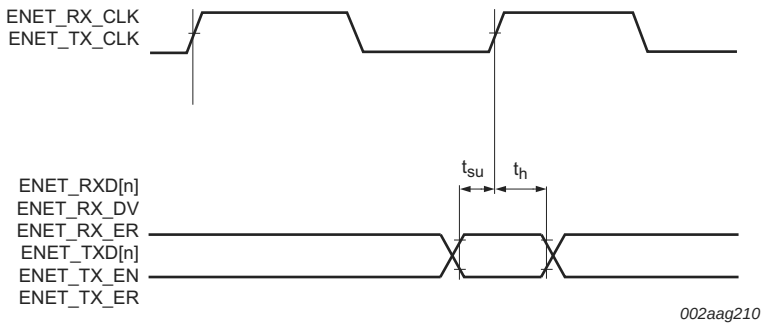
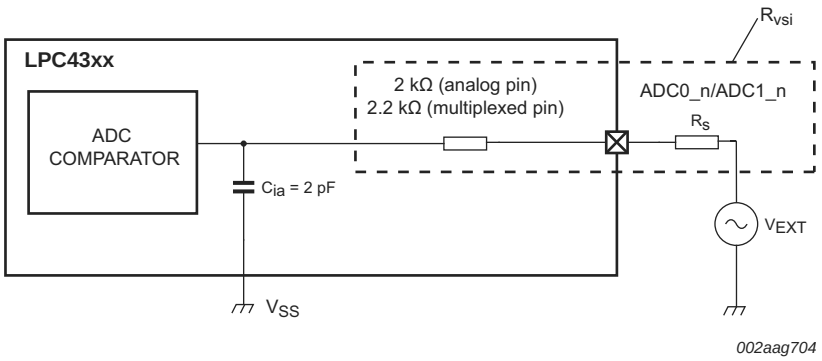


Fig 36. Ethernet timing



$Rs < 1/((7 \times f_{clk(ADC)} \times C_{ia}) - 2\ k\Omega)$

Fig 39. ADC interface to pins

Table 39. DAC characteristics

$V_{DDA(3V3)}$ over specified ranges; T_{amb} = −40 °C to +85 °C; unless otherwise specified

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
E_D	differential linearity error	2.7 V ≤ $V_{DDA(3V3)}$ ≤ 3.6 V	[1]	-	±0.8	-	LSB
		2.2 V ≤ $V_{DDA(3V3)}$ < 2.7 V		-	±1.0	-	LSB
$E_{L(adj)}$	integral non-linearity	code = 0 to 975 2.7 V ≤ $V_{DDA(3V3)}$ ≤ 3.6 V	[1]	-	±1.0	-	LSB
		2.2 V ≤ $V_{DDA(3V3)}$ < 2.7 V		-	±1.5	-	LSB
E_O	offset error	2.7 V ≤ $V_{DDA(3V3)}$ ≤ 3.6 V	[1]	-	±0.8	-	LSB
		2.2 V ≤ $V_{DDA(3V3)}$ < 2.7 V		-	±1.0	-	LSB
E_G	gain error	2.7 V ≤ $V_{DDA(3V3)}$ ≤ 3.6 V	[1]	-	±0.3	-	%
		2.2 V ≤ $V_{DDA(3V3)}$ < 2.7 V		-	±1.0	-	%
C_L	load capacitance			-	-	200	pF
R_L	load resistance			1	-	-	kΩ
t_s	settling time		[1]		0.4		μσ

[1] In the DAC CR register, bit BIAS = 0 (see the *LPC43xx user manual*).

[2] Settling time is calculated within 1/2 LSB of the final value.

Table 42. LCD panel connections for TFT panels

External pin	TFT 12 bit (4:4:4 mode)		TFT 16 bit (5:6:5 mode)		TFT 16 bit (1:5:5:5 mode)		TFT 24 bit	
	LPC43xx pin used	LCD function	LPC43xx pin used	LCD function	LPC43xx pin used	LCD function	LPC43xx pin used	LCD function
LCD_VD0	-	-	-	-	-	-	P4_1	RED0
LCD_LP	P7_6	LCDLP	P7_6	LCDLP	P7_6	LCDLP	P7_6	LCDLP
LCD_ENAB /LCDM	P4_6	LCDENAB/ LCDM	P4_6	LCDENAB/ LCDM	P4_6	LCDENAB/ LCDM	P4_6	LCDENAB/ LCDM
LCD_FP	P4_5	LCDFP	P4_5	LCDFP	P4_5	LCDFP	P4_5	LCDFP
LCD_DCLK	P4_7	LCDDCLK	P4_7	LCDDCLK	P4_7	LCDDCLK	P4_7	LCDDCLK
LCD_LE	P7_0	LCDLE	P7_0	LCDLE	P7_0	LCDLE	P7_0	LCDLE
LCD_PWR	P7_7	LCDPWR	P7_7	LCDPWR	P7_7	LCDPWR	P7_7	LCDPWR
GP_CLKIN	PF_4	LCDCLKIN	PF_4	LCDCLKIN	PF_4	LCDCLKIN	PF_4	LCDCLKIN

13.2 Crystal oscillator

The crystal oscillator is controlled by the XTAL_OSC_CTRL register in the CGU (see *LPC43xx user manual*).

The crystal oscillator operates at frequencies of 1 MHz to 25 MHz. This frequency can be boosted to a higher frequency, up to the maximum CPU operating frequency, by the PLL.

The oscillator can operate in one of two modes: slave mode and oscillation mode.

- In slave mode the input clock signal should be coupled by means of a capacitor of 100 pF (C_C in Figure 40), with an amplitude of at least 200 mV (rms). The XTAL2 pin in this configuration can be left unconnected.
- External components and models used in oscillation mode are shown in Figure 41, and in Table 43 and Table 44. Since the feedback resistance is integrated on chip, only a crystal and the capacitances CX1 and CX2 need to be connected externally in case of fundamental mode oscillation (the fundamental frequency is represented by L, CL and RS). Capacitance C_P in Figure 41 represents the parallel package capacitance and should not be larger than 7 pF. Parameters FC, CL, RS and CP are supplied by the crystal manufacturer.

Table 43. Recommended values for $C_{X1/X2}$ in oscillation mode (crystal and external components parameters) low frequency mode

Fundamental oscillation frequency	Maximum crystal series resistance R_S	External load capacitors C_{X1}, C_{X2}
2 MHz	< 200 Ω	33 pF, 33 pF
	< 200 Ω	39 pF, 39 pF
	< 200 Ω	56 pF, 56 pF
4 MHz	< 200 Ω	18 pF, 18 pF
	< 200 Ω	39 pF, 39 pF
	< 200 Ω	56 pF, 56 pF
8 MHz	< 200 Ω	18 pF, 18 pF
	< 200 Ω	39 pF, 39 pF

13.9.1 Inverting single-ended circuit

For the inverting single-ended circuit only one op-amp is needed. A 1.24 V shunt voltage reference is used for creating an offset voltage of 450 mV. The disadvantage is that the signal output of the circuit is inverted. However, this can be easily solved in software by subtracting the ADC output from 4095, which is the maximum value of the 12-bit result.

(2)

$$Vout = Vcom\frac{R4}{R3 + R4} \times \left(1 + \frac{R2}{R1}\right) - Vin\_pos\frac{R2}{R1}$$

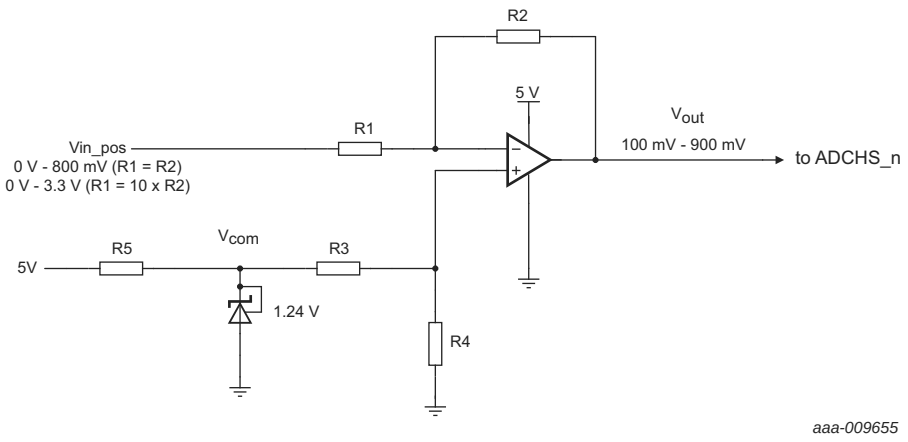


Fig 50. Inverting single-ended circuit for 12-bit ADCHS input