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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	I²C, IrDA, SPI, UART/USART
Peripherals	DMA, I²S, LVD, POR, PWM, WDT
Number of I/O	60
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 24x16b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	80-FQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mk11dx128vlk5

Field	Description	Values
Q	Qualification status	• M = Fully qualified, general market flow • P = Prequalification
C	Speed	• G = 50 MHz
F	Flash memory configuration	• G = 128 KB + Flex • H = 256 KB + Flex • 9 = 512 KB
T	Temperature range (°C)	• V = –40 to 105
PP	Package identifier	• MC = 121 MAPBGA

This tables lists some examples of small package marking along with the original part numbers:

Original part number	Alternate part number
MK11DX128VLK5	M11GGVLK
MK11DX256VMC5	M11GHVMC

3 Terminology and guidelines

3.1 Definition: Operating requirement

An *operating requirement* is a specified value or range of values for a technical characteristic that you must guarantee during operation to avoid incorrect operation and possibly decreasing the useful life of the chip.

3.1.1 Example

This is an example of an operating requirement:

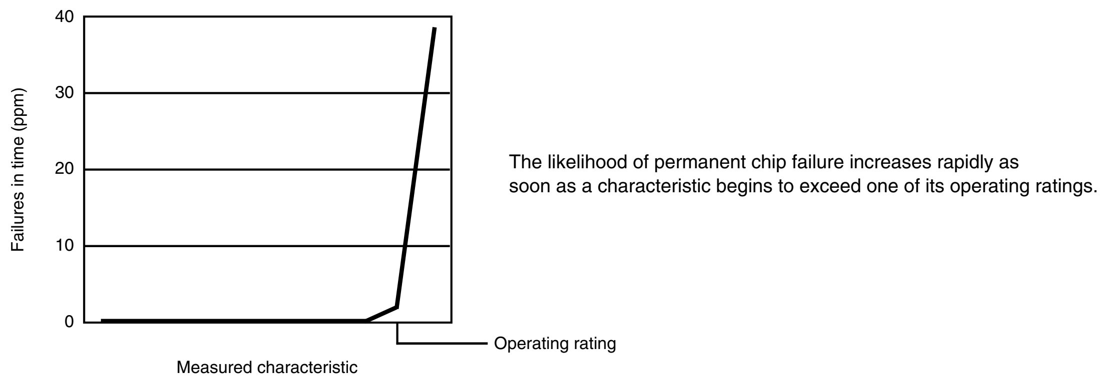
Symbol	Description	Min.	Max.	Unit
V_{DD}	1.0 V core supply voltage	0.9	1.1	V

3.4.1 Example

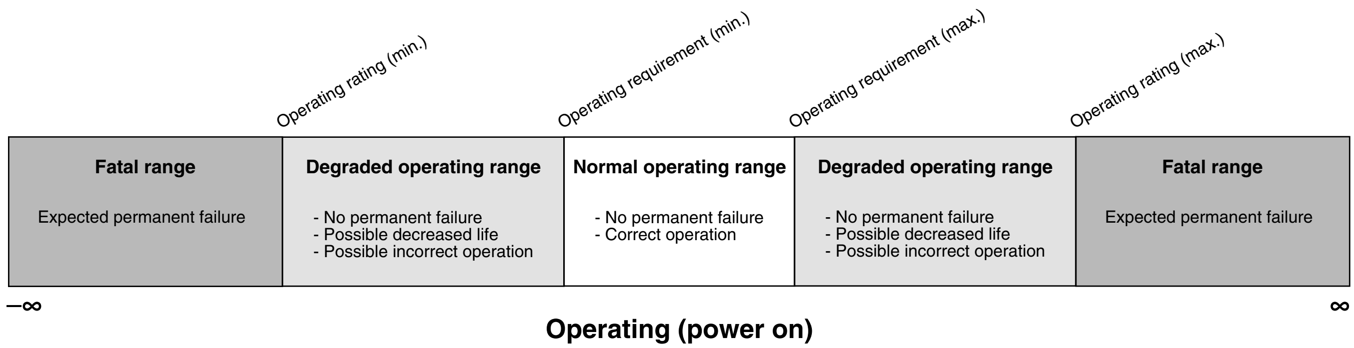
This is an example of an operating rating:

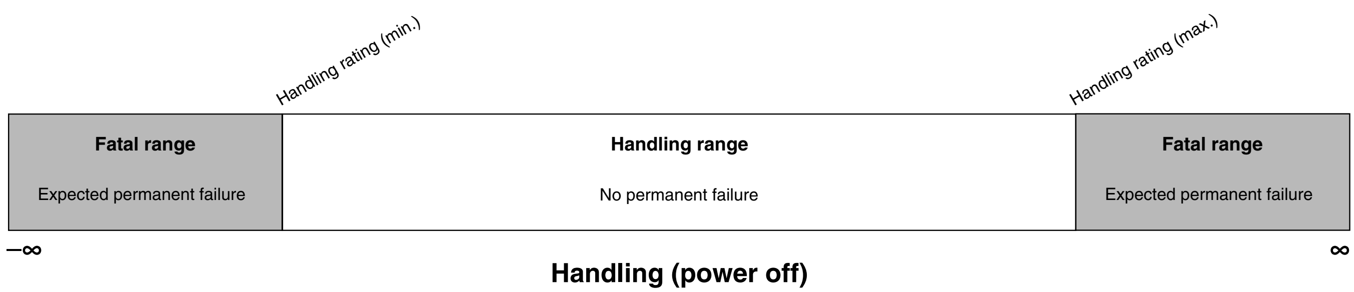
Symbol	Description	Min.	Max.	Unit
V_{DD}	1.0 V core supply voltage	–0.3	1.2	V

3.5 Result of exceeding a rating



3.6 Relationship between ratings and operating requirements





3.7 Guidelines for ratings and operating requirements

Follow these guidelines for ratings and operating requirements:

- Never exceed any of the chip's ratings.
- During normal operation, don't exceed any of the chip's operating requirements.
- If you must exceed an operating requirement at times other than during normal operation (for example, during power sequencing), limit the duration as much as possible.

3.8 Definition: Typical value

A *typical value* is a specified value for a technical characteristic that:

- Lies within the range of values specified by the operating behavior
- Given the typical manufacturing process, is representative of that characteristic during operation when you meet the typical-value conditions or other specified conditions

Typical values are provided as design guidelines and are neither tested nor guaranteed.

3.8.1 Example 1

This is an example of an operating behavior that includes a typical value:

Symbol	Description	Min.	Typ.	Max.	Unit
I_{WP}	Digital I/O weak pullup/pulldown current	10	70	130	µA

3.8.2 Example 2

This is an example of a chart that shows typical values for various voltage and temperature conditions:

4.2 Moisture handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
MSL	Moisture sensitivity level	—	3	—	1

1. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

4.3 ESD handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
V_{HBM}	Electrostatic discharge voltage, human body model	-2000	+2000	V	1
V_{CDM}	Electrostatic discharge voltage, charged-device model	-500	+500	V	2
I_{LAT}	Latch-up current at ambient temperature of 105°C	-100	+100	mA	3

1. Determined according to JEDEC Standard JESD22-A114, *Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)*.
2. Determined according to JEDEC Standard JESD22-C101, *Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components*.
3. Determined according to JEDEC Standard JESD78, *IC Latch-Up Test*.

4.4 Voltage and current operating ratings

Symbol	Description	Min.	Max.	Unit
V_{DD}	Digital supply voltage	–0.3	3.8	V
I_{DD}	Digital supply current	—	155	mA
V_{DIO}	Digital input voltage (except $\overline{\text{RESET}}$, EXTAL, and XTAL)	–0.3		V
V_{AIO}	Analog[1], $\overline{\text{RESET}}$, EXTAL, and XTAL input voltage	–0.3	V_{DD} + 0.3	V
I_D	Maximum current single pin limit (applies to all digital pins)	–25	25	mA
V_{DDA}	Analog supply voltage	V_{DD} – 0.3	V_{DD} + 0.3	V
VREGIN	USB regulator input	–0.3	6.0	V
V_{BAT}	RTC battery supply voltage	–0.3	3.8	V

1. Analog pins are defined as pins that do not have an associated general purpose I/O port function.

5 General

5.1 AC electrical characteristics

Unless otherwise specified, propagation delays are measured from the 50% to the 50% point, and rise and fall times are measured at the 20% and 80% points, as shown in the following figure.

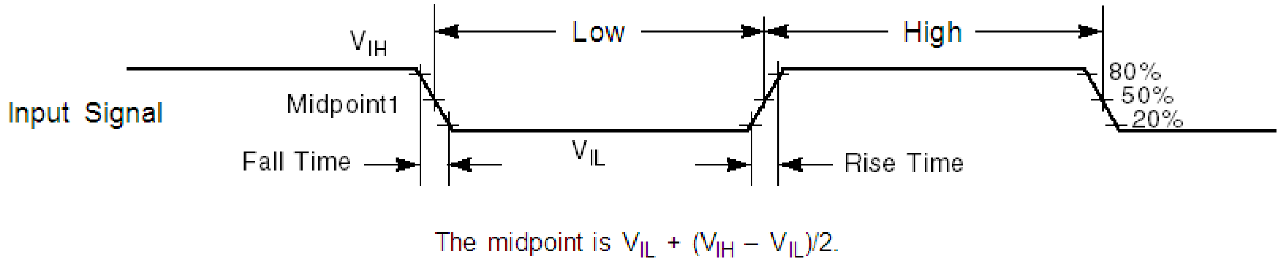


Figure 1. Input signal measurement reference

5.2 Nonswitching electrical specifications

5.2.1 Voltage and current operating requirements

Table 1. Voltage and current operating requirements

Symbol	Description	Min.	Max.	Unit	Notes
V_{DD}	Supply voltage	1.71	3.6	V	
V_{DDA}	Analog supply voltage	1.71	3.6	V	
$V_{DD} – V_{DDA}$	V_{DD}-to-V_{DDA} differential voltage	–0.1	0.1	V	
$V_{SS} – V_{SSA}$	V_{SS}-to-V_{SSA} differential voltage	–0.1	0.1	V	
V_{BAT}	RTC battery supply voltage	1.71	3.6	V	
V_{IH}	Input high voltage • $2.7\ V \le V_{DD} \le 3.6\ V$ • $1.7\ V \le V_{DD} \le 2.7\ V$	 $0.7 \times V_{DD}$ $0.75 \times V_{DD}$	 — —	 V V	
V_{IL}	Input low voltage • $2.7\ V \le V_{DD} \le 3.6\ V$ • $1.7\ V \le V_{DD} \le 2.7\ V$	 — —	 $0.35 \times V_{DD}$ $0.3 \times V_{DD}$	 V V	
V_{HYS}	Input hysteresis	$0.06 \times V_{DD}$	—	V	
I_{ICIO}	I/O pin DC injection current — single pin • $V_{IN} < V_{SS}$-0.3V (Negative current injection) • $V_{IN} > V_{DD}$+0.3V (Positive current injection)	 -3 —	 — +3	 mA	1

Table continues on the next page...

5.2.4 Power mode transition operating behaviors

All specifications except t_{POR}, and VLLSx→RUN recovery times in the following table assume this clock configuration:

- CPU and system clocks = 50 MHz
- Bus clock = 50 MHz
- Flash clock = 25 MHz
- MCG mode: FEI

Table 5. Power mode transition operating behaviors

Symbol	Description	Min.	Max.	Unit	Notes
t_{POR}	After a POR event, amount of time from the point V_{DD} reaches 1.71 V to execution of the first instruction across the operating temperature range of the chip. • 1.71 V/(V_{DD} slew rate) ≤ 300 μs • 1.71 V/(V_{DD} slew rate) > 300 μs	 — —	 300 1.7 V / (V_{DD} slew rate)	μs	1
	• VLLS0 → RUN	—	135	μs	
	• VLLS1 → RUN	—	135	μs	
	• VLLS2 → RUN	—	85	μs	
	• VLLS3 → RUN	—	85	μs	
	• LLS → RUN	—	6	μs	
	• VLPS → RUN	—	5.2	μs	
	• STOP → RUN	—	5.2	μs	

1. Normal boot (FTFL_OPT[LPBOOT]=1)

5.2.5 Power consumption operating behaviors

Table 6. Power consumption operating behaviors

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I_{DDA}	Analog supply current	—	—	See note	mA	1
I_{DD_RUN}	Run mode current — all peripheral clocks disabled, code executing from flash • @ 1.8 V • @ 3.0 V	 — —	 12.98 12.93	 14 13.8	 mA mA	2

Table continues on the next page...

Table 6. Power consumption operating behaviors (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes

I_{DD_RUN}	Run mode current — all peripheral clocks enabled, code executing from flash
	• @ 1.8 V
	• @ 3.0 V
	  • @ 25°C
	  • @ 125°C
		
		—
		
		—
		—
			
			17.04
			
			17.01
			19.8
				
				19.3
				
				18.9
				21.3
					
					mA
					
					mA
					mA
						3, 4

I_{DD_WAIT}	Wait mode high frequency current at 3.0 V — all peripheral clocks disabled	—	7.95	9.5	mA	2
I_{DD_WAIT}	Wait mode reduced frequency current at 3.0 V — all peripheral clocks disabled	—	5.88	7.4	mA	5
I_{DD_STOP}	Stop mode current at 3.0 V • @ –40 to 25°C • @ 50°C • @ 70°C • @ 105°C	—	320 360 410 610	436 489 620 1100	μA	
I_{DD_VLPR}	Very-low-power run mode current at 3.0 V — all peripheral clocks disabled	—	754	—	μA	6
I_{DD_VLPR}	Very-low-power run mode current at 3.0 V — all peripheral clocks enabled	—	1.1	—	mA	7
I_{DD_VLPW}	Very-low-power wait mode current at 3.0 V	—	437	—	μA	8
I_{DD_VLPS}	Very-low-power stop mode current at 3.0 V • @ –40 to 25°C • @ 50°C • @ 70°C • @ 105°C	—	7.33 14 28 110	24.2 32 48 280	μA	
I_{DD_LLS}	Low leakage stop mode current at 3.0 V • @ –40 to 25°C • @ 50°C • @ 70°C • @ 105°C	—	3.14 6.48 13.85 55.53	4.8 28.3 44.6 71.3	μA	
I_{DD_VLLS3}	Very low-leakage stop mode 3 current at 3.0 V • @ –40 to 25°C • @ 50°C • @ 70°C • @ 105°C	—	2.19 4.35 8.92 35.33	3.4 4.35 24.6 45.3	μA	
I_{DD_VLLS2}	Very low-leakage stop mode 2 current at 3.0 V • @ –40 to 25°C • @ 50°C • @ 70°C • @ 105°C	—	1.77 2.81 5.20 19.88	3.1 13.8 22.3 34.2	μA	

Table continues on the next page...

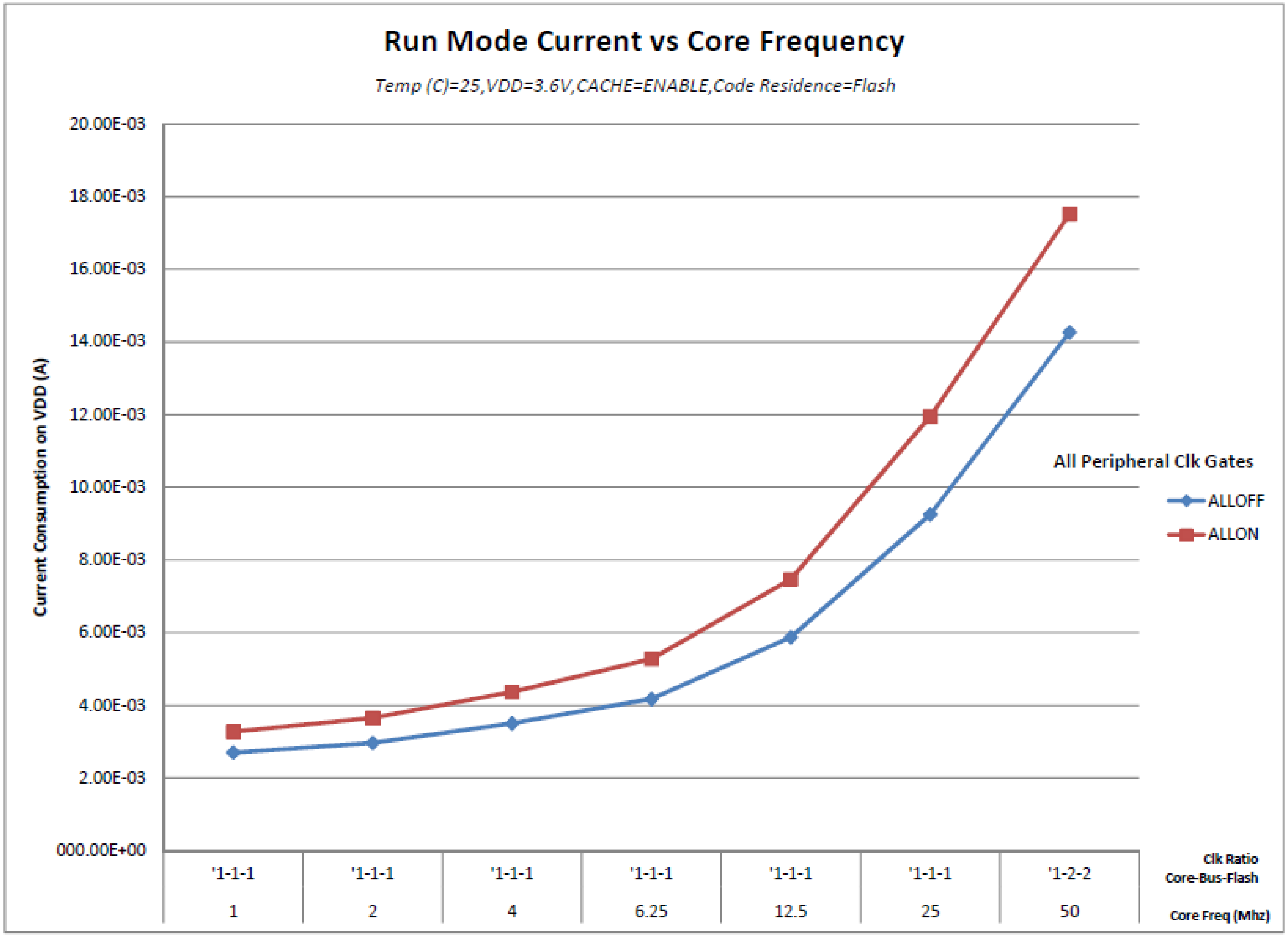


Figure 2. Run mode supply current vs. core frequency

1. The frequency limitations in VLPR mode here override any frequency specification listed in the timing specification for any other module.

5.3.2 General switching specifications

These general purpose specifications apply to all pins configured for:

- GPIO signaling
- Other peripheral module signaling not explicitly stated elsewhere

Table 10. General switching specifications

Symbol	Description	Min.	Max.	Unit	Notes
	GPIO pin interrupt pulse width (digital glitch filter disabled) — Synchronous path	1.5	—	Bus clock cycles	1, 2
	GPIO pin interrupt pulse width (digital glitch filter disabled, analog filter enabled) — Asynchronous path	100	—	ns	3
	GPIO pin interrupt pulse width (digital glitch filter disabled, analog filter disabled) — Asynchronous path	50	—	ns	3
	External reset pulse width (digital glitch filter disabled)	100	—	ns	3
	Port rise and fall time (high drive strength)				4
	• Slew disabled				
	• $1.71 \leq V_{DD} \leq 2.7V$	—	13	ns	
	• $2.7 \leq V_{DD} \leq 3.6V$	—	7	ns	
	• Slew enabled				
	• $1.71 \leq V_{DD} \leq 2.7V$	—	36	ns	
	• $2.7 \leq V_{DD} \leq 3.6V$	—	24	ns	
	Port rise and fall time (low drive strength)				5
	• Slew disabled				
	• $1.71 \leq V_{DD} \leq 2.7V$	—	12	ns	
	• $2.7 \leq V_{DD} \leq 3.6V$	—	6	ns	
	• Slew enabled				
	• $1.71 \leq V_{DD} \leq 2.7V$	—	36	ns	
	• $2.7 \leq V_{DD} \leq 3.6V$	—	24	ns	

1. This is the minimum pulse width that is guaranteed to pass through the pin synchronization circuitry. Shorter pulses may or may not be recognized. In Stop, VLPS, LLS, and VLLSx modes, the synchronizer is bypassed so shorter pulses can be recognized in that case.
2. The greater synchronous and asynchronous timing must be met.
3. This is the minimum pulse width that is guaranteed to be recognized as a pin interrupt request in Stop, VLPS, LLS, and VLLSx modes.
4. 75 pF load
5. 15 pF load

5.4 Thermal specifications

5.4.1 Thermal operating requirements

Table 11. Thermal operating requirements

Symbol	Description	Min.	Max.	Unit
T_J	Die junction temperature	–40	125	°C
T_A	Ambient temperature	–40	105	°C

5.4.2 Thermal attributes

Board type	Symbol	Description	80 LQFP	Unit	Notes
Single-layer (1s)	$R_{θJA}$	Thermal resistance, junction to ambient (natural convection)	50	°C/W	1, 2
Four-layer (2s2p)	$R_{θJA}$	Thermal resistance, junction to ambient (natural convection)	35	°C/W	1, 3
Single-layer (1s)	$R_{θJMA}$	Thermal resistance, junction to ambient (200 ft./min. air speed)	39	°C/W	1,3
Four-layer (2s2p)	$R_{θJMA}$	Thermal resistance, junction to ambient (200 ft./min. air speed)	29	°C/W	1,3
—	$R_{θJB}$	Thermal resistance, junction to board	19	°C/W	4
—	$R_{θJC}$	Thermal resistance, junction to case	8	°C/W	5
—	$Ψ_{JT}$	Thermal characterization parameter, junction to package top outside center (natural convection)	2	°C/W	6

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Determined according to JEDEC Standard JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions—Natural Convection (Still Air)* with the single layer board horizontal. For the LQFP, the board meets the JESD51-3 specification. For the MAPBGA, the board meets the JESD51-9 specification.

Table 13. JTAG full voltage range electricals

Symbol	Description	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
J1	TCLK frequency of operation • Boundary Scan • JTAG and CJTAG • Serial Wire Debug	 0 0 0	 10 20 40	MHz
J2	TCLK cycle period	1/J1	—	ns
J3	TCLK clock pulse width • Boundary Scan • JTAG and CJTAG • Serial Wire Debug	 50 25 12.5	 — — —	 ns ns ns
J4	TCLK rise and fall times	—	3	ns
J5	Boundary scan input data setup time to TCLK rise	20	—	ns
J6	Boundary scan input data hold time after TCLK rise	0	—	ns
J7	TCLK low to boundary scan output data valid	—	25	ns
J8	TCLK low to boundary scan output high-Z	—	25	ns
J9	TMS, TDI input data setup time to TCLK rise	8	—	ns
J10	TMS, TDI input data hold time after TCLK rise	1.4	—	ns
J11	TCLK low to TDO data valid	—	22.1	ns
J12	TCLK low to TDO high-Z	—	22.1	ns
J13	$\overline{\text{TRST}}$ assert time	100	—	ns
J14	$\overline{\text{TRST}}$ setup time (negation) to TCLK high	8	—	ns

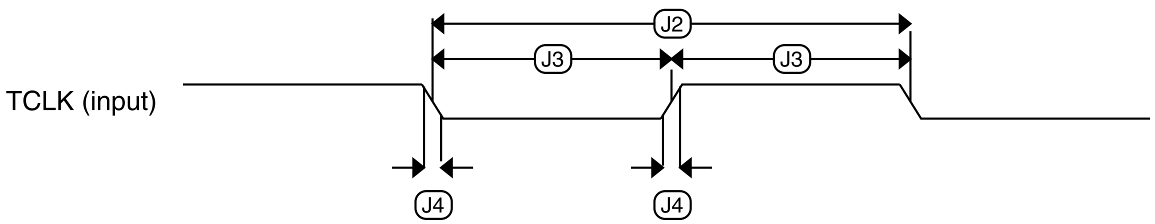


Figure 4. Test clock input timing

Table 22. NVM reliability specifications (continued)

Symbol	Description	Min.	Typ.[1]	Max.	Unit	Notes
$t_{nvmretd1k}$	Data retention after up to 1 K cycles	20	100	—	years	
$n_{nvmcycd}$	Cycling endurance	10 K	50 K	—	cycles	2
FlexRAM as EEPROM						
$t_{nvmretee100}$	Data retention up to 100% of write endurance	5	50	—	years	
$t_{nvmretee10}$	Data retention up to 10% of write endurance	20	100	—	years	
	Write endurance					3
$n_{nvmwree16}$	• EEPROM backup to FlexRAM ratio = 16	35 K	175 K	—	writes	
$n_{nvmwree128}$	• EEPROM backup to FlexRAM ratio = 128	315 K	1.6 M	—	writes	
$n_{nvmwree512}$	• EEPROM backup to FlexRAM ratio = 512	1.27 M	6.4 M	—	writes	
$n_{nvmwree4k}$	• EEPROM backup to FlexRAM ratio = 4096	10 M	50 M	—	writes	

1. Typical data retention values are based on measured response accelerated at high temperature and derated to a constant 25 °C use profile. Engineering Bulletin EB618 does not apply to this technology. Typical endurance defined in Engineering Bulletin EB619.
2. Cycling endurance represents number of program/erase cycles at -40 °C ≤ T_j ≤ °C.
3. Write endurance represents the number of writes to each FlexRAM location at -40 °C ≤Tj ≤ °C influenced by the cycling endurance of the FlexNVM (same value as data flash) and the allocated EEPROM backup per subsystem. Minimum and typical values assume all byte-writes to FlexRAM.

6.4.2 EzPort switching specifications

Table 23. EzPort switching specifications

Num	Description	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
EP1	EZP_CK frequency of operation (all commands except READ)	—	$f_{SYS}/2$	MHz
EP1a	EZP_CK frequency of operation (READ command)	—	$f_{SYS}/8$	MHz
EP2	$\overline{\text{EZP\_CS}}$ negation to next $\overline{\text{EZP\_CS}}$ assertion	2 x t_{EZP_CK}	—	ns
EP3	$\overline{\text{EZP\_CS}}$ input valid to EZP_CK high (setup)	5	—	ns
EP4	EZP_CK high to $\overline{\text{EZP\_CS}}$ input invalid (hold)	5	—	ns
EP5	EZP_D input valid to EZP_CK high (setup)	2	—	ns
EP6	EZP_CK high to EZP_D input invalid (hold)	5	—	ns
EP7	EZP_CK low to EZP_Q output valid	—		ns
EP8	EZP_CK low to EZP_Q output invalid (hold)	0	—	ns
EP9	$\overline{\text{EZP\_CS}}$ negation to EZP_Q tri-state	—	12	ns

6.6.2 CMP and 6-bit DAC electrical specifications

Table 26. Comparator and 6-bit DAC electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit
V_{DD}	Supply voltage	1.71	—	3.6	V
I_{DDHS}	Supply current, High-speed mode (EN=1, PMODE=1)	—	—	200	μA
I_{DDLS}	Supply current, low-speed mode (EN=1, PMODE=0)	—	—	20	μA
V_{AIN}	Analog input voltage	V_{SS} – 0.3	—	V_{DD}	V
V_{AIO}	Analog input offset voltage	—	—	20	mV
V_H	Analog comparator hysteresis[1]				
	• CR0[HYSTCTR] = 00	—	5	—	mV
	• CR0[HYSTCTR] = 01	—	10	—	mV
	• CR0[HYSTCTR] = 10	—	20	—	mV
	• CR0[HYSTCTR] = 11	—	30	—	mV
V_{CMPOh}	Output high	V_{DD} – 0.5	—	—	V
V_{CMPOl}	Output low	—	—	0.5	V
t_{DHS}	Propagation delay, high-speed mode (EN=1, PMODE=1)	20	50	200	ns
t_{DLS}	Propagation delay, low-speed mode (EN=1, PMODE=0)	80	250	600	ns
	Analog comparator initialization delay[2]	—	—	40	μs
I_{DAC6b}	6-bit DAC current adder (enabled)	—	7	—	μA
INL	6-bit DAC integral non-linearity	–0.5	—	0.5	LSB[3]
DNL	6-bit DAC differential non-linearity	–0.3	—	0.3	LSB

1. Typical hysteresis is measured with input voltage range limited to 0.6 to V_{DD}–0.6 V.
2. Comparator initialization delay is defined as the time between software writes to change control inputs (Writes to CMP_DACCR[DACEN], CMP_DACCR[VRSEL], CMP_DACCR[VOSEL], CMP_MUXCR[PSEL], and CMP_MUXCR[MSEL]) and the comparator output settling to a stable level.
3. 1 LSB = $V_{reference}$/64

6.8.1 DSPI switching specifications (limited voltage range)

The DMA Serial Peripheral Interface (DSPI) provides a synchronous serial bus with master and slave operations. Many of the transfer attributes are programmable. The tables below provide DSPI timing characteristics for classic SPI timing modes. Refer to the DSPI chapter of the Reference Manual for information on the modified transfer formats used for communicating with slower peripheral devices.

Table 27. Master mode DSPI timing (limited voltage range)

Num	Description	Min.	Max.	Unit	Notes
	Operating voltage	2.7	3.6	V	
	Frequency of operation	—	25	MHz	
DS1	DSPI_SCK output cycle time	2 x t_{BUS}	—	ns	
DS2	DSPI_SCK output high/low time	$(t_{SCK}/2) - 2$	$(t_{SCK}/2) + 2$	ns	
DS3	DSPI_PCS*n* valid to DSPI_SCK delay	$(t_{BUS} \times 2) - 2$	—	ns	1
DS4	DSPI_SCK to DSPI_PCS*n* invalid delay	$(t_{BUS} \times 2) - 2$	—	ns	2
DS5	DSPI_SCK to DSPI_SOUT valid	—	8.5	ns	
DS6	DSPI_SCK to DSPI_SOUT invalid	–2	—	ns	
DS7	DSPI_SIN to DSPI_SCK input setup	15	—	ns	
DS8	DSPI_SCK to DSPI_SIN input hold	0	—	ns	

1. The delay is programmable in SPIx_CTARn[PSSCK] and SPIx_CTARn[CSSCK].
2. The delay is programmable in SPIx_CTARn[PASC] and SPIx_CTARn[ASC].

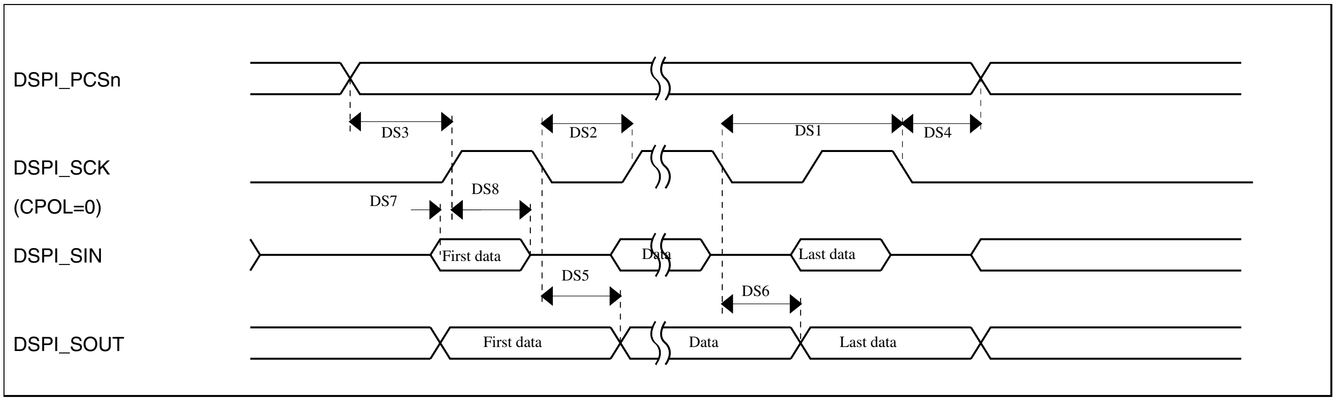


Figure 14. DSPI classic SPI timing — master mode

Table 28. Slave mode DSPI timing (limited voltage range)

Num	Description	Min.	Max.	Unit
	Operating voltage	2.7	3.6	V
	Frequency of operation		12.5	MHz
DS9	DSPI_SCK input cycle time	4 x t_{BUS}	—	ns

Table continues on the next page...

Table 28. Slave mode DSPI timing (limited voltage range) (continued)

Num	Description	Min.	Max.	Unit
DS10	DSPI_SCK input high/low time	$(t_{SCK}/2) - 2$	$(t_{SCK}/2) + 2$	ns
DS11	DSPI_SCK to DSPI_SOUT valid	—	10	ns
DS12	DSPI_SCK to DSPI_SOUT invalid	0	—	ns
DS13	DSPI_SIN to DSPI_SCK input setup	2	—	ns
DS14	DSPI_SCK to DSPI_SIN input hold	7	—	ns
DS15	$\overline{\text{DSPI\_SS}}$ active to DSPI_SOUT driven	—	14	ns
DS16	$\overline{\text{DSPI\_SS}}$ inactive to DSPI_SOUT not driven	—	14	ns

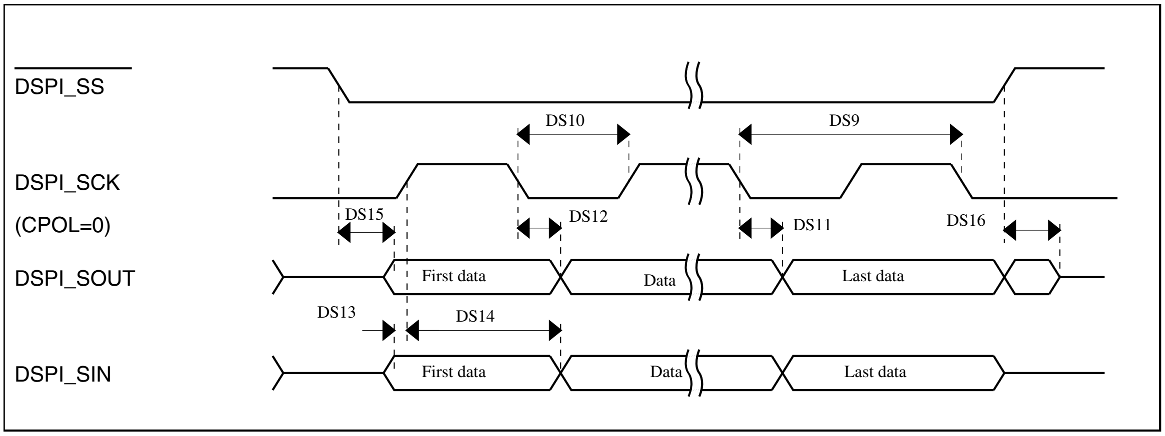


Figure 15. DSPI classic SPI timing — slave mode

6.8.2 DSPI switching specifications (full voltage range)

The DMA Serial Peripheral Interface (DSPI) provides a synchronous serial bus with master and slave operations. Many of the transfer attributes are programmable. The tables below provides DSPI timing characteristics for classic SPI timing modes. Refer to the DSPI chapter of the Reference Manual for information on the modified transfer formats used for communicating with slower peripheral devices.

Table 29. Master mode DSPI timing (full voltage range)

Num	Description	Min.	Max.	Unit	Notes
	Operating voltage	1.71	3.6	V	1
	Frequency of operation	—	12.5	MHz	
DS1	DSPI_SCK output cycle time	$4 \times t_{BUS}$	—	ns	
DS2	DSPI_SCK output high/low time	$(t_{SCK}/2) - 4$	$(t_{SCK/2}) + 4$	ns	
DS3	DSPI_PCS*n* valid to DSPI_SCK delay	$(t_{BUS} \times 2) - 4$	—	ns	2

Table continues on the next page...

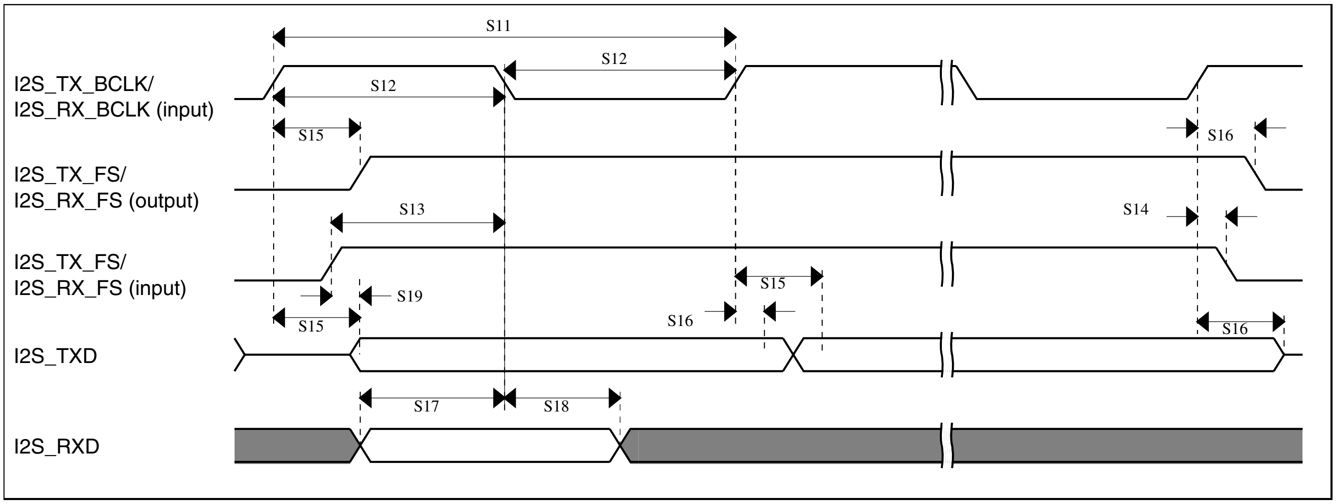


Figure 19. I2S/SAI timing — slave modes

6.8.6 VLPR, VLPW, and VLPS mode performance over the full operating voltage range

This section provides the operating performance over the full operating voltage for the device in VLPR, VLPW, and VLPS modes.

Table 33. I2S/SAI master mode timing in VLPR, VLPW, and VLPS modes (full voltage range)

Num.	Characteristic	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
S1	I2S_MCLK cycle time	62.5	—	ns
S2	I2S_MCLK pulse width high/low	45%	55%	MCLK period
S3	I2S_TX_BCLK/I2S_RX_BCLK cycle time (output)	250	—	ns
S4	I2S_TX_BCLK/I2S_RX_BCLK pulse width high/low	45%	55%	BCLK period
S5	I2S_TX_BCLK/I2S_RX_BCLK to I2S_TX_FS/ I2S_RX_FS output valid	—	45	ns
S6	I2S_TX_BCLK/I2S_RX_BCLK to I2S_TX_FS/ I2S_RX_FS output invalid	0	—	ns
S7	I2S_TX_BCLK to I2S_TXD valid	—	45	ns
S8	I2S_TX_BCLK to I2S_TXD invalid	0	—	ns
S9	I2S_RXD/I2S_RX_FS input setup before I2S_RX_BCLK	75	—	ns
S10	I2S_RXD/I2S_RX_FS input hold after I2S_RX_BCLK	0	—	ns

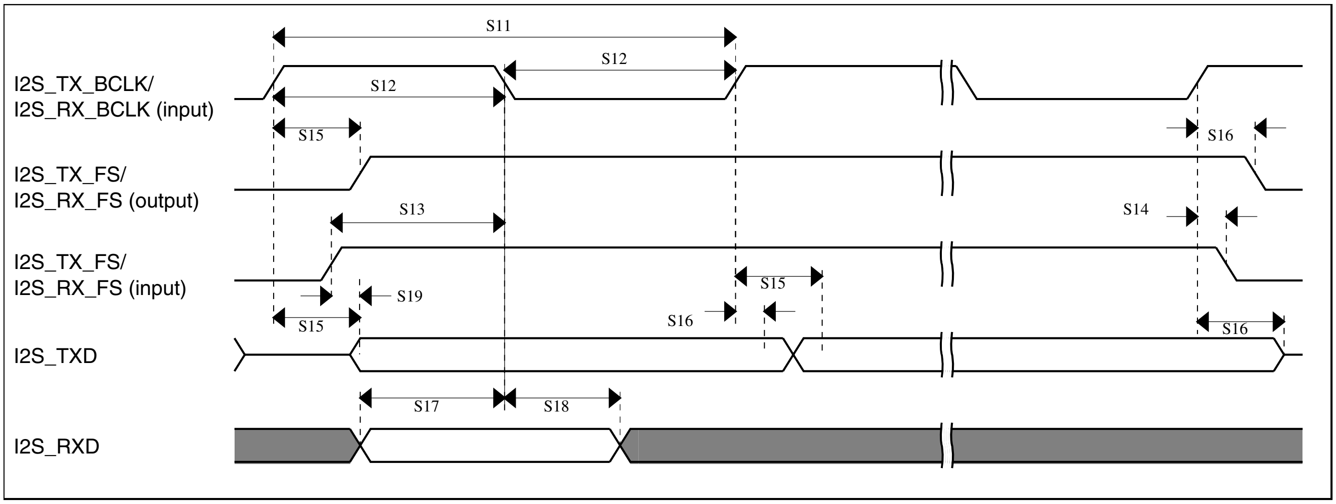


Figure 21. I2S/SAI timing — slave modes

7 Dimensions

7.1 Obtaining package dimensions

Package dimensions are provided in package drawings.

To find a package drawing, go to freescale.com and perform a keyword search for the drawing's document number:

If you want the drawing for this package	Then use this document number
80-pin LQFP	98ASS23174W

8 Pinout

8.1 K11 Signal Multiplexing and Pin Assignments

The following table shows the signals available on each pin and the locations of these pins on the devices supported by this document. The Port Control Module is responsible for selecting which ALT functionality is available on each pin.

NOTE

- The analog input signals ADC0_SE10, ADC0_SE11, ADC0_DP1, and ADC0_DM1 are available only for K11, K12, K21, and K22 devices and are not present on K10 and K20 devices.

- The TRACE signals on PTE0, PTE1, PTE2, PTE3, and PTE4 are available only for K11, K12, K21, and K22 devices and are not present on K10 and K20 devices.
- If the VBAT pin is not used, the VBAT pin should be left floating. Do not connect VBAT pin to VSS.
- The FTM_CLKIN signals on PTB16 and PTB17 are available only for K11, K12, K21, and K22 devices and is not present on K10 and K20 devices. For K22D devices this signal is on ALT4, and for K22F devices, this signal is on ALT7.
- The FTM0_CH2 signal on PTC5/LLWU_P9 is available only for K11, K12, K21, and K22 devices and is not present on K10 and K20 devices.
- The I2C0_SCL signal on PTD2/LLWU_P13 and I2C0_SDA signal on PTD3 are available only for K11, K12, K21, and K22 devices and are not present on K10 and K20 devices.

80 LQFP	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
1	ADC0_SE10	ADC0_SE10	PTE0	SPI1_PCS1	UART1_TX		TRACE_CLKOUT	I2C1_SDA	RTC_CLKOUT	
2	ADC0_SE11	ADC0_SE11	PTE1/ LLWU_P0	SPI1_SOUT	UART1_RX		TRACE_D3	I2C1_SCL	SPI1_SIN	
3	ADC0_DP1	ADC0_DP1	PTE2/ LLWU_P1	SPI1_SCK	UART1_CTS_b		TRACE_D2			
4	ADC0_DM1	ADC0_DM1	PTE3	SPI1_SIN	UART1_RTS_b		TRACE_D1		SPI1_SOUT	
5	DISABLED		PTE4/ LLWU_P2	SPI1_PCS0	UART3_TX		TRACE_D0			
6	DISABLED		PTE5	SPI1_PCS2	UART3_RX					
7	VDD	VDD								
8	VSS	VSS								
9	ADC0_SE4a	ADC0_SE4a	PTE16	SPI0_PCS0	UART2_TX	FTM_CLKIN0		FTM0_FLT3		
10	ADC0_SE5a	ADC0_SE5a	PTE17	SPI0_SCK	UART2_RX	FTM_CLKIN1		LPTMR0_ALT3		
11	ADC0_SE6a	ADC0_SE6a	PTE18	SPI0_SOUT	UART2_CTS_b	I2C0_SDA				
12	ADC0_SE7a	ADC0_SE7a	PTE19	SPI0_SIN	UART2_RTS_b	I2C0_SCL				
13	ADC0_DP0	ADC0_DP0								
14	ADC0_DM0	ADC0_DM0								
15	ADC0_DP3	ADC0_DP3								
16	ADC0_DM3	ADC0_DM3								
17	VDDA	VDDA								
18	VREFH	VREFH								
19	VREFL	VREFL								

80 LQFP	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
20	VSSA	VSSA								
21	TAMPER0/ RTC_WAKEUP_ B	TAMPER0/ RTC_WAKEUP_ B								
22	TAMPER1	TAMPER1								
23	XTAL32	XTAL32								
24	EXTAL32	EXTAL32								
25	VBAT	VBAT								
26	JTAG_TCLK/ SWD_CLK/ EZP_CLK		PTA0	UART0_CTS_b/ UART0_COL_b	FTM0_CH5				JTAG_TCLK/ SWD_CLK	EZP_CLK
27	JTAG_TDI/ EZP_DI		PTA1	UART0_RX	FTM0_CH6				JTAG_TDI	EZP_DI
28	JTAG_TDO/ TRACE_SWO/ EZP_DO		PTA2	UART0_TX	FTM0_CH7				JTAG_TDO/ TRACE_SWO	EZP_DO
29	JTAG_TMS/ SWD_DIO		PTA3	UART0_RTS_b	FTM0_CH0				JTAG_TMS/ SWD_DIO	
30	NMI_b/ EZP_CS_b		PTA4/ LLWU_P3		FTM0_CH1				NMI_b	EZP_CS_b
31	DISABLED		PTA5		FTM0_CH2			I2S0_TX_BCLK	JTAG_TRST_b	
32	DISABLED		PTA12		FTM1_CH0			I2S0_TXD0	FTM1_QD_PHA	
33	DISABLED		PTA13/ LLWU_P4		FTM1_CH1			I2S0_TX_FS	FTM1_QD_PHB	
34	DISABLED		PTA14	SPI0_PCS0	UART0_TX			I2S0_RX_BCLK	I2S0_TXD1	
35	DISABLED		PTA15	SPI0_SCK	UART0_RX			I2S0_RXD0		
36	DISABLED		PTA16	SPI0_SOUT	UART0_CTS_b/ UART0_COL_b			I2S0_RX_FS	I2S0_RXD1	
37	DISABLED		PTA17	SPI0_SIN	UART0_RTS_b			I2S0_MCLK		
38	VDD	VDD								
39	VSS	VSS								
40	EXTAL0	EXTAL0	PTA18		FTM0_FLT2	FTM_CLKIN0				
41	XTAL0	XTAL0	PTA19		FTM1_FLT0	FTM_CLKIN1		LPTMR0_ALT1		
42	RESET_b	RESET_b								
43	ADC0_SE8	ADC0_SE8	PTB0/ LLWU_P5	I2C0_SCL	FTM1_CH0			FTM1_QD_PHA		
44	ADC0_SE9	ADC0_SE9	PTB1	I2C0_SDA	FTM1_CH1			FTM1_QD_PHB		
45	ADC0_SE12	ADC0_SE12	PTB2	I2C0_SCL	UART0_RTS_b			FTM0_FLT3		
46	ADC0_SE13	ADC0_SE13	PTB3	I2C0_SDA	UART0_CTS_b/ UART0_COL_b			FTM0_FLT0		
47	DISABLED		PTB10	SPI1_PCS0	UART3_RX			FTM0_FLT1		
48	DISABLED		PTB11	SPI1_SCK	UART3_TX			FTM0_FLT2		
49	DISABLED		PTB12	UART3_RTS_b	FTM1_CH0	FTM0_CH4		FTM1_QD_PHA		
50	DISABLED		PTB13	UART3_CTS_b	FTM1_CH1	FTM0_CH5		FTM1_QD_PHB		
51	DISABLED		PTB16	SPI1_SOUT	UART0_RX			EWM_IN	FTM_CLKIN0	

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