Renesas Electronics America Inc - R5F51303ADFK#30 Datasheet

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	RX
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	I²C, LINbus, SCI, SPI
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	52
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	8K x 8
RAM Size	10K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 14x12b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f51303adfk-30

Table 4.1 List of I/O Registers (Address Order) (5 / 18)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles
0008 864Ah	MTU4	Timer A/D Converter Start Request Cycle Set Buffer Register B	TADCOBRB	16	16	2 or 3 PCLKB
0008 8660h	MTU	Timer Waveform Control Register	TWCR	8	8, 16	2 or 3 PCLKB
0008 8680h	MTU	Timer Start Register	TSTR	8	8, 16	2 or 3 PCLKB
0008 8681h	MTU	Timer Synchronous Register	TSYR	8	8, 16	2 or 3 PCLKB
0008 8684h	MTU	Timer Read/Write Enable Register	TRWER	8	8, 16	2 or 3 PCLKB
0008 8690h	MTU0	Noise Filter Control Register	NFCR	8	8, 16	2 or 3 PCLKB
0008 8691h	MTU1	Noise Filter Control Register	NFCR	8	8, 16	2 or 3 PCLKB
0008 8692h	MTU2	Noise Filter Control Register	NFCR	8	8, 16	2 or 3 PCLKB
0008 8693h	MTU3	Noise Filter Control Register	NFCR	8	8, 16	2 or 3 PCLKB
0008 8694h	MTU4	Noise Filter Control Register	NFCR	8	8, 16	2 or 3 PCLKB
0008 8695h	MTU5	Noise Filter Control Register	NFCR	8	8, 16	2 or 3 PCLKB
0008 8700h	MTU0	Timer Control Register	TCR	8	8	2 or 3 PCLKB
0008 8701h	MTU0	Timer Mode Register	TMDR	8	8	2 or 3 PCLKB
0008 8702h	MTU0	Timer I/O Control Register H	TIORH	8	8	2 or 3 PCLKB
0008 8703h	MTU0	Timer I/O Control Register L	TIORL	8	8	2 or 3 PCLKB
0008 8704h	MTU0	Timer Interrupt Enable Register	TIER	8	8	2 or 3 PCLKB
0008 8705h	MTU0	Timer Status Register	TSR	8	8	2 or 3 PCLKB
0008 8706h	MTU0	Timer Counter	TCNT	16	16	2 or 3 PCLKB
0008 8708h	MTU0	Timer General Register A	TGRA	16	16	2 or 3 PCLKB
0008 870Ah	MTU0	Timer General Register B	TGRB	16	16	2 or 3 PCLKB
0008 870Ch	MTU0	Timer General Register C	TGRC	16	16	2 or 3 PCLKB
0008 870Eh	MTU0	Timer General Register D	TGRD	16	16	2 or 3 PCLKB
0008 8720h	MTU0	Timer General Register E	TGRE	16	16	2 or 3 PCLKB
0008 8722h	MTU0	Timer General Register F	TGRF	16	16	2 or 3 PCLKB
0008 8724h	MTU0	Timer Interrupt Enable Register 2	TIER2	8	8	2 or 3 PCLKB
0008 8726h	MTU0	Timer Buffer Operation Transfer Mode Register	TBTM	8	8	2 or 3 PCLKB
0008 8780h	MTU1	Timer Control Register	TCR	8	8	2 or 3 PCLKB
0008 8781h	MTU1	Timer Mode Register	TMDR	8	8	2 or 3 PCLKB
0008 8782h	MTU1	Timer I/O Control Register	TIOR	8	8	2 or 3 PCLKB
0008 8784h	MTU1	Timer Interrupt Enable Register	TIER	8	8	2 or 3 PCLKB
0008 8785h	MTU1	Timer Status Register	TSR	8	8	2 or 3 PCLKB
0008 8786h	MTU1	Timer Counter	TCNT	16	16	2 or 3 PCLKB
0008 8788h	MTU1	Timer General Register A	TGRA	16	16	2 or 3 PCLKB
0008 878Ah	MTU1	Timer General Register B	TGRB	16	16	2 or 3 PCLKB
0008 8790h	MTU1	Timer Input Capture Control Register	TICCR	8	8	2 or 3 PCLKB
0008 8800h	MTU2	Timer Control Register	TCR	8	8	2 or 3 PCLKB
0008 8801h	MTU2	Timer Mode Register	TMDR	8	8	2 or 3 PCLKB
0008 8802h	MTU2	Timer I/O Control Register	TIOR	8	8	2 or 3 PCLKB
0008 8804h	MTU2	Timer Interrupt Enable Register	TIER	8	8	2 or 3 PCLKB
0008 8805h	MTU2	Timer Status Register	TSR	8	8	2 or 3 PCLKB
0008 8806h	MTU2	Timer Counter	TCNT	16	16	2 or 3 PCLKB
0008 8808h	MTU2	Timer General Register A	TGRA	16	16	2 or 3 PCLKB
0008 880Ah	MTU2	Timer General Register B	TGRB	16	16	2 or 3 PCLKB
0008 8880h	MTU5	Timer Counter U	TCNTU	16	16	2 or 3 PCLKB
0008 8882h	MTU5	Timer General Register U	TGRU	16	16	2 or 3 PCLKB
0008 8884h	MTU5	Timer Control Register U	TCRU	8	8	2 or 3 PCLKB
0008 8886h	MTU5	Timer I/O Control Register U	TIORU	8	8	2 or 3 PCLKB
0008 8890h	MTU5	Timer Counter V	TCNTV	16	16	2 or 3 PCLKB
0008 8892h	MTU5	Timer General Register V	TGRV	16	16	2 or 3 PCLKB
0008 8894h	MTU5	Timer Control Register V	TCRV	8	8	2 or 3 PCLKB
0008 8896h	MTU5	Timer I/O Control Register V	TIORV	8	8	2 or 3 PCLKB
0008 88A0h	MTU5	Timer Counter W	TCNTW	16	16	2 or 3 PCLKB

Table 4.1 List of I/O Registers (Address Order) (16 / 18)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles
0008 C414h	RTC	Binary Counter 2 Alarm Register	BCNT2AR	8	8	2 or 3 PCLKB
0008 C416h	RTC	Day-of-Week Alarm Register	RWKAR	8	8	2 or 3 PCLKB
0008 C416h	RTC	Binary Counter 3 Alarm Register	BCNT3AR	8	8	2 or 3 PCLKB
0008 C418h	RTC	Date Alarm Register	RDAYAR	8	8	2 or 3 PCLKB
0008 C418h	RTC	Binary Counter 0 Alarm Enable Register	BCNT0AER	8	8	2 or 3 PCLKB
0008 C41Ah	RTC	Month Alarm Register	RMONAR	8	8	2 or 3 PCLKB
0008 C41Ah	RTC	Binary Counter 1 Alarm Enable Register	BCNT1AER	8	8	2 or 3 PCLKB
0008 C41Ch	RTC	Year Alarm Register	RYRAR	16	16	2 or 3 PCLKB
0008 C41Ch	RTC	Binary Counter 2 Alarm Enable Register	BCNT2AER	16	16	2 or 3 PCLKB
0008 C41Eh	RTC	Year Alarm Enable Register	RYRAREN	8	8	2 or 3 PCLKB
0008 C41Eh	RTC	Binary Counter 3 Alarm Enable Register	BCNT3AER	8	8	2 or 3 PCLKB
0008 C422h	RTC	RTC Control Register 1	RCR1	8	8	2 or 3 PCLKB
0008 C424h	RTC	RTC Control Register 2	RCR2	8	8	2 or 3 PCLKB
0008 C426h	RTC	RTC Control Register 3	RCR3	8	8	2 or 3 PCLKB
0008 C42Eh	RTC	Time Error Adjustment Register	RADJ	8	8	2 or 3 PCLKB
0008 C580h	CMPB	Comparator B Control Register 1	CPBCNT1	8	8	2 or 3 PCLKB
0008 C581h	CMPB	Comparator B Control Register 2	CPBCNT2	8	8	2 or 3 PCLKB
0008 C582h	CMPB	Comparator B Flag Register	CPBFLG	8	8	2 or 3 PCLKB
0008 C583h	CMPB	Comparator B Interrupt Control Register	CPBINT	8	8	2 or 3 PCLKB
0008 C584h	CMPB	Comparator B Filter Select Register	CPBF	8	8	2 or 3 PCLKB
0008 C585h	CMPB	Comparator B Mode Select Register	CPBMD	8	8	2 or 3 PCLKB
0008 C586h	CMPB	Comparator B Reference Input Voltage Select Register	CPBREF	8	8	2 or 3 PCLKB
0008 C587h	CMPB	Comparator B Output Control Register	CPBOCR	8	8	2 or 3 PCLKB
000A 0900h	CTSU	CTSU Control Register 0	CTSUCR0	8	8	1 or 2 PCLKB
000A 0901h	CTSU	CTSU Control Register 1	CTSUCR1	8	8	1 or 2 PCLKB
000A 0902h	CTSU	CTSU Synchronous Noise Reduction Setting Register	CTSUSDPRS	8	8	1 or 2 PCLKB
000A 0903h	CTSU	CTSU Sensor Stabilization Wait Control Register	CTSUSST	8	8	1 or 2 PCLKB
000A 0904h	CTSU	CTSU Measurement Channel Register 0	CTSUMCH0	8	8	1 or 2 PCLKB
000A 0905h	CTSU	CTSU Measurement Channel Register 1	CTSUMCH1	8	8	1 or 2 PCLKB
000A 0906h	CTSU	CTSU Channel Enable Control Register 0	CTSUCHAC0	8	8	1 or 2 PCLKB
000A 0907h	CTSU	CTSU Channel Enable Control Register 1	CTSUCHAC1	8	8	1 or 2 PCLKB
000A 0908h	CTSU	CTSU Channel Enable Control Register 2	CTSUCHAC2	8	8	1 or 2 PCLKB
000A 0909h	CTSU	CTSU Channel Enable Control Register 3	CTSUCHAC3	8	8	1 or 2 PCLKB
000A 090Ah	CTSU	CTSU Channel Enable Control Register 4	CTSUCHAC4	8	8	1 or 2 PCLKB
000A 090Bh	CTSU	CTSU Channel Transmit/Receive Control Register 0	CTSUCHTRC0	8	8	1 or 2 PCLKB
000A 090Ch	CTSU	CTSU Channel Transmit/Receive Control Register 1	CTSUCHTRC1	8	8	1 or 2 PCLKB
000A 090Dh	CTSU	CTSU Channel Transmit/Receive Control Register 2	CTSUCHTRC2	8	8	1 or 2 PCLKB
000A 090Eh	CTSU	CTSU Channel Transmit/Receive Control Register 3	CTSUCHTRC3	8	8	1 or 2 PCLKB
000A 090Fh	CTSU	CTSU Channel Transmit/Receive Control Register 4	CTSUCHTRC4	8	8	1 or 2 PCLKB
000A 0910h	CTSU	CTSU High-Pass Noise Reduction Control Register	CTSUDCLKC	8	8	1 or 2 PCLKB
000A 0911h	CTSU	CTSU Status Register	CTSUST	8	8	1 or 2 PCLKB
000A 0912h	CTSU	CTSU High-Pass Noise Reduction Spectrum Diffusion Control Register	CTSUSSC	16	16	1 or 2 PCLKB
000A 0914h	CTSU	CTSU Sensor Offset Register 0	CTSUSO0	16	16	1 or 2 PCLKB
000A 0916h	CTSU	CTSU Sensor Offset Register 1	CTSUSO1	16	16	1 or 2 PCLKB
000A 0918h	CTSU	CTSU Sensor Counter	CTSUSC	16	16	1 or 2 PCLKB
000A 091Ah	CTSU	CTSU Reference Counter	CTSURC	16	16	1 or 2 PCLKB
000A 091Ch	CTSU	CTSU Error Status Register	CTSUERRS	16	16	1 or 2 PCLKB
000A 0B00h	REMC0	Function Select Register 0	REMCON0	8	8	1 or 2 PCLKB
000A 0B01h	REMC0	Function Select Register 1	REMCON1	8	8	1 or 2 PCLKB
000A 0B02h	REMC0	Status Register	REMSTS	8	8	1 or 2 PCLKB
000A 0B03h	REMC0	Interrupt Control Register	REMINT	8	8	1 or 2 PCLKB
000A 0B04h	REMC0	Compare Control Register	REMCPC	8	8	1 or 2 PCLKB

5.2 DC Characteristics

Table 5.3 DC Characteristics (1)

Conditions: 2.7 V ≤ VCC ≤ 5.5 V, 2.7 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Schmitt trigger input voltage	RIIC input pin (except for SMBus)	V_{IH}	VCC × 0.7	—	5.8	V	
	Ports P12, P13, P16, P17 (5 V tolerant)		VCC × 0.8	—	5.8		
	Ports P14, P15, Ports P20 to P27, Ports P30 to P37, Ports P50 to P55, Ports PA0 to PA7, Ports PB0 to PB7, Ports PC0 to PC7, Ports PD0 to PD7, Ports PE0 to PE7, Ports PH0 to PH3, Ports PJ1, PJ3, RES#		VCC × 0.8	—	VCC + 0.3		
	Ports P03 to P07, Ports P40 to P47, Ports PJ6, PJ7		AVCC0 × 0.8	—	AVCC0 + 0.3		
	RIIC input pin (except for SMBus)	V_{IL}	–0.3	—	VCC × 0.3		
	Ports P03 to P07, Ports P40 to P47, Ports PJ6, PJ7		–0.3	—	AVCC0 × 0.2		
	Ports other than above		–0.3	—	VCC × 0.2		
	RIIC input pin (except for SMBus)	ΔV_T	VCC × 0.05	—	—		
	Ports P12, P13, P16, P17 (5 V tolerant)		VCC × 0.05	—	—		
	Ports P03 to P07, Ports P40 to P47, Ports PJ6, PJ7		AVCC0 × 0.1	—	—		
	Ports other than above		VCC × 0.1	—	—		
Input level voltage (except for Schmitt trigger input pins)	MD	V_{IH}	VCC × 0.9	—	VCC + 0.3	V	
	EXTAL (external clock input)		VCC × 0.8	—	VCC + 0.3		
	RIIC input pin (SMBus)		2.1	—	VCC + 0.3		
	MD	V_{IL}	–0.3	—	VCC × 0.1		
	EXTAL (external clock input)		–0.3	—	VCC × 0.2		
	RIIC input pin (SMBus)		–0.3	—	0.8		

Table 5.4 DC Characteristics (2)

Conditions: 1.8 V ≤ VCC = AVCC0 < 2.0 V, 2.0 V ≤ VCC < 2.7 V, 2.0 V ≤ AVCC0 < 2.7 V, VSS = AVSS0 = 0 V, Ta = –40 to +105°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Schmitt trigger input voltage	Ports P12, P13, P16, P17 (5 V tolerant)	V_{IH}	VCC × 0.8	—	5.8	V	
	Ports P14, P15, Ports P20 to P27, Ports P30 to P37, Ports P50 to P55, Ports PA0 to PA7, Ports PB0 to PB7, Ports PC0 to PC7, Ports PD0 to PD7, Ports PE0 to PE7, Ports PH0 to PH3, Ports PJ1, PJ3, RES#		VCC × 0.8	—	VCC + 0.3		
	Ports P03 to P07, Ports P40 to P47, Ports PJ6, PJ7		AVCC0 × 0.8	—	AVCC0 + 0.3		
	Ports P03 to P07, Ports P40 to P47, Ports PJ6, PJ7	V_{IL}	–0.3	—	AVCC0 × 0.2		
	Ports other than above		–0.3	—	VCC × 0.2		
	Ports P03 to P07, Ports P40 to P47, Ports PJ6, PJ7	ΔV_T	AVCC0 × 0.01	—	—		
	Ports other than above		VCC × 0.01	—	—		
Input level voltage (except for Schmitt trigger input pins)	MD	V_{IH}	VCC × 0.9	—	VCC + 0.3	V	
	EXTAL (external clock input)		VCC × 0.8	—	VCC + 0.3		
	MD	V_{IL}	–0.3	—	VCC × 0.1		
	EXTAL (external clock input)		–0.3	—	VCC × 0.2		

Table 5.5 DC Characteristics (3)

Conditions: 1.8 V ≤ VCC = AVCC0 < 2.0 V, 2.0 V ≤ VCC ≤ 5.5 V, 2.0 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, Ta = –40 to +105°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Input leakage current	RES#, MD, port P35	$\lvert I_{in} \rvert$	—	—	1.0	µA	V_{in} = 0V, VCC
Three-state leakage current (off-state)	Ports for 5-V tolerant	$\lvert I_{TSI} \rvert$	—	—	1.0	µA	V_{in} = 0V, 5.8V
	Ports except for 5 V tolerant		—	—	0.2		V_{in} = 0V, VCC
Input capacitance	All input pins (except for port P35)	C_{in}	—	—	15	pF	V_{in} = 0mV, f = 1MHz, T_a = 25°C
	port P35		—	—	30		

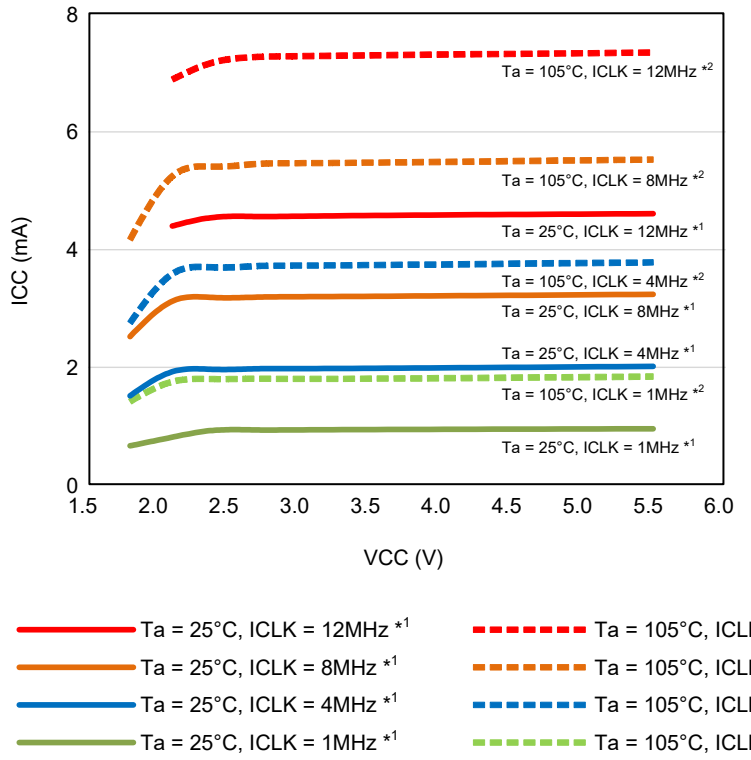
Table 5.6 DC Characteristics (4)

Conditions: 1.8 V ≤ VCC = AVCC0 < 2.0 V, 2.0 V ≤ VCC < 5.5 V, 2.0 V ≤ AVCC0 < 5.5 V, VSS = AVSS0 = 0 V, Ta = –40 to +105°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Input pull-up resistor	All ports (except for port P35)	R_U	10	20	50	kΩ	V_{in} = 0 V

Item					Symbol	Typ.	Max.	Unit	Test Conditions
Supply current*1	Middle-speed operating modes	Deep sleep mode	No peripheral operation*6	ICLK = 12 MHz	I_{CC}	1.0	—	mA	
				ICLK = 8 MHz		0.7	—		
				ICLK = 4 MHz		0.2	—		
				ICLK = 1 MHz		0.1	—		
			All peripheral operation: Normal*7	ICLK = 12 MHz		2.3	—		
				ICLK = 8 MHz		1.6	—		
				ICLK = 4 MHz		1.0	—		
				ICLK = 1 MHz		0.7	—		
		Increase during flash rewrite*5				2.5	—		
	Low-speed operating mode	Normal operating mode	No peripheral operation*8	ICLK = 32.768 kHz	I_{CC}	3.8	—	μA	
			All peripheral operation: Normal*10	ICLK = 32.768 kHz		10.9	—		
			All peripheral operation: Max.*10	ICLK = 32.768 kHz		—	29.2		
		Sleep mode	No peripheral operation*8	ICLK = 32.768 kHz		2.1	—		
			All peripheral operation: Normal*9	ICLK = 32.768 kHz		6.0	—		
		Deep sleep mode	No peripheral operation*8	ICLK = 32.768 kHz		1.6	—		
			All peripheral operation: Normal*9	ICLK = 32.768 kHz		5.0	—		

Note 1. Supply current values do not include output charge/discharge current from all pins. The values apply when internal pull-up MOSs are in the off state.
Note 2. Clock supply to the peripheral functions is stopped. This does not include BGO operation. The clock source is PLL. FCLK and PCLK are set to divided by 64.
Note 3. Clocks are supplied to the peripheral functions. This does not include BGO operation. The clock source is PLL. FCLK and PCLK are set to the same frequency as ICLK.
Note 4. Values when VCC = 3.3 V.
Note 5. This is the increase for programming or erasure of the ROM or E2 DataFlash during program execution.
Note 6. Clock supply to the peripheral function is stopped. The clock source is PLL when ICLK is 12 MHz, HOCO when ICLK is 8 MHz, and LOCO otherwise. FCLK and PCLK are set to divided by 64.
Note 7. Clocks are supplied to the peripheral functions. The clock source is PLL when ICLK is 12 MHz, HOCO when ICLK is (MHz, and LOCO otherwise. FCLK and PCLK are set to the same frequency as ICLK.
Note 8. Clock supply to the peripheral functions is stopped. The clock source is the sub-clock oscillator. FCLK and PCLK are set to divided by 64.
Note 9. Clocks are supplied to the peripheral functions. The clock source is the sub-clock oscillator. FCLK and PCLK are set to the same frequency as ICLK.
Note 10. Values when the MSTPCRA.MSTPA17 bit (12-bit A/D converter module stop bit) is set to “transition to the module stop state is made”.



Note 1. All peripheral operation is normal. This does not include BGO operation. Average value of the tested middle samples during product evaluation.
Note 2. All peripheral operation is maximum. This does not include BGO operation. Average value of the tested upper-limit samples during product evaluation.

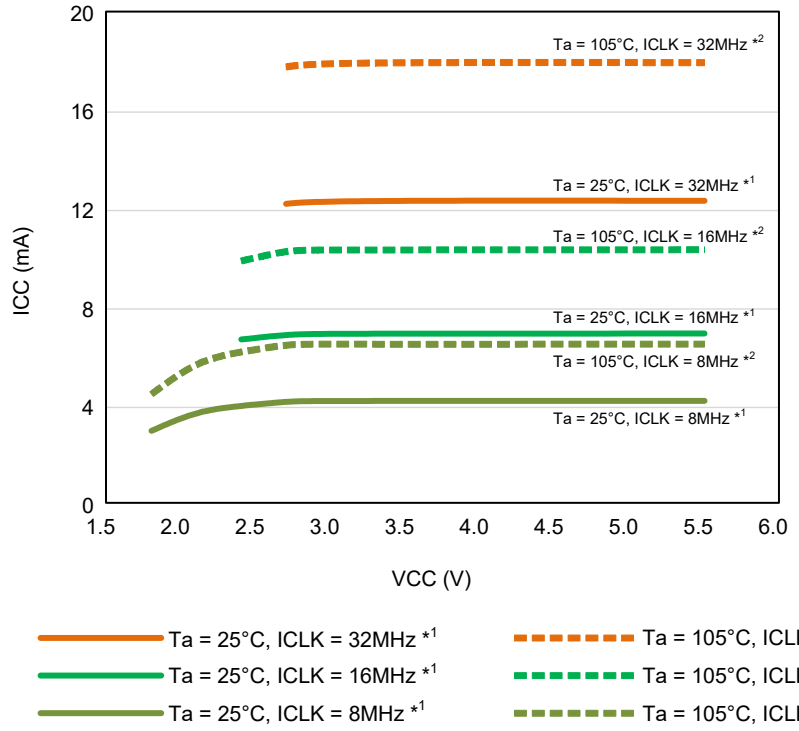
Figure 5.2 Voltage Dependency in Middle-Speed Operating Mode (Reference Data)

[Products with at least 256 Kbytes of flash memory or 100-pin packages]

Table 5.8 DC Characteristics (5)

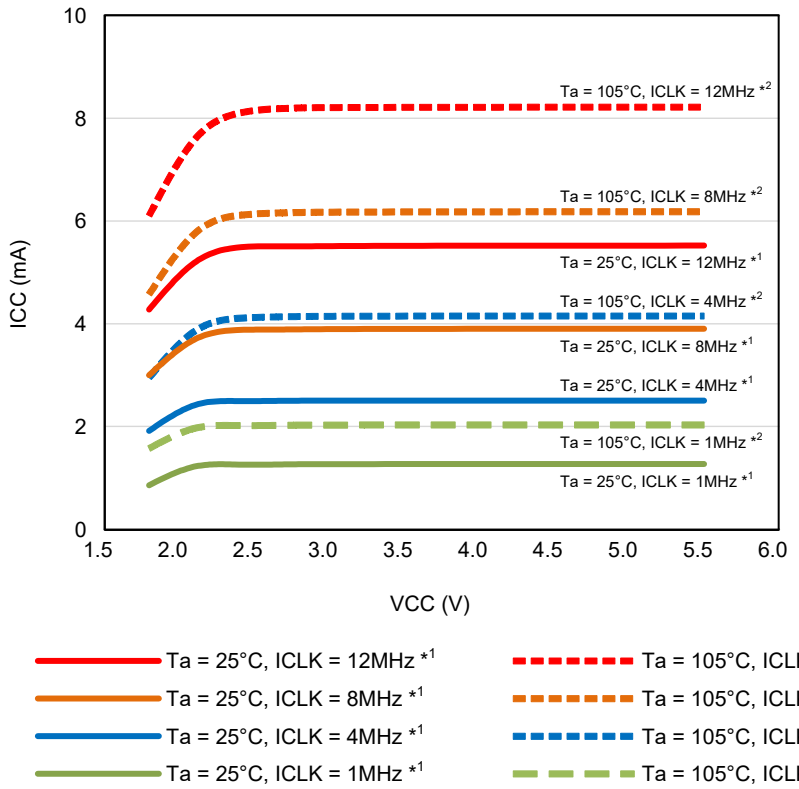
Conditions: 1.8 V ≤ VCC = AVCC0 < 2.0 V, 2.0 V ≤ VCC ≤ 5.5 V, 2.0 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, Ta = –40 to +105°C

Item					Symbol	Typ.	Max.	Unit	Test Conditions
Supply current*1	High-speed operating mode	Normal operating mode	No peripheral operation*2	ICLK = 32MHz	I_{CC}	3.5	—	mA	
				ICLK = 16MHz		2.4	—		
				ICLK = 8MHz		1.8	—		
			All peripheral operation: Normal*3	ICLK = 32MHz		12.4	—		
				ICLK = 16MHz		7.0	—		
				ICLK = 8MHz		4.3	—		
			All peripheral operation: Max.*3	ICLK = 32MHz		—	25.4		
		Sleep mode	No peripheral operation*2	ICLK = 32MHz		1.8	—		
				ICLK = 16MHz		1.4	—		
				ICLK = 8MHz		1.2	—		
			All peripheral operation: Normal*3	ICLK = 32MHz		6.5	—		
				ICLK = 16MHz		3.8	—		
				ICLK = 8MHz		2.5	—		
		Deep sleep mode	No peripheral operation*2	ICLK = 32MHz		1.1	—		
				ICLK = 16MHz		0.9	—		
				ICLK = 8MHz		0.8	—		
			All peripheral operation: Normal*3	ICLK = 32MHz		5.2	—		
				ICLK = 16MHz		3.0	—		
				ICLK = 8MHz		1.9	—		
		Increase during flash rewrite*5				2.5	—		
	Middle-speed operating modes	Normal operating mode	No peripheral operation*6	ICLK = 12MHz	I_{CC}	2.1	—	mA	
				ICLK = 8MHz		1.4	—		
				ICLK = 4MHz		0.7	—		
				ICLK = 1MHz		0.3	—		
			All peripheral operation: Normal*7	ICLK = 12MHz		5.5	—		
				ICLK = 8MHz		3.9	—		
				ICLK = 4MHz		2.4	—		
				ICLK = 1MHz		1.1	—		
			All peripheral operation: Max.*7	ICLK = 12MHz		—	11.6		
		Sleep mode	No peripheral operation*6	ICLK = 12MHz	I_{CC}	1.4	—	mA	
				ICLK = 8MHz		0.8	—		
				ICLK = 4MHz		0.3	—		
				ICLK = 1MHz		0.2	—		
			All peripheral operation: Normal*7	ICLK = 12MHz		3.2	—		
				ICLK = 8MHz		2.2	—		
				ICLK = 4MHz		1.4	—		
				ICLK = 1MHz		0.8	—		



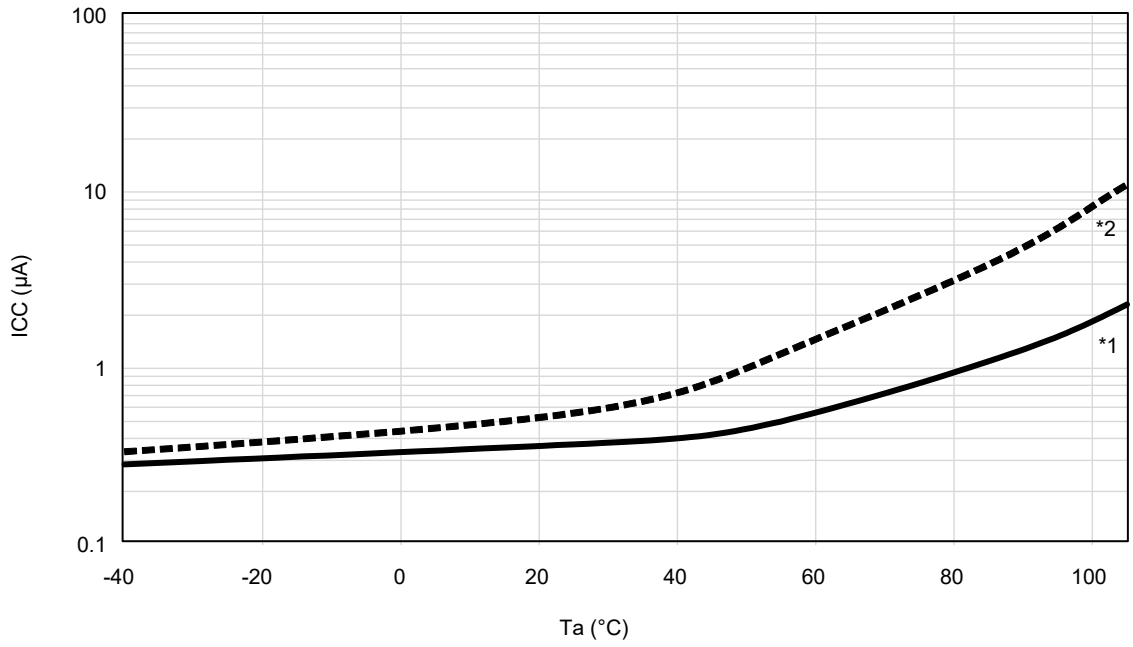
Note 1. All peripheral operation is normal. This does not include BGO operation. Average value of the tested middle samples during product evaluation.
Note 2. All peripheral operation is maximum. This does not include BGO operation. Average value of the tested upper-limit samples during product evaluation.

Figure 5.4 Voltage Dependency in High-Speed Operating Mode (Reference Data)



Note 1. All peripheral operation is normal. This does not include BGO operation. Average value of the tested middle samples during product evaluation.
Note 2. All peripheral operation is maximum. This does not include BGO operation. Average value of the tested upper-limit samples during product evaluation.

Figure 5.5 Voltage Dependency in Middle-Speed Operating Mode (Reference Data)



Note 1. Average value of the tested middle samples during product evaluation.
Note 2. Average value of the tested upper-limit samples during product evaluation.

Figure 5.8 Temperature Dependency in Software Standby Mode (Reference Data)

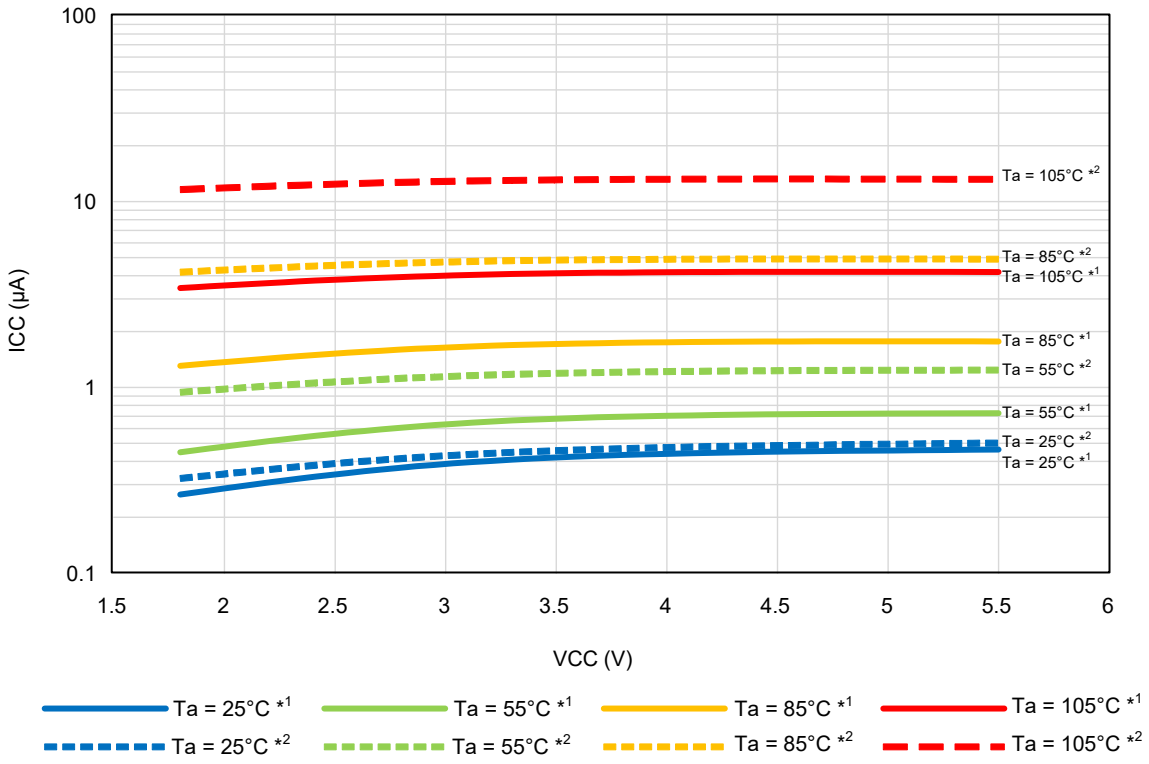
[Products with at least 256 Kbytes of flash memory or 100-pin packages]

Table 5.10 DC Characteristics (6)

Conditions: 1.8 V ≤ VCC = AVCC0 < 2.0 V, 2.0 V ≤ VCC ≤ 5.5 V, 2.0 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, Ta = –40 to +105°C

Item			Symbol	Typ.*3	Max.	Unit	Test Conditions
Supply current*1	Software standby mode*2	T_a = 25°C	I_{CC}	0.41	0.98	μA	
		T_a = 55°C		0.66	2.78		
		T_a = 85°C		1.69	9.65		
		T_a = 105°C		4.08	25.04		
	Increment for RTC operation*4			0.40	—		RCR3.RTCDV[2:0] set to low drive capacity
				1.21	—		RCR3.RTCDV[2:0] set to normal drive capacity
	Increment for low-power timer operation			0.37	—		LPTCR1.LPCNTCKSEL set to IWDT-dedicated on-chip oscillator
	Increment for Independent Watchdog Timer operation			0.37	—		
	Increment for REMC operation			0.44*4	—		REMCON1.CSRC[3:0] set to Sub-clock RCR3.RTCDV[2:0] set to low drive capacity
				1.34*4	—		REMCON1.CSRC[3:0] set to Sub-clock RCR3.RTCDV[2:0] set to normal drive capacity
				235	—		REMCON1.CSRC[3:0] set to HOCO clock/512

Note 1. Supply current values are with all output pins unloaded and all input pull-up MOSs in the off state.
Note 2. The IWDT, LVD, and CMPB are stopped.
Note 3. VCC = 3.3 V.
Note 4. Includes the oscillation circuit.



Note 1. Average value of the tested middle samples during product evaluation.
Note 2. Average value of the tested upper-limit samples during product evaluation.

Figure 5.9 Voltage Dependency in Software Standby Mode (Reference Data)

Table 5.12 DC Characteristics (8)

Conditions: 1.8 V ≤ VCC = AVCC0 < 2.0 V, 2.0 V ≤ VCC ≤ 5.5 V, 2.0 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, Ta = –40 to +105°C

Item		Symbol	Min.	Typ.*4	Max.	Unit	Test Conditions
Analog power supply current	During A/D conversion (at high-speed conversion)	I_{AVCC}	—	0.7	1.7	mA	
	During A/D conversion (at low-speed conversion)		—	0.6	1.0		
	During D/A conversion (per channel)*1		—	—	1.5		
	Waiting for A/D and D/A conversion (all units)		—	—	0.4	µA	
Reference power supply current	During A/D conversion (at high-speed conversion)	I_{REFH0}	—	25	150	µA	
	Waiting for A/D conversion (all units)		—	—	60	nA	
LVD0	—	I_{LVD}	—	0.1	—	µA	
LVD1, 2	Per channel		—	0.15	—	µA	
Temperature sensor*3	—	I_{TEMP}	—	75	—	µA	
Comparator B operating current*3	Window function enabled	I_{CMP}*2	—	12.5	28.6	µA	
	Comparator high-speed mode (per channel)		—	3.2	16.2	µA	
	Comparator low-speed mode (per channel)		—	1.7	4.4	µA	
CUSU operating current	During measurement (CPU is in sleep mode) Base clock: 2 MHz Pin capacity: 50 pF	I_{CTSU}	—	150	—	µA	

Note 1. The value of the D/A converter is the value of the power supply current including the reference current.
Note 2. Current consumed only by the comparator B module.
Note 3. ICurrent consumed by the power supply (VCC).
Note 4. When VCC = AVCC0 = 3.3 V.

Table 5.13 DC Characteristics (9)

Conditions: 1.8 V ≤ VCC = AVCC0 < 2.0 V, 2.0 V ≤ VCC ≤ 5.5 V, 2.0 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, Ta = –40 to +105°C

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
RAM standby voltage	V_{RAM}	1.8	—	—	V	

Table 5.14 DC Characteristics (10)

Conditions: 1.8 V ≤ VCC = AVCC0 < 2.0 V, 2.0 V ≤ VCC ≤ 5.5 V, 2.0 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, Ta = –40 to +105°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Power-on VCC rising gradient	At normal startup*1	SrVCC	0.02	—	20	ms/V	
	During fast startup time*2		0.02	—	2		
	Voltage monitoring 0 reset enabled at startup*3, *4		0.02	—	—		

Note 1. When OFS1.(FASTSTUP, LVDAS) = 11b.
Note 2. When OFS1.(FASTSTUP, LVDAS) = 01b.
Note 3. When OFS1.LVDAS = 0.
Note 4. Turn on the power supply voltage according to the normal startup rising gradient because the register settings set by OFS1 are not read in boot mode.

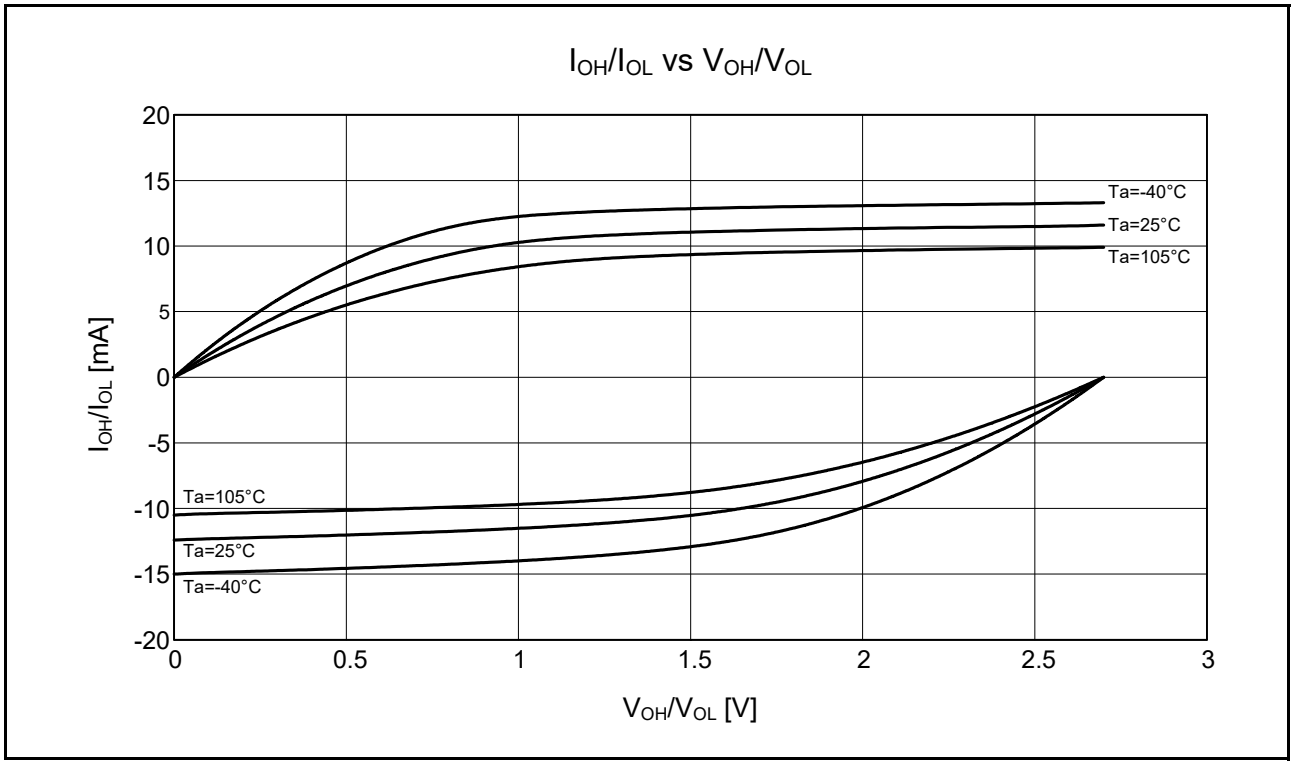


Figure 5.14 V_{OH}/V_{OL} and I_{OH}/I_{OL} Temperature Characteristics at VCC = 2.7 V When Normal Output is Selected (Reference Data)

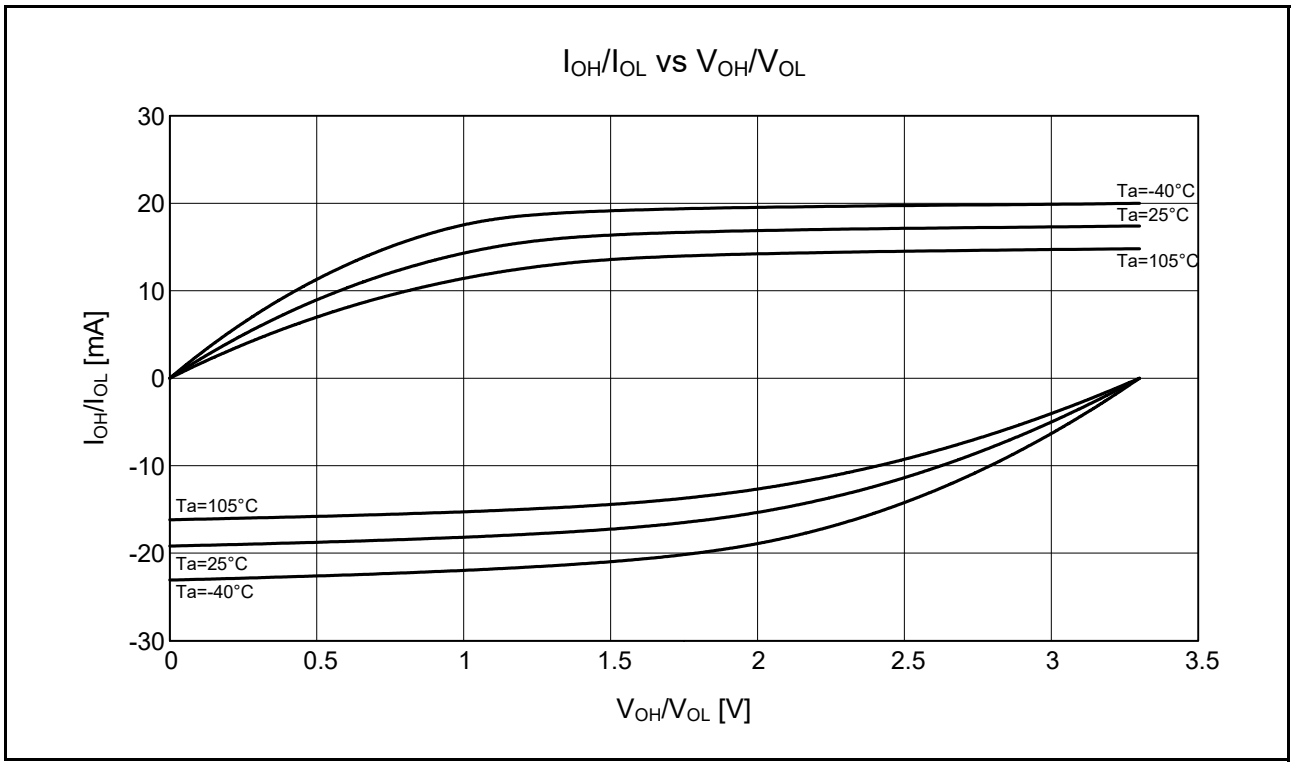


Figure 5.15 V_{OH}/V_{OL} and I_{OH}/I_{OL} Temperature Characteristics at VCC = 3.3 V When Normal Output is Selected (Reference Data)

5.3.4 Control Signal Timing

Table 5.32 Control Signal Timing

Conditions: 1.8 V ≤ VCC = AVCC0 < 2.0 V, 2.0 V ≤ VCC ≤ 5.5 V, 2.0 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, Ta = –40 to +105°C

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	
NMI pulse width	t_{NMIW}	200	—	—	ns	NMI digital filter disabled (NMIFLTE.NFLTEN = 0)	$t_{Pcyc} \times 2 \le 200$ ns
		$t_{Pcyc} \times 2$*1	—	—			$t_{Pcyc} \times 2 > 200$ ns
		200	—	—		NMI digital filter enabled (NMIFLTE.NFLTEN = 1)	$t_{NMICK} \times 3 \le 200$ ns
		$t_{NMICK} \times 3.5$*2	—	—			$t_{NMICK} \times 3 > 200$ ns
IRQ pulse width	t_{IRQW}	200	—	—	ns	IRQ digital filter disabled (IRQFLTE0.FLTENi = 0)	$t_{Pcyc} \times 2 \le 200$ ns
		$t_{Pcyc} \times 2$*1	—	—			$t_{Pcyc} \times 2 > 200$ ns
		200	—	—		IRQ digital filter enabled (IRQFLTE0.FLTENi = 1)	$t_{IRQCK} \times 3 \le 200$ ns
		$t_{IRQCK} \times 3.5$*3	—	—			$t_{IRQCK} \times 3 > 200$ ns

Note: 200 ns minimum in software standby mode.
Note 1. t_{Pcyc} indicates the cycle of PCLKB.
Note 2. t_{NMICK} indicates the cycle of the NMI digital filter sampling clock.
Note 3. t_{IRQCK} indicates the cycle of the IRQi digital filter sampling clock (i = 0 to 7).

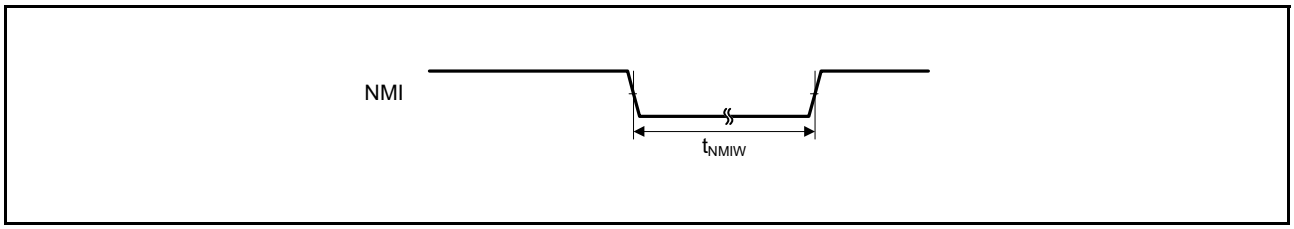


Figure 5.39 NMI Interrupt Input Timing

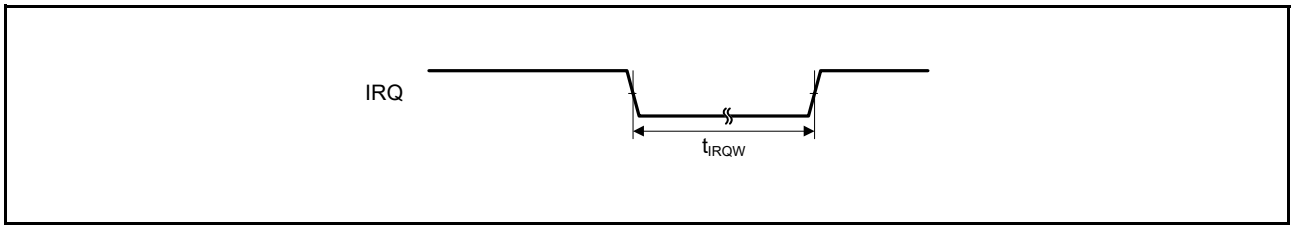


Figure 5.40 IRQ Interrupt Input Timing

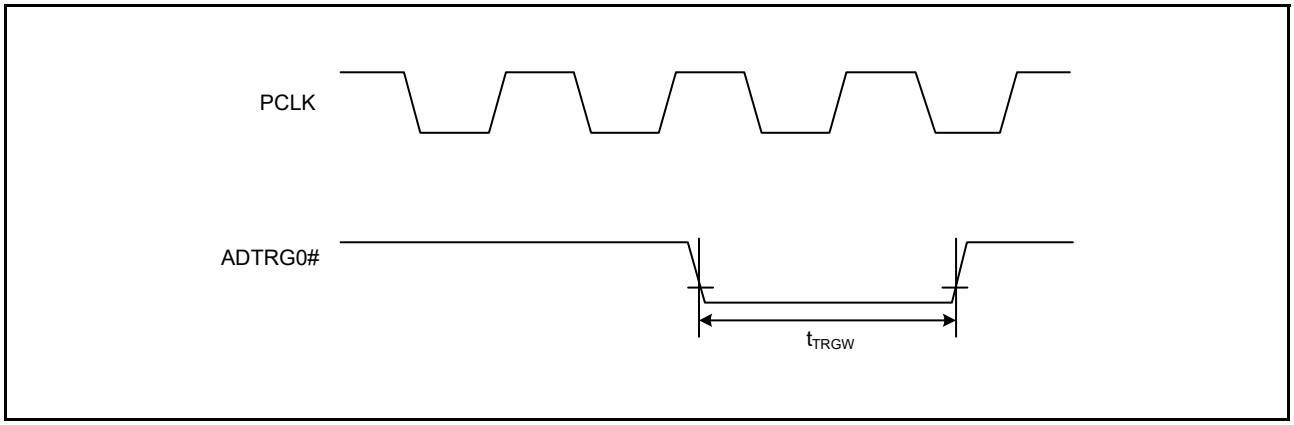


Figure 5.48 A/D Converter External Trigger Input Timing

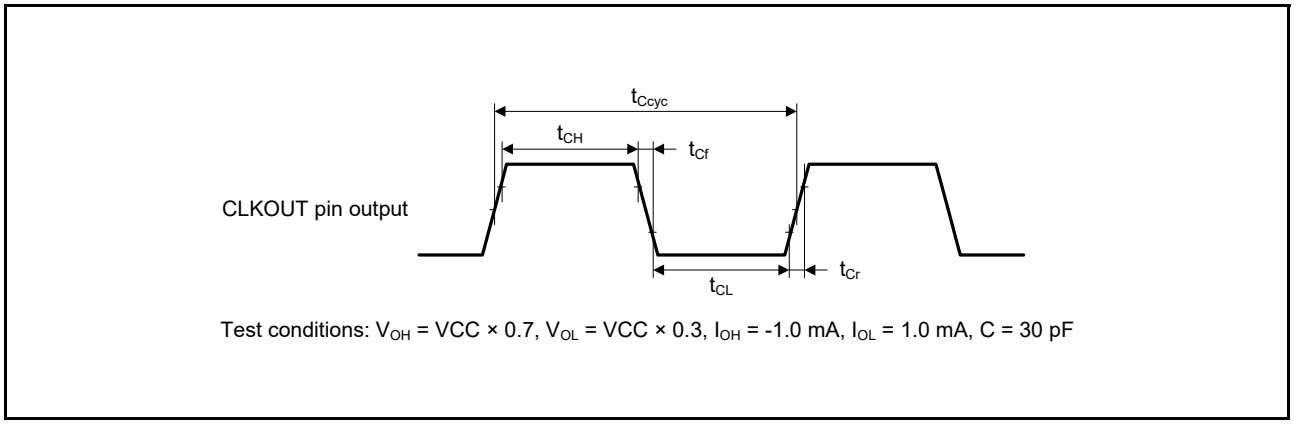


Figure 5.49 CLKOUT Output Timing

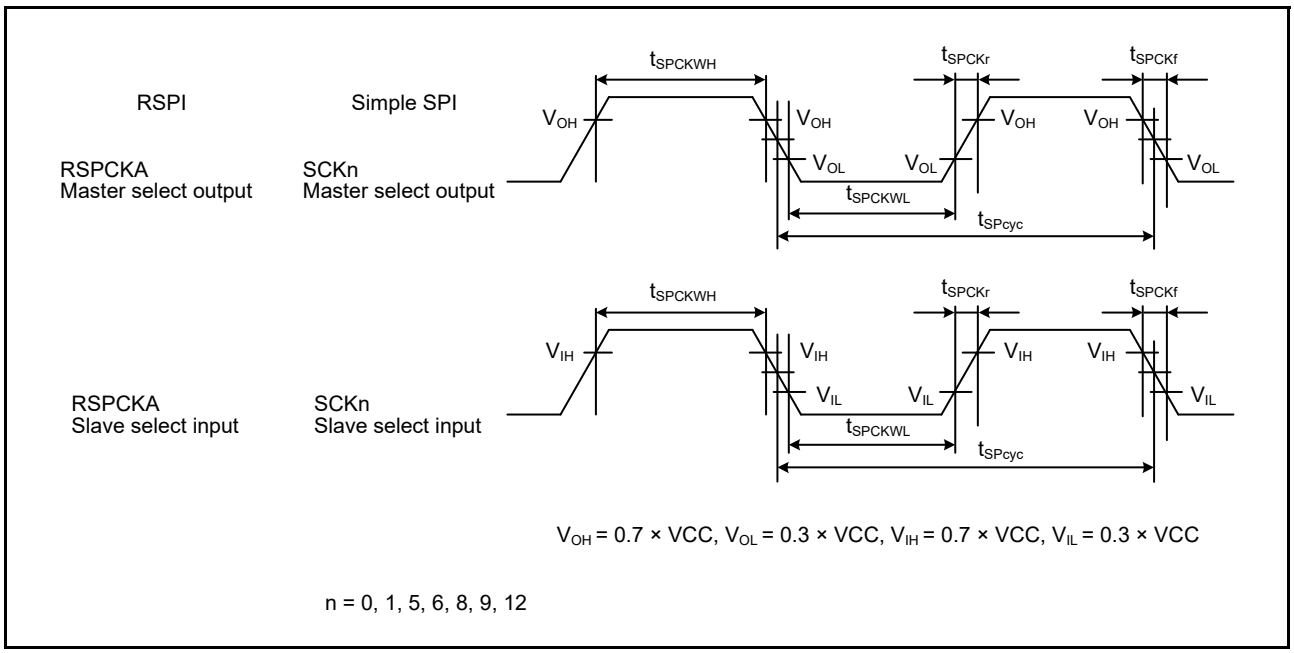


Figure 5.50 RSPI Clock Timing and Simple SPI Clock Timing

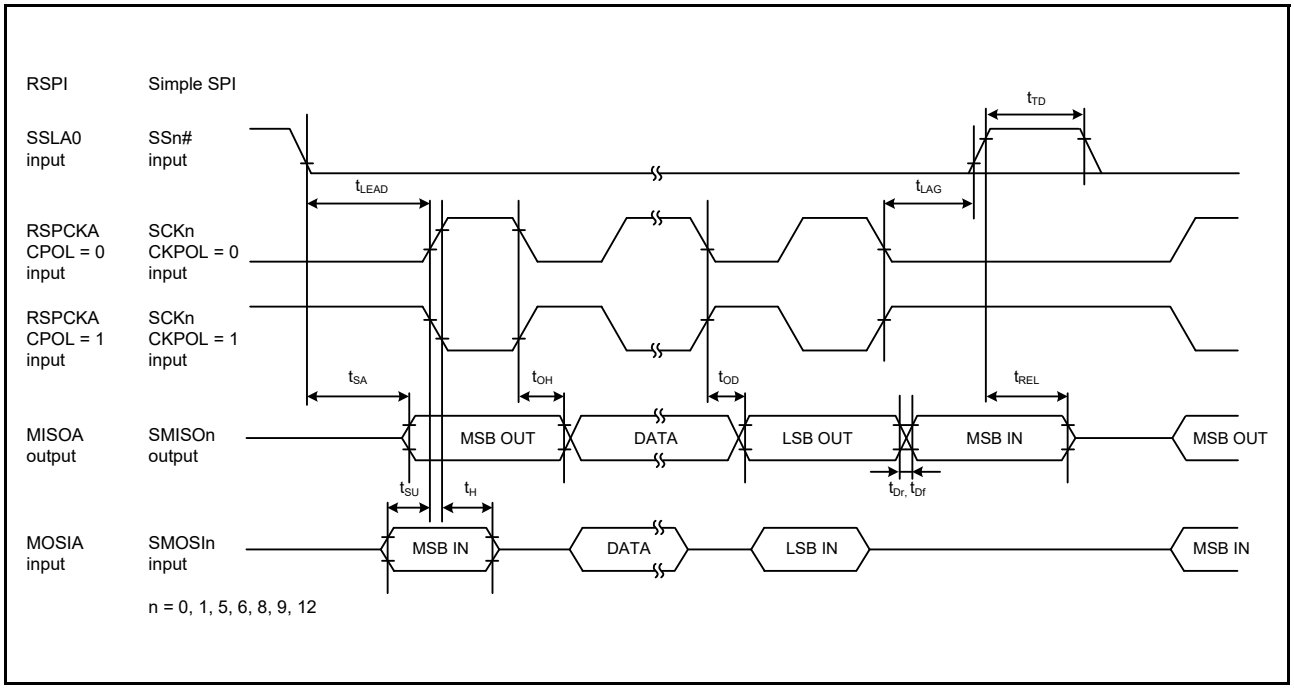


Figure 5.53 RSPI Timing (Slave, CPHA = 0) and Simple SPI Clock Timing (Slave, CKPH = 1)

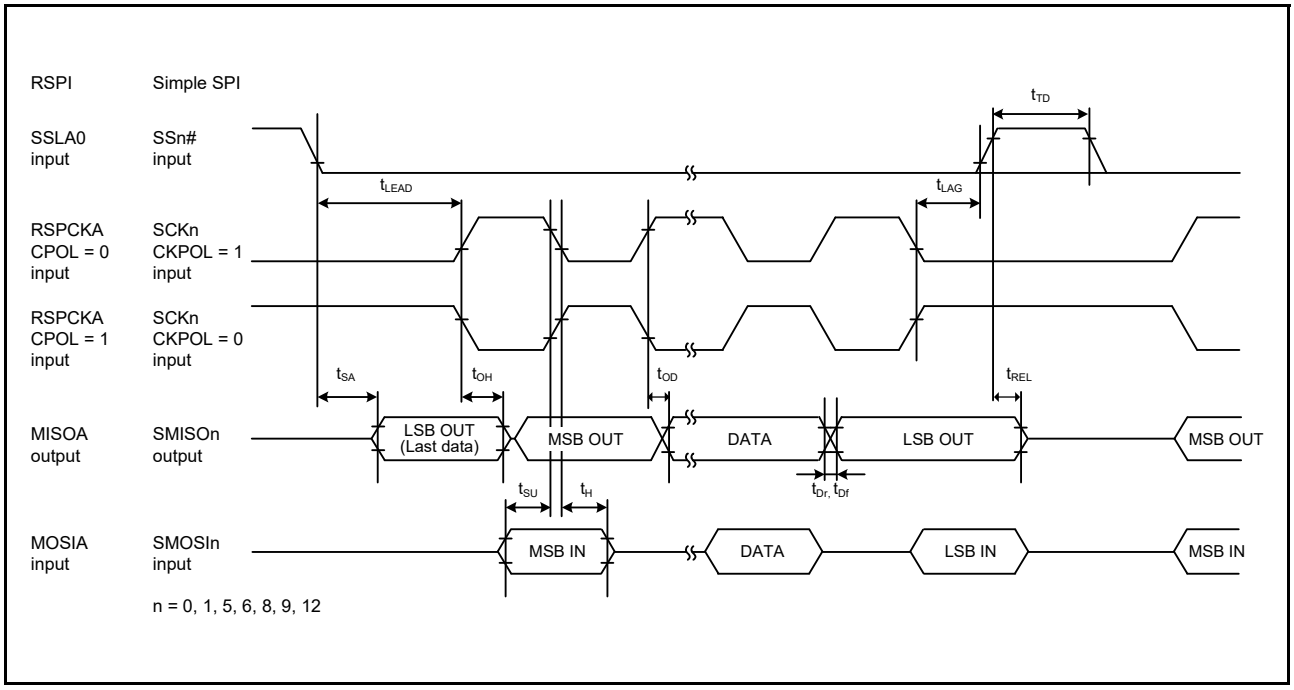


Figure 5.54 RSPI Timing (Slave, CPHA = 1) and Simple SPI Clock Timing (Slave, CKPH = 0)

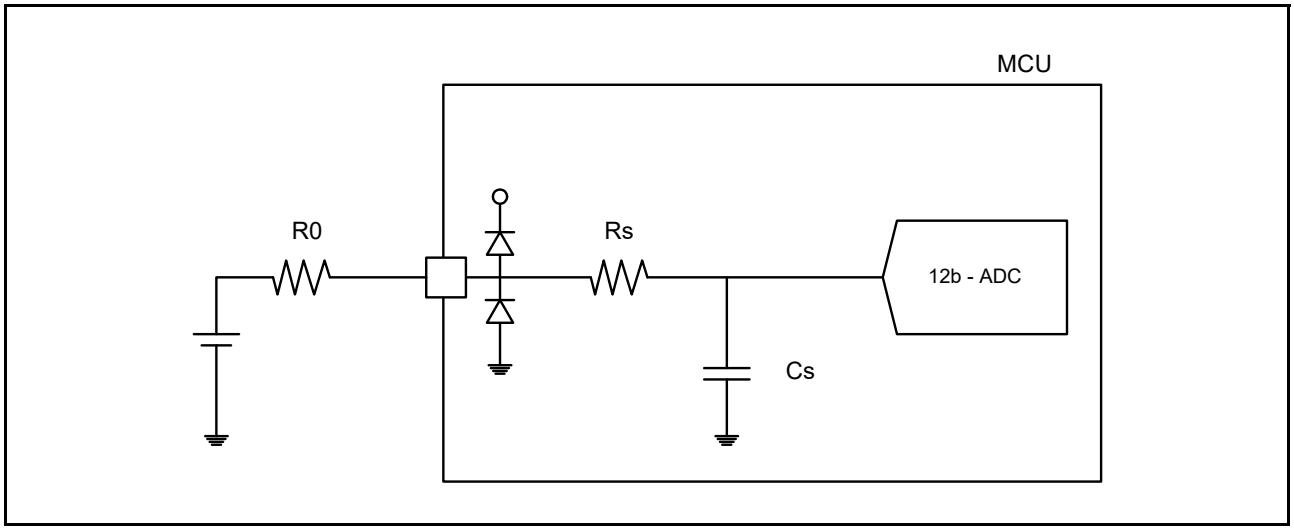


Figure 5.57 Equivalent Circuit

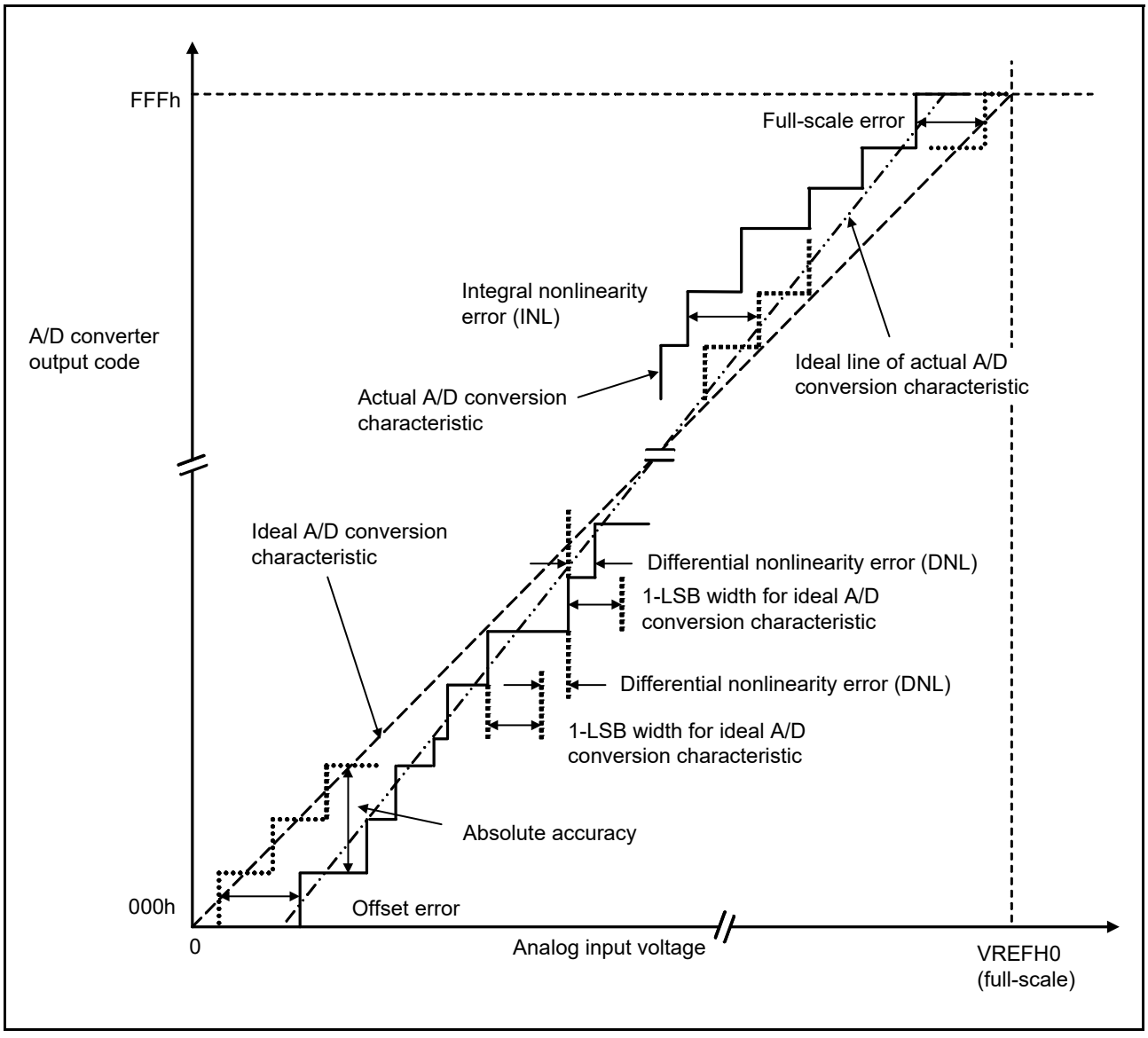


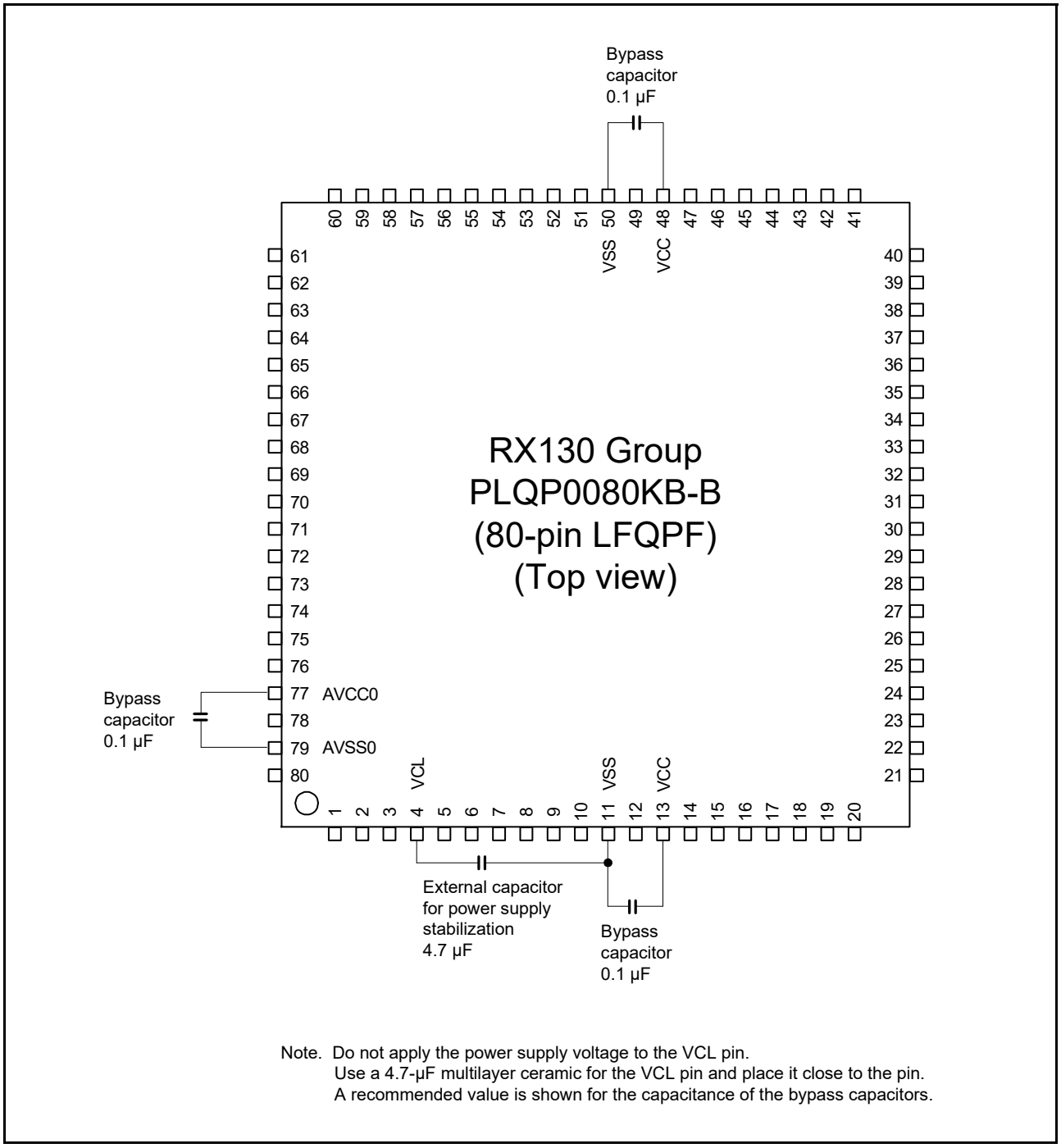
Figure 5.58 Illustration of A/D Converter Characteristic Terms

5.7 Comparator Characteristics

Table 5.47 Comparator Characteristics

Conditions: 1.8 V ≤ VCC = AVCC0 < 2.0 V, 2.0 V ≤ VCC ≤ 5.5 V, 2.0 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
CVREFB0 to CVREFB1 input reference voltage		VREF	0	—	VCC – 1.4	V	
CMPB0 to CMPB1 input voltage		VI	–0.3	—	VCC + 0.3	V	
Offset	Comparator high-speed mode	—	—	—	50	mV	
	Comparator high-speed mode Window function enabled	—	—	—	60	mV	
	Comparator low-speed mode	—	—	—	40	mV	
Comparator output delay time	Comparator high-speed mode	Td	—	—	1.2	µs	VCC = 3 V, input slew rate ≥ 50 mV/µs
	Comparator high-speed mode Window function enabled	Tdw	—	—	2.0	µs	
	Comparator low-speed mode	Td	—	—	5.0	µs	
High-side reference voltage (comparator high-speed mode, window function enabled)		VRFH	—	VCC × 0.76	—	V	
Low-side reference voltage (comparator high-speed mode, window function enabled)		VRFL	—	VCC × 0.24	—	V	
Operation stabilization wait time		Tcmp	100	—	—	µs	



Note. Do not apply the power supply voltage to the VCL pin.
Use a 4.7-µF multilayer ceramic for the VCL pin and place it close to the pin.
A recommended value is shown for the capacitance of the bypass capacitors.

Figure 5.68 Connecting Capacitors (80 Pins)

REVISION HISTORY	RX130 Group Datasheet

Classifications

- Items with Technical Update document number: Changes according to the corresponding issued Technical Update
- Items without Technical Update document number: Minor changes that do not require Technical Update to be issued

Rev.	Date	Description		Classification
		Page	Summary	
1.00	Oct 30, 2015	—	First edition, issued	
2.00	Sep 01, 2017	All	Products with at least 256 Kbytes of code flash memory and 100-pin packages added	
		4. I/O Registers		
		42	Table 4.1 List of I/O Registers (Address Order), changed	TN-RX*-A179A/E
		5. Electrical Characteristics		
		49	Table 5.2 Recommended Operating Voltage Conditions Note 3, added	
		57 to 61	The characteristics of products with at least 256 Kbytes of flash memory or 100-pin packages added	
		64, 65	The characteristics of products with at least 256 Kbytes of flash memory or 100-pin packages added	
		90	Table 5.34 Timing of On-Chip Peripheral Modules (2), changed	TN-RX*-A179A/E
		91	Table 5.35 Timing of On-Chip Peripheral Modules (3), changed	
		93	Table 5.38 Timing of On-Chip Peripheral Modules (6), added	
		111	Table 5.48 CTSU Characteristics, item for products with at least 256 Kbytes of flash memory or 100-pin packages added	
		113	Table 5.50 Power-On Reset Circuit and Voltage Detection Circuit Characteristics (2), item with Vdet0_0 to Vdet0_3 selected added	
		117	Table 5.53 ROM (Flash Memory for Code Storage) Characteristics (2) High-Speed Operating Mode, erasure time (128-Kbyte) deleted and erasure time (256-Kbyte) added	
		118	Table 5.54 ROM (Flash Memory for Code Storage) Characteristics (3) Middle-Speed Operating Mode, erasure time (128-Kbyte) deleted and erasure time (256-Kbyte) added	