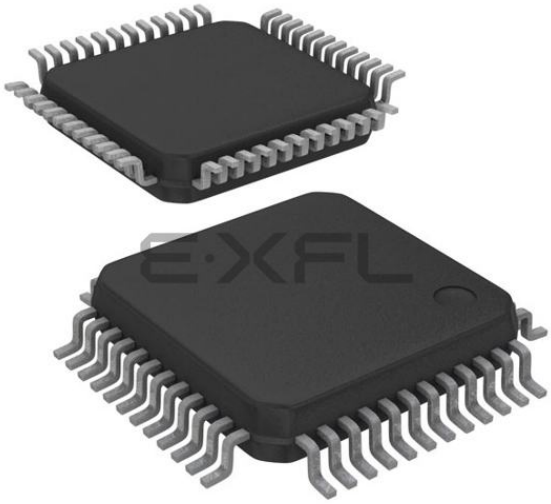

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	RX
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	I²C, LINbus, SCI, SPI
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	38
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	8K x 8
RAM Size	10K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 10x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LFQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f51303adfl-30

1.2 List of Products

Table 1.3 is a lists of products, and Figure 1.1 shows how to read the product part no., memory capacity, and package type.

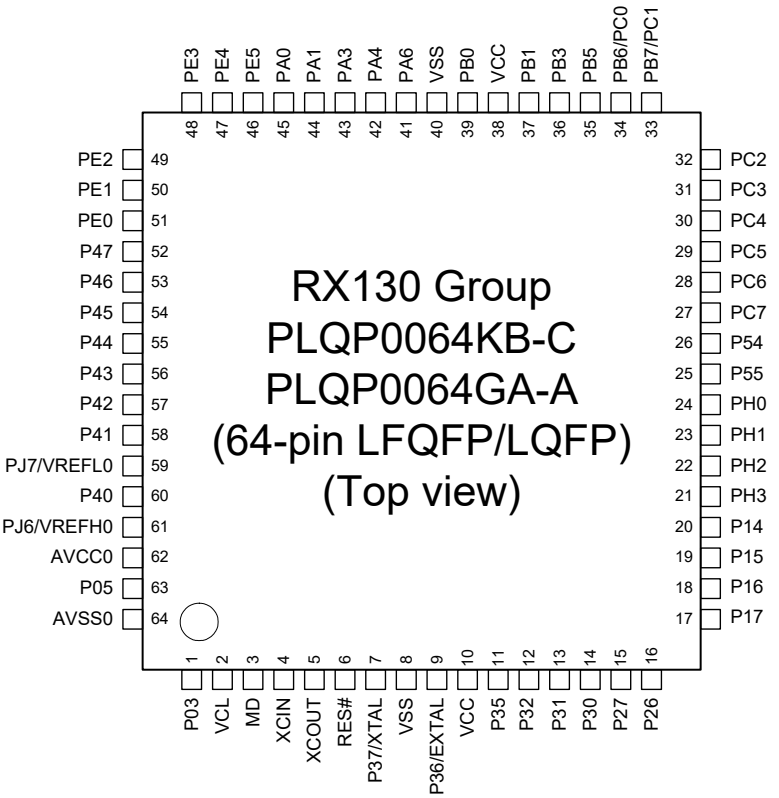
Table 1.3 List of Products (1/2)

Group	Part No.	Part No. (for Orders)	Package	ROM Capacity	RAM Capacity	E2 DataFlash	Operating Frequency (Max.)	Operating Temperature
RX130	R5F51308ADFP	R5F51308ADFP#30	PLQP0100KB-B	512 Kbytes	48 Kbytes	8 Kbytes	32 MHz	–40 to +85°C
	R5F51308ADFN	R5F51308ADFN#30	PLQP0080KB-B					
	R5F51308ADFM	R5F51308ADFM#30	PLQP0064KB-C					
	R5F51308ADFK	R5F51308ADFK#30	PLQP0064GA-A					
	R5F51308ADFL	R5F51308ADFL#30	PLQP0048KB-B					
	R5F51308ADNE	R5F51308ADNE#U0	PWQN0048KB-A					
	R5F51307ADFP	R5F51307ADFP#30	PLQP0100KB-B	384 Kbytes				
	R5F51307ADFN	R5F51307ADFN#30	PLQP0080KB-B					
	R5F51307ADFM	R5F51307ADFM#30	PLQP0064KB-C					
	R5F51307ADFK	R5F51307ADFK#30	PLQP0064GA-A					
	R5F51307ADFL	R5F51307ADFL#30	PLQP0048KB-B					
	R5F51307ADNE	R5F51307ADNE#U0	PWQN0048KB-A					
	R5F51306ADFP	R5F51306ADFP#30	PLQP0100KB-B	256 Kbytes	32 Kbytes			
	R5F51306ADFN	R5F51306ADFN#30	PLQP0080KB-B					
	R5F51306ADFM	R5F51306ADFM#30	PLQP0064KB-C					
	R5F51306ADFK	R5F51306ADFK#30	PLQP0064GA-A					
	R5F51306ADFL	R5F51306ADFL#30	PLQP0048KB-B					
	R5F51306ADNE	R5F51306ADNE#U0	PWQN0048KB-A					
	R5F51305ADFP	R5F51305ADFP#30	PLQP0100KB-B	128 Kbytes	16 Kbytes			
	R5F51305ADFN	R5F51305ADFN#30	PLQP0080KB-B					
	R5F51305ADFM	R5F51305ADFM#30	PLQP0064KB-C					
	R5F51305ADFK	R5F51305ADFK#30	PLQP0064GA-A					
	R5F51305ADFL	R5F51305ADFL#30	PLQP0048KB-B					
	R5F51305ADNE	R5F51305ADNE#U0	PWQN0048KB-A					
	R5F51303ADFN	R5F51303ADFN#30	PLQP0080KB-B	64 Kbytes	10 Kbytes			
	R5F51303ADFM	R5F51303ADFM#30	PLQP0064KB-C					
	R5F51303ADFK	R5F51303ADFK#30	PLQP0064GA-A					
	R5F51303ADFL	R5F51303ADFL#30	PLQP0048KB-B					
	R5F51303ADNE	R5F51303ADNE#U0	PWQN0048KB-A					

Table 1.3 List of Products (2/2)

Group	Part No.	Part No. (for Orders)	Package	ROM Capacity	RAM Capacity	E2 DataFlash	Operating Frequency (Max.)	Operating Temperature
RX130	R5F51308AGFP	R5F51308AGFP#30	PLQP0100KB-B	512 Kbytes	48 Kbytes	8 Kbytes	32 MHz	–40 to +105°C
	R5F51308AGFN	R5F51308AGFN#30	PLQP0080KB-B					
	R5F51308AGFM	R5F51308AGFM#30	PLQP0064KB-C					
	R5F51308AGFK	R5F51308AGFK#30	PLQP0064GA-A					
	R5F51308AGFL	R5F51308AGFL#30	PLQP0048KB-B					
	R5F51308AGNE	R5F51308AGNE#U0	PWQN0048KB-A					
	R5F51307AGFP	R5F51307AGFP#30	PLQP0100KB-B	384 Kbytes				
	R5F51307AGFN	R5F51307AGFN#30	PLQP0080KB-B					
	R5F51307AGFM	R5F51307AGFM#30	PLQP0064KB-C					
	R5F51307AGFK	R5F51307AGFK#30	PLQP0064GA-A					
	R5F51307AGFL	R5F51307AGFL#30	PLQP0048KB-B					
	R5F51307AGNE	R5F51307AGNE#U0	PWQN0048KB-A					
	R5F51306AGFP	R5F51306AGFP#30	PLQP0100KB-B	256 Kbytes	32 Kbytes			
	R5F51306AGFN	R5F51306AGFN#30	PLQP0080KB-B					
	R5F51306AGFM	R5F51306AGFM#30	PLQP0064KB-C					
	R5F51306AGFK	R5F51306AGFK#30	PLQP0064GA-A					
	R5F51306AGFL	R5F51306AGFL#30	PLQP0048KB-B					
	R5F51306AGNE	R5F51306AGNE#U0	PWQN0048KB-A					
	R5F51305AGFP	R5F51305AGFP#30	PLQP0100KB-B	128 Kbytes	16 Kbytes			
	R5F51305AGFN	R5F51305AGFN#30	PLQP0080KB-B					
	R5F51305AGFM	R5F51305AGFM#30	PLQP0064KB-C					
	R5F51305AGFK	R5F51305AGFK#30	PLQP0064GA-A					
	R5F51305AGFL	R5F51305AGFL#30	PLQP0048KB-B					
	R5F51305AGNE	R5F51305AGNE#U0	PWQN0048KB-A					
	R5F51303AGFN	R5F51303AGFN#30	PLQP0080KB-B	64 Kbytes	10 Kbytes			
	R5F51303AGFM	R5F51303AGFM#30	PLQP0064KB-C					
	R5F51303AGFK	R5F51303AGFK#30	PLQP0064GA-A					
	R5F51303AGFL	R5F51303AGFL#30	PLQP0048KB-B					
	R5F51303AGNE	R5F51303AGNE#U0	PWQN0048KB-A					

Note: The part numbers for orders above are used for products in mass production or under development when this manual is issued. Refer to the Renesas Electronics Corporation website for the latest part numbers.



Note: This figure indicates the power supply pins and I/O ports.
For the pin configuration, see the table “List of Pins and Pin Functions (64-Pin LFQFP/LQFP)”.

Figure 1.5 Pin Assignments of the 64-Pin LFQFP/LQFP

Table 1.7 List of Pins and Pin Functions (64-Pin LFQFP/LQFP) (2/2)

Pin No.	Power Supply, Clock, System Control	I/O Port	Timers (MTU, TMR, POE)	Communications (SCIg, SCIh, RSPI, RIIC)	Touch sensing	Others
49		PE2	MTIOC4A	RXD12/RXDX12/SMISO12/SSCL12	TS35	IRQ7/AN018/CVREFB0
50		PE1	MTIOC4C	TXD12/TXDX12/SIOX12/SMOSI12/ SSDA12		AN017/CMPB0
51		PE0		SCK12		AN016
52		P47*1				AN007
53		P46*1				AN006
54		P45*1				AN005
55		P44*1				AN004
56		P43*1				AN003
57		P42*1				AN002
58		P41*1				AN001
59	VREFL0	PJ7*1				
60		P40*1				AN000
61	VREFH0	PJ6*1				
62	AVCC0					
63		P05*1				DA1
64	AVSS0					

Note 1. The power source of the I/O buffer for these pins is AVCC0.
Note 2. PC0 and PC1 are valid only when the port switching function is selected.

Table 4.1 List of I/O Registers (Address Order) (4 / 18)

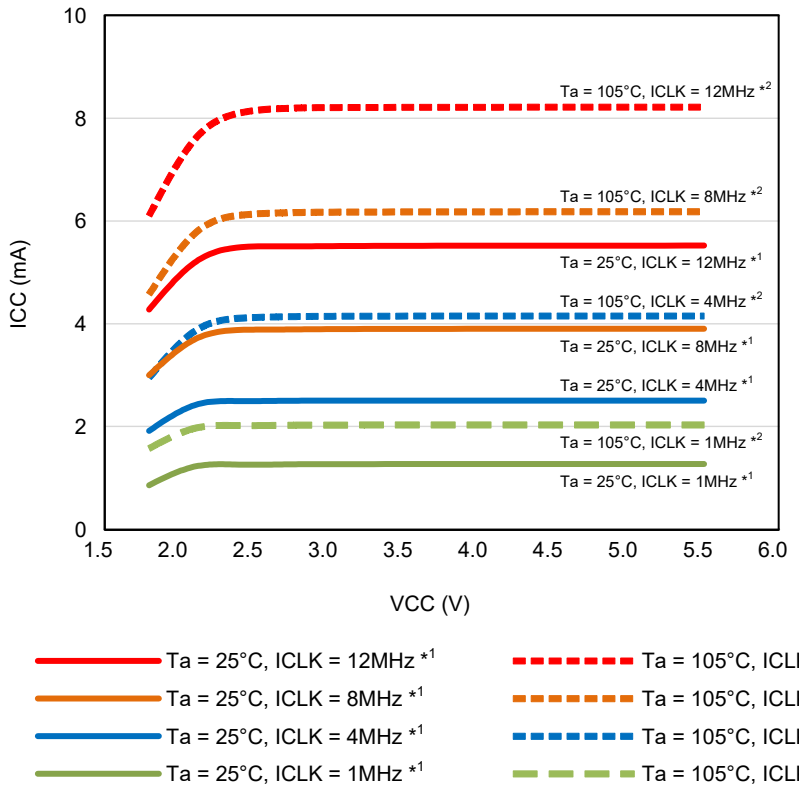
Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles
0008 838Dh	RSPI0	RSPI Slave Select Negation Delay Register	SSLND	8	8	2 or 3 PCLKB
0008 838Eh	RSPI0	RSPI Next-Access Delay Register	SPND	8	8	2 or 3 PCLKB
0008 838Fh	RSPI0	RSPI Control Register 2	SPCR2	8	8	2 or 3 PCLKB
0008 8390h	RSPI0	RSPI Command Register 0	SPCMD0	16	16	2 or 3 PCLKB
0008 8392h	RSPI0	RSPI Command Register 1	SPCMD1	16	16	2 or 3 PCLKB
0008 8394h	RSPI0	RSPI Command Register 2	SPCMD2	16	16	2 or 3 PCLKB
0008 8396h	RSPI0	RSPI Command Register 3	SPCMD3	16	16	2 or 3 PCLKB
0008 8398h	RSPI0	RSPI Command Register 4	SPCMD4	16	16	2 or 3 PCLKB
0008 839Ah	RSPI0	RSPI Command Register 5	SPCMD5	16	16	2 or 3 PCLKB
0008 839Ch	RSPI0	RSPI Command Register 6	SPCMD6	16	16	2 or 3 PCLKB
0008 839Eh	RSPI0	RSPI Command Register 7	SPCMD7	16	16	2 or 3 PCLKB
0008 8600h	MTU3	Timer Control Register	TCR	8	8	2 or 3 PCLKB
0008 8601h	MTU4	Timer Control Register	TCR	8	8	2 or 3 PCLKB
0008 8602h	MTU3	Timer Mode Register	TMDR	8	8	2 or 3 PCLKB
0008 8603h	MTU4	Timer Mode Register	TMDR	8	8	2 or 3 PCLKB
0008 8604h	MTU3	Timer I/O Control Register H	TIORH	8	8	2 or 3 PCLKB
0008 8605h	MTU3	Timer I/O Control Register L	TIORL	8	8	2 or 3 PCLKB
0008 8606h	MTU4	Timer I/O Control Register H	TIORH	8	8	2 or 3 PCLKB
0008 8607h	MTU4	Timer I/O Control Register L	TIORL	8	8	2 or 3 PCLKB
0008 8608h	MTU3	Timer Interrupt Enable Register	TIER	8	8	2 or 3 PCLKB
0008 8609h	MTU4	Timer Interrupt Enable Register	TIER	8	8	2 or 3 PCLKB
0008 860Ah	MTU	Timer Output Master Enable Registers	TOER	8	8	2 or 3 PCLKB
0008 860Dh	MTU	Timer Gate Control Registers	TGCR	8	8	2 or 3 PCLKB
0008 860Eh	MTU	Timer Output Control Register 1	TOCR1	8	8	2 or 3 PCLKB
0008 860Fh	MTU	Timer Output Control Register 2	TOCR2	8	8	2 or 3 PCLKB
0008 8610h	MTU3	Timer Counter	TCNT	16	16	2 or 3 PCLKB
0008 8612h	MTU4	Timer Counter	TCNT	16	16	2 or 3 PCLKB
0008 8614h	MTU	Timer Cycle Data Register	TCDR	16	16	2 or 3 PCLKB
0008 8616h	MTU	Timer Dead Time Data Register	TDDR	16	16	2 or 3 PCLKB
0008 8618h	MTU3	Timer General Register A	TGRA	16	16	2 or 3 PCLKB
0008 861Ah	MTU3	Timer General Register B	TGRB	16	16	2 or 3 PCLKB
0008 861Ch	MTU4	Timer General Register A	TGRA	16	16	2 or 3 PCLKB
0008 861Eh	MTU4	Timer General Register B	TGRB	16	16	2 or 3 PCLKB
0008 8620h	MTU	Timer Subcounter	TCNTS	16	16	2 or 3 PCLKB
0008 8622h	MTU	Timer Cycle Buffer Register	TCBR	16	16	2 or 3 PCLKB
0008 8624h	MTU3	Timer General Register C	TGRC	16	16	2 or 3 PCLKB
0008 8626h	MTU3	Timer General Register D	TGRD	16	16	2 or 3 PCLKB
0008 8628h	MTU4	Timer General Register C	TGRC	16	16	2 or 3 PCLKB
0008 862Ah	MTU4	Timer General Register D	TGRD	16	16	2 or 3 PCLKB
0008 862Ch	MTU3	Timer Status Register	TSR	8	8	2 or 3 PCLKB
0008 862Dh	MTU4	Timer Status Register	TSR	8	8	2 or 3 PCLKB
0008 8630h	MTU	Timer Interrupt Skipping Set Register	TITCR	8	8	2 or 3 PCLKB
0008 8631h	MTU	Timer Interrupt Skipping Counter	TITCNT	8	8	2 or 3 PCLKB
0008 8632h	MTU	Timer Buffer Transfer Set Register	TBTER	8	8	2 or 3 PCLKB
0008 8634h	MTU	Timer Dead Time Enable Register	TDER	8	8	2 or 3 PCLKB
0008 8636h	MTU	Timer Output Level Buffer Register	TOLBR	8	8	2 or 3 PCLKB
0008 8638h	MTU3	Timer Buffer Operation Transfer Mode Register	TBTM	8	8	2 or 3 PCLKB
0008 8639h	MTU4	Timer Buffer Operation Transfer Mode Register	TBTM	8	8	2 or 3 PCLKB
0008 8640h	MTU4	Timer A/D Converter Start Request Control Register	TADCR	16	16	2 or 3 PCLKB
0008 8644h	MTU4	Timer A/D Converter Start Request Cycle Set Register A	TADCORA	16	16	2 or 3 PCLKB
0008 8646h	MTU4	Timer A/D Converter Start Request Cycle Set Register B	TADCORB	16	16	2 or 3 PCLKB
0008 8648h	MTU4	Timer A/D Converter Start Request Cycle Set Buffer Register A	TADCOBRA	16	16	2 or 3 PCLKB

Table 4.1 List of I/O Registers (Address Order) (6 / 18)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles
0008 88A2h	MTU5	Timer General Register W	TGRW	16	16	2 or 3 PCLKB
0008 88A4h	MTU5	Timer Control Register W	TCRW	8	8	2 or 3 PCLKB
0008 88A6h	MTU5	Timer I/O Control Register W	TIORW	8	8	2 or 3 PCLKB
0008 88B2h	MTU5	Timer Interrupt Enable Register	TIER	8	8	2 or 3 PCLKB
0008 88B4h	MTU5	Timer Start Register	TSTR	8	8	2 or 3 PCLKB
0008 88B6h	MTU5	Timer Compare Match Clear Register	TCNTCMPCLR	8	8	2 or 3 PCLKB
0008 8900h	POE	Input Level Control/Status Register 1	ICSR1	16	8, 16	2 or 3 PCLKB
0008 8902h	POE	Output Level Control/Status Register 1	OCSR1	16	8, 16	2 or 3 PCLKB
0008 8908h	POE	Input Level Control/Status Register 2	ICSR2	16	8, 16	2 or 3 PCLKB
0008 890Ah	POE	Software Port Output Enable Register	SPOER	8	8	2 or 3 PCLKB
0008 890Bh	POE	Port Output Enable Control Register 1	POECR1	8	8	2 or 3 PCLKB
0008 890Ch	POE	Port Output Enable Control Register 2	POECR2	8	8	2 or 3 PCLKB
0008 890Eh	POE	Input Level Control/Status Register 3	ICSR3	16	8, 16	2 or 3 PCLKB
0008 9000h	S12AD	A/D Control Register	ADCSR	16	16	2 or 3 PCLKB
0008 9004h	S12AD	A/D Channel Select Register A0	ADANSA0	16	16	2 or 3 PCLKB
0008 9006h	S12AD	A/D Channel Select Register A1	ADANSA1	16	16	2 or 3 PCLKB
0008 9008h	S12AD	A/D-Converted Value Addition/Average Function Select Register 0	ADADS0	16	16	2 or 3 PCLKB
0008 900Ah	S12AD	A/D-Converted Value Addition/Average Function Select Register 1	ADADS1	16	16	2 or 3 PCLKB
0008 900Ch	S12AD	A/D-Converted Value Addition/Average Count Select Register	ADADC	8	8	2 or 3 PCLKB
0008 900Eh	S12AD	A/D Control Extended Register	ADCER	16	16	2 or 3 PCLKB
0008 9010h	S12AD	A/D Conversion Start Trigger Select Register	ADSTRGR	16	16	2 or 3 PCLKB
0008 9012h	S12AD	A/D Conversion Extended Input Control Register	ADEXICR	16	16	2 or 3 PCLKB
0008 9014h	S12AD	A/D Channel Select Register B0	ADANSB0	16	16	2 or 3 PCLKB
0008 9016h	S12AD	A/D Channel Select Register B1	ADANSB1	16	16	2 or 3 PCLKB
0008 9018h	S12AD	A/D Data Duplication Register	ADDBLDR	16	16	2 or 3 PCLKB
0008 901Ah	S12AD	A/D Temperature Sensor Data Register	ADTSDR	16	16	2 or 3 PCLKB
0008 901Ch	S12AD	A/D Internal Reference Voltage Data Register	ADOCDR	16	16	2 or 3 PCLKB
0008 901Eh	S12AD	A/D Self-Diagnosis Data Register	ADRD	16	16	2 or 3 PCLKB
0008 9020h	S12AD	A/D Data Register 0	ADDR0	16	16	2 or 3 PCLKB
0008 9022h	S12AD	A/D Data Register 1	ADDR1	16	16	2 or 3 PCLKB
0008 9024h	S12AD	A/D Data Register 2	ADDR2	16	16	2 or 3 PCLKB
0008 9026h	S12AD	A/D Data Register 3	ADDR3	16	16	2 or 3 PCLKB
0008 9028h	S12AD	A/D Data Register 4	ADDR4	16	16	2 or 3 PCLKB
0008 902Ah	S12AD	A/D Data Register 5	ADDR5	16	16	2 or 3 PCLKB
0008 902Ch	S12AD	A/D Data Register 6	ADDR6	16	16	2 or 3 PCLKB
0008 902Eh	S12AD	A/D Data Register 7	ADDR7	16	16	2 or 3 PCLKB
0008 9040h	S12AD	A/D Data Register 16	ADDR16	16	16	2 or 3 PCLKB
0008 9042h	S12AD	A/D Data Register 17	ADDR17	16	16	2 or 3 PCLKB
0008 9044h	S12AD	A/D Data Register 18	ADDR18	16	16	2 or 3 PCLKB
0008 9046h	S12AD	A/D Data Register 19	ADDR19	16	16	2 or 3 PCLKB
0008 9048h	S12AD	A/D Data Register 20	ADDR20	16	16	2 or 3 PCLKB
0008 904Ah	S12AD	A/D Data Register 21	ADDR21	16	16	2 or 3 PCLKB
0008 904Ch	S12AD	A/D Data Register 22	ADDR22	16	16	2 or 3 PCLKB
0008 904Eh	S12AD	A/D Data Register 23	ADDR23	16	16	2 or 3 PCLKB
0008 9050h	S12AD	A/D Data Register 24	ADDR24	16	16	2 or 3 PCLKB
0008 9052h	S12AD	A/D Data Register 25	ADDR25	16	16	2 or 3 PCLKB
0008 9054h	S12AD	A/D Data Register 26	ADDR26	16	16	2 or 3 PCLKB
0008 9056h	S12AD	A/D Data Register 27	ADDR27	16	16	2 or 3 PCLKB
0008 9058h	S12AD	A/D Data Register 28	ADDR28	16	16	2 or 3 PCLKB
0008 905Ah	S12AD	A/D Data Register 29	ADDR29	16	16	2 or 3 PCLKB
0008 905Ch	S12AD	A/D Data Register 30	ADDR30	16	16	2 or 3 PCLKB

Table 4.1 List of I/O Registers (Address Order) (10 / 18)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles
0008 A10Fh	SCI8	Transmit Data Register L	TDRL	8	8	2 or 3 PCLKB
0008 A110h	SCI8	Receive Data Register HL	RDRHL	16	16	2 or 3 PCLKB
0008 A110h	SCI8	Receive Data Register H	RDRH	8	8	2 or 3 PCLKB
0008 A111h	SCI8	Receive Data Register L	RDRL	8	8	2 or 3 PCLKB
0008 A112h	SCI8	Modulation Duty Register	MDDR	8	8	2 or 3 PCLKB
0008 A120h	SCI9	Serial Mode Register	SMR	8	8	2 or 3 PCLKB
0008 A121h	SCI9	Bit Rate Register	BRR	8	8	2 or 3 PCLKB
0008 A122h	SCI9	Serial Control Register	SCR	8	8	2 or 3 PCLKB
0008 A123h	SCI9	Transmit Data Register	TDR	8	8	2 or 3 PCLKB
0008 A124h	SCI9	Serial Status Register	SSR	8	8	2 or 3 PCLKB
0008 A125h	SCI9	Receive Data Register	RDR	8	8	2 or 3 PCLKB
0008 A126h	SMCI9	Smart Card Mode Register	SCMR	8	8	2 or 3 PCLKB
0008 A127h	SCI9	Serial Extended Mode Register	SEMR	8	8	2 or 3 PCLKB
0008 A128h	SCI9	Noise Filter Setting Register	SNFR	8	8	2 or 3 PCLKB
0008 A129h	SCI9	I^2C Mode Register 1	SIMR1	8	8	2 or 3 PCLKB
0008 A12Ah	SCI9	I^2C Mode Register 2	SIMR2	8	8	2 or 3 PCLKB
0008 A12Bh	SCI9	I^2C Mode Register 3	SIMR3	8	8	2 or 3 PCLKB
0008 A12Ch	SCI9	I^2C Status Register	SISR	8	8	2 or 3 PCLKB
0008 A12Dh	SCI9	SPI Mode Register	SPMR	8	8	2 or 3 PCLKB
0008 A12Eh	SCI9	Transmit Data Register HL	TDRHL	16	16	2 or 3 PCLKB
0008 A12Eh	SCI9	Transmit Data Register H	TDRH	8	8	2 or 3 PCLKB
0008 A12Fh	SCI9	Transmit Data Register L	TDRL	8	8	2 or 3 PCLKB
0008 A130h	SCI9	Receive Data Register HL	RDRHL	16	16	2 or 3 PCLKB
0008 A130h	SCI9	Receive Data Register H	RDRH	8	8	2 or 3 PCLKB
0008 A131h	SCI9	Receive Data Register L	RDRL	8	8	2 or 3 PCLKB
0008 A132h	SCI9	Modulation Duty Register	MDDR	8	8	2 or 3 PCLKB
0008 B000h	CAC	CAC Control Register 0	CACR0	8	8	2 or 3 PCLKB
0008 B001h	CAC	CAC Control Register 1	CACR1	8	8	2 or 3 PCLKB
0008 B002h	CAC	CAC Control Register 2	CACR2	8	8	2 or 3 PCLKB
0008 B003h	CAC	CAC Interrupt Request Enable Register	CAICR	8	8	2 or 3 PCLKB
0008 B004h	CAC	CAC Status Register	CASTR	8	8	2 or 3 PCLKB
0008 B006h	CAC	CAC Upper-Limit Value Setting Register	CAULVR	16	16	2 or 3 PCLKB
0008 B008h	CAC	CAC Lower-Limit Value Setting Register	CALLVR	16	16	2 or 3 PCLKB
0008 B00Ah	CAC	CAC Counter Buffer Register	CACNTBR	16	16	2 or 3 PCLKB
0008 B080h	DOC	DOC Control Register	DOCR	8	8	2 or 3 PCLKB
0008 B082h	DOC	DOC Data Input Register	DODIR	16	16	2 or 3 PCLKB
0008 B084h	DOC	DOC Data Setting Register	DODSR	16	16	2 or 3 PCLKB
0008 B100h	ELC	Event Link Control Register	ELCR	8	8	2 or 3 PCLKB
0008 B102h	ELC	Event Link Setting Register 1	ELSR1	8	8	2 or 3 PCLKB
0008 B103h	ELC	Event Link Setting Register 2	ELSR2	8	8	2 or 3 PCLKB
0008 B104h	ELC	Event Link Setting Register 3	ELSR3	8	8	2 or 3 PCLKB
0008 B105h	ELC	Event Link Setting Register 4	ELSR4	8	8	2 or 3 PCLKB
0008 B108h	ELC	Event Link Setting Register 7	ELSR7	8	8	2 or 3 PCLKB
0008 B109h	ELC	Event Link Setting Register 8	ELSR8	8	8	2 or 3 PCLKB
0008 B10Bh	ELC	Event Link Setting Register 10	ELSR10	8	8	2 or 3 PCLKB
0008 B10Dh	ELC	Event Link Setting Register 12	ELSR12	8	8	2 or 3 PCLKB
0008 B10Fh	ELC	Event Link Setting Register 14	ELSR14	8	8	2 or 3 PCLKB
0008 B110h	ELC	Event Link Setting Register 15	ELSR15	8	8	2 or 3 PCLKB
0008 B111h	ELC	Event Link Setting Register 16	ELSR16	8	8	2 or 3 PCLKB
0008 B113h	ELC	Event Link Setting Register 18	ELSR18	8	8	2 or 3 PCLKB
0008 B115h	ELC	Event Link Setting Register 20	ELSR20	8	8	2 or 3 PCLKB
0008 B117h	ELC	Event Link Setting Register 22	ELSR22	8	8	2 or 3 PCLKB



Note 1. All peripheral operation is normal. This does not include BGO operation. Average value of the tested middle samples during product evaluation.
Note 2. All peripheral operation is maximum. This does not include BGO operation. Average value of the tested upper-limit samples during product evaluation.

Figure 5.5 Voltage Dependency in Middle-Speed Operating Mode (Reference Data)

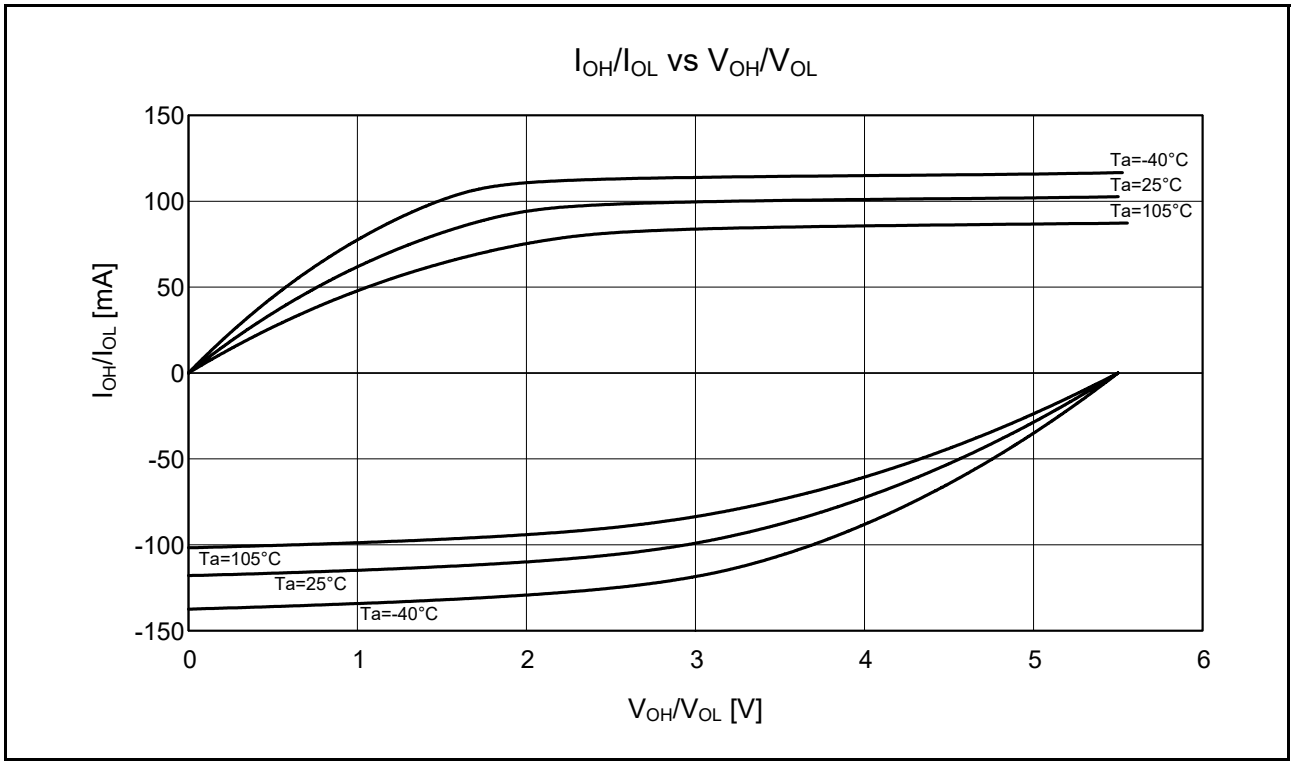


Figure 5.21 **V_{OH}/V_{OL} and I_{OH}/I_{OL} Temperature Characteristics at VCC = 5.5 V When High-Drive Output is Selected (Reference Data)**

When the main clock oscillator wait control register (MOSCWTCR) is set to 00h.

Table 5.29 Timing of Recovery from Low Power Consumption Modes (3)

Conditions: 1.8 V ≤ VCC = AVCC0 < 2.0 V, 2.0 V ≤ VCC ≤ 5.5 V, 2.0 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, Ta = –40 to +105°C

Item			Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Recovery time from software standby mode*1	Low-speed mode	Sub-clock oscillator operating	t_{SBYSC}	—	600	750	µs	Figure 5.37

Note: Note Values when the frequencies of PCLKB, PCLKD, and FCLK are not divided.
Note 1. The sub-clock continues oscillating in software standby mode during low-speed mode.

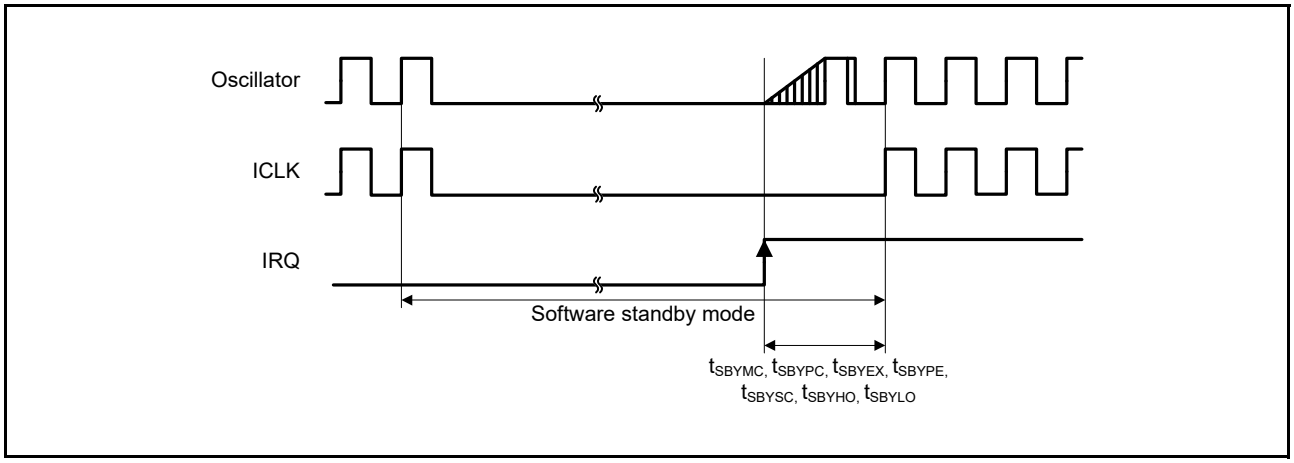


Figure 5.37 Software Standby Mode Recovery Timing

Table 5.30 Timing of Recovery from Low Power Consumption Modes (4)

Conditions: 1.8 V ≤ VCC = AVCC0 < 2.0 V, 2.0 V ≤ VCC ≤ 5.5 V, 2.0 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, Ta = –40 to +105°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Recovery time from deep sleep mode*1	High-speed mode*2	t_{DSLP}	—	2	3.5	µs	Figure 5.38
	Middle-speed mode*3	t_{DSLP}	—	3	4	µs	
	Low-speed mode*4	t_{DSLP}	—	400	500	µs	

Note: Note Values when the frequencies of PCLKB, PCLKD, and FCLK are not divided.
Note 1. Oscillators continue oscillating in deep sleep mode.
Note 2. When the frequency of the system clock is 32 MHz.
Note 3. When the frequency of the system clock is 12 MHz.
Note 4. When the frequency of the system clock is 32.768 kHz.

5.3.4 Control Signal Timing

Table 5.32 Control Signal Timing

Conditions: 1.8 V ≤ VCC = AVCC0 < 2.0 V, 2.0 V ≤ VCC ≤ 5.5 V, 2.0 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, Ta = –40 to +105°C

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	
NMI pulse width	t_{NMIW}	200	—	—	ns	NMI digital filter disabled (NMIFLTE.NFLTEN = 0)	$t_{Pcyc} \times 2 \le 200$ ns
		$t_{Pcyc} \times 2$*1	—	—			$t_{Pcyc} \times 2 > 200$ ns
		200	—	—		NMI digital filter enabled (NMIFLTE.NFLTEN = 1)	$t_{NMICK} \times 3 \le 200$ ns
		$t_{NMICK} \times 3.5$*2	—	—			$t_{NMICK} \times 3 > 200$ ns
IRQ pulse width	t_{IRQW}	200	—	—	ns	IRQ digital filter disabled (IRQFLTE0.FLTENi = 0)	$t_{Pcyc} \times 2 \le 200$ ns
		$t_{Pcyc} \times 2$*1	—	—			$t_{Pcyc} \times 2 > 200$ ns
		200	—	—		IRQ digital filter enabled (IRQFLTE0.FLTENi = 1)	$t_{IRQCK} \times 3 \le 200$ ns
		$t_{IRQCK} \times 3.5$*3	—	—			$t_{IRQCK} \times 3 > 200$ ns

Note: 200 ns minimum in software standby mode.
Note 1. t_{Pcyc} indicates the cycle of PCLKB.
Note 2. t_{NMICK} indicates the cycle of the NMI digital filter sampling clock.
Note 3. t_{IRQCK} indicates the cycle of the IRQi digital filter sampling clock (i = 0 to 7).

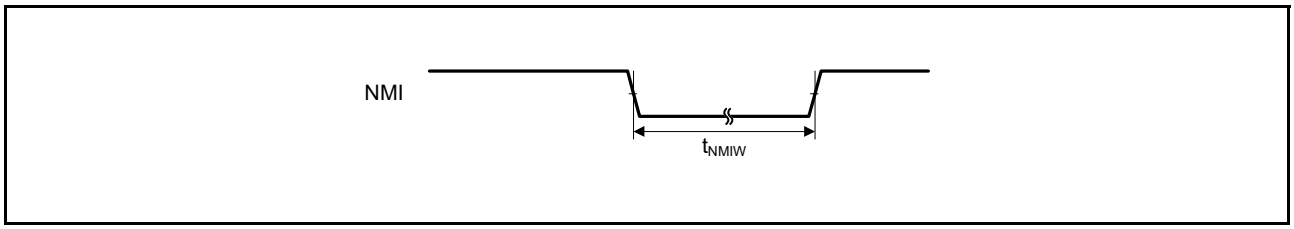


Figure 5.39 NMI Interrupt Input Timing

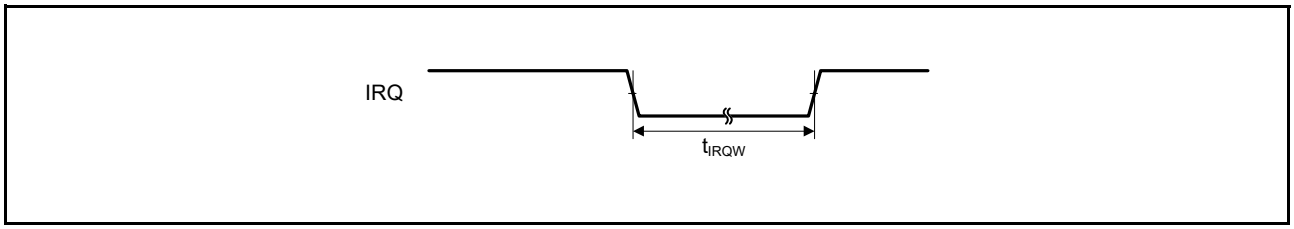
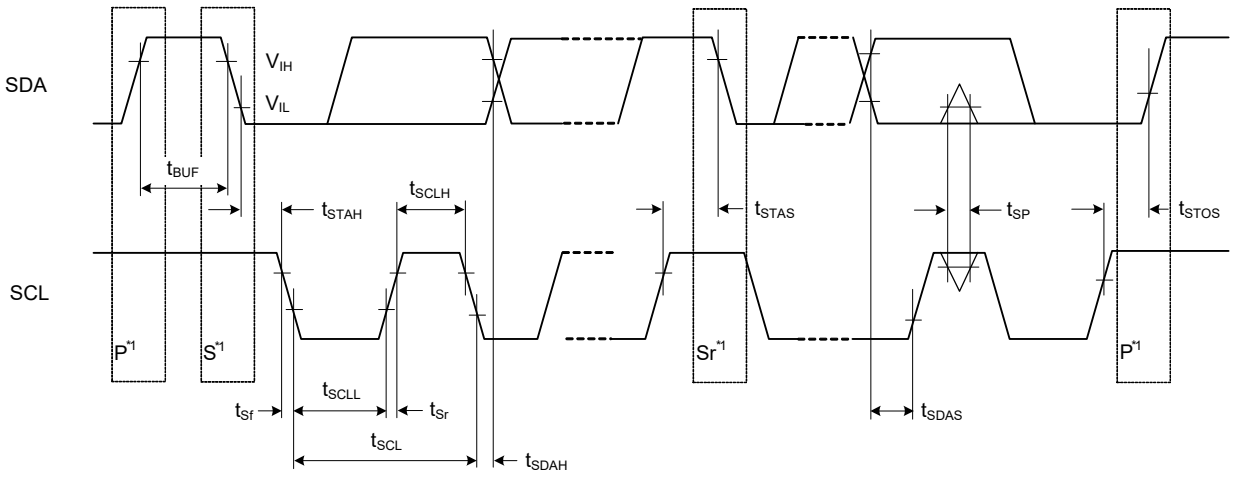


Figure 5.40 IRQ Interrupt Input Timing



Note 1. S, P, and Sr indicate the following conditions, respectively.
S: START condition
P: STOP condition
Sr: Repeated START condition

Test conditions
V_{IH} = VCC × 0.7, V_{IL} = VCC × 0.3

Figure 5.55 RIIC Bus Interface Input/Output Timing and Simple I²C Bus Interface Input/Output Timing

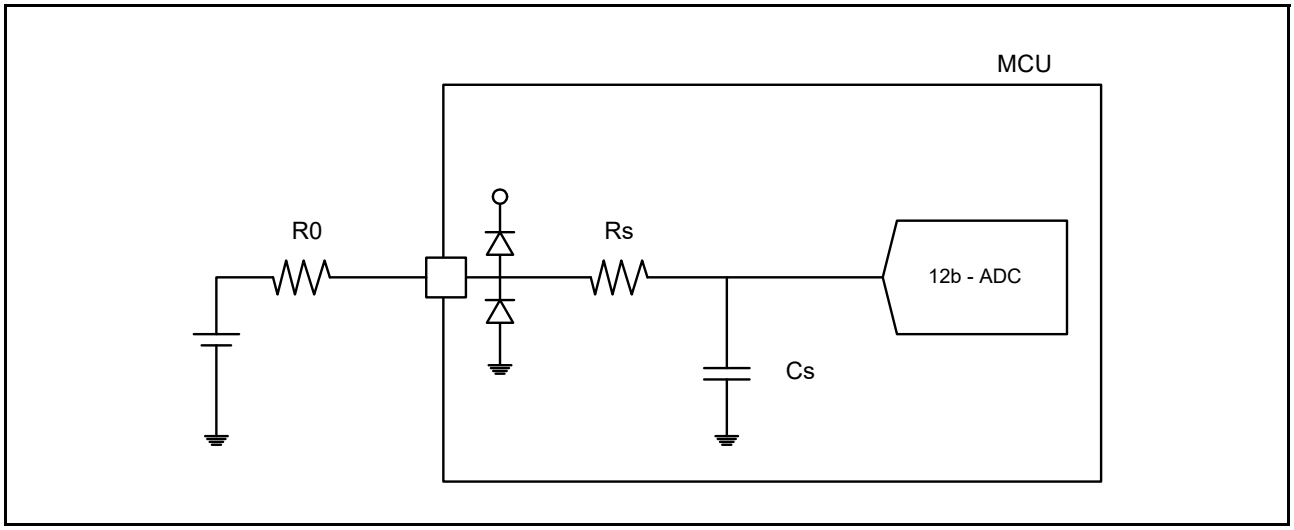


Figure 5.57 Equivalent Circuit

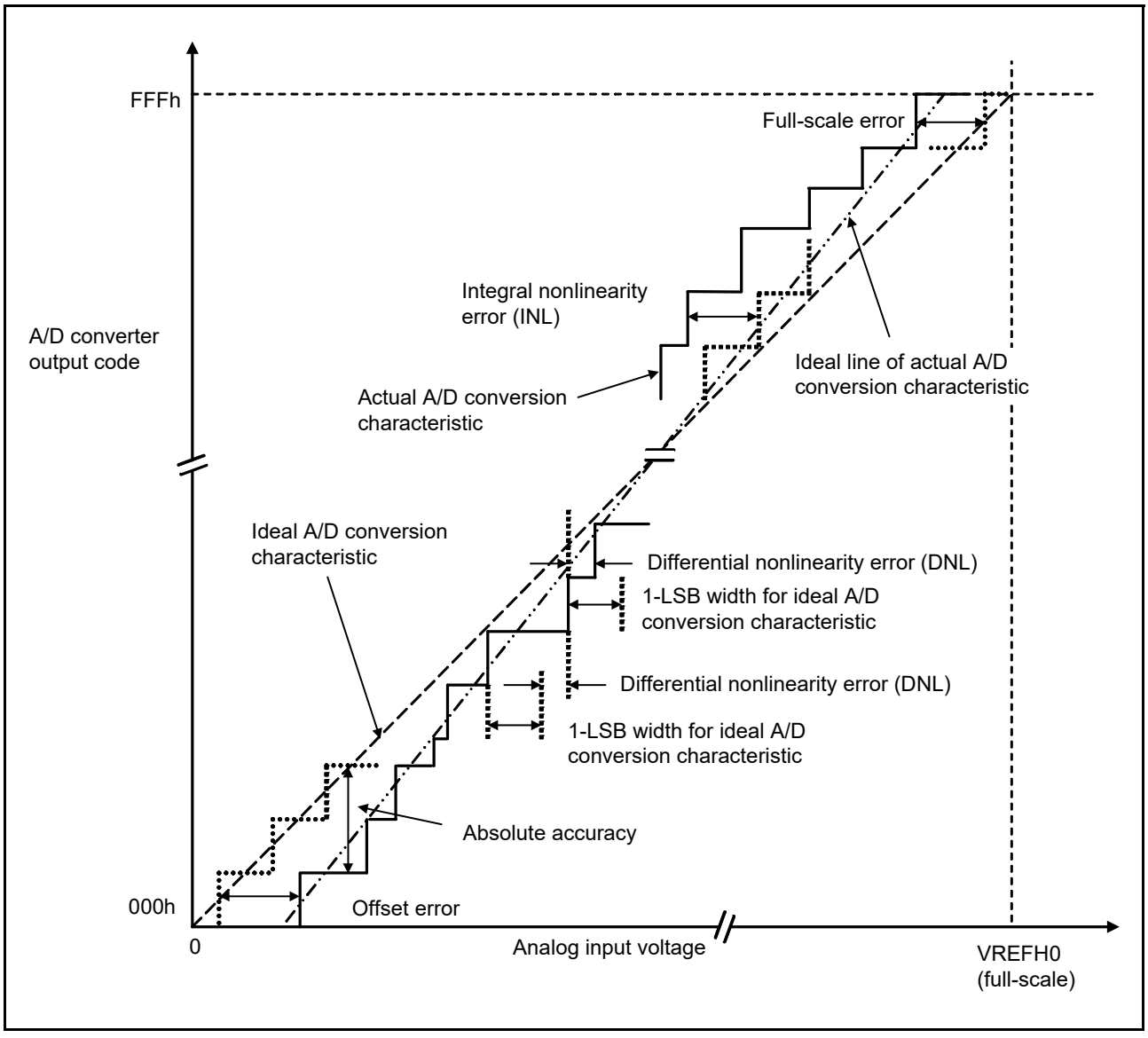
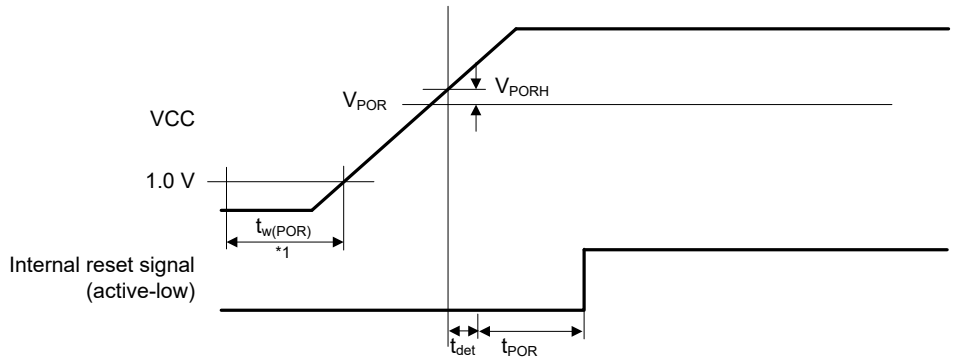


Figure 5.58 Illustration of A/D Converter Characteristic Terms



Note 1. $t_{w(POR)}$ is the time required for a power-on reset to be enabled while the external power VCC is being held below the valid voltage (1.0 V).
When VCC turns on, maintain $t_{w(POR)}$ for 1.0 ms or more.

Figure 5.62 Power-On Reset Timing

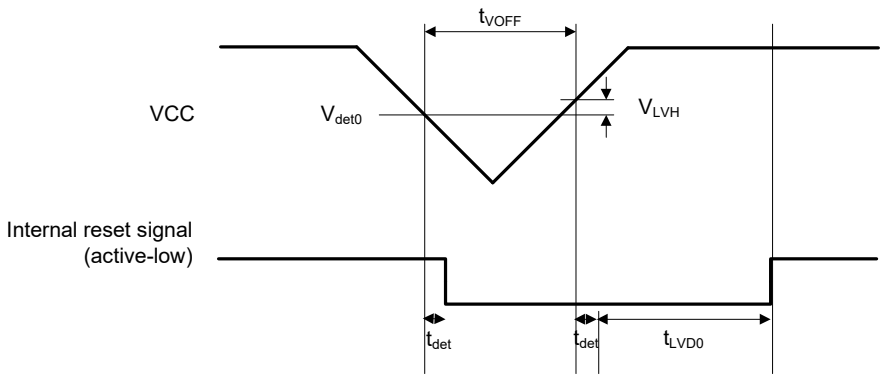


Figure 5.63 Voltage Detection Circuit Timing (V_{det0})

5.12 E2 DataFlash Characteristics (Flash Memory for Data Storage)

Table 5.55 E2 DataFlash Characteristics (1)

Item		Symbol	Min.	Typ.	Max.	Unit	Conditions
Reprogramming/erasure cycle*1		N_{DPEC}	100000	1000000	—	Times	
Data retention	After 10000 times of N_{DPEC}	t_{DDRP}	20*2, *3	—	—	Year	T_a = +85°C
	After 100000 times of N_{DPEC}		5*2, *3	—	—	Year	
	After 1000000 times of N_{DPEC}		—	1*2, *3	—	Year	T_a = +25°C

Note 1. The reprogram/erase cycle is the number of erasing for each block. When the reprogram/erase cycle is n times (n = 100000), erasing can be performed n times for each block. For instance, when 1-byte programming is performed 1000 times for different addresses in 1-Kbyte block and then the entire block is erased, the reprogram/erase cycle is counted as one. However, programming the same address for several times as one erasing is not enabled (overwriting is prohibited).
Note 2. Characteristic when using the flash memory programmer and the self-programming library provided from Renesas Electronics.
Note 3. These results are obtained from reliability testing.

Table 5.56 E2 DataFlash Characteristics (2): high-speed operating mode

Conditions: 2.7 V ≤ VCC ≤ 5.5 V, 2.7 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V

Temperature range for the programming/erasure operation: T_a = –40 to +105°C

Item		Symbol	FCLK = 1 MHz			FCLK = 32 MHz			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Programming time	1-byte	t_{DP1}	—	86	761	—	40.5	374	µs
Erasure time	1-Kbyte	t_{DE1K}	—	17.4	456	—	6.15	228	ms
	8-Kbyte	t_{DE8K}	—	60.4	499	—	9.3	231	ms
Blank check time	1-byte	t_{DBC1}	—	—	48	—	—	15.9	µs
	1-Kbyte	t_{DBC1K}	—	—	1.58	—	—	0.127	µs
Erase operation forcible stop time		t_{DSED}	—	—	21.5	—	—	12.8	µs
DataFlash STOP recovery time		t_{DSTOP}	5.0	—	—	5	—	—	µs

Note: Does not include the time until each operation of the flash memory is started after instructions are executed by software.
Note: The lower-limit frequency of FCLK is 1 MHz during programming or erasing of the flash memory. When using FCLK at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.
Note: The frequency accuracy of FCLK should be ±3.5%.

Table 5.57 E2 DataFlash Characteristics (3): middle-speed operating mode

Conditions: 1.8 V ≤ VCC = AVCC0 < 2.0 V, 2.0 V ≤ VCC ≤ 5.5 V, 2.0 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V

Temperature range for the programming/erasure operation: T_a = –40 to +85°C

Item		Symbol	FCLK = 1 MHz			FCLK = 8 MHz			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Programming time	1-byte	t_{DP1}	—	126	1160	—	85.4	818	µs
Erasure time	1-Kbyte	t_{DE1K}	—	17.5	457	—	7.76	259	ms
	8-Kbyte	t_{DE8K}	—	60.5	500	—	4.2	66.9	ms
Blank check time	1-byte	t_{DBC1}	—	—	78	—	—	50	µs
	1-Kbyte	t_{DBC1K}	—	—	1.61	—	—	0.369	ms
Erase operation forcible stop time		t_{DSED}	—	—	33.5	—	—	25.5	µs
DataFlash STOP recovery time		t_{DSTOP}	720	—	—	720	—	—	ns

Note: Does not include the time until each operation of the flash memory is started after instructions are executed by software.
Note: The lower-limit frequency of FCLK is 1 MHz during programming or erasing of the flash memory. When using FCLK at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.
Note: The frequency accuracy of FCLK should be ±3.5%.

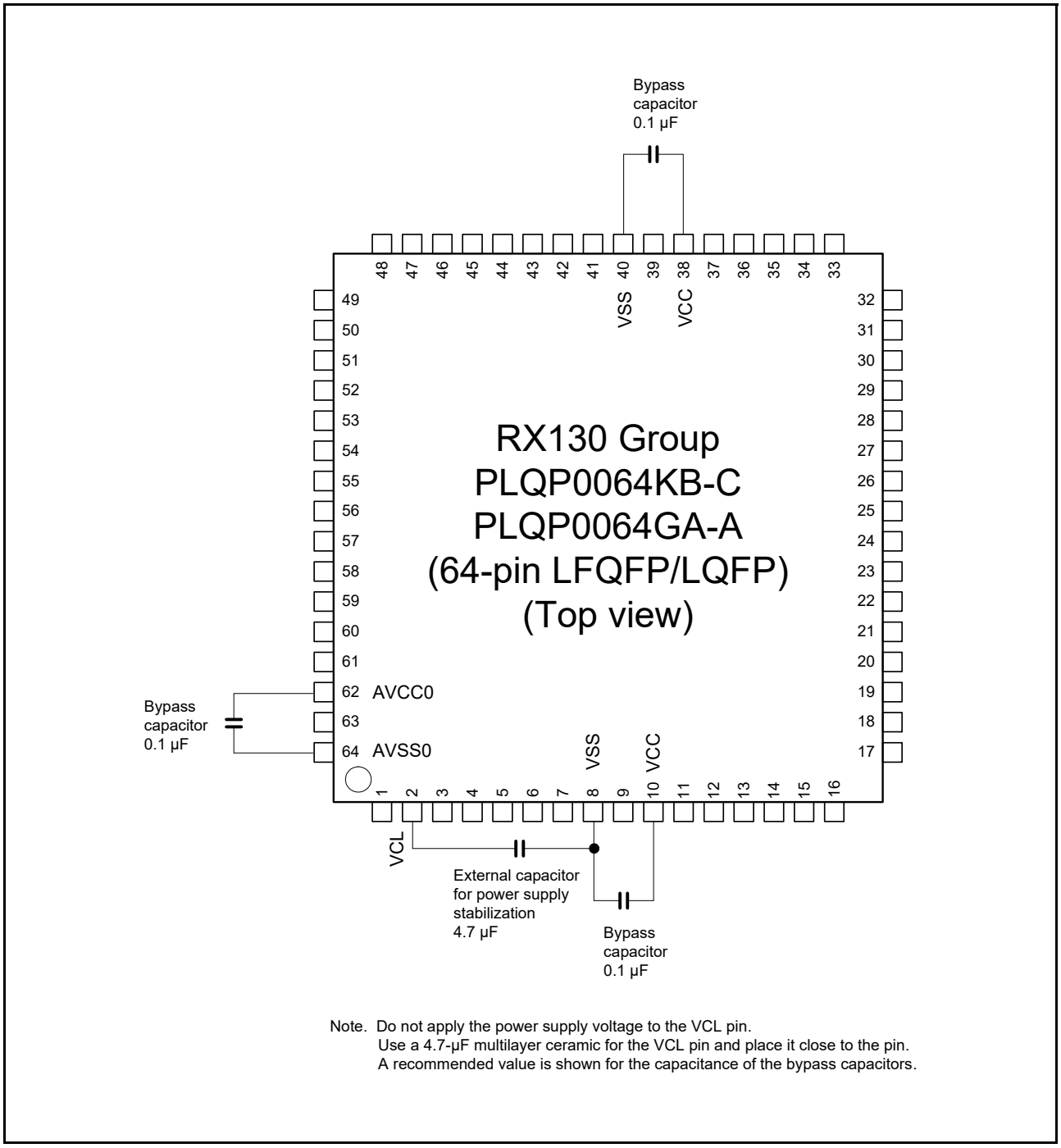
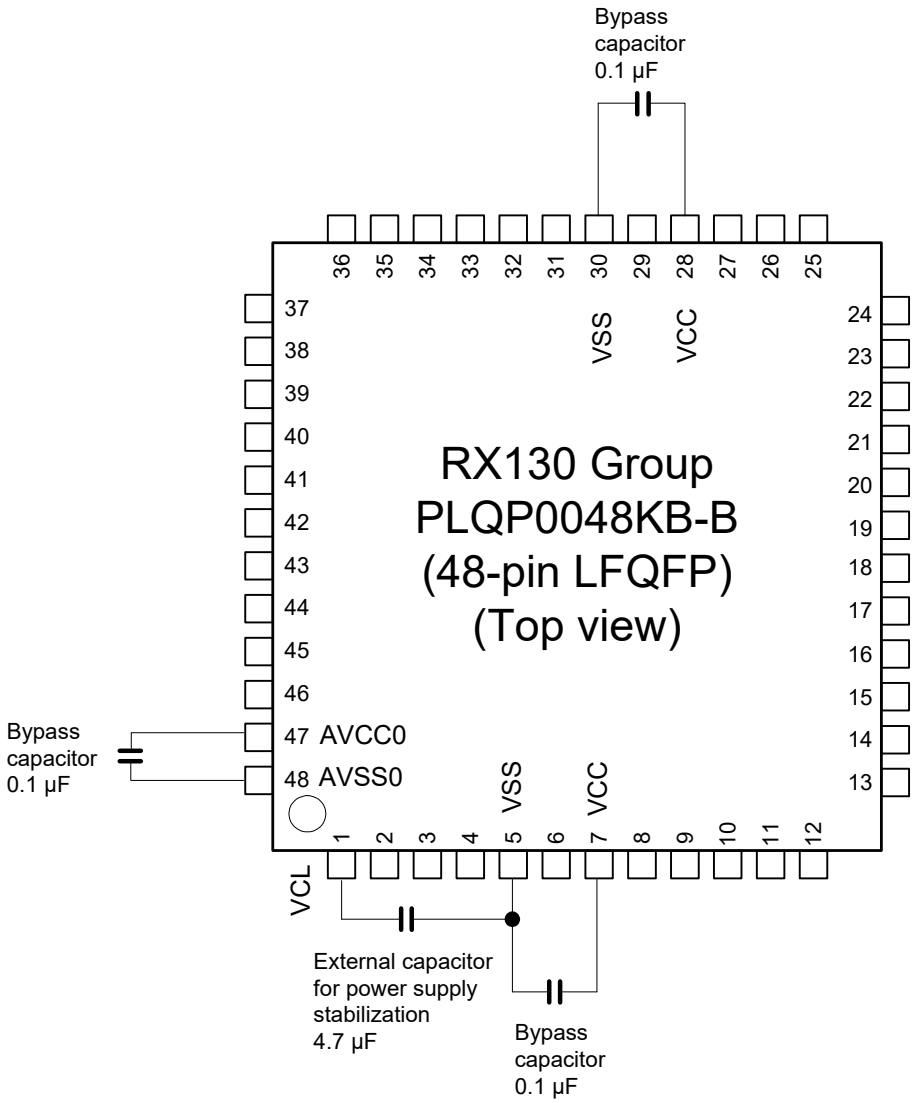


Figure 5.69 Connecting Capacitors (64 Pins)



Note. Do not apply the power supply voltage to the VCL pin.
Use a 4.7-µF multilayer ceramic for the VCL pin and place it close to the pin.
A recommended value is shown for the capacitance of the bypass capacitors.

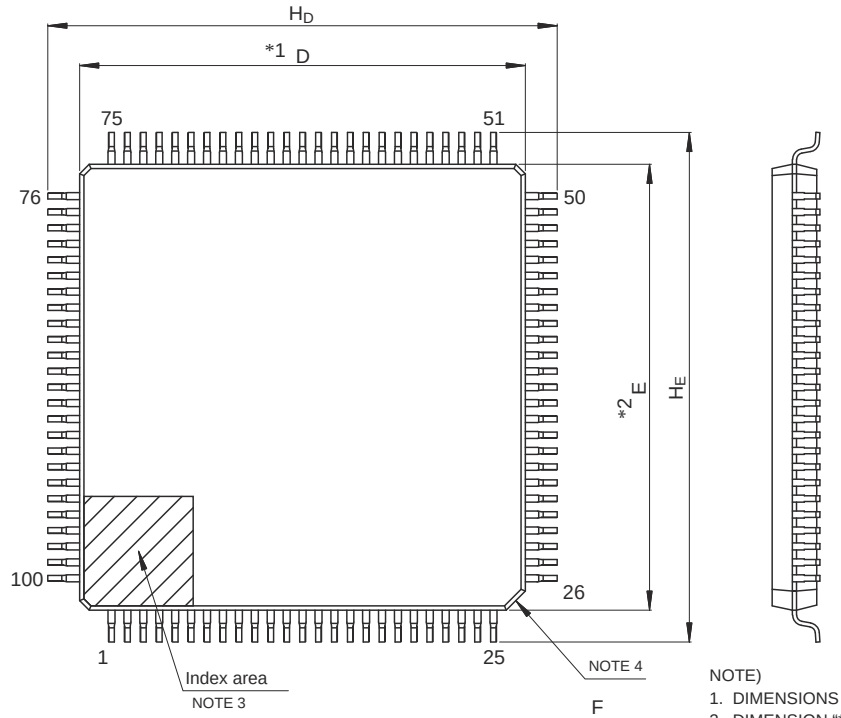
Figure 5.70 Connecting Capacitors (48 Pins)

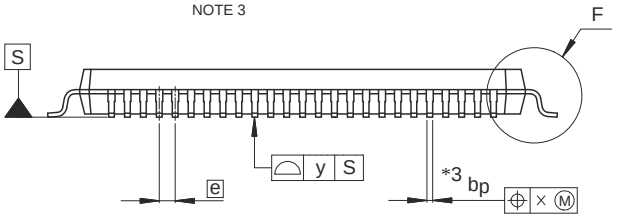
Appendix 1. Package Dimensions

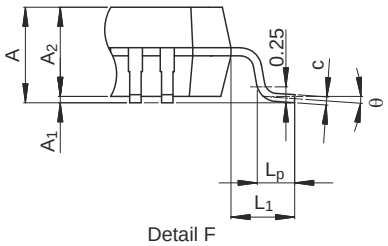
Information on the latest version of the package dimensions or mountings has been displayed in “Packages” on Renesas Electronics Corporation website.

JEITA Package Code	RENESAS Code	Previous Code	MASS (Typ) [g]
P-LFQFP100-14x14-0.50	PLQP0100KB-B	—	0.6

Unit: mm





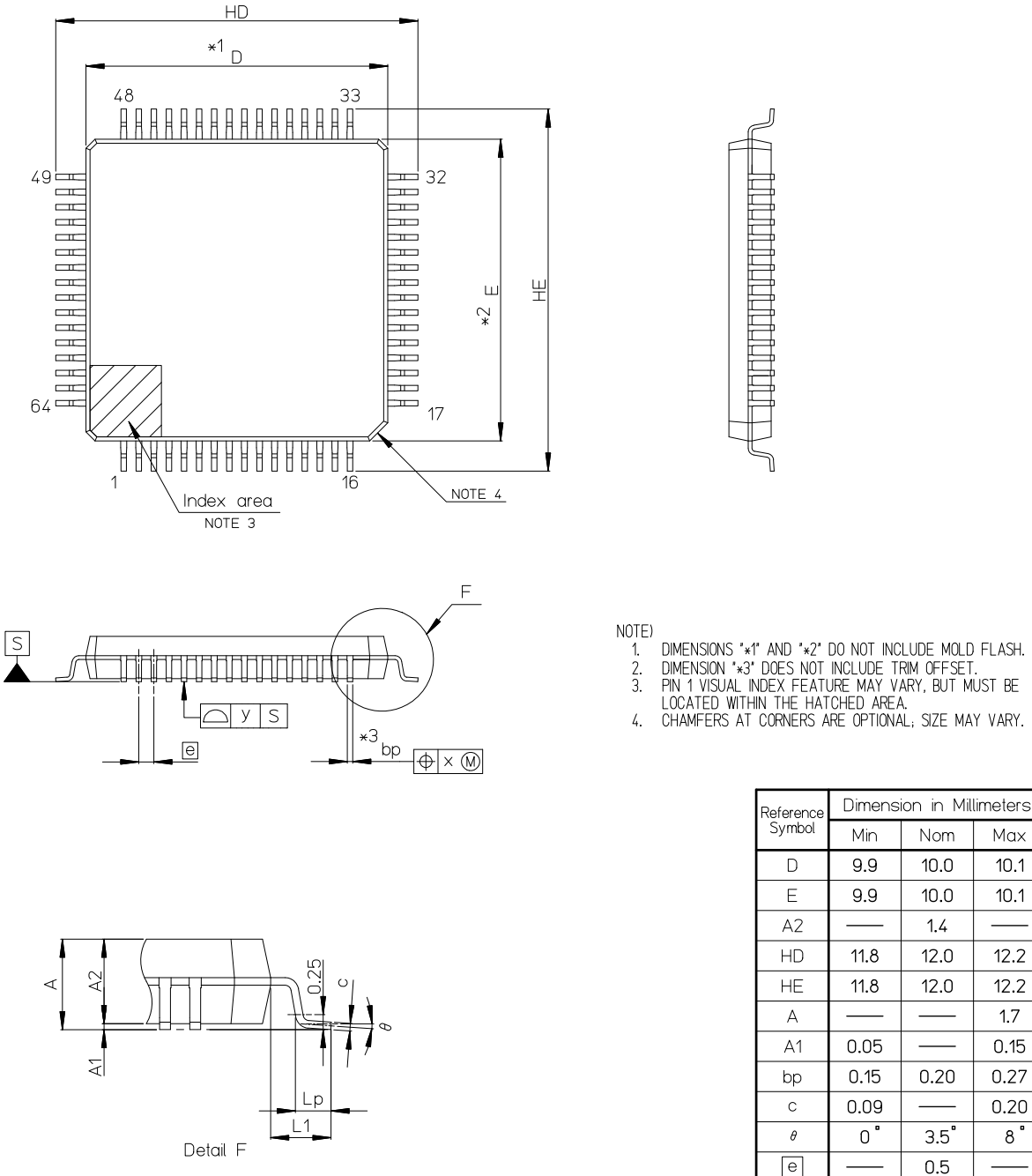


NOTE)
1. DIMENSIONS “*1” AND “*2” DO NOT INCLUDE MOLD FLASH.
2. DIMENSION “*3” DOES NOT INCLUDE TRIM OFFSET.
3. PIN 1 VISUAL INDEX FEATURE MAY VARY, BUT MUST BE LOCATED WITHIN THE HATCHED AREA.
4. CHAMFERS AT CORNERS ARE OPTIONAL, SIZE MAY VARY.

Reference Symbol	Dimensions in millimeters		
	Min	Nom	Max
D	13.9	14.0	14.1
E	13.9	14.0	14.1
A_2	—	1.4	—
H_D	15.8	16.0	16.2
H_E	15.8	16.0	16.2
A	—	—	1.7
A_1	0.05	—	0.15
b_p	0.15	0.20	0.27
c	0.09	—	0.20
θ	0°	3.5°	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
L_p	0.45	0.6	0.75
L_1	—	1.0	—

Figure A 100-Pin LFQFP (PLQP0100KB-B)

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LFQFP64-10x10-0.50	PLQP0064KB-C	——	0.3g



NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.
3. PIN 1 VISUAL INDEX FEATURE MAY VARY, BUT MUST BE LOCATED WITHIN THE HATCHED AREA.
4. CHAMFERS AT CORNERS ARE OPTIONAL; SIZE MAY VARY.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	9.9	10.0	10.1
E	9.9	10.0	10.1
A2	——	1.4	——
HD	11.8	12.0	12.2
HE	11.8	12.0	12.2
A	——	——	1.7
A1	0.05	——	0.15
bp	0.15	0.20	0.27
c	0.09	——	0.20
θ	0°	3.5°	8°
e	——	0.5	——
x	——	——	0.08
y	——	——	0.08
Lp	0.45	0.6	0.75
L1	——	1.0	——

Figure D 64-Pin LFQFP (PLQP0064KB-C)

REVISION HISTORY	RX130 Group Datasheet

Classifications

- Items with Technical Update document number: Changes according to the corresponding issued Technical Update
- Items without Technical Update document number: Minor changes that do not require Technical Update to be issued

Rev.	Date	Description		Classification
		Page	Summary	
1.00	Oct 30, 2015	—	First edition, issued	
2.00	Sep 01, 2017	All	Products with at least 256 Kbytes of code flash memory and 100-pin packages added	
		4. I/O Registers		
		42	Table 4.1 List of I/O Registers (Address Order), changed	TN-RX*-A179A/E
		5. Electrical Characteristics		
		49	Table 5.2 Recommended Operating Voltage Conditions Note 3, added	
		57 to 61	The characteristics of products with at least 256 Kbytes of flash memory or 100-pin packages added	
		64, 65	The characteristics of products with at least 256 Kbytes of flash memory or 100-pin packages added	
		90	Table 5.34 Timing of On-Chip Peripheral Modules (2), changed	TN-RX*-A179A/E
		91	Table 5.35 Timing of On-Chip Peripheral Modules (3), changed	
		93	Table 5.38 Timing of On-Chip Peripheral Modules (6), added	
		111	Table 5.48 CTSU Characteristics, item for products with at least 256 Kbytes of flash memory or 100-pin packages added	
		113	Table 5.50 Power-On Reset Circuit and Voltage Detection Circuit Characteristics (2), item with Vdet0_0 to Vdet0_3 selected added	
		117	Table 5.53 ROM (Flash Memory for Code Storage) Characteristics (2) High-Speed Operating Mode, erasure time (128-Kbyte) deleted and erasure time (256-Kbyte) added	
		118	Table 5.54 ROM (Flash Memory for Code Storage) Characteristics (3) Middle-Speed Operating Mode, erasure time (128-Kbyte) deleted and erasure time (256-Kbyte) added	