Renesas Electronics America Inc - R5F51303ADFM#30 Datasheet

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	RX
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	I²C, LINbus, SCI, SPI
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	52
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	8K x 8
RAM Size	10K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 14x12b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LFQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f51303adfm-30

Table 1.1 Outline of Specifications (3/3)

Classification	Module/Function	Description
Communication functions	Serial peripheral interface (RSPIa)	• 1 channel • Transfer facility Using the MOSI (master out, slave in), MISO (master in, slave out), SSL (slave select), and RSPCK (RSPI clock) signals enables serial transfer through SPI operation (four lines) or clock-synchronous operation (three lines) • Capable of handling serial transfer as a master or slave • Data formats • Choice of LSB-first or MSB-first transfer The number of bits in each transfer can be changed to 8, 9, 10, 11, 12, 13, 14, 15, 16, 20, 24, or 32 bits. 128-bit buffers for transmission and reception Up to four frames can be transmitted or received in a single transfer operation (with each frame having up to 32 bits) • Double buffers for both transmission and reception
	Remote control signal receiver (REMC)	• 2 channels • Four pattern matching (header, data 0, data 1, and special data detection) • 8-byte receive buffer per unit • The operating clock can be selected from among the PCLK, sub-clock, HOCO, IWDTCLK, and TMR.
12-bit A/D converter (S12ADE)		• 12 bits (24 channels × 1 unit) • 12-bit resolution • Minimum conversion time: 1.4 µs per channel when the ADCLK is operating at 32 MHz • Operating modes Scan mode (single scan mode, continuous scan mode, and group scan mode) Group A priority control (only for group scan mode) • Sampling variable Sampling time can be set up for each channel. • Self-diagnostic function • Double trigger mode (A/D conversion data duplicated) • Detection of analog input disconnection • Conversion results compare features • A/D conversion start conditions A software trigger, a trigger from a timer (MTU), an external trigger signal, or ELC • Event linking by the ELC
Temperature sensor (TEMPSA)		• 1 channel • The voltage output from the temperature sensor is converted into a digital value by the 12-bit A/D converter.
D/A converter (DA)		• 2 channels • 8-bit resolution • Output voltage: 0V to AVCC0
CRC calculator (CRC)		• CRC code generation for arbitrary amounts of data in 8-bit units • Select any of three generating polynomials: $X^8 + X^2 + X + 1$, $X^{16} + X^{15} + X^2 + 1$, or $X^{16} + X^{12} + X^5 + 1$ • Generation of CRC codes for use with LSB-first or MSB-first communications is selectable.
Comparator B (CMPBa)		• 2 channels • Function to compare the reference voltage and the analog input voltage • Window comparator operation or standard comparator operation is selectable
Capacitive touch sensing unit (CTSUa)		Detection pin: 36 channels
Data operation circuit (DOC)		Comparison, addition, and subtraction of 16-bit data
Unique ID		32-byte ID code for the MCU
Power supply voltages/Operating frequencies		VCC = 1.8 to 2.4 V: 8 MHz, VCC = 2.4 to 2.7 V: 16 MHz, VCC = 2.7 to 5.5 V: 32 MHz
Operating temperature range		D version: –40 to +85°C, G version: –40 to +105°C
Packages		100-pin LFQFP (PLQP0100KB-B) 14 × 14 mm, 0.5 mm pitch 80-pin LFQFP (PLQP0080KB-B) 12 × 12 mm, 0.5 mm pitch 64-pin LFQFP (PLQP0064KB-C) 10 × 10 mm, 0.5 mm pitch 64-pin LQFP (PLQP0064GA-A) 14 × 14 mm, 0.8 mm pitch 48-pin LFQFP (PLQP0048KB-B) 7 × 7 mm, 0.5 mm pitch 48-pin HWQFN (PWQN0048KB-A) 7 × 7 mm, 0.5 mm pitch
On-chip debugging system		E1 emulator (FINE interface)

Note 1. When the realtime clock is not to be used, refer to section 24.5.7, Initialization Procedure When the Realtime Clock is Not to be Used.

1.3 Block Diagram

Figure 1.2 shows a block diagram.

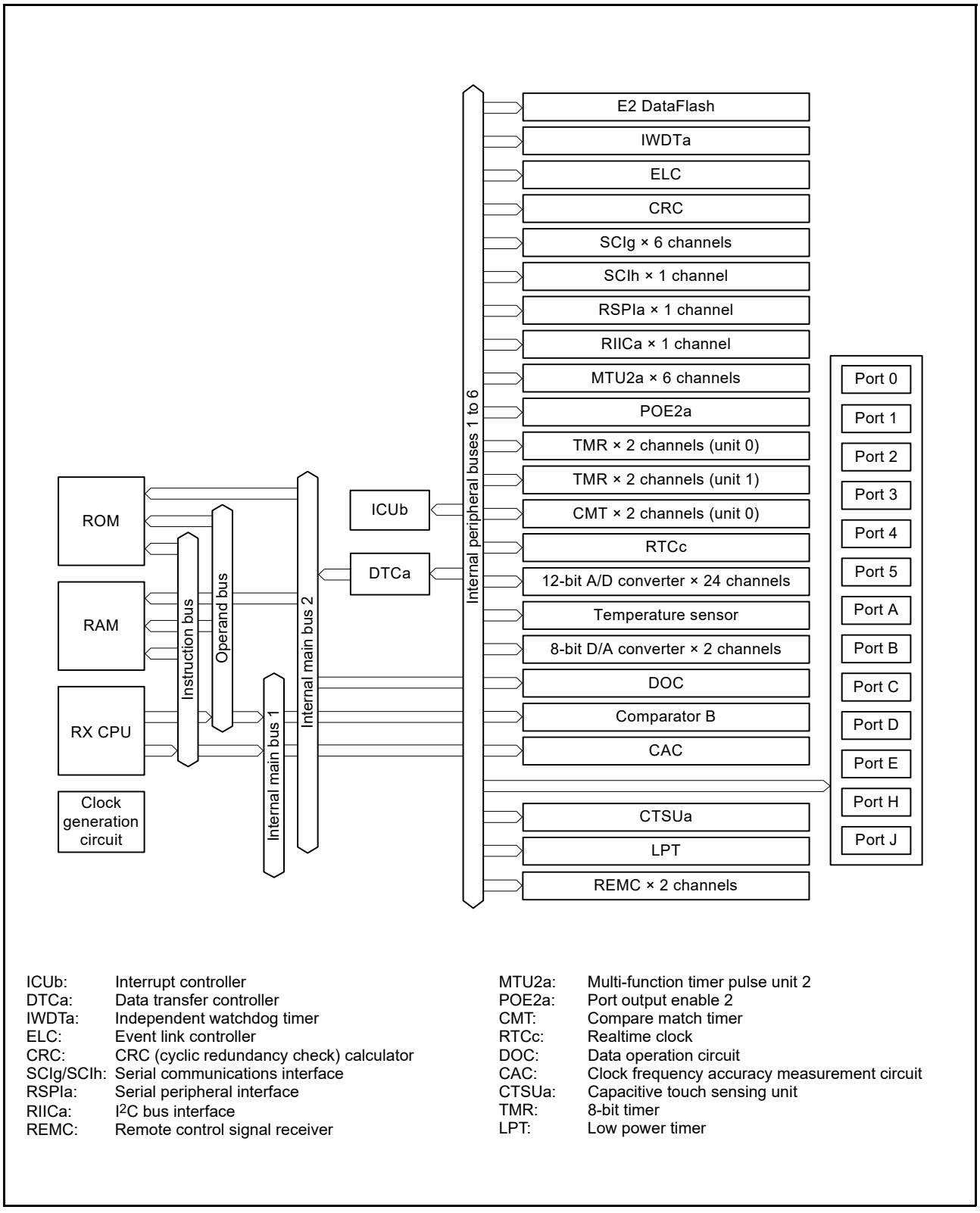


Figure 1.2 Block Diagram

1.4 Pin Functions

Table 1.4 lists the pin functions.

Table 1.4 Pin Functions (1/3)

Classifications	Pin Name	I/O	Description
Power supply	VCC	Input	Power supply pin. Connect it to the system power supply.
	VCL	—	Connect this pin to the VSS pin via the 4.7 μF smoothing capacitor used to stabilize the internal power supply. Place the capacitor close to the pin.
	VSS	Input	Ground pin. Connect it to the system power supply (0 V).
Clock	XTAL	Output	Pins for connecting a crystal. An external clock can be input through the EXTAL pin.
	EXTAL	Input	
	XCIN	Input	Input/output pins for the sub-clock oscillator. Connect a crystal between XCIN and XCOUT.
	XCOUT	Output	
	CLKOUT	Output	Clock output pin.
Operating mode control	MD	Input	Pin for setting the operating mode. The signal levels on this pin must not be changed during operation.
System control	RES#	Input	Reset pin. This MCU enters the reset state when this signal goes low.
CAC	CACREF	Input	Input pin for the clock frequency accuracy measurement circuit.
On-chip emulator	FINED	I/O	FINE interface pin.
Interrupts	NMI	Input	Non-maskable interrupt request pin.
	IRQ0 to IRQ7	Input	Interrupt request pins.
Multi-function timer pulse unit 2	MTIOC0A, MTIOC0B, MTIOC0C, MTIOC0D	I/O	The TGRA0 to TGRD0 input capture input/output compare output/PWM output pins.
	MTIOC1A, MTIOC1B	I/O	The TGRA1 and TGRB1 input capture input/output compare output/PWM output pins.
	MTIOC2A, MTIOC2B	I/O	The TGRA2 and TGRB2 input capture input/output compare output/PWM output pins.
	MTIOC3A, MTIOC3B, MTIOC3C, MTIOC3D	I/O	The TGRA3 to TGRD3 input capture input/output compare output/PWM output pins.
	MTIOC4A, MTIOC4B, MTIOC4C, MTIOC4D	I/O	The TGRA4 to TGRD4 input capture input/output compare output/PWM output pins.
	MTIC5U, MTIC5V, MTIC5W	Input	The TGRU5, TGRV5, and TGRW5 input capture input/external pulse input pins.
	MTCLKA, MTCLKB, MTCLKC, MTCLKD	Input	Input pins for the external clock.
Port output enable 2	POE0# to POE3#, POE8#	Input	Input pins for request signals to place the MTU pins in the high impedance state.
Realtime clock	RTCOUT	Output	Output pin for the 1-Hz/64-Hz clock.
8-bit timer	TMO0 to TMO3	Output	Compare match output pins.
	TMCI0 to TMCI3	Input	Input pins for the external clock to be input to the counter.
	TMRI0 to TMRI3	Input	Counter reset input pins.

Table 1.4 Pin Functions (2/3)

Classifications	Pin Name	I/O	Description
Serial communications interface (SCIg)	• Asynchronous mode/clock synchronous mode		
	SCK0, SCK1, SCK5, SCK6, SCK8, SCK9	I/O	Input/output pins for the clock.
	RXD0, RXD1, RXD5, RXD6, RXD8, RXD9	Input	Input pins for received data.
	TXD0, TXD1, TXD5, TXD6, TXD8, TXD9	Output	Output pins for transmitted data.
	CTS0#, CTS1#, CTS5#, CTS6#, CTS8#, CTS9#	Input	Input pins for controlling the start of transmission and reception.
	RTS0#, RTS1#, RTS5#, RTS6#, RTS8#, RTS9#	Output	Output pins for controlling the start of transmission and reception.
	• Simple I^2C mode		
	SSCL0, SSCL1, SSCL5, SSCL6, SSCL8, SSCL9	I/O	Input/output pins for the I^2C clock.
	SSDA0, SSDA1, SSDA5, SSDA6, SSDA8, SSDA9	I/O	Input/output pins for the I^2C data.
	• Simple SPI mode		
	SCK0, SCK1, SCK5, SCK6, SCK8, SCK9	I/O	Input/output pins for the clock.
	SMISO0, SMISO1, SMISO5, SMISO6, SMISO8, SMISO9	I/O	Input/output pins for slave transmit data.
	SMOSI0, SMOSI1, SMOSI5, SMOSI6, SMOSI8, SMOSI9	I/O	Input/output pins for master transmit data.
	SS0#, SS1#, SS5#, SS6#, SS8#, SS9#	Input	Slave-select input pins.
Serial communications interface (SCIh)	• Asynchronous mode/clock synchronous mode		
	SCK12	I/O	Input/output pin for the clock.
	RXD12	Input	Input pin for receiving data.
	TXD12	Output	Output pin for transmitting data.
	CTS12#	Input	Input pin for controlling the start of transmission and reception.
	RTS12#	Output	Output pin for controlling the start of transmission and reception.
	• Simple I^2C mode		
	SSCL12	I/O	Input/output pin for the I^2C clock.
	SSDA12	I/O	Input/output pin for the I^2C data.
	• Simple SPI mode		
	SCK12	I/O	Input/output pin for the clock.
	SMISO12	I/O	Input/output pin for slave transmit data.
	SMOSI12	I/O	Input/output pin for master transmit data.
	SS12#	Input	Slave-select input pin.
	• Extended serial mode		
	RXDX12	Input	Input pin for data reception by SCIf.
	TXDX12	Output	Output pin for data transmission by SCIf.
	SIOX12	I/O	Input/output pin for data reception or transmission by SCIf.
I^2C bus interface	SCL	I/O	Input/output pin for I^2C bus interface clocks. Bus can be directly driven by the N-channel open drain output.
	SDA	I/O	Input/output pin for I^2C bus interface data. Bus can be directly driven by the N-channel open drain output.

Table 4.1 List of I/O Registers (Address Order) (6 / 18)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles
0008 88A2h	MTU5	Timer General Register W	TGRW	16	16	2 or 3 PCLKB
0008 88A4h	MTU5	Timer Control Register W	TCRW	8	8	2 or 3 PCLKB
0008 88A6h	MTU5	Timer I/O Control Register W	TIORW	8	8	2 or 3 PCLKB
0008 88B2h	MTU5	Timer Interrupt Enable Register	TIER	8	8	2 or 3 PCLKB
0008 88B4h	MTU5	Timer Start Register	TSTR	8	8	2 or 3 PCLKB
0008 88B6h	MTU5	Timer Compare Match Clear Register	TCNTCMPCLR	8	8	2 or 3 PCLKB
0008 8900h	POE	Input Level Control/Status Register 1	ICSR1	16	8, 16	2 or 3 PCLKB
0008 8902h	POE	Output Level Control/Status Register 1	OCSR1	16	8, 16	2 or 3 PCLKB
0008 8908h	POE	Input Level Control/Status Register 2	ICSR2	16	8, 16	2 or 3 PCLKB
0008 890Ah	POE	Software Port Output Enable Register	SPOER	8	8	2 or 3 PCLKB
0008 890Bh	POE	Port Output Enable Control Register 1	POECR1	8	8	2 or 3 PCLKB
0008 890Ch	POE	Port Output Enable Control Register 2	POECR2	8	8	2 or 3 PCLKB
0008 890Eh	POE	Input Level Control/Status Register 3	ICSR3	16	8, 16	2 or 3 PCLKB
0008 9000h	S12AD	A/D Control Register	ADCSR	16	16	2 or 3 PCLKB
0008 9004h	S12AD	A/D Channel Select Register A0	ADANSA0	16	16	2 or 3 PCLKB
0008 9006h	S12AD	A/D Channel Select Register A1	ADANSA1	16	16	2 or 3 PCLKB
0008 9008h	S12AD	A/D-Converted Value Addition/Average Function Select Register 0	ADADS0	16	16	2 or 3 PCLKB
0008 900Ah	S12AD	A/D-Converted Value Addition/Average Function Select Register 1	ADADS1	16	16	2 or 3 PCLKB
0008 900Ch	S12AD	A/D-Converted Value Addition/Average Count Select Register	ADADC	8	8	2 or 3 PCLKB
0008 900Eh	S12AD	A/D Control Extended Register	ADCER	16	16	2 or 3 PCLKB
0008 9010h	S12AD	A/D Conversion Start Trigger Select Register	ADSTRGR	16	16	2 or 3 PCLKB
0008 9012h	S12AD	A/D Conversion Extended Input Control Register	ADEXICR	16	16	2 or 3 PCLKB
0008 9014h	S12AD	A/D Channel Select Register B0	ADANSB0	16	16	2 or 3 PCLKB
0008 9016h	S12AD	A/D Channel Select Register B1	ADANSB1	16	16	2 or 3 PCLKB
0008 9018h	S12AD	A/D Data Duplication Register	ADDBLDR	16	16	2 or 3 PCLKB
0008 901Ah	S12AD	A/D Temperature Sensor Data Register	ADTSDR	16	16	2 or 3 PCLKB
0008 901Ch	S12AD	A/D Internal Reference Voltage Data Register	ADOCDR	16	16	2 or 3 PCLKB
0008 901Eh	S12AD	A/D Self-Diagnosis Data Register	ADRD	16	16	2 or 3 PCLKB
0008 9020h	S12AD	A/D Data Register 0	ADDR0	16	16	2 or 3 PCLKB
0008 9022h	S12AD	A/D Data Register 1	ADDR1	16	16	2 or 3 PCLKB
0008 9024h	S12AD	A/D Data Register 2	ADDR2	16	16	2 or 3 PCLKB
0008 9026h	S12AD	A/D Data Register 3	ADDR3	16	16	2 or 3 PCLKB
0008 9028h	S12AD	A/D Data Register 4	ADDR4	16	16	2 or 3 PCLKB
0008 902Ah	S12AD	A/D Data Register 5	ADDR5	16	16	2 or 3 PCLKB
0008 902Ch	S12AD	A/D Data Register 6	ADDR6	16	16	2 or 3 PCLKB
0008 902Eh	S12AD	A/D Data Register 7	ADDR7	16	16	2 or 3 PCLKB
0008 9040h	S12AD	A/D Data Register 16	ADDR16	16	16	2 or 3 PCLKB
0008 9042h	S12AD	A/D Data Register 17	ADDR17	16	16	2 or 3 PCLKB
0008 9044h	S12AD	A/D Data Register 18	ADDR18	16	16	2 or 3 PCLKB
0008 9046h	S12AD	A/D Data Register 19	ADDR19	16	16	2 or 3 PCLKB
0008 9048h	S12AD	A/D Data Register 20	ADDR20	16	16	2 or 3 PCLKB
0008 904Ah	S12AD	A/D Data Register 21	ADDR21	16	16	2 or 3 PCLKB
0008 904Ch	S12AD	A/D Data Register 22	ADDR22	16	16	2 or 3 PCLKB
0008 904Eh	S12AD	A/D Data Register 23	ADDR23	16	16	2 or 3 PCLKB
0008 9050h	S12AD	A/D Data Register 24	ADDR24	16	16	2 or 3 PCLKB
0008 9052h	S12AD	A/D Data Register 25	ADDR25	16	16	2 or 3 PCLKB
0008 9054h	S12AD	A/D Data Register 26	ADDR26	16	16	2 or 3 PCLKB
0008 9056h	S12AD	A/D Data Register 27	ADDR27	16	16	2 or 3 PCLKB
0008 9058h	S12AD	A/D Data Register 28	ADDR28	16	16	2 or 3 PCLKB
0008 905Ah	S12AD	A/D Data Register 29	ADDR29	16	16	2 or 3 PCLKB
0008 905Ch	S12AD	A/D Data Register 30	ADDR30	16	16	2 or 3 PCLKB

Table 4.1 List of I/O Registers (Address Order) (18 / 18)

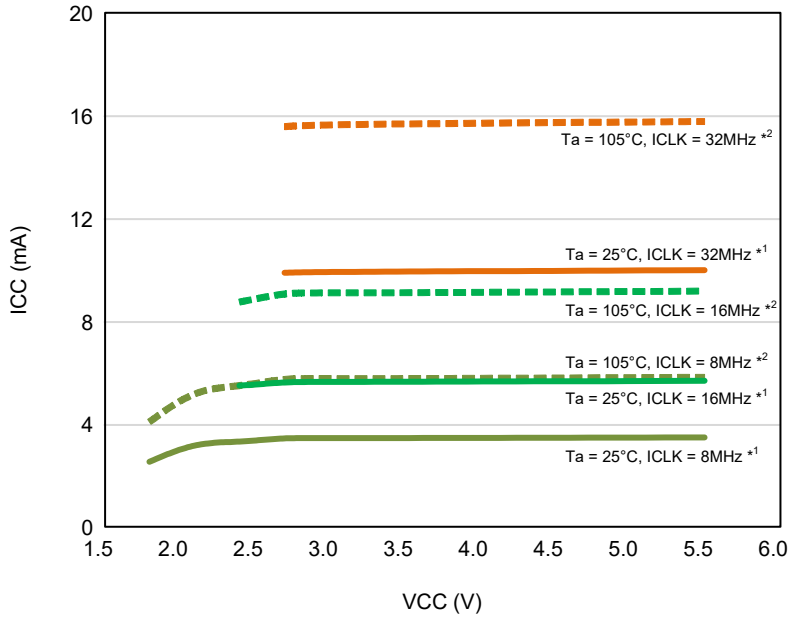
Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles
007F C0B2h	FLASH	Flash Access Window Start Address Monitor Register	FAWSMR	16	16	2 or 3 FCLK
007F C0B4h	FLASH	Flash Access Window End Address Monitor Register	FAWEMR	16	16	2 or 3 FCLK
007F C0B6h	FLASH	Flash Initial Setting Register	FISR	8	8	2 or 3 FCLK
007F C0B7h	FLASH	Flash Extra Area Control Register	FEXCR	8	8	2 or 3 FCLK
007F C0B8h	FLASH	Flash Error Address Monitor Register L	FEAML	16	16	2 or 3 FCLK
007F C0BAh	FLASH	Flash Error Address Monitor Register H	FEAMH	8	8	2 or 3 FCLK
007F C0C0h	FLASH	Protection Unlock Register	FPR	8	8	2 or 3 FCLK
007F C0C1h	FLASH	Protection Unlock Status Register	FPSR	8	8	2 or 3 FCLK
007F C0C2h	FLASH	Flash Read Buffer Register L	FRBL	16	16	2 or 3 FCLK
007F C0C4h	FLASH	Flash Read Buffer Register H	FRBH	16	16	2 or 3 FCLK
007F FF80h	FLASH	Flash P/E Mode Control Register	FPMCR	8	8	2 or 3 FCLK
007F FF81h	FLASH	Flash Area Select Register	FASR	8	8	2 or 3 FCLK
007F FF82h	FLASH	Flash Processing Start Address Register L	FSARL	16	16	2 or 3 FCLK
007F FF84h	FLASH	Flash Processing Start Address Register H	FSARH	8	8	2 or 3 FCLK
007F FF85h	FLASH	Flash Control Register	FCR	8	8	2 or 3 FCLK
007F FF86h	FLASH	Flash Processing End Address Register L	FEARL	16	16	2 or 3 FCLK
007F FF88h	FLASH	Flash Processing End Address Register H	FEARH	8	8	2 or 3 FCLK
007F FF89h	FLASH	Flash Reset Register	FRESETR	8	8	2 or 3 FCLK
007F FF8Ah	FLASH	Flash Status Register 0	FSTATR0	8	8	2 or 3 FCLK
007F FF8Bh	FLASH	Flash Status Register 1	FSTATR1	8	8	2 or 3 FCLK
007F FF8Ch	FLASH	Flash Write Buffer Register L	FWBL	16	16	2 or 3 FCLK
007F FF8Eh	FLASH	Flash Write Buffer Register H	FWBH	16	16	2 or 3 FCLK
007F FFB2h	FLASH	Flash P/E Mode Entry Register	FENTRYR	16	16	2 or 3 FCLK
007F FFBEh	CTSU	CTSU Reference Current Calibration Register	CTSUTRMR	8	8	2 or 3 FCLK

[Products with 128 Kbytes of flash memory or less (except for 100-pin packages)]

Table 5.7 DC Characteristics (5)

Conditions: 1.8 V ≤ VCC = AVCC0 < 2.0 V, 2.0 V ≤ VCC ≤ 5.5 V, 2.0 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, Ta = –40 to +105°C

Item					Symbol	Typ.	Max.	Unit	Test Conditions
Supply current*1	High-speed operating mode	Normal operating mode	No peripheral operation*2	ICLK = 32MHz	I_{CC}	3.1	—	mA	
				ICLK = 16MHz		2.1	—		
				ICLK = 8MHz		1.6	—		
			All peripheral operation: Normal*3	ICLK = 32MHz		10.0	—		
				ICLK = 16MHz		5.7	—		
				ICLK = 8MHz		3.5	—		
			All peripheral operation: Max.*3	ICLK = 32MHz		—	17.5		
		Sleep mode	No peripheral operation*2	ICLK = 32MHz		1.6	—		
				ICLK = 16MHz		1.2	—		
				ICLK = 8MHz		1.1	—		
			All peripheral operation: Normal*3	ICLK = 32MHz		5.3	—		
				ICLK = 16MHz		3.2	—		
				ICLK = 8MHz		2.0	—		
		Deep sleep mode	No peripheral operation*2	ICLK = 32MHz		1.0	—		
				ICLK = 16MHz		0.9	—		
				ICLK = 8MHz		0.8	—		
			All peripheral operation: Normal*3	ICLK = 32MHz		4.2	—		
				ICLK = 16MHz		2.5	—		
				ICLK = 8MHz		1.7	—		
		Increase during flash rewrite*5				2.5	—		
	Middle-speed operating modes	Normal operating mode	No peripheral operation*6	ICLK = 12MHz	I_{CC}	1.9	—	mA	
				ICLK = 8MHz		1.2	—		
				ICLK = 4MHz		0.6	—		
				ICLK = 1MHz		0.3	—		
			All peripheral operation: Normal*7	ICLK = 12MHz		4.6	—		
				ICLK = 8MHz		3.2	—		
				ICLK = 4MHz		2.0	—		
				ICLK = 1MHz		0.9	—		
			All peripheral operation: Max.*7	ICLK = 12MHz		—	8.2		
		Sleep mode	No peripheral operation*6	ICLK = 12MHz	I_{CC}	1.2	—	mA	
				ICLK = 8MHz		0.8	—		
				ICLK = 4MHz		0.3	—		
				ICLK = 1MHz		0.2	—		
			All peripheral operation: Normal*7	ICLK = 12MHz		2.7	—		
				ICLK = 8MHz		1.9	—		
				ICLK = 4MHz		1.2	—		
				ICLK = 1MHz		0.7	—		



Note 1. All peripheral operation is normal. This does not include BGO operation. Average value of the tested middle samples during product evaluation.
Note 2. All peripheral operation is maximum. This does not include BGO operation. Average value of the tested upper-limit samples during product evaluation.

Figure 5.1 Voltage Dependency in High-Speed Operating Mode (Reference Data)

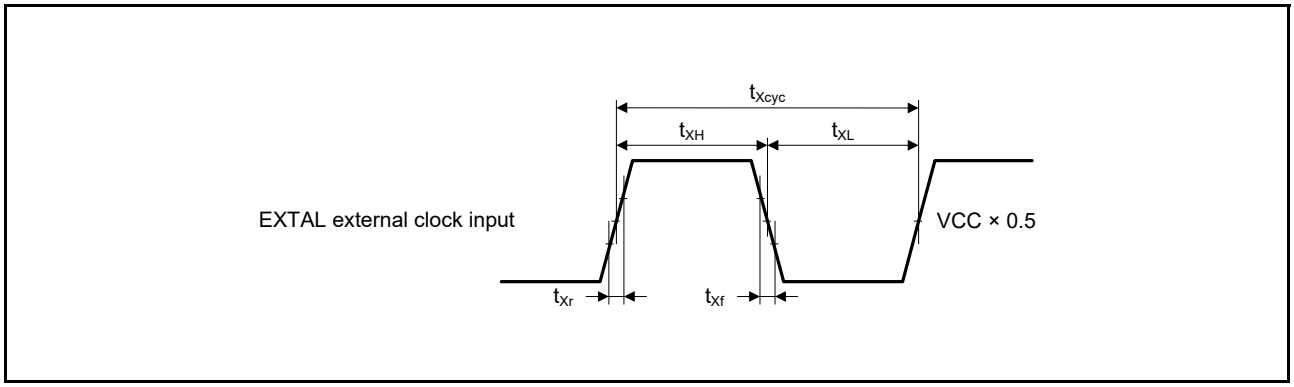


Figure 5.26 EXTAL External Clock Input Timing

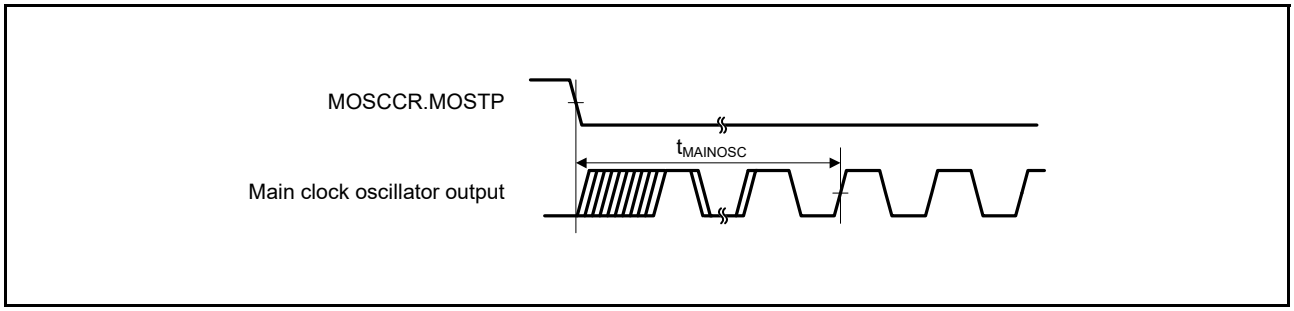


Figure 5.27 Main Clock Oscillation Start Timing

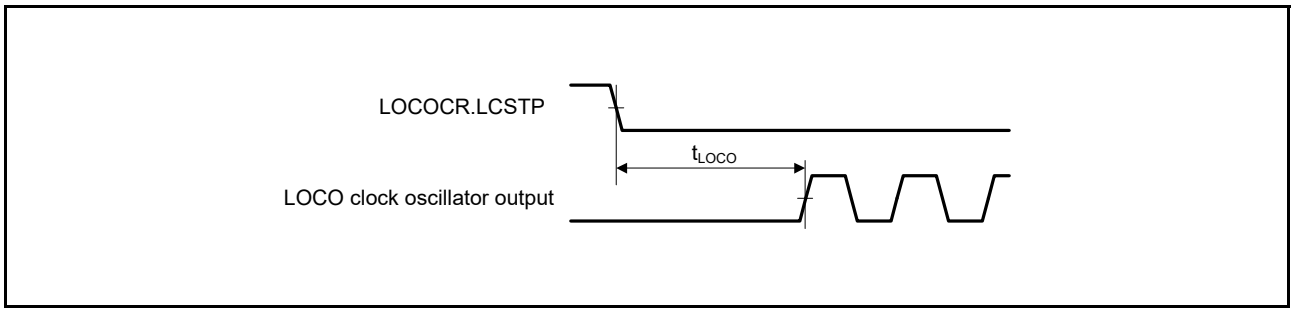


Figure 5.28 LOCO Clock Oscillation Start Timing

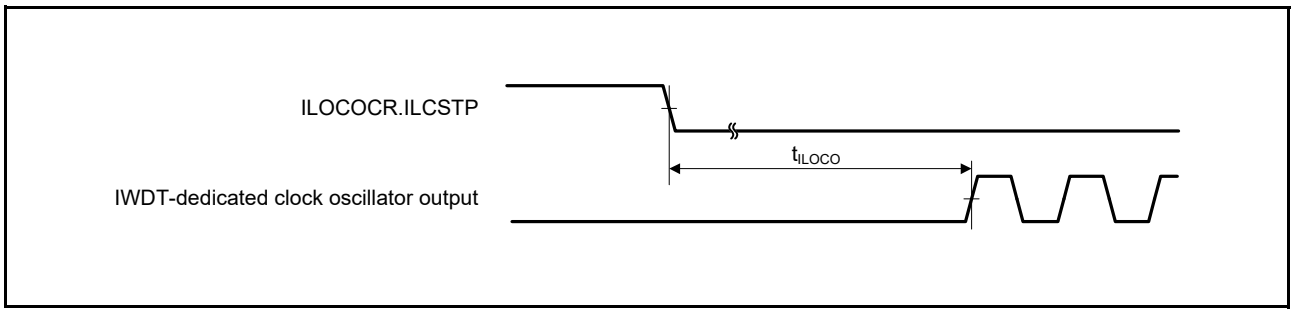


Figure 5.29 IWDT-Dedicated Clock Oscillation Start Timing

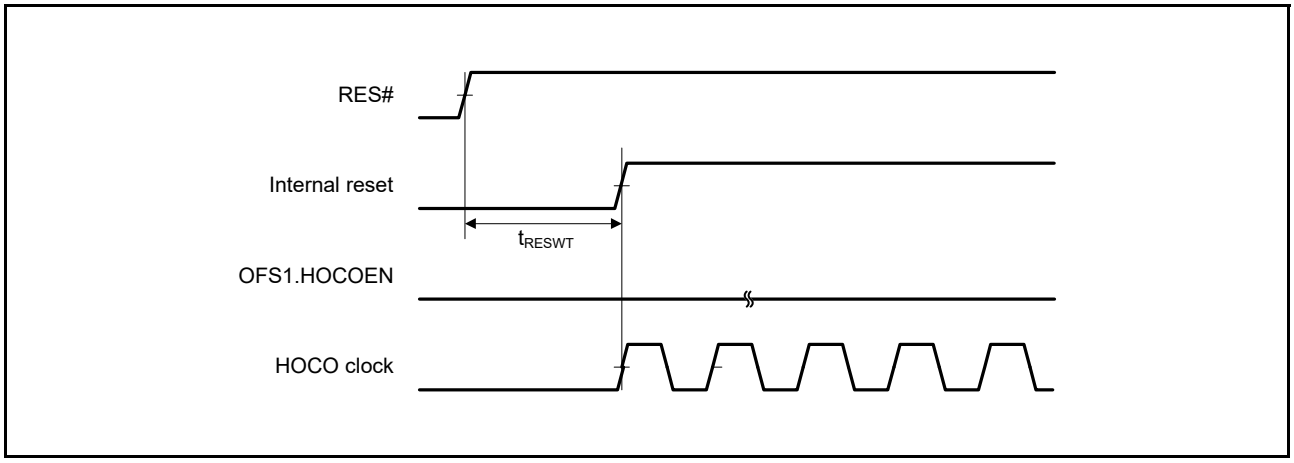


Figure 5.30 HOCO Clock Oscillation Start Timing (After Reset is Canceled by Setting OFS1.HOCOEN Bit to 0)

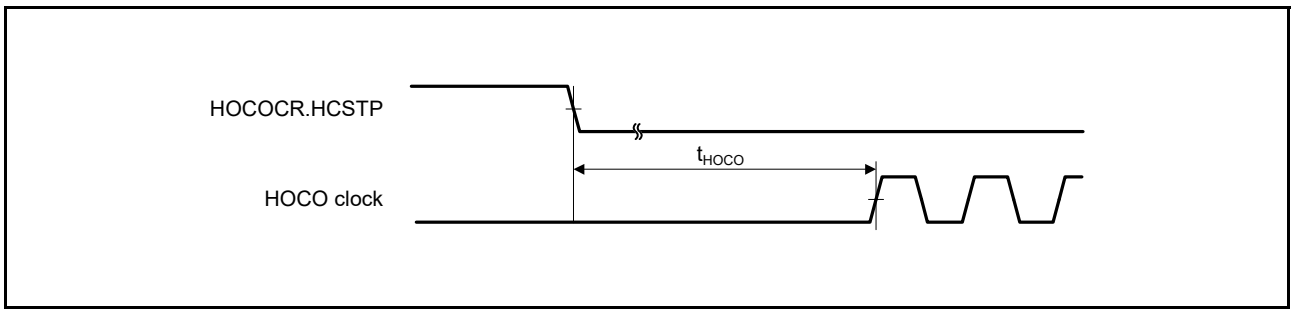


Figure 5.31 HOCO Clock Oscillation Start Timing (Oscillation is Started by Setting HOCOCR.HCSTP Bit)

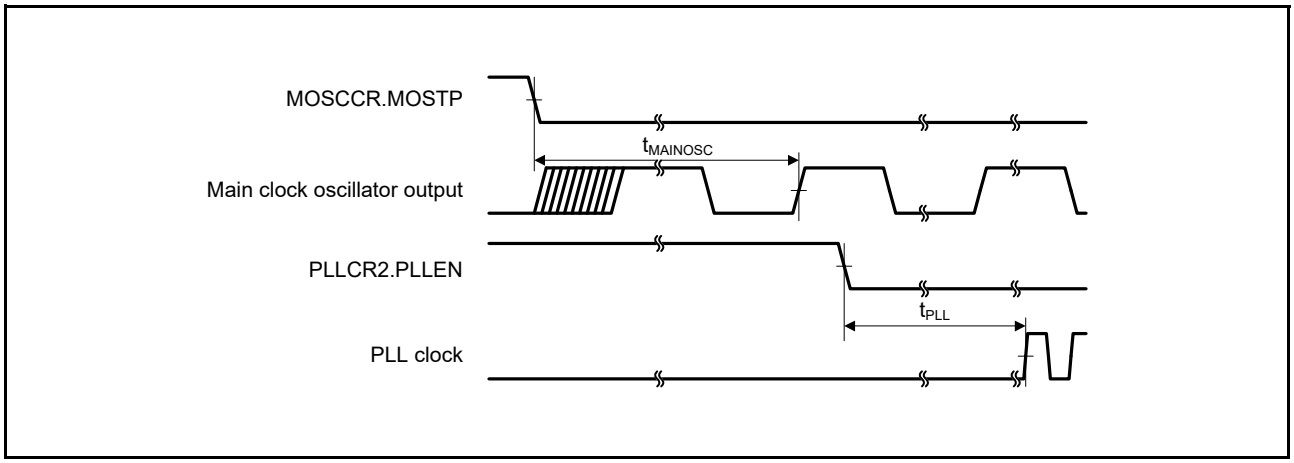


Figure 5.32 PLL Clock Oscillation Start Timing (PLL is Operated after Main Clock Oscillation Has Settled)

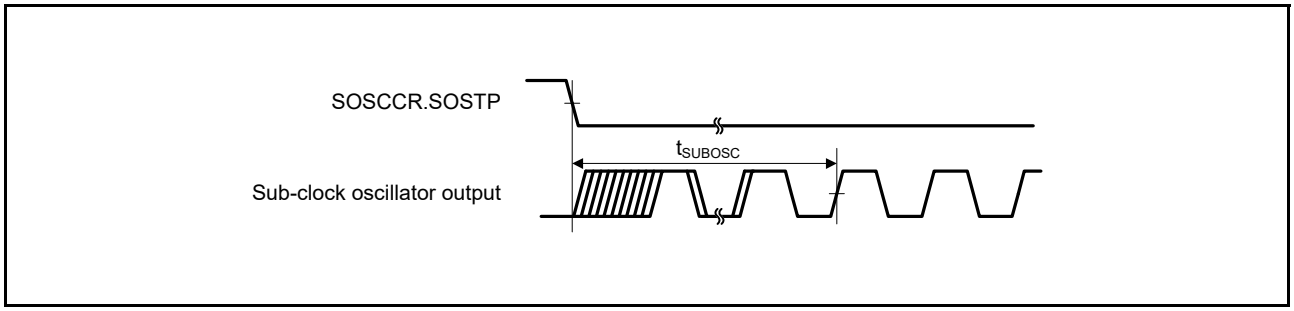


Figure 5.33 Sub-Clock Oscillation Start Timing

5.3.2 Reset Timing

Table 5.26 Reset Timing

Conditions: 1.8 V ≤ VCC = AVCC0 < 2.0 V, 2.0 V ≤ VCC ≤ 5.5 V, 2.0 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, Ta = –40 to +105°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
RES# pulse width	At power-on	t_{RESWP}	3	—	—	ms	Figure 5.34
	Other than above	t_{RESW}	30	—	—	μs	Figure 5.35
Wait time after RES# cancellation (at power-on)	At normal startup*1	t_{RESWT}	—	8.5	—	ms	Figure 5.34
	During fast startup time*2	t_{RESWT}	—	560	—	μs	
Wait time after RES# cancellation (during powered-on state)		t_{RESWT}	—	120	—	μs	Figure 5.35
Independent watchdog timer reset period		t_{RESWIW}	—	1	—	IWDT clock cycle	Figure 5.36
Software reset period		t_{RESWSW}	—	1	—	ICLK cycle	
Wait time after independent watchdog timer reset cancellation*3		t_{RESWT2}	—	300	—	μs	
Wait time after software reset cancellation		t_{RESWT2}	—	170	—	μs	

Note 1. When OFS1.(LVDAS, FASTSTUP) = 11b.
Note 2. When OFS1.(LVDAS, FASTSTUP) = a value other than 11b.
Note 3. When IWDTCR.CKS[3:0] = 0000b.

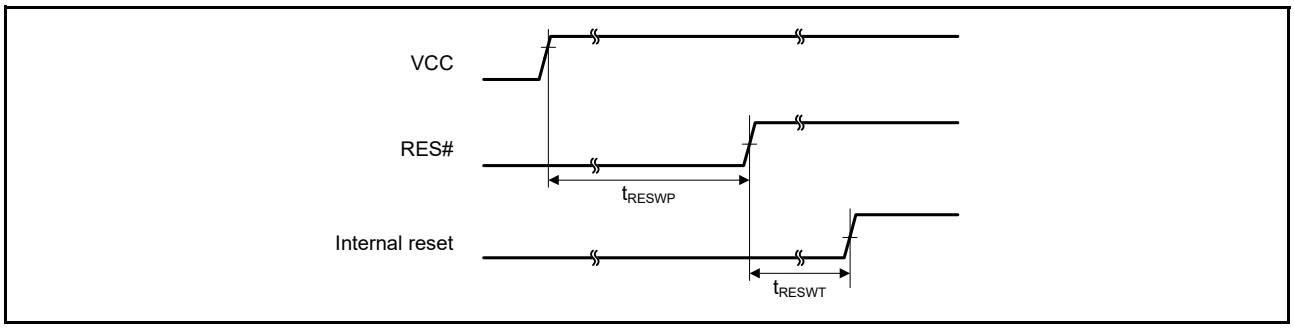


Figure 5.34 Reset Input Timing at Power-On

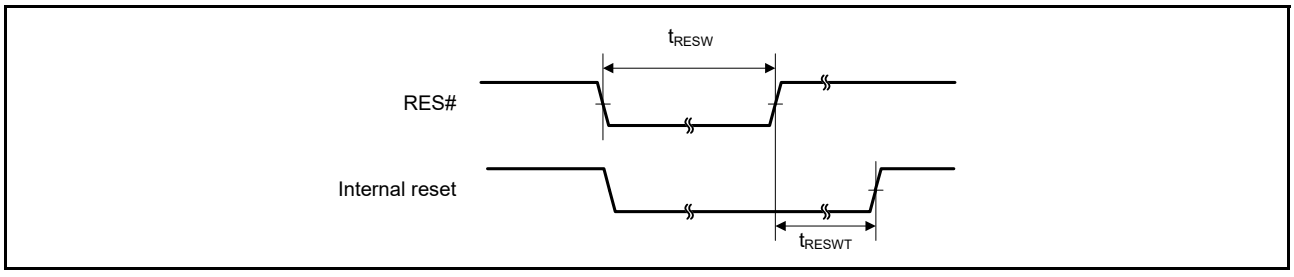


Figure 5.35 Reset Input Timing (1)

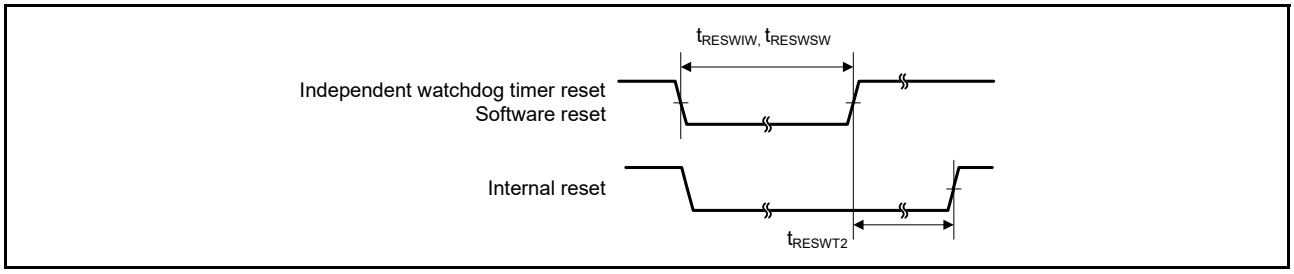


Figure 5.36 Reset Input Timing (2)

5.3.5 Timing of On-Chip Peripheral Modules

Table 5.33 Timing of On-Chip Peripheral Modules (1)

Conditions: 1.8 V ≤ VCC = AVCC0 < 2.0 V, 2.0 V ≤ VCC ≤ 5.5 V, 2.0 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, Ta = –40 to +105°C

Item				Symbol	Min.	Max.	Unit *1	Test Conditions
I/O ports	Input data pulse width			t_{PRW}	1.5	—	t_{Pcyc}	Figure 5.41
MTU2	Input capture input pulse width		Single-edge setting	t_{TICW}	1.5	—	t_{Pcyc}	Figure 5.42
			Both-edge setting		2.5	—		
	Input capture input rise/fall time			t_{TICr}, t_{TICf}	—	0.1	μs/V	
	Timer clock pulse width		Single-edge setting	t_{TCKWH}, t_{TCKWL}	1.5	—	t_{Pcyc}	Figure 5.43
			Both-edge setting		2.5	—		
			Phase counting mode		2.5	—		
	Timer clock rise/fall time			t_{TCKr}, t_{TCKf}	—	0.1	μs/V	
POE2	POE# input pulse width			t_{POEW}	1.5	—	t_{Pcyc}	Figure 5.44
	POE# input rise/fall time			t_{POEr}, t_{POEf}	—	0.1	μs/V	
TMR	Timer clock pulse width		Single-edge setting	t_{TMCWH}, t_{TMCWL}	1.5	—	t_{Pcyc}	Figure 5.45
			Both-edge setting		2.5	—		
	Timer clock rise/fall time			t_{TMCr}, t_{TMCf}	—	0.1	μs/V	
SCI	Input clock cycle time		Asynchronous	t_{Scyc}	4	—	t_{Pcyc}	Figure 5.46
			Clock synchronous		6	—		
	Input clock pulse width			t_{SCKW}	0.4	0.6	t_{Scyc}	
	Input clock rise time			t_{SCKr}	—	20	ns	
	Input clock fall time			t_{SCKf}	—	20	ns	
	Output clock cycle time		Asynchronous	t_{Scyc}	16	—	t_{Pcyc}	Figure 5.47
			Clock synchronous		4	—		
	Output clock pulse width			t_{SCKW}	0.4	0.6	t_{Scyc}	
	Output clock rise time			t_{SCKr}	—	20	ns	
	Output clock fall time			t_{SCKf}	—	20	ns	
	Transmit data delay time (master)	Clock synchronous		t_{TXD}	—	40	ns	
	Transmit data delay time (slave)	Clock synchronous	2.7 V or above		—	65	ns	
			1.8 V or above		—	100	ns	
	Receive data setup time (master)	Clock synchronous	2.7 V or above	t_{RXS}	65	—	ns	
			1.8 V or above		90	—	ns	
	Receive data setup time (slave)	Clock synchronous			40	—	ns	
	Receive data hold time	Clock synchronous		t_{RXH}	40	—	ns	
A/D converter	Trigger input pulse width			t_{TRGW}	1.5	—	t_{Pcyc}	Figure 5.48
CAC	CACREF input pulse width		$t_{Pcyc} \le t_{cac}$ *2	t_{CACREF}	4.5 t_{cac} + 3 t_{Pcyc}	—	ns	
			$t_{Pcyc} > t_{cac}$ *2		5 t_{cac} + 6.5 t_{Pcyc}			
	CACREF input rise/fall time			$t_{CACREFr}$, $t_{CACREFf}$	—	0.1	μs/V	

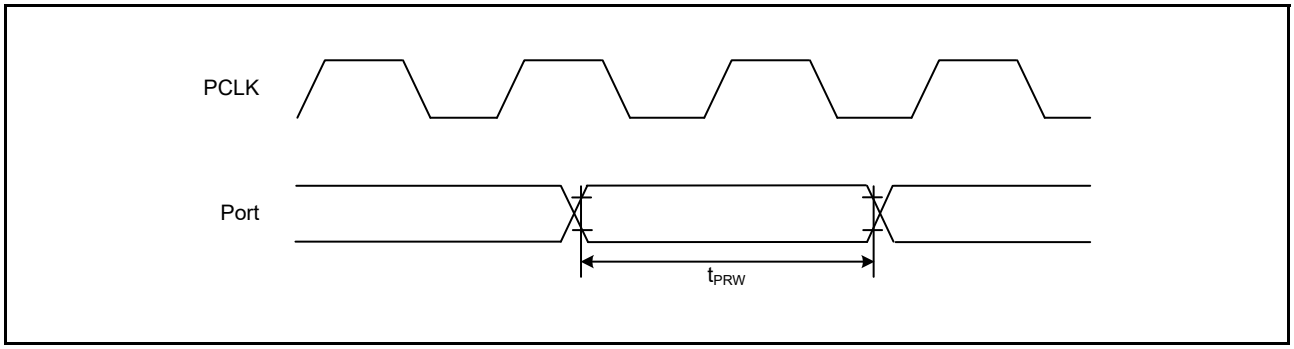


Figure 5.41 I/O Port Input Timing

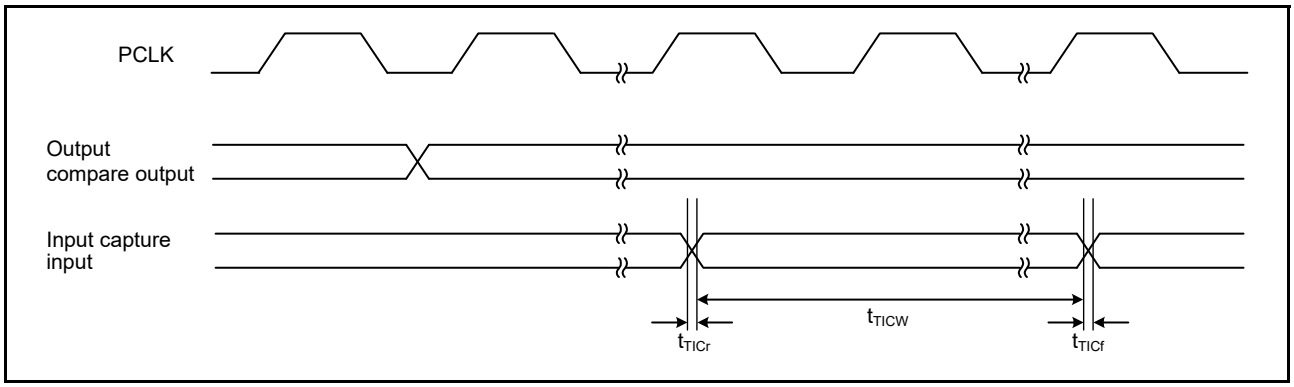


Figure 5.42 MTU2 Input/Output Timing

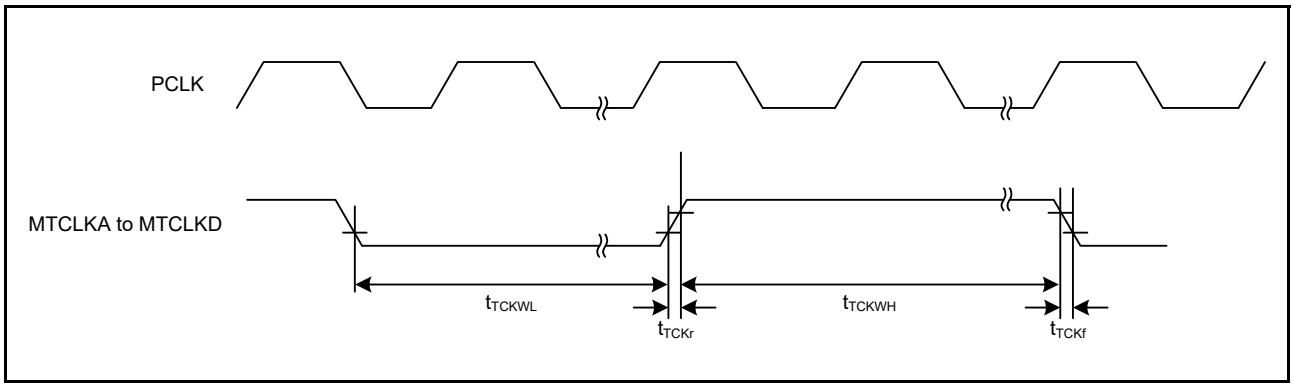


Figure 5.43 MTU2 Clock Input Timing

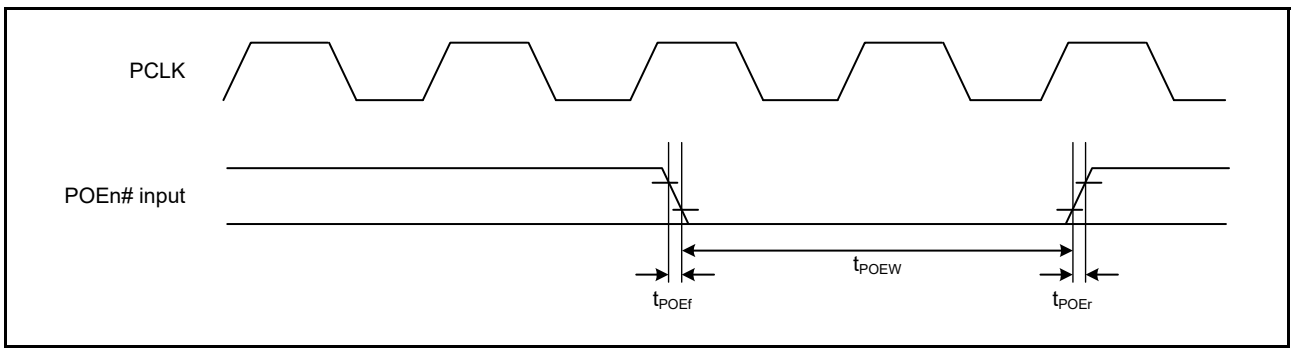


Figure 5.44 POE# Input Timing

Table 5.39 A/D Conversion Characteristics (1)

Conditions: 2.7 V ≤ VCC ≤ 5.5 V, 2.7 V ≤ AVCC0 ≤ 5.5 V, 2.7 V ≤ VREFH0 ≤ AVCC0, Reference voltage = VREFH0, VSS = AVSS0 = VREFL0 = 0 V, T_a = –40 to +105°C

Item		Min.	Typ.	Max.	Unit	Test Conditions
Frequency		1	—	32	MHz	
Resolution		—	—	12	Bit	
Conversion time*1 (Operation at PCLKD = 32 MHz)	Permissible signal source impedance (Max.) = 0.3 kΩ	1.41	—	—	µs	High-precision channel ADCSR.ADHSC bit = 0 ADSSTRn = 0Dh
		2.25	—	—	µs	Normal-precision channel ADCSR.ADHSC bit = 0 ADSSTRn = 28h
Analog input capacitance	Cs	—	—	15	pF	Pin capacitance included
Analog input resistance	Rs	—	—	2.5	kΩ	
Analog input effective range		0	—	VREFH0	V	
Offset error		—	±0.5	±4.5	LSB	High-precision channel
				±6.0	LSB	Other than above
Full-scale error		—	±0.75	±4.5	LSB	High-precision channel
				±6.0	LSB	Other than above
Quantization error		—	± 0.5	—	LSB	
Absolute accuracy		—	±1.25	±5.0	LSB	High-precision channel
				±8.0	LSB	Other than above
DNL differential nonlinearity error		—	±1.0	—	LSB	
INL integral nonlinearity error		—	±1.0	±3.0	LSB	

Note: The characteristics apply when no pin functions other than A/D converter input are used. Absolute accuracy includes quantization errors. Offset error, full-scale error, DNL differential nonlinearity error, and INL integral nonlinearity error do not include quantization errors.

Note 1. The conversion time is the sum of the sampling time and the comparison time. As the test conditions, the number of sampling states is indicated.

5.5 D/A Conversion Characteristics

Table 5.45 D/A Conversion Characteristics (1)

Conditions: 1.8 V ≤ VCC = AVCC0 < 2.0 V, 2.0 V ≤ VCC ≤ 5.5 V, 2.0 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Resolution		—	—	—	8	Bit	
Conversion time	VCC=2.7 to 5.5 V	t_{DCONV}	—	—	3.0	µs	35-pF capacitive load
	VCC=1.8 to 2.7 V		—	—	6.0		
Absolute accuracy	VCC=2.4 to 5.5 V	—	—	—	±3.0	LSB	2-MΩ resistive load
	VCC=1.8 to 2.4 V	—	—	—	±3.5		
	VCC=2.4 to 5.5 V	—	—	—	±2.0	LSB	4-MΩ resistive load
	VCC=1.8 to 2.4 V	—	—	—	±2.5		
RO output resistance		—	—	6.4	—	kΩ	

5.6 Temperature Sensor Characteristics

Table 5.46 Temperature Sensor Characteristics

Conditions: 2.0 V ≤ VCC ≤ 5.5 V, 2.0 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Relative accuracy	—	—	±1.5	—	°C	2.4 V or above
		—	±2.0	—		Below 2.4 V
Temperature slope	—	—	–3.65	—	mV/°C	
Output voltage (25°C)	—	—	1.05	—	V	VCC = 3.3 V
Temperature sensor start time	t_{START}	—	—	5	µs	
Sampling time	—	5	—	—	µs	

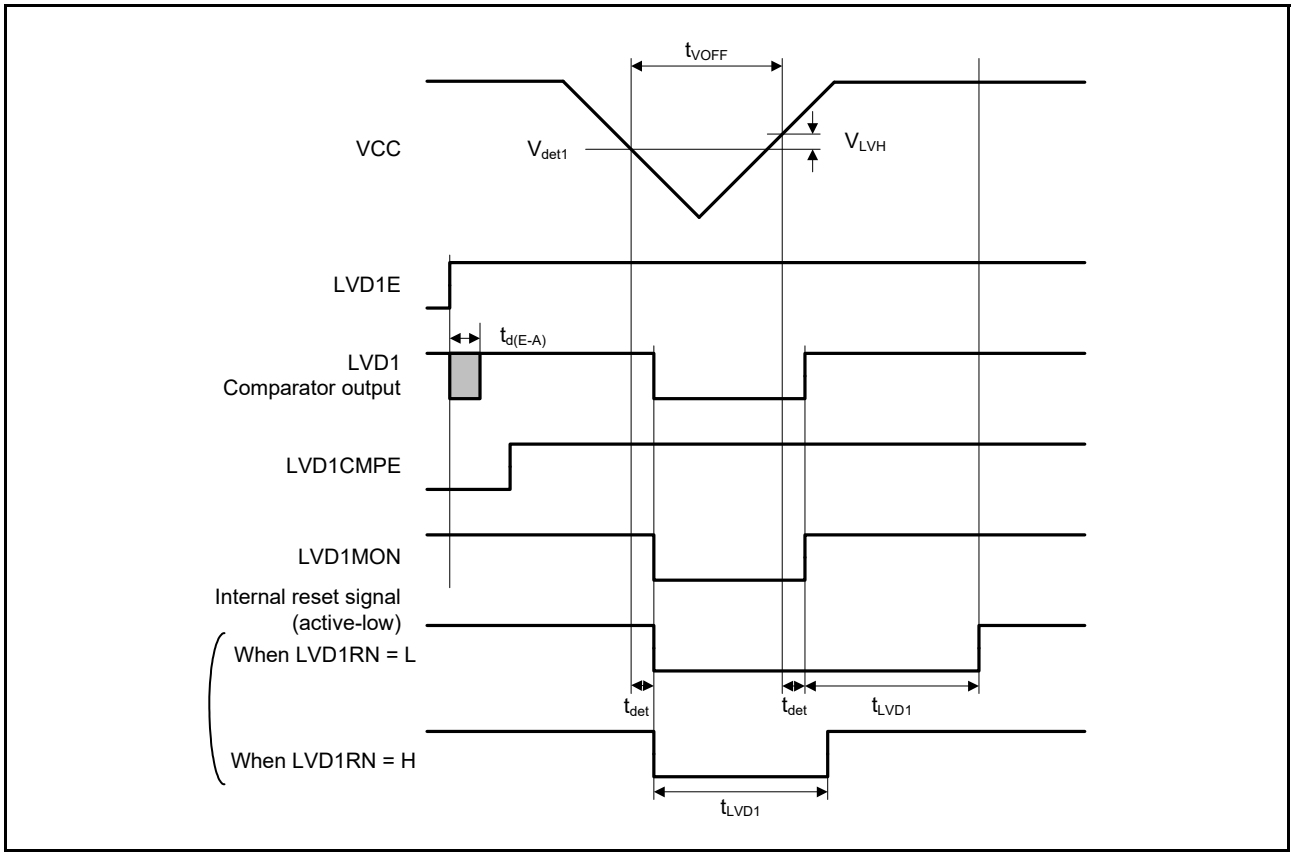


Figure 5.64 Voltage Detection Circuit Timing (V_{det1})

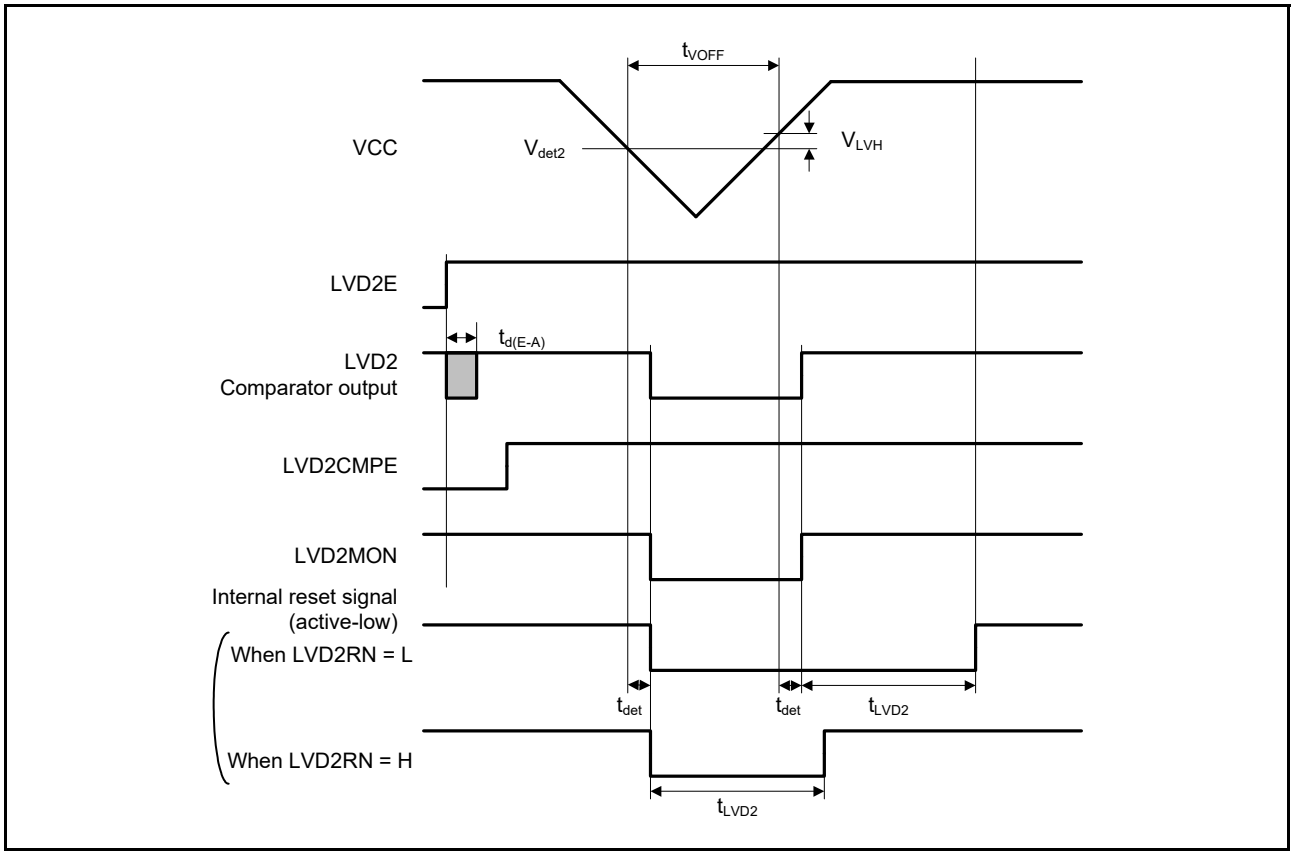


Figure 5.65 Voltage Detection Circuit Timing (V_{det2})

5.10 Oscillation Stop Detection Timing

Table 5.51 Oscillation Stop Detection Timing

Conditions: 1.8 V ≤ VCC = AVCC0 < 2.0 V, 2.0 V ≤ VCC ≤ 5.5 V, 2.0 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Detection time	t_{dr}	—	—	1	ms	Figure 5.66

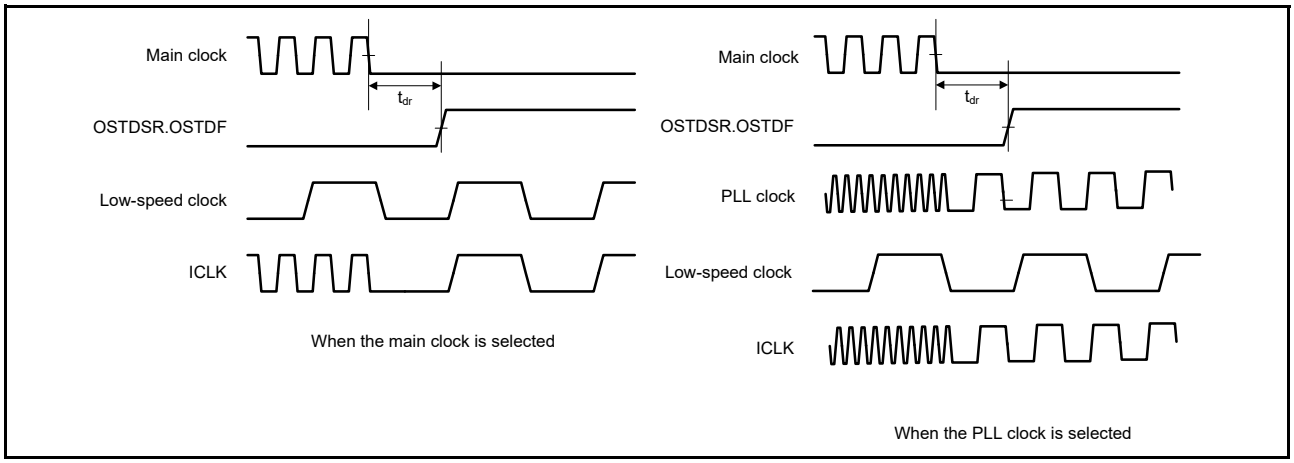
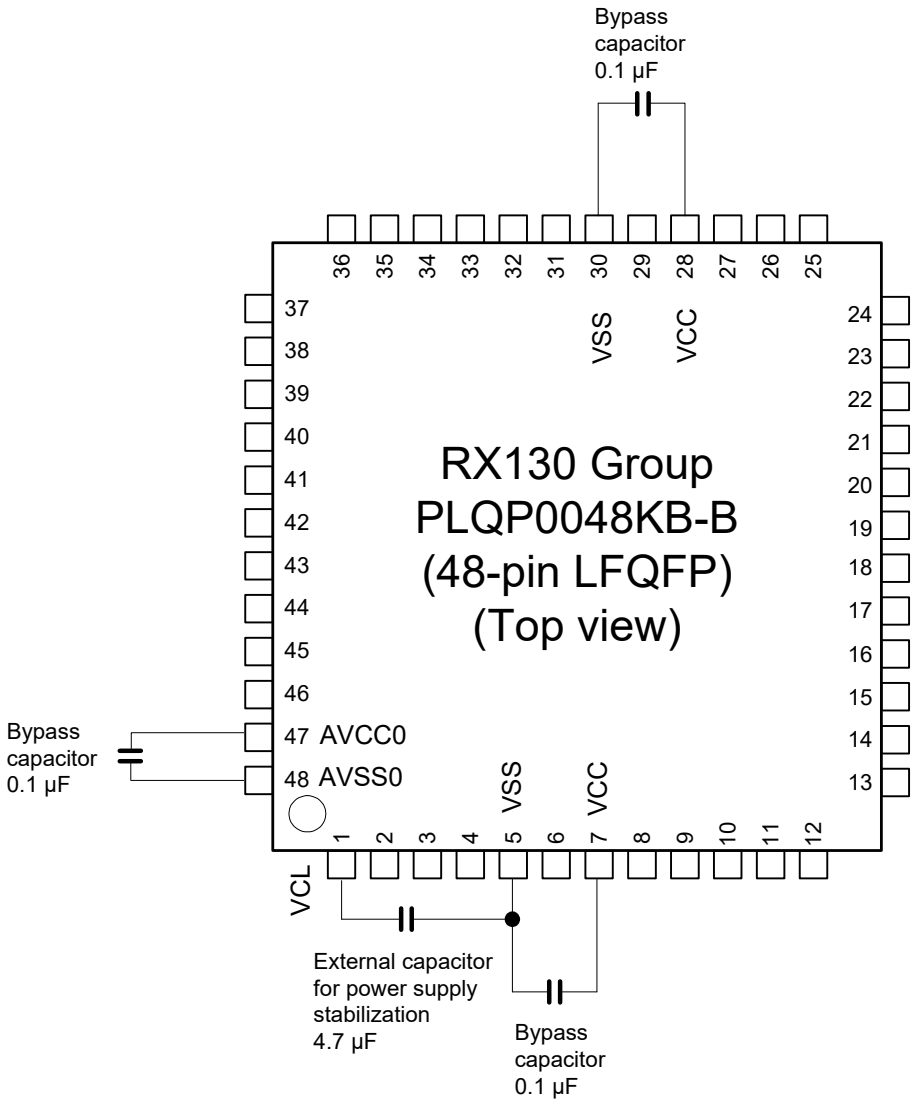


Figure 5.66 Oscillation Stop Detection Timing



Note. Do not apply the power supply voltage to the VCL pin.
Use a 4.7-µF multilayer ceramic for the VCL pin and place it close to the pin.
A recommended value is shown for the capacitance of the bypass capacitors.

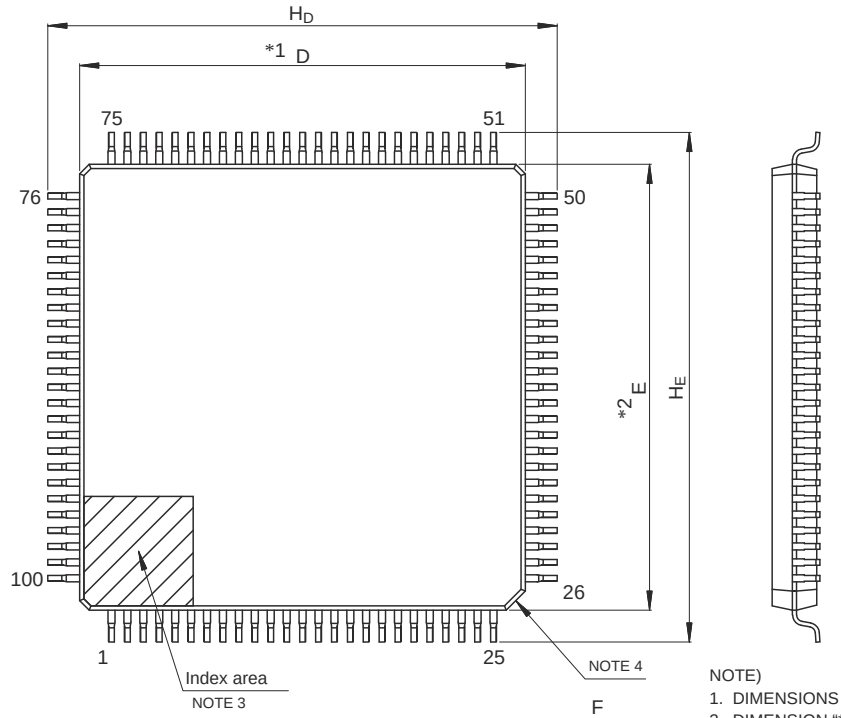
Figure 5.70 Connecting Capacitors (48 Pins)

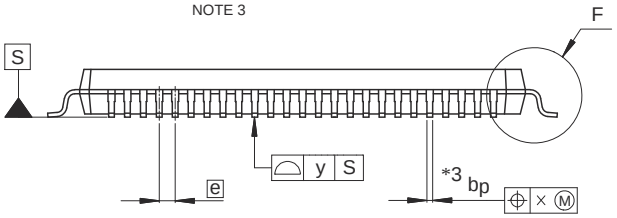
Appendix 1. Package Dimensions

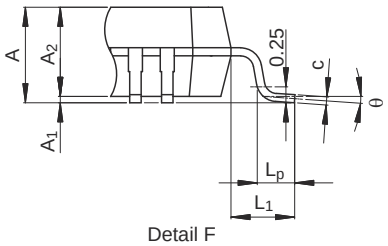
Information on the latest version of the package dimensions or mountings has been displayed in “Packages” on Renesas Electronics Corporation website.

JEITA Package Code	RENESAS Code	Previous Code	MASS (Typ) [g]
P-LFQFP100-14x14-0.50	PLQP0100KB-B	—	0.6

Unit: mm







NOTE)
1. DIMENSIONS “*1” AND “*2” DO NOT INCLUDE MOLD FLASH.
2. DIMENSION “*3” DOES NOT INCLUDE TRIM OFFSET.
3. PIN 1 VISUAL INDEX FEATURE MAY VARY, BUT MUST BE LOCATED WITHIN THE HATCHED AREA.
4. CHAMFERS AT CORNERS ARE OPTIONAL, SIZE MAY VARY.

Reference Symbol	Dimensions in millimeters		
	Min	Nom	Max
D	13.9	14.0	14.1
E	13.9	14.0	14.1
A_2	—	1.4	—
H_D	15.8	16.0	16.2
H_E	15.8	16.0	16.2
A	—	—	1.7
A_1	0.05	—	0.15
b_p	0.15	0.20	0.27
c	0.09	—	0.20
θ	0°	3.5°	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
L_p	0.45	0.6	0.75
L_1	—	1.0	—

Figure A 100-Pin LFQFP (PLQP0100KB-B)

REVISION HISTORY	RX130 Group Datasheet

Classifications

- Items with Technical Update document number: Changes according to the corresponding issued Technical Update
- Items without Technical Update document number: Minor changes that do not require Technical Update to be issued

Rev.	Date	Description		Classification
		Page	Summary	
1.00	Oct 30, 2015	—	First edition, issued	
2.00	Sep 01, 2017	All	Products with at least 256 Kbytes of code flash memory and 100-pin packages added	
		4. I/O Registers		
		42	Table 4.1 List of I/O Registers (Address Order), changed	TN-RX*-A179A/E
		5. Electrical Characteristics		
		49	Table 5.2 Recommended Operating Voltage Conditions Note 3, added	
		57 to 61	The characteristics of products with at least 256 Kbytes of flash memory or 100-pin packages added	
		64, 65	The characteristics of products with at least 256 Kbytes of flash memory or 100-pin packages added	
		90	Table 5.34 Timing of On-Chip Peripheral Modules (2), changed	TN-RX*-A179A/E
		91	Table 5.35 Timing of On-Chip Peripheral Modules (3), changed	
		93	Table 5.38 Timing of On-Chip Peripheral Modules (6), added	
		111	Table 5.48 CTSU Characteristics, item for products with at least 256 Kbytes of flash memory or 100-pin packages added	
		113	Table 5.50 Power-On Reset Circuit and Voltage Detection Circuit Characteristics (2), item with Vdet0_0 to Vdet0_3 selected added	
		117	Table 5.53 ROM (Flash Memory for Code Storage) Characteristics (2) High-Speed Operating Mode, erasure time (128-Kbyte) deleted and erasure time (256-Kbyte) added	
		118	Table 5.54 ROM (Flash Memory for Code Storage) Characteristics (3) Middle-Speed Operating Mode, erasure time (128-Kbyte) deleted and erasure time (256-Kbyte) added	