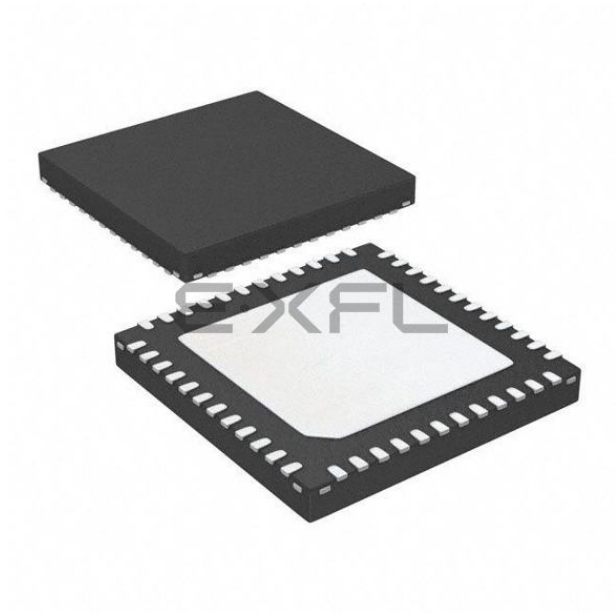
Renesas Electronics America Inc - R5F51303ADNE#U0 Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	RX
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	I²C, LINbus, SCI, SPI
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	38
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	8K x 8
RAM Size	10K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 10x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-WFQFN Exposed Pad
Supplier Device Package	48-HWQFN (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f51303adne-u0

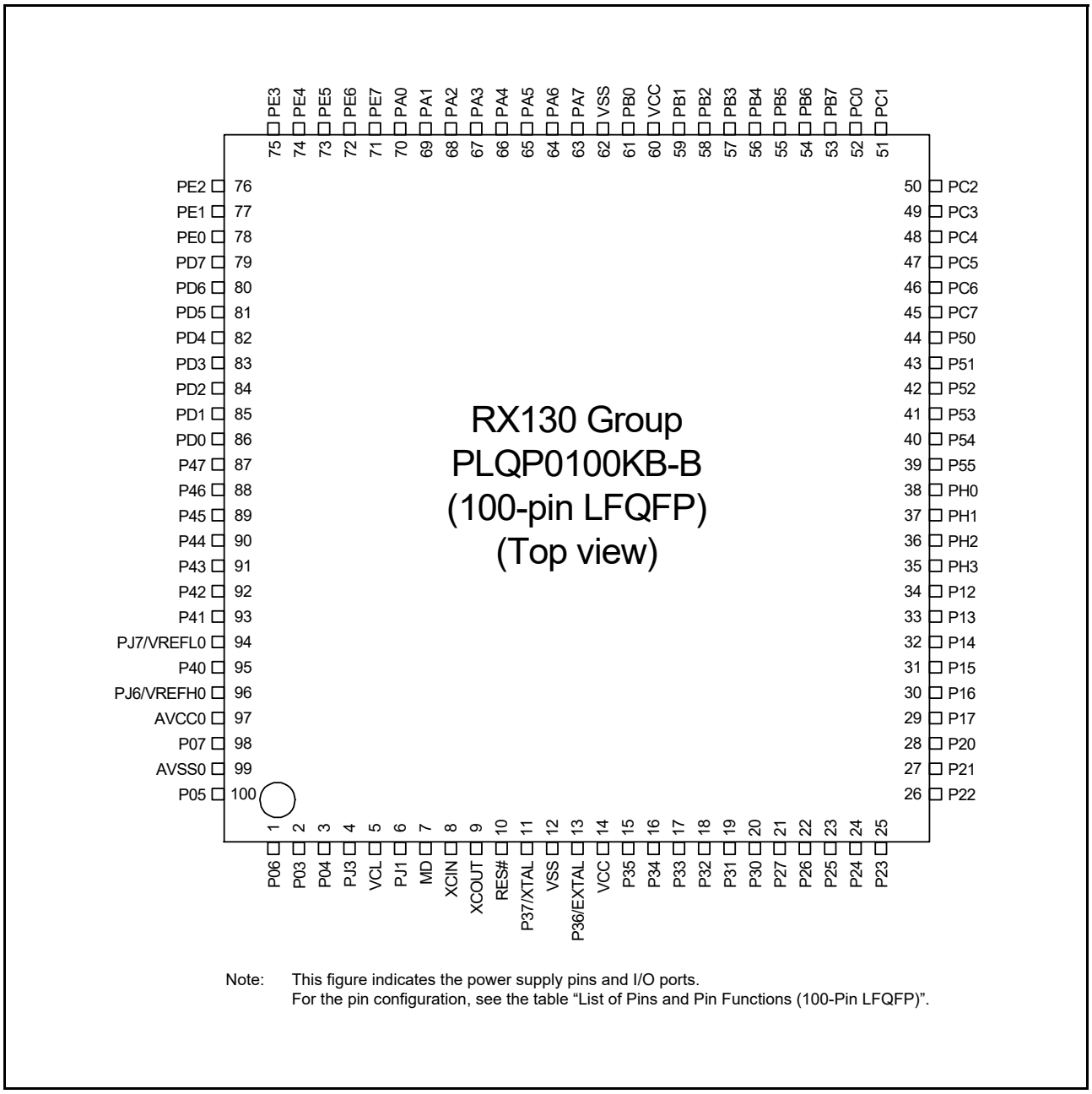
Table 1.1 Outline of Specifications (3/3)

Classification	Module/Function	Description
Communication functions	Serial peripheral interface (RSPIa)	• 1 channel • Transfer facility Using the MOSI (master out, slave in), MISO (master in, slave out), SSL (slave select), and RSPCK (RSPI clock) signals enables serial transfer through SPI operation (four lines) or clock-synchronous operation (three lines) • Capable of handling serial transfer as a master or slave • Data formats • Choice of LSB-first or MSB-first transfer The number of bits in each transfer can be changed to 8, 9, 10, 11, 12, 13, 14, 15, 16, 20, 24, or 32 bits. 128-bit buffers for transmission and reception Up to four frames can be transmitted or received in a single transfer operation (with each frame having up to 32 bits) • Double buffers for both transmission and reception
	Remote control signal receiver (REMC)	• 2 channels • Four pattern matching (header, data 0, data 1, and special data detection) • 8-byte receive buffer per unit • The operating clock can be selected from among the PCLK, sub-clock, HOCO, IWDTCLK, and TMR.
12-bit A/D converter (S12ADE)		• 12 bits (24 channels × 1 unit) • 12-bit resolution • Minimum conversion time: 1.4 µs per channel when the ADCLK is operating at 32 MHz • Operating modes Scan mode (single scan mode, continuous scan mode, and group scan mode) Group A priority control (only for group scan mode) • Sampling variable Sampling time can be set up for each channel. • Self-diagnostic function • Double trigger mode (A/D conversion data duplicated) • Detection of analog input disconnection • Conversion results compare features • A/D conversion start conditions A software trigger, a trigger from a timer (MTU), an external trigger signal, or ELC • Event linking by the ELC
Temperature sensor (TEMPSA)		• 1 channel • The voltage output from the temperature sensor is converted into a digital value by the 12-bit A/D converter.
D/A converter (DA)		• 2 channels • 8-bit resolution • Output voltage: 0V to AVCC0
CRC calculator (CRC)		• CRC code generation for arbitrary amounts of data in 8-bit units • Select any of three generating polynomials: $X^8 + X^2 + X + 1$, $X^{16} + X^{15} + X^2 + 1$, or $X^{16} + X^{12} + X^5 + 1$ • Generation of CRC codes for use with LSB-first or MSB-first communications is selectable.
Comparator B (CMPBa)		• 2 channels • Function to compare the reference voltage and the analog input voltage • Window comparator operation or standard comparator operation is selectable
Capacitive touch sensing unit (CTSUa)		Detection pin: 36 channels
Data operation circuit (DOC)		Comparison, addition, and subtraction of 16-bit data
Unique ID		32-byte ID code for the MCU
Power supply voltages/Operating frequencies		VCC = 1.8 to 2.4 V: 8 MHz, VCC = 2.4 to 2.7 V: 16 MHz, VCC = 2.7 to 5.5 V: 32 MHz
Operating temperature range		D version: –40 to +85°C, G version: –40 to +105°C
Packages		100-pin LFQFP (PLQP0100KB-B) 14 × 14 mm, 0.5 mm pitch 80-pin LFQFP (PLQP0080KB-B) 12 × 12 mm, 0.5 mm pitch 64-pin LFQFP (PLQP0064KB-C) 10 × 10 mm, 0.5 mm pitch 64-pin LQFP (PLQP0064GA-A) 14 × 14 mm, 0.8 mm pitch 48-pin LFQFP (PLQP0048KB-B) 7 × 7 mm, 0.5 mm pitch 48-pin HWQFN (PWQN0048KB-A) 7 × 7 mm, 0.5 mm pitch
On-chip debugging system		E1 emulator (FINE interface)

Note 1. When the realtime clock is not to be used, refer to section 24.5.7, Initialization Procedure When the Realtime Clock is Not to be Used.

1.5 Pin Assignments

Figure 1.3 to Figure 1.7 show the pin assignments. Table 1.5 to Table 1.8 show the lists of pins and pin functions.



Note: This figure indicates the power supply pins and I/O ports.
For the pin configuration, see the table “List of Pins and Pin Functions (100-Pin LFQFP)”.

Figure 1.3 Pin Assignments of the 100-Pin LFQFP

Table 1.6 List of Pins and Pin Functions (80-Pin LFQFP) (1/2)

Pin No.	Power Supply, Clock, System Control	I/O Port	Timers (MTU, TMR, POE)	Communications (SCIg, SCIh, RSPI, RIIC)	Touch sensing	Others
1		P06*1				
2		P03*1				DA0
3		P04*1				
4	VCL					
5		PJ1	MTIOC3A			
6	MD					FINED
7	XCIN					
8	XCOUT					
9	RES#					
10	XTAL	P37				
11	VSS					
12	EXTAL	P36				
13	VCC					
14		P35				NMI
15		P34	MTIOC0A/TMCI3/POE2#	SCK6		IRQ4
16		P32	MTIOC0C/TMO3	TXD6/SMOSI6/SSDA6	TS0	IRQ2/RTCOUT
17		P31	MTIOC4D/TMCI2	CTS1#/RTS1#/SS1#	TS1	IRQ1
18		P30	MTIOC4B/TMRI3/POE8#	RXD1/SMISO1/SSCL1	TS2	IRQ0
19		P27	MTIOC2B/TMCI3	SCK1	TS3	
20		P26	MTIOC2A/TMO1	TXD1/SMOSI1/SSDA1	TS4	
21		P21	MTIOC1B/TMCI0			
22		P20	MTIOC1A/TMRI0			
23	(5V tolerant)	P17	MTIOC3A/MTIOC3B/TMO1/ POE8#	SCK1/MISOA/SDA		IRQ7
24	(5V tolerant)	P16	MTIOC3C/MTIOC3D/TMO2	TXD1/SMOSI1/SSDA1/MOSIA/SCL		IRQ6/RTCOUT/ ADTRG0#
25		P15	MTIOC0B/MTCLKB/TMCI2	RXD1/SMISO1/SSCL1	TS5	IRQ5
26		P14	MTIOC3A/MTCLKA/TMRI2	CTS1#/RTS1#/SS1#	TS6	IRQ4
27	(5V tolerant)	P13	MTIOC0B/TMO3	SDA		IRQ3
28	(5V tolerant)	P12	TMCI1	SCL		IRQ2
29		PH3	TMCI0		TS7	
30		PH2	TMRI0		TS8	IRQ1
31		PH1	TMO0		TS9	IRQ0
32		PH0			TS10	CACREF
33		P55	MTIOC4D/TMO3		TS11	
34		P54	MTIOC4B/TMCI1		TS12	
35		PC7	MTIOC3A/TMO2/MTCLKB	MISOA	TS13	CACREF
36		PC6	MTIOC3C/MTCLKA/TMCI2	MOSIA	TS14	
37		PC5	MTIOC3B/MTCLKD/TMRI2	RSPCKA	TS15	
38		PC4	MTIOC3D/MTCLKC/TMCI1/ POE0#	SCK5/SSLA0	TSCAP	
39		PC3	MTIOC4D	TXD5/SMOSI5/SSDA5	TS16	
40		PC2	MTIOC4B	RXD5/SMISO5/SSCL5/SSLA3	TS17	
41		PB7/ PC1*2	MTIOC3B		TS18	
42		PB6/ PC0*2	MTIOC3D		TS19	
43		PB5	MTIOC2A/MTIOC1B/TMRI1/ POE1#		TS20	
44		PB4			TS21	
45		PB3	MTIOC0A/MTIOC4A/TMO0/ POE3#	SCK6	TS22	
46		PB2		CTS6#/RTS6#/SS6#	TS23	
47		PB1	MTIOC0C/MTIOC4C/TMCI0	TXD6/SMOSI6/SSDA6	TS24	IRQ4/CMPOB1
48	VCC					
49		PB0	MTIC5W	RXD6/SMISO6/SSCL6/RSPCKA	TS25	

4.1 I/O Register Addresses (Address Order)

Table 4.1 List of I/O Registers (Address Order) (1 / 18)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles
0008 0000h	SYSTEM	Mode Monitor Register	MDMONR	16	16	3 ICLK
0008 0008h	SYSTEM	System Control Register 1	SYSCR1	16	16	3 ICLK
0008 000Ch	SYSTEM	Standby Control Register	SBYCR	16	16	3 ICLK
0008 0010h	SYSTEM	Module Stop Control Register A	MSTPCRA	32	32	3 ICLK
0008 0014h	SYSTEM	Module Stop Control Register B	MSTPCRB	32	32	3 ICLK
0008 0018h	SYSTEM	Module Stop Control Register C	MSTPCRC	32	32	3 ICLK
0008 001Ch	SYSTEM	Module Stop Control Register D	MSTPCRD	32	32	3 ICLK
0008 0020h	SYSTEM	System Clock Control Register	SCKCR	32	32	3 ICLK
0008 0026h	SYSTEM	System Clock Control Register 3	SCKCR3	16	16	3 ICLK
0008 0028h	SYSTEM	PLL Control Register	PLLCR	16	16	3 ICLK
0008 002Ah	SYSTEM	PLL Control Register 2	PLLCR2	8	8	3 ICLK
0008 0032h	SYSTEM	Main Clock Oscillator Control Register	MOSCCR	8	8	3 ICLK
0008 0033h	SYSTEM	Sub-Clock Oscillator Control Register	SOSCCR	8	8	3 ICLK
0008 0034h	SYSTEM	Low-Speed On-Chip Oscillator Control Register	LOCOCR	8	8	3 ICLK
0008 0035h	SYSTEM	IWDT-Dedicated On-Chip Oscillator Control Register	ILOCOCR	8	8	3 ICLK
0008 0036h	SYSTEM	High-Speed On-Chip Oscillator Control Register	HOCOCR	8	8	3 ICLK
0008 003Ch	SYSTEM	Oscillation Stabilization Flag Register	OSCOVFSR	8	8	3 ICLK
0008 003Dh	SYSTEM	High-Speed On-Chip Oscillator Forced Oscillation Control Register	HOFCR	8	8	3 ICLK
0008 003Eh	SYSTEM	CLKOUT Output Control Register	CKOCR	16	16	3 ICLK
0008 0040h	SYSTEM	Oscillation Stop Detection Control Register	OSTDCR	8	8	3 ICLK
0008 0041h	SYSTEM	Oscillation Stop Detection Status Register	OSTDSR	8	8	3 ICLK
0008 0060h	SYSTEM	Low-Speed On-Chip Oscillator Trimming Register	LOCOTRR	8	8	3 ICLK
0008 0064h	SYSTEM	IWDT-Dedicated On-Chip Oscillator Trimming Register	ILOCOTRR	8	8	3 ICLK
0008 0068h	SYSTEM	High-Speed On-Chip Oscillator Trimming Register 0	HOCOTRR0	8	8	3 ICLK
0008 00A0h	SYSTEM	Operating Power Control Register	OPCCR	8	8	3 ICLK
0008 00A1h	SYSTEM	Sleep Mode Return Clock Source Switching Register	RSTCKCR	8	8	3 ICLK
0008 00A2h	SYSTEM	Main Clock Oscillator Wait Control Register	MOSCWTCR	8	8	3 ICLK
0008 00AAh	SYSTEM	Sub Operating Power Control Register	SOPCCR	8	8	3 ICLK
0008 00B0h	LPT	Low-Power Timer Control Register 1	LPTCR1	8	8	3 ICLK
0008 00B1h	LPT	Low-Power Timer Control Register 2	LPTCR2	8	8	3 ICLK
0008 00B2h	LPT	Low-Power Timer Control Register 3	LPTCR3	8	8	3 ICLK
0008 00B4h	LPT	Low-Power Timer Cycle Setting Register	LPTPRD	16	16	3 ICLK
0008 00B8h	LPT	Low-Power Timer Compare Register 0	LPCMR0	16	16	3 ICLK
0008 00BCh	LPT	Low-Power Timer Standby Wakeup Enable Register	LPWUCR	16	16	3 ICLK
0008 00C0h	SYSTEM	Reset Status Register 2	RSTSR2	8	8	3 ICLK
0008 00C2h	SYSTEM	Software Reset Register	SWRR	16	16	3 ICLK
0008 00E0h	SYSTEM	Voltage Monitoring 1 Circuit Control Register 1	LVD1CR1	8	8	3 ICLK
0008 00E1h	SYSTEM	Voltage Monitoring 1 Circuit Status Register	LVD1SR	8	8	3 ICLK
0008 00E2h	SYSTEM	Voltage Monitoring 2 Circuit Control Register 1	LVD2CR1	8	8	3 ICLK
0008 00E3h	SYSTEM	Voltage Monitoring 2 Circuit Status Register	LVD2SR	8	8	3 ICLK
0008 03FEh	SYSTEM	Protect Register	PRCR	16	16	3 ICLK
0008 1300h	BSC	Bus Error Status Clear Register	BERCLR	8	8	2 ICLK
0008 1304h	BSC	Bus Error Monitoring Enable Register	BEREN	8	8	2 ICLK
0008 1308h	BSC	Bus Error Status Register 1	BERSR1	8	8	2 ICLK
0008 130Ah	BSC	Bus Error Status Register 2	BERSR2	16	16	2 ICLK
0008 1310h	BSC	Bus Priority Control Register	BUSPRI	16	16	2 ICLK
0008 2400h	DTC	DTC Control Register	DTCCR	8	8	2 ICLK
0008 2404h	DTC	DTC Vector Base Register	DTCVBR	32	32	2 ICLK
0008 2408h	DTC	DTC Address Mode Register	DTCADMOD	8	8	2 ICLK

Table 4.1 List of I/O Registers (Address Order) (17 / 18)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles
000A 0B05h	REMC0	Compare Value Setting Register	REMCPD	8	8	1 or 2 PCLKB
000A 0B06h	REMC0	Header Pattern Minimum Width Setting Register	HDPMIN	16	16	1 or 2 PCLKB
000A 0B08h	REMC0	Header Pattern Maximum Width Setting Register	HDPMAX	16	16	1 or 2 PCLKB
000A 0B0Ah	REMC0	Data '0' Pattern Minimum Width Setting Register	D0PMIN	8	8	1 or 2 PCLKB
000A 0B0Bh	REMC0	Data '0' Pattern Maximum Width Setting Register	D0PMAX	8	8	1 or 2 PCLKB
000A 0B0Ch	REMC0	Data '1' Pattern Minimum Width Setting Register	D1PMIN	8	8	1 or 2 PCLKB
000A 0B0Dh	REMC0	Data '1' Pattern Maximum Width Setting Register	D1PMAX	8	8	1 or 2 PCLKB
000A 0B0Eh	REMC0	Special Data Pattern Minimum Width Setting Register	SDPMIN	16	16	1 or 2 PCLKB
000A 0B10h	REMC0	Special Data Pattern Maximum Width Setting Register	SDPMAX	16	16	1 or 2 PCLKB
000A 0B12h	REMC0	Pattern End Setting Register	REMPE	16	16	1 or 2 PCLKB
000A 0B14h	REMC0	Reception Standby Control Register	REMSTC	8	8	1 or 2 PCLKB
000A 0B15h	REMC0	Receive Bit Count Register	REMRBIT	8	8	1 or 2 PCLKB
000A 0B16h	REMC0	Receive Data 0 Register	REMDAT0	8	8	1 or 2 PCLKB
000A 0B17h	REMC0	Receive Data 1 Register	REMDAT1	8	8	1 or 2 PCLKB
000A 0B18h	REMC0	Receive Data 2 Register	REMDAT2	8	8	1 or 2 PCLKB
000A 0B19h	REMC0	Receive Data 3 Register	REMDAT3	8	8	1 or 2 PCLKB
000A 0B1Ah	REMC0	Receive Data 4 Register	REMDAT4	8	8	1 or 2 PCLKB
000A 0B1Bh	REMC0	Receive Data 5 Register	REMDAT5	8	8	1 or 2 PCLKB
000A 0B1Ch	REMC0	Receive Data 6 Register	REMDAT6	8	8	1 or 2 PCLKB
000A 0B1Dh	REMC0	Receive Data 7 Register	REMDAT7	8	8	1 or 2 PCLKB
000A 0B1Eh	REMC0	Measurement Result Register	REMTIM	16	16	1 or 2 PCLKB
000A 0B80h	REMC1	Function Select Register 0	REMCON0	8	8	1 or 2 PCLKB
000A 0B81h	REMC1	Function Select Register 1	REMCON1	8	8	1 or 2 PCLKB
000A 0B82h	REMC1	Status Register	REMSTS	8	8	1 or 2 PCLKB
000A 0B83h	REMC1	Interrupt Control Register	REMINT	8	8	1 or 2 PCLKB
000A 0B84h	REMC1	Compare Control Register	REMCPC	8	8	1 or 2 PCLKB
000A 0B85h	REMC1	Compare Value Setting Register	REMCPD	8	8	1 or 2 PCLKB
000A 0B86h	REMC1	Header Pattern Minimum Width Setting Register	HDPMIN	16	16	1 or 2 PCLKB
000A 0B88h	REMC1	Header Pattern Maximum Width Setting Register	HDPMAX	16	16	1 or 2 PCLKB
000A 0B8Ah	REMC1	Data '0' Pattern Minimum Width Setting Register	D0PMIN	8	8	1 or 2 PCLKB
000A 0B8Bh	REMC1	Data '0' Pattern Maximum Width Setting Register	D0PMAX	8	8	1 or 2 PCLKB
000A 0B8Ch	REMC1	Data '1' Pattern Minimum Width Setting Register	D1PMIN	8	8	1 or 2 PCLKB
000A 0B8Dh	REMC1	Data '1' Pattern Maximum Width Setting Register	D1PMAX	8	8	1 or 2 PCLKB
000A 0B8Eh	REMC1	Special Data Pattern Minimum Width Setting Register	SDPMIN	16	16	1 or 2 PCLKB
000A 0B90h	REMC1	Special Data Pattern Maximum Width Setting Register	SDPMAX	16	16	1 or 2 PCLKB
000A 0B92h	REMC1	Pattern End Setting Register	REMPE	16	16	1 or 2 PCLKB
000A 0B94h	REMC1	Reception Standby Control Register	REMSTC	8	8	1 or 2 PCLKB
000A 0B95h	REMC1	Receive Bit Count Register	REMRBIT	8	8	1 or 2 PCLKB
000A 0B96h	REMC1	Receive Data 0 Register	REMDAT0	8	8	1 or 2 PCLKB
000A 0B97h	REMC1	Receive Data 1 Register	REMDAT1	8	8	1 or 2 PCLKB
000A 0B98h	REMC1	Receive Data 2 Register	REMDAT2	8	8	1 or 2 PCLKB
000A 0B99h	REMC1	Receive Data 3 Register	REMDAT3	8	8	1 or 2 PCLKB
000A 0B9Ah	REMC1	Receive Data 4 Register	REMDAT4	8	8	1 or 2 PCLKB
000A 0B9Bh	REMC1	Receive Data 5 Register	REMDAT5	8	8	1 or 2 PCLKB
000A 0B9Ch	REMC1	Receive Data 6 Register	REMDAT6	8	8	1 or 2 PCLKB
000A 0B9Dh	REMC1	Receive Data 7 Register	REMDAT7	8	8	1 or 2 PCLKB
000A 0B9Eh	REMC1	Measurement Result Register	REMTIM	16	16	1 or 2 PCLKB
000A 0C00h	REMCOM	HOCO Clock Supply Control Register	HOSCR	8	8	1 or 2 PCLKB
007F C090h	FLASH	E2 DataFlash Control Register	DFLCTL	8	8	2 or 3 FCLK
007F C0ACh	TEMPS	Temperature Sensor Calibration Data Register	TSCDRL	8	8	2 or 3 FCLK
007F C0ADh	TEMPS	Temperature Sensor Calibration Data Register	TSCDRH	8	8	2 or 3 FCLK
007F C0B0h	FLASH	Flash Start-Up Setting Monitor Register	FSCMR	16	16	2 or 3 FCLK

Table 4.1 List of I/O Registers (Address Order) (18 / 18)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles
007F C0B2h	FLASH	Flash Access Window Start Address Monitor Register	FAWSMR	16	16	2 or 3 FCLK
007F C0B4h	FLASH	Flash Access Window End Address Monitor Register	FAWEMR	16	16	2 or 3 FCLK
007F C0B6h	FLASH	Flash Initial Setting Register	FISR	8	8	2 or 3 FCLK
007F C0B7h	FLASH	Flash Extra Area Control Register	FEXCR	8	8	2 or 3 FCLK
007F C0B8h	FLASH	Flash Error Address Monitor Register L	FEAML	16	16	2 or 3 FCLK
007F C0BAh	FLASH	Flash Error Address Monitor Register H	FEAMH	8	8	2 or 3 FCLK
007F C0C0h	FLASH	Protection Unlock Register	FPR	8	8	2 or 3 FCLK
007F C0C1h	FLASH	Protection Unlock Status Register	FPSR	8	8	2 or 3 FCLK
007F C0C2h	FLASH	Flash Read Buffer Register L	FRBL	16	16	2 or 3 FCLK
007F C0C4h	FLASH	Flash Read Buffer Register H	FRBH	16	16	2 or 3 FCLK
007F FF80h	FLASH	Flash P/E Mode Control Register	FPMCR	8	8	2 or 3 FCLK
007F FF81h	FLASH	Flash Area Select Register	FASR	8	8	2 or 3 FCLK
007F FF82h	FLASH	Flash Processing Start Address Register L	FSARL	16	16	2 or 3 FCLK
007F FF84h	FLASH	Flash Processing Start Address Register H	FSARH	8	8	2 or 3 FCLK
007F FF85h	FLASH	Flash Control Register	FCR	8	8	2 or 3 FCLK
007F FF86h	FLASH	Flash Processing End Address Register L	FEARL	16	16	2 or 3 FCLK
007F FF88h	FLASH	Flash Processing End Address Register H	FEARH	8	8	2 or 3 FCLK
007F FF89h	FLASH	Flash Reset Register	FRESETR	8	8	2 or 3 FCLK
007F FF8Ah	FLASH	Flash Status Register 0	FSTATR0	8	8	2 or 3 FCLK
007F FF8Bh	FLASH	Flash Status Register 1	FSTATR1	8	8	2 or 3 FCLK
007F FF8Ch	FLASH	Flash Write Buffer Register L	FWBL	16	16	2 or 3 FCLK
007F FF8Eh	FLASH	Flash Write Buffer Register H	FWBH	16	16	2 or 3 FCLK
007F FFB2h	FLASH	Flash P/E Mode Entry Register	FENTRYR	16	16	2 or 3 FCLK
007F FFBEh	CTSU	CTSU Reference Current Calibration Register	CTSUTRMR	8	8	2 or 3 FCLK

5. Electrical Characteristics

5.1 Absolute Maximum Ratings

Table 5.1 Absolute Maximum Ratings

Conditions: VSS = AVSS0 = VREFL0 = 0 V

Item		Symbol	Value	Unit
Power supply voltage		VCC	–0.3 to +6.5	V
Input voltage	Ports for 5 V tolerant*1	V_{in}	–0.3 to +6.5	V
	Ports P03 to P07, Ports P40 to P47, Ports PJ6, PJ7		–0.3 to AVCC0 + 0.3	V
	Ports other than above		–0.3 to VCC + 0.3	
Reference power supply voltage		VREFH0	–0.3 to AVCC0 + 0.3	V
Analog power supply voltage		AVCC0	–0.3 to +6.5	V
Analog input voltage	When AN000 to AN007 used	V_{AN}	–0.3 to AVCC0 + 0.3	V
	When AN016 to AN031 used		–0.3 to VCC + 0.3	
Operating temperature*2		T_{opr}	–40 to +85 –40 to +105	°C
Storage temperature		T_{stg}	–55 to +125	°C

Caution: Permanent damage to the MCU may result if absolute maximum ratings are exceeded.

To preclude any malfunctions due to noise interference, insert capacitors of high frequency characteristics between the VCC and VSS pins, between the AVCC0 and AVSS0 pins, and between the VREFH0 and VREFL0 pins. Place capacitors of about 0.1 µF as close as possible to every power supply pin and use the shortest and heaviest possible traces.

Connect the VCL pin to a VSS pin via a 4.7 µF capacitor. The capacitor must be placed close to the pin, refer to section 5.13.1, Connecting VCL Capacitor and Bypass Capacitors

Do not input signals or an I/O pull-up power supply to ports other than 5-V tolerant ports while the device is not powered.

The current injection that results from input of such a signal or I/O pull-up may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements.

Even if –0.3 to +6.5 V is input to 5-V tolerant ports, it will not cause problems such as damage to the MCU.

Note 1. Ports P12, P13, P16, and P17 are 5 V tolerant.

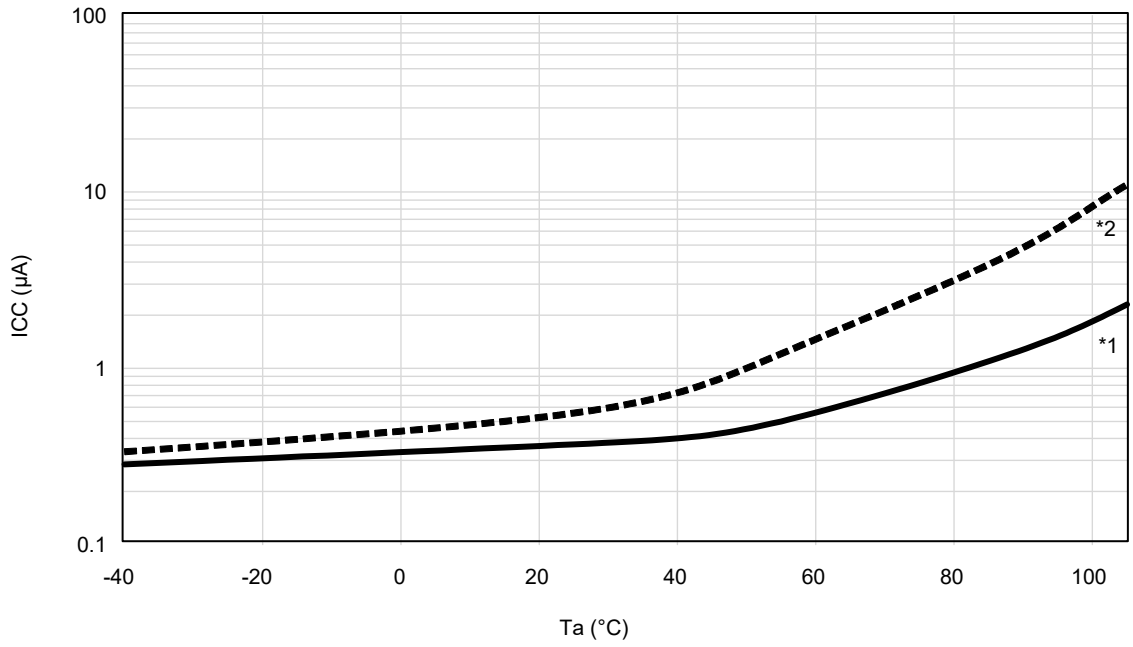
Note 2. The upper limit of operating temperature is 85°C or 105°C, depending on the product. For details, refer to section 1.2, List of Products.

[Products with at least 256 Kbytes of flash memory or 100-pin packages]

Table 5.8 DC Characteristics (5)

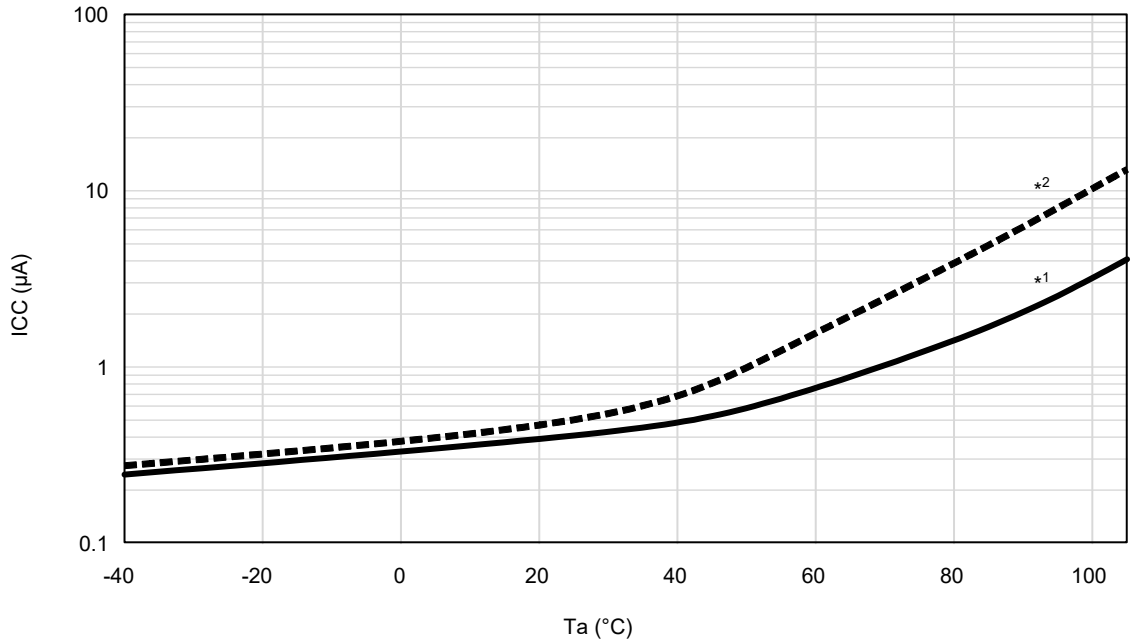
Conditions: 1.8 V ≤ VCC = AVCC0 < 2.0 V, 2.0 V ≤ VCC ≤ 5.5 V, 2.0 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, Ta = –40 to +105°C

Item					Symbol	Typ.	Max.	Unit	Test Conditions
Supply current*1	High-speed operating mode	Normal operating mode	No peripheral operation*2	ICLK = 32MHz	I_{CC}	3.5	—	mA	
				ICLK = 16MHz		2.4	—		
				ICLK = 8MHz		1.8	—		
			All peripheral operation: Normal*3	ICLK = 32MHz		12.4	—		
				ICLK = 16MHz		7.0	—		
				ICLK = 8MHz		4.3	—		
			All peripheral operation: Max.*3	ICLK = 32MHz		—	25.4		
		Sleep mode	No peripheral operation*2	ICLK = 32MHz		1.8	—		
				ICLK = 16MHz		1.4	—		
				ICLK = 8MHz		1.2	—		
			All peripheral operation: Normal*3	ICLK = 32MHz		6.5	—		
				ICLK = 16MHz		3.8	—		
				ICLK = 8MHz		2.5	—		
		Deep sleep mode	No peripheral operation*2	ICLK = 32MHz		1.1	—		
				ICLK = 16MHz		0.9	—		
				ICLK = 8MHz		0.8	—		
			All peripheral operation: Normal*3	ICLK = 32MHz		5.2	—		
				ICLK = 16MHz		3.0	—		
				ICLK = 8MHz		1.9	—		
		Increase during flash rewrite*5				2.5	—		
	Middle-speed operating modes	Normal operating mode	No peripheral operation*6	ICLK = 12MHz	I_{CC}	2.1	—	mA	
				ICLK = 8MHz		1.4	—		
				ICLK = 4MHz		0.7	—		
				ICLK = 1MHz		0.3	—		
			All peripheral operation: Normal*7	ICLK = 12MHz		5.5	—		
				ICLK = 8MHz		3.9	—		
				ICLK = 4MHz		2.4	—		
				ICLK = 1MHz		1.1	—		
			All peripheral operation: Max.*7	ICLK = 12MHz		—	11.6		
		Sleep mode	No peripheral operation*6	ICLK = 12MHz	I_{CC}	1.4	—	mA	
				ICLK = 8MHz		0.8	—		
				ICLK = 4MHz		0.3	—		
				ICLK = 1MHz		0.2	—		
			All peripheral operation: Normal*7	ICLK = 12MHz		3.2	—		
				ICLK = 8MHz		2.2	—		
				ICLK = 4MHz		1.4	—		
				ICLK = 1MHz		0.8	—		



Note 1. Average value of the tested middle samples during product evaluation.
Note 2. Average value of the tested upper-limit samples during product evaluation.

Figure 5.8 Temperature Dependency in Software Standby Mode (Reference Data)



Note 1. Average value of the tested middle samples during product evaluation.
Note 2. Average value of the tested upper-limit samples during product evaluation.

Figure 5.10 Temperature Dependency in Software Standby Mode (Reference Data)

Table 5.11 DC Characteristics (7)

Conditions: 1.8 V ≤ VCC = AVCC0 < 2.0 V, 2.0 V ≤ VCC ≤ 5.5 V, 2.0 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V

Item	Symbol	Typ.	Max.	Unit	Test Conditions
Permissible total power consumption*1	P_d	—	300	mW	D version
		—	105		G version

Note: Please contact a Renesas Electronics sales office for information on the derating of the G-version product. Derating is the systematic reduction of load to improve reliability.
Note 1. Total power dissipated by the entire chip (including output currents)

Table 5.18 Permissible Output Currents (2)

Conditions: 1.8 V ≤ VCC = AVCC0 < 2.0 V, 2.0 V ≤ VCC ≤ 5.5 V, 2.0 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, Ta = –40 to +105°C

Item			Symbol	Max.	Unit
Permissible output low current (average value per pin)	Ports P03 to P07, Ports P40 to P47, Ports PJ6, PJ7		I_{OL}	4.0	mA
	Ports other than above	Normal output mode		4.0	
		High-drive output mode		8.0	
Permissible output low current (maximum value per pin)	Ports P03 to P07, Ports P40 to P47, Ports PJ6, PJ7			4.0	
	Ports other than above	Normal output mode		4.0	
		High-drive output mode		8.0	
Permissible output low current	Total of Ports P03 to P07, Ports P40 to P47, Ports PJ6, PJ7		ΣI_{OL}	30	
	Total of Ports P12 to P17, Ports P20 to P27, Ports P30 to P37, Ports PH2, PH3, Ports PJ1, PJ3			30	
	Total of Ports P50 to P55, Ports PB0 to PB7, Ports PC0 to PC7, Ports PH0, PH1			30	
	Total of Ports PA0 to PA7, Ports PD0 to PD7, Ports PE0 to PE7			30	
	Total of all output pins			60	
Permissible output high current (average value per pin)	Ports P03 to P07, Ports P40 to P47, Ports PJ6, PJ7		I_{OH}	–4.0	
	Ports other than above	Normal output mode		–4.0	
		High-drive output mode		–8.0	
Permissible output high current (maximum value per pin)	Ports P03 to P07, Ports P40 to P47, Ports PJ6, PJ7			–4.0	
	Ports other than above	Normal output mode		–4.0	
		High-drive output mode		–8.0	
Permissible output high current	Total of Ports P03 to P07, Ports P40 to P47, Ports PJ6, PJ7		ΣI_{OH}	–30	
	Total of Ports P12 to P17, Ports P20 to P27, Ports P30 to P37, Ports PH2, PH3, Ports PJ1, PJ3			–30	
	Total of Ports P50 to P55, Ports PB0 to PB7, Ports PC0 to PC7, Ports PH0, PH1			–30	
	Total of Ports PA0 to PA7, Ports PD0 to PD7, Ports PE0 to PE7			–30	
	Total of all output pins			–60	

Note: Do not exceed the permissible total supply current.

5.2.1 Normal I/O Pin Output Characteristics (1)

Figure 5.12 to Figure 5.16 show the characteristics when normal output is selected by the drive capacity control register.

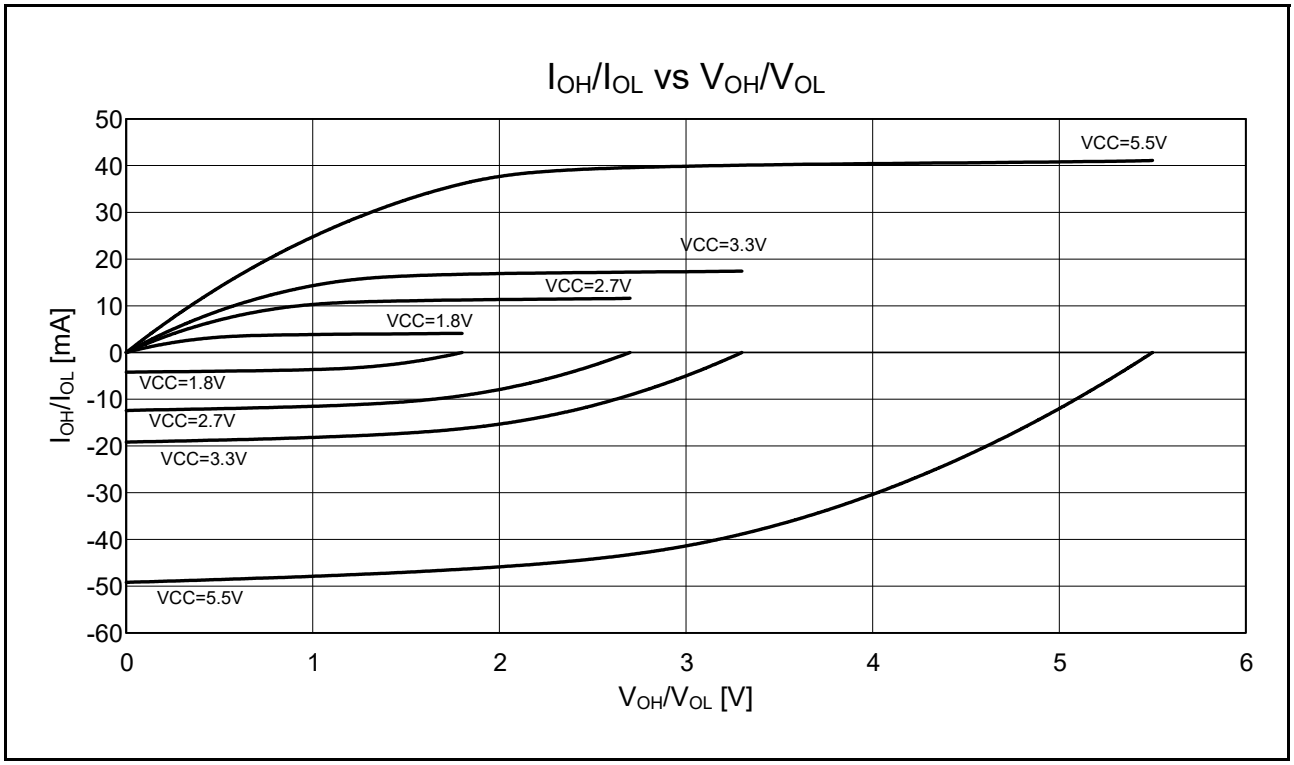


Figure 5.12 V_{OH}/V_{OL} and I_{OH}/I_{OL} Voltage Characteristics at T_a = 25°C When Normal Output is Selected (Reference Data)

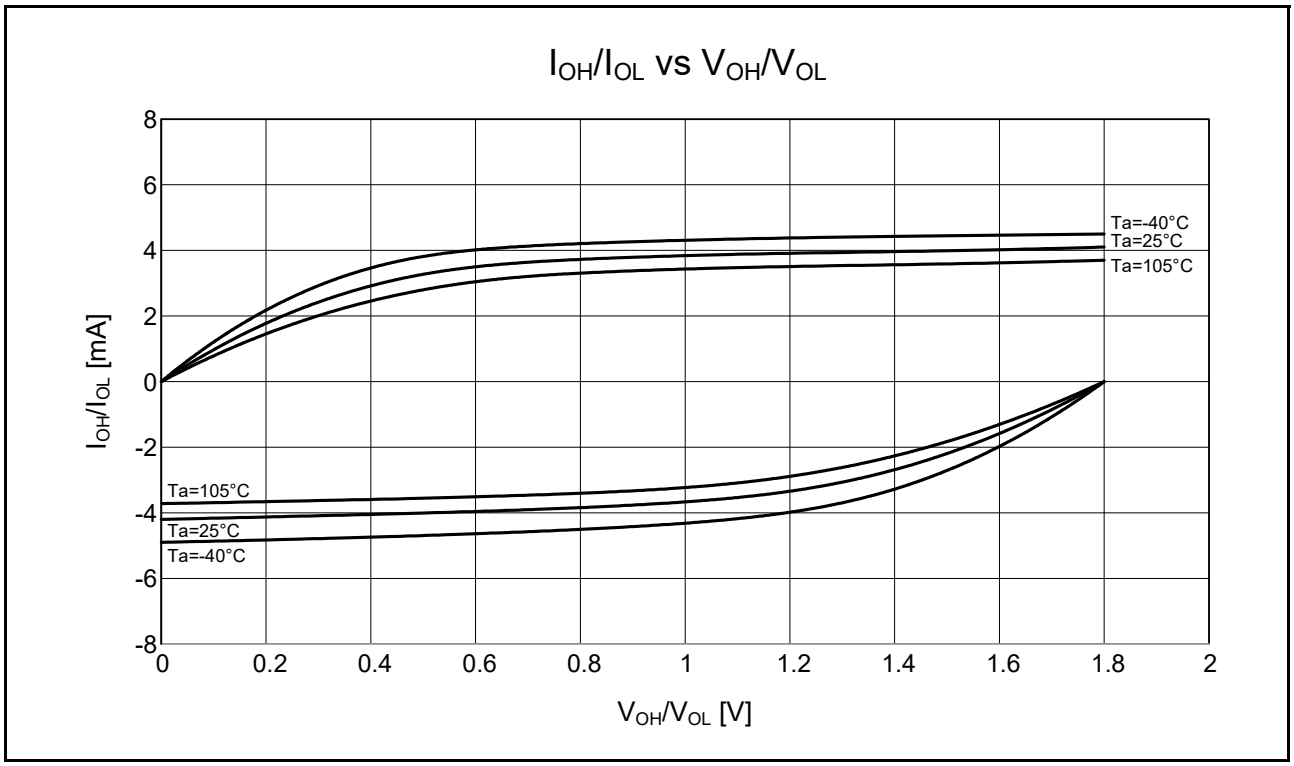


Figure 5.13 V_{OH}/V_{OL} and I_{OH}/I_{OL} Temperature Characteristics at VCC = 1.8 V When Normal Output is Selected (Reference Data)

5.3 AC Characteristics

5.3.1 Clock Timing

Table 5.22 Operating Frequency Value (High-Speed Operating Mode)

Conditions: 1.8 V ≤ VCC = AVCC0 < 2.0 V, 2.0 V ≤ VCC ≤ 5.5 V, 2.0 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, Ta = –40 to +105°C

Item		Symbol	VCC			Unit
			1.8 V ≤ VCC < 2.4 V	2.4 V ≤ VCC < 2.7 V	2.7 V ≤ VCC ≤ 5.5 V	
Maximum operating frequency*4	System clock (ICLK)	f_{max}	8	16	32	MHz
	FlashIF clock (FCLK)*1, *2		8	16	32	
	Peripheral module clock (PCLKB)		8	16	32	
	Peripheral module clock (PCLKD)*3		8	16	32	

Note 1. The lower-limit frequency of FCLK is 1 MHz during programming or erasing of the flash memory. When using FCLK at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.
Note 2. The frequency accuracy of FCLK should be ±3.5%.
Note 3. The lower-limit frequency of PCLKD is 4 MHz at 2.4 V or above and 1 MHz at below 2.4 V when the A/D converter is in use.
Note 4. The maximum operating frequency does not include HOCO error or PLL jitter. See Table 5.25, Clock Timing.

Table 5.23 Operating Frequency Value (Middle-Speed Operating Mode)

Conditions: 1.8 V ≤ VCC = AVCC0 < 2.0 V, 2.0 V ≤ VCC ≤ 5.5 V, 2.0 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, Ta = –40 to +105°C

Item		Symbol	VCC			Unit
			1.8 V ≤ VCC < 2.4 V	2.4 V ≤ VCC < 2.7 V	2.7 V ≤ VCC ≤ 5.5 V	
Maximum operating frequency*4	System clock (ICLK)	f_{max}	8	12	12	MHz
	FlashIF clock (FCLK)*1, *2		8	12	12	
	Peripheral module clock (PCLKB)		8	12	12	
	Peripheral module clock (PCLKD)*3		8	12	12	

Note 1. The lower-limit frequency of FCLK is 1 MHz during programming or erasing of the flash memory. When using FCLK at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.
Note 2. The frequency accuracy of FCLK should be ±3.5%.
Note 3. The lower-limit frequency of PCLKD is 4 MHz at 2.4 V or above and 1 MHz at below 2.4 V when the A/D converter is in use.
Note 4. The maximum operating frequency does not include HOCO error or PLL jitter. See Table 5.25, Clock Timing

Table 5.24 Operating Frequency Value (Low-Speed Operating Mode)

Conditions: 1.8 V ≤ VCC = AVCC0 < 2.0 V, 2.0 V ≤ VCC ≤ 5.5 V, 2.0 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, Ta = –40 to +105°C

Item		Symbol	VCC			Unit
			1.8 V ≤ VCC < 2.4 V	2.4 V ≤ VCC < 2.7 V	2.7 V ≤ VCC ≤ 5.5 V	
Maximum operating frequency	System clock (ICLK)	f_{max}	32.768			kHz
	FlashIF clock (FCLK)*1		32.768			
	Peripheral module clock (PCLKB)		32.768			
	Peripheral module clock (PCLKD)*2		32.768			

Note 1. Programming and erasing the flash memory is impossible.
Note 2. The A/D converter cannot be used.

Table 5.25 Clock Timing

Conditions: 1.8 V ≤ VCC = AVCC0 < 2.0 V, 2.0 V ≤ VCC ≤ 5.5 V, 2.0 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, Ta = –40 to +105°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
EXTAL external clock input cycle time		t_{Xcyc}	50	—	—	ns	Figure 5.26
EXTAL external clock input high pulse width		t_{XH}	20	—	—	ns	
EXTAL external clock input low pulse width		t_{XL}	20	—	—	ns	
EXTAL external clock rise time		t_{Xr}	—	—	5	ns	
EXTAL external clock fall time		t_{Xf}	—	—	5	ns	
EXTAL external clock input wait time*1		t_{XWT}	0.5	—	—	μs	
Main clock oscillator oscillation frequency*2	2.4 ≤ VCC ≤ 5.5	f_{MAIN}	1	—	20	MHz	
	1.8 ≤ VCC < 2.4		1	—	8		
Main clock oscillation stabilization time (crystal)*2		$t_{MAINOSC}$	—	3	—	ms	Figure 5.27
Main clock oscillation stabilization time (ceramic resonator)*2		$t_{MAINOSC}$	—	50	—	μs	
LOCO clock oscillation frequency		f_{LOCO}	3.44	4.0	4.56	MHz	
LOCO clock oscillation stabilization time		t_{LOCO}	—	—	0.5	μs	Figure 5.28
IWDT-dedicated clock oscillation frequency		f_{ILOCO}	12.75	15	17.25	kHz	
IWDT-dedicated clock oscillation stabilization time		t_{ILOCO}	—	—	50	μs	Figure 5.29
HOCO clock oscillation frequency		f_{HOCO} (32 MHz)	31.52	32	32.48	MHz	T_a = –40 to + 85°C
			31.68	32	32.32		T_a = 0 to + 55°C
			31.36	32	32.64		T_a = –40 to +105°C
HOCO clock oscillation stabilization time		t_{HOCO}	—	—	30	μs	Figure 5.31
PLL input frequency*3		f_{PLLIN}	4	—	8	MHz	
PLL circuit oscillation frequency*3		f_{PLL}	24	—	32	MHz	
PLL clock oscillation stabilization time		t_{PLL}	—	—	50	μs	Figure 5.32
PLL free-running oscillation frequency		f_{PLLFR}	—	8	—	MHz	
Sub-clock oscillator oscillation frequency*5		f_{SUB}	—	32.768	—	kHz	
Sub-clock oscillation stabilization time*4		t_{SUBOSC}	—	0.5	—	s	Figure 5.33

Note 1. Time until the clock can be used after the main clock oscillator stop bit (MOSCCR.MOSTP) is set to 0 (operating).

Note 2. Reference values when an 8-MHz resonator is used.
When specifying the main clock oscillator stabilization time, set the MOSCWTCR register with a stabilization time value that is equal to or greater than the resonator-manufacturer-recommended value.
After changing the setting of the MOSCCR.MOSTP bit so that the main clock oscillator operates, read the OSCOVFSR.MOOVF flag to confirm that is has become 1, and then start using the main clock.

Note 3. The VCC range should be 2.4 to 5.5 V when the PLL is used.

Note 4. Reference value when a 32.768-kHz resonator is used.
After changing the setting of the SOSCCR.SOSTP bit or RCR3.RTCEN bit so that the sub-clock oscillator operates, only start using the sub-clock after the sub-clock oscillation stabilization wait time that is equal to or greater than the oscillator-manufacturer-recommended value has elapsed.

Note 5. Only 32.768-kHz can be used.

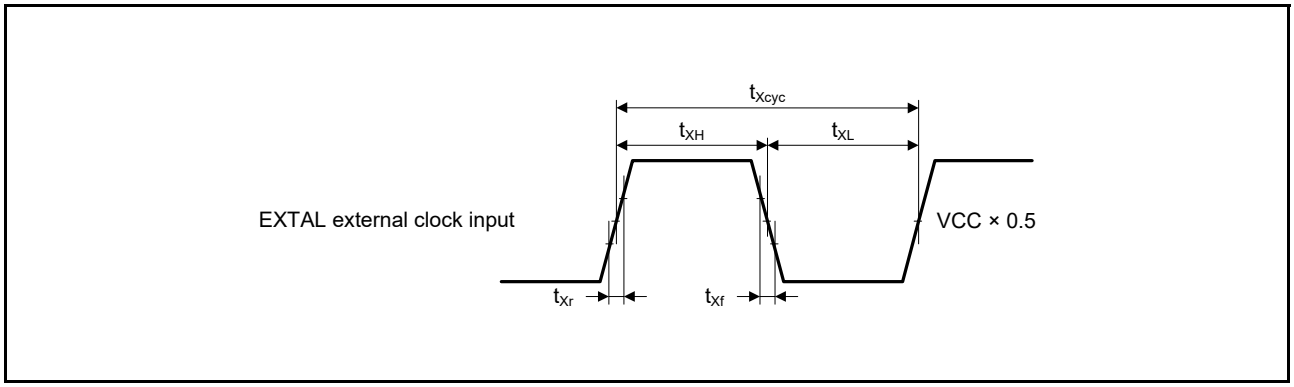


Figure 5.26 EXTAL External Clock Input Timing

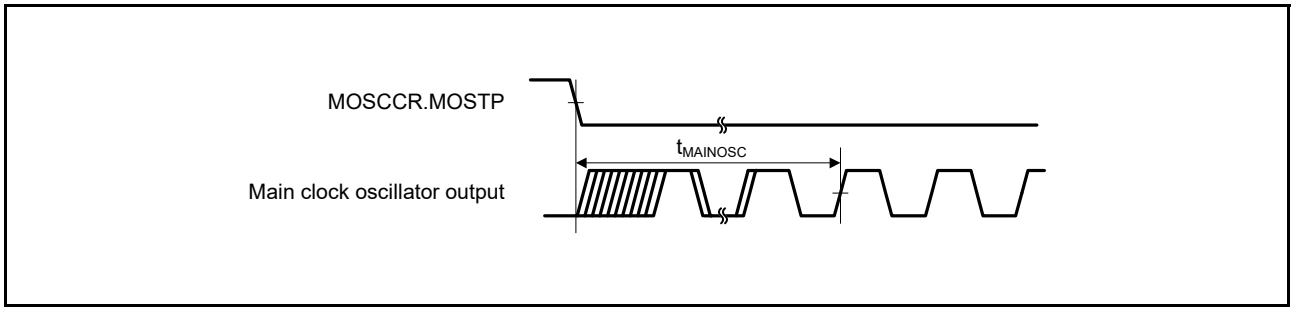


Figure 5.27 Main Clock Oscillation Start Timing

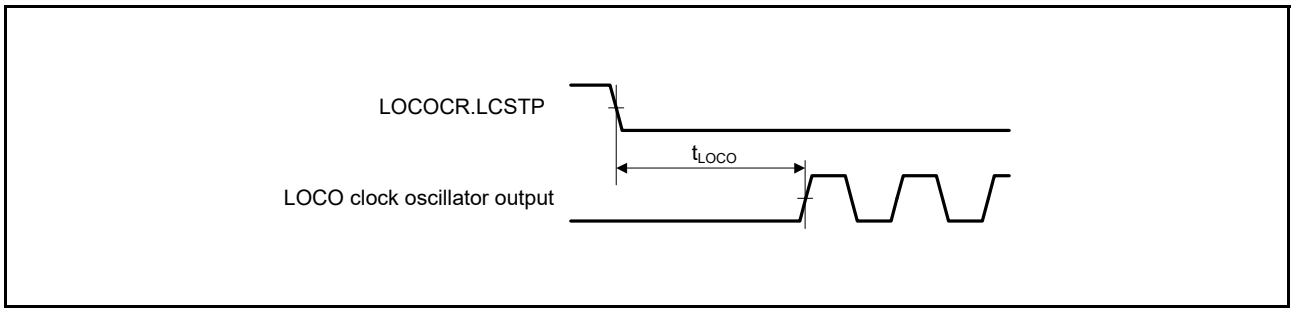


Figure 5.28 LOCO Clock Oscillation Start Timing

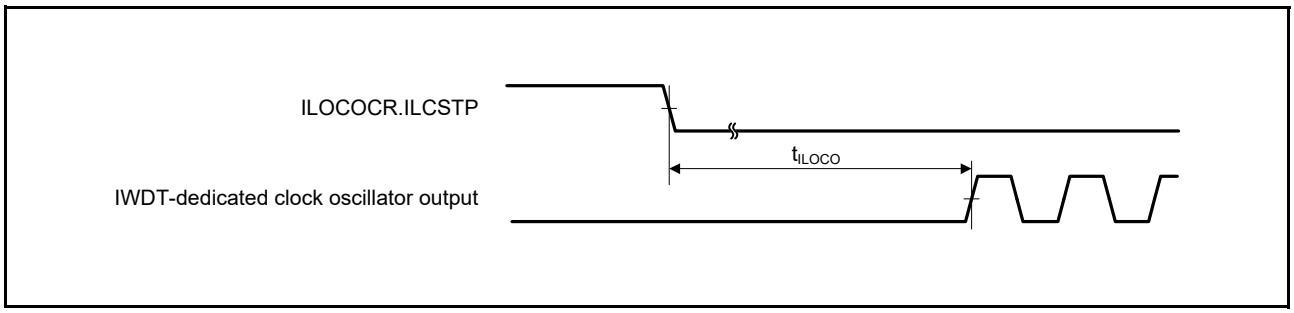


Figure 5.29 IWDT-Dedicated Clock Oscillation Start Timing

When the main clock oscillator wait control register (MOSCWTCR) is set to 00h.

Table 5.29 Timing of Recovery from Low Power Consumption Modes (3)

Conditions: 1.8 V ≤ VCC = AVCC0 < 2.0 V, 2.0 V ≤ VCC ≤ 5.5 V, 2.0 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, Ta = –40 to +105°C

Item			Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Recovery time from software standby mode*1	Low-speed mode	Sub-clock oscillator operating	t_{SBYSC}	—	600	750	µs	Figure 5.37

Note: Note Values when the frequencies of PCLKB, PCLKD, and FCLK are not divided.
Note 1. The sub-clock continues oscillating in software standby mode during low-speed mode.

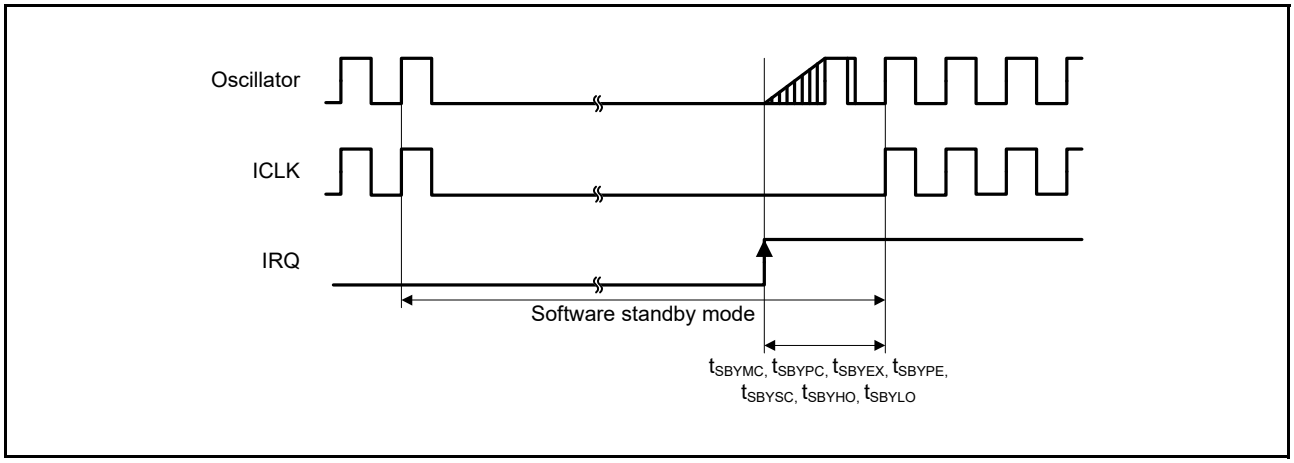


Figure 5.37 Software Standby Mode Recovery Timing

Table 5.30 Timing of Recovery from Low Power Consumption Modes (4)

Conditions: 1.8 V ≤ VCC = AVCC0 < 2.0 V, 2.0 V ≤ VCC ≤ 5.5 V, 2.0 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, Ta = –40 to +105°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Recovery time from deep sleep mode*1	High-speed mode*2	t_{DSLP}	—	2	3.5	µs	Figure 5.38
	Middle-speed mode*3	t_{DSLP}	—	3	4	µs	
	Low-speed mode*4	t_{DSLP}	—	400	500	µs	

Note: Note Values when the frequencies of PCLKB, PCLKD, and FCLK are not divided.
Note 1. Oscillators continue oscillating in deep sleep mode.
Note 2. When the frequency of the system clock is 32 MHz.
Note 3. When the frequency of the system clock is 12 MHz.
Note 4. When the frequency of the system clock is 32.768 kHz.

Absolute accuracy

Absolute accuracy is the difference between output code based on the theoretical A/D conversion characteristics, and the actual A/D conversion result. When measuring absolute accuracy, the voltage at the midpoint of the width of analog input voltage (1-LSB width), that can meet the expectation of outputting an equal code based on the theoretical A/D conversion characteristics, is used as an analog input voltage. For example, if 12-bit resolution is used and if reference voltage (VREFH0 = 3.072 V), then 1-LSB width becomes 0.75 mV, and 0 mV, 0.75 mV, 1.5 mV, ... are used as analog input voltages.
If analog input voltage is 6 mV, absolute accuracy = ±5 LSB means that the actual A/D conversion result is in the range of 003h to 00Dh though an output code, 008h, can be expected from the theoretical A/D conversion characteristics.

Integral nonlinearity error (INL)

Integral nonlinearity error is the maximum deviation between the ideal line when the measured offset and full-scale errors are zeroed, and the actual output code.

Differential nonlinearity error (DNL)

Differential nonlinearity error is the difference between 1-LSB width based on the ideal A/D conversion characteristics and the width of the actual output code.

Offset error

Offset error is the difference between a transition point of the ideal first output code and the actual first output code.

Full-scale error

Full-scale error is the difference between a transition point of the ideal last output code and the actual last output code.

5.10 Oscillation Stop Detection Timing

Table 5.51 Oscillation Stop Detection Timing

Conditions: 1.8 V ≤ VCC = AVCC0 < 2.0 V, 2.0 V ≤ VCC ≤ 5.5 V, 2.0 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Detection time	t_{dr}	—	—	1	ms	Figure 5.66

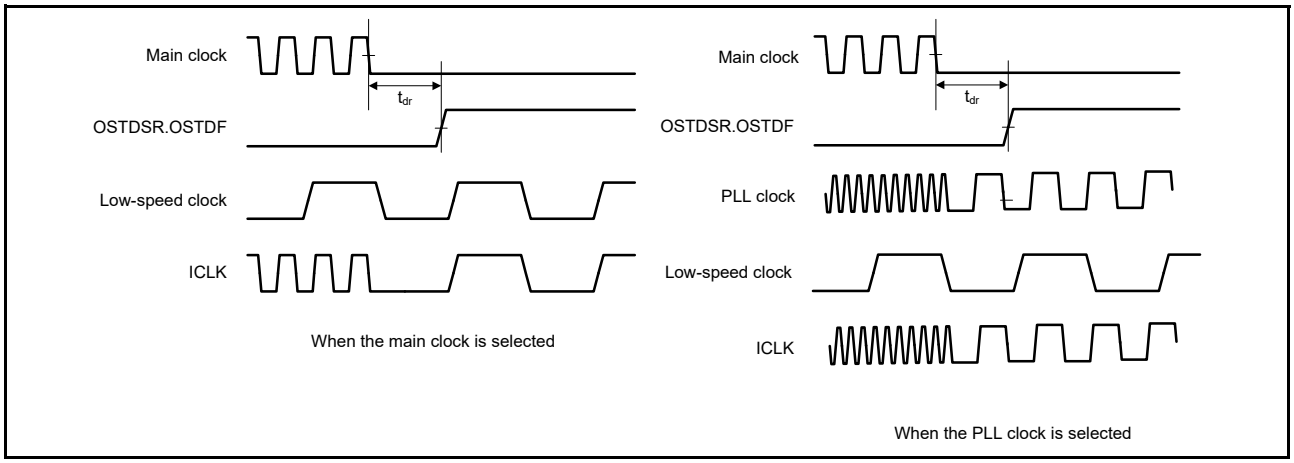


Figure 5.66 Oscillation Stop Detection Timing

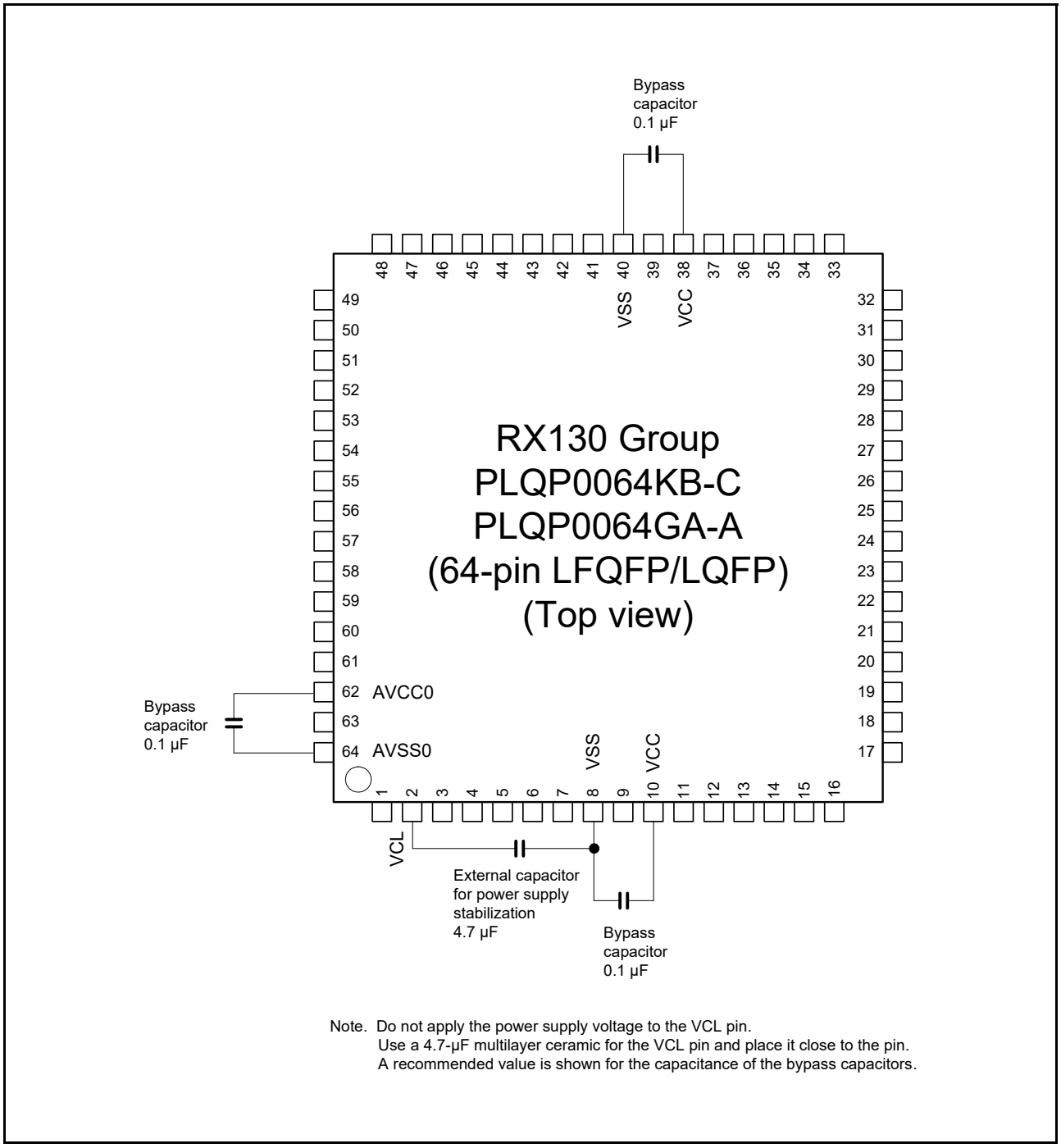
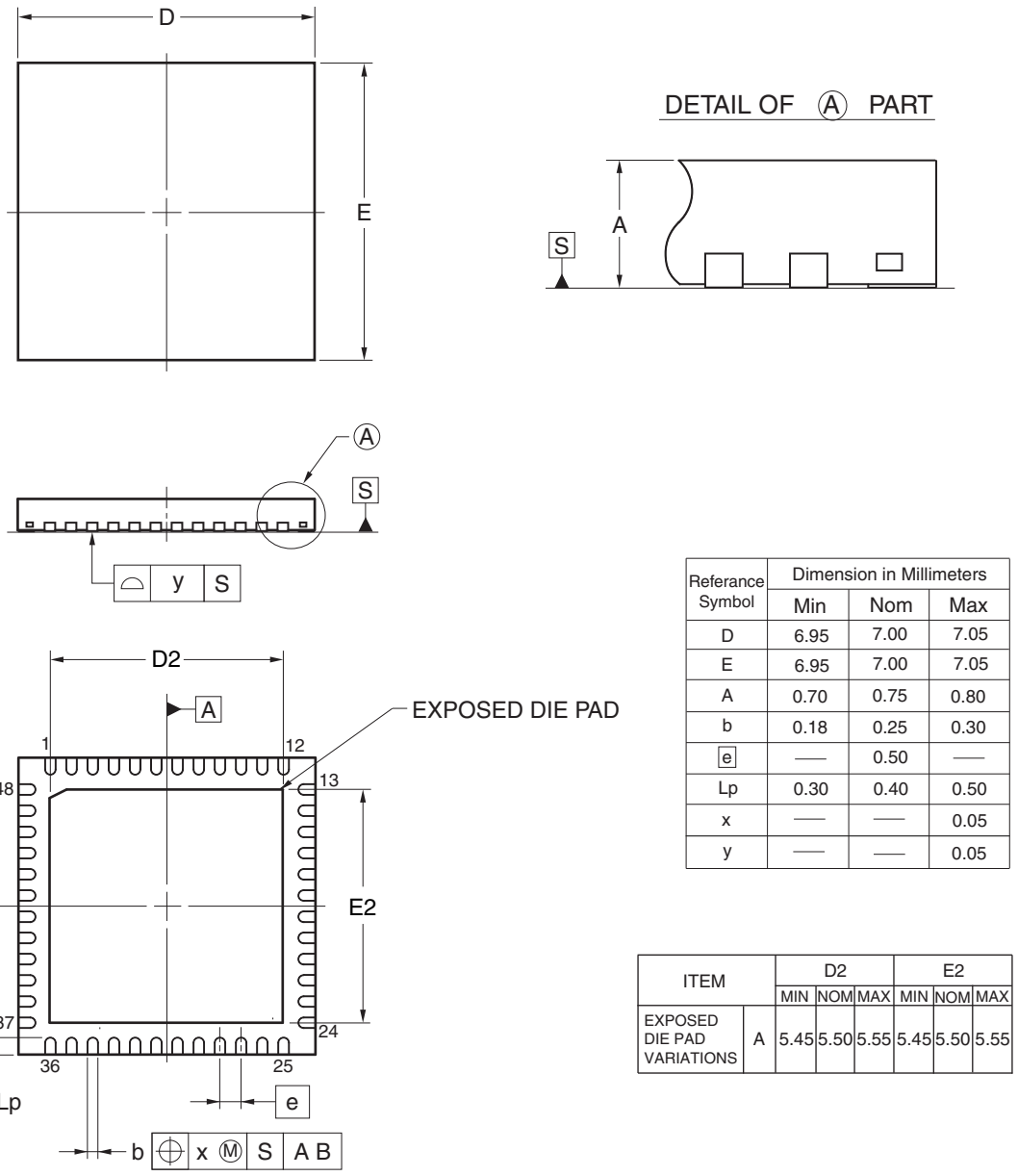


Figure 5.69 Connecting Capacitors (64 Pins)

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-HWQFN48-7x7-0.50	PWQN0048KB-A	48PJN-A P48K8-50-5B4-5	0.13



Referance Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	6.95	7.00	7.05
E	6.95	7.00	7.05
A	0.70	0.75	0.80
b	0.18	0.25	0.30
e	—	0.50	—
Lp	0.30	0.40	0.50
x	—	—	0.05
y	—	—	0.05

ITEM		D2			E2		
		MIN	NOM	MAX	MIN	NOM	MAX
EXPOSED DIE PAD VARIATIONS	A	5.45	5.50	5.55	5.45	5.50	5.55

Figure E 48-Pin HWQFN (PWQN0048KB-A)