Renesas Electronics America Inc - R5F51305ADFM#30 Datasheet

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	RX
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	I²C, LINbus, SCI, SPI
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	52
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	8K x 8
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 14x12b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LFQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f51305adfm-30

Table 1.1 Outline of Specifications (2/3)

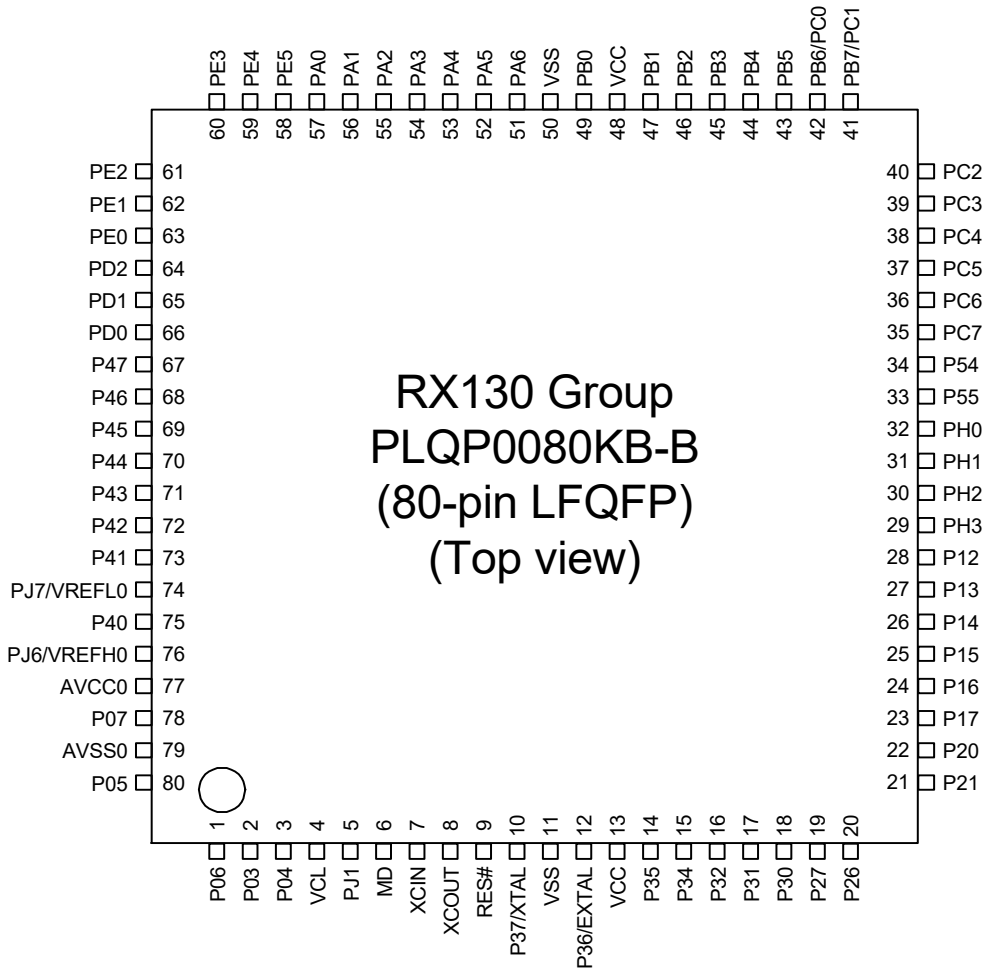
Classification	Module/Function	Description
DMA	Data transfer controller (DTCa)	• Transfer modes: Normal transfer, repeat transfer, and block transfer • Activation sources: Interrupts • Chain transfer function
I/O ports	General I/O ports	100-pin /80-pin /64-pin /48-pin • I/O: 88/68/52/38 • Input: 1/1/1/1 • Pull-up resistors: 88/68/52/38 • Open-drain outputs: 67/47/35/26 • 5-V tolerance: 4/4/2/2
Event link controller (ELC)		• Event signals of 47 types can be directly connected to the module • Operations of timer modules are selectable at event input • Capable of event link operation for port B
Multi-function pin controller (MPC)		Capable of selecting the input/output function from multiple pins
Timers	Multi-function timer pulse unit 2 (MTU2a)	• (16 bits × 6 channels) × 1 unit • Up to 16 pulse-input/output lines and three pulse-input lines are available based on the six 16-bit timer channels • Select from among eight or seven counter-input clock signals for each channel (PCLK/1, PCLK/4, PCLK/16, PCLK/64, PCLK/256, PCLK/1024, MTCLKA, MTCLKB, MTCLKC, MTCLKD) other than channel 5, for which only four signals are available. • Input capture function • 21 output compare/input capture registers • Pulse output mode • Complementary PWM output mode • Reset synchronous PWM mode • Phase-counting mode • Capable of generating conversion start triggers for the A/D converter
	Port output enable 2 (POE2a)	Controls the high-impedance state of the MTU's waveform output pins
	Compare match timer (CMT)	• (16 bits × 2 channels) × 1 unit • Select from among four clock signals (PCLK/8, PCLK/32, PCLK/128, PCLK/512)
	Independent watchdog timer (IWDTa)	• 14 bits × 1 channel • Count clock: Dedicated low-speed on-chip oscillator for the IWDT Frequency divided by 1, 16, 32, 64, 128, or 256
	Realtime clock (RTCc)*1	• Clock source: Sub-clock • Calendar count mode or binary count mode selectable • Interrupts: Alarm interrupt, periodic interrupt, and carry interrupt
	Low power timer (LPT)	• 16 bits × 1 channel • Clock source: Sub-clock, Dedicated low-speed on-chip oscillator for the IWDT Frequency divided by 2, 4, 8, 16, or 32
	8-bit timer (TMR)	• (8 bits × 2 channels) × 2 units • Seven internal clocks (PCLK/1, PCLK/2, PCLK/8, PCLK/32, PCLK/64, PCLK/1024, and PCLK/8192) and an external clock can be selected • Pulse output and PWM output with any duty cycle are available • Two channels can be cascaded and used as a 16-bit timer
Communication functions	Serial communications interfaces (SCIg, SCIh)	• 7 channels (channel 0, 1, 5, 6, 8, 9: SCIg, channel 12: SCIh) • SCIg Serial communications modes: Asynchronous, clock synchronous, and smart-card interface On-chip baud rate generator allows selection of the desired bit rate Choice of LSB-first or MSB-first transfer Average transfer rate clock can be input from TMR timers for SCI5, SCI6, and SCI12 Start-bit detection: Level or edge detection is selectable. Simple I^2C Simple SPI 9-bit transfer mode Bit rate modulation Event linking by the ELC (only on channel 5) • SCIh (The following functions are added to SCIg) Supports the serial communications protocol, which contains the start frame and information frame Supports the LIN format
	I^2C bus interface (RIICa)	• 1 channel • Communications formats: I^2C bus format/SMBus format • Master mode or slave mode selectable • Supports fast mode

1.4 Pin Functions

Table 1.4 lists the pin functions.

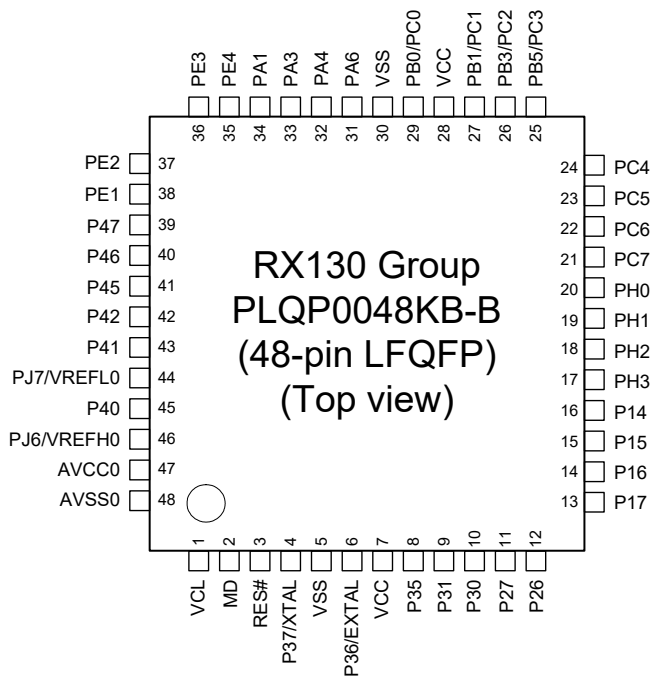
Table 1.4 Pin Functions (1/3)

Classifications	Pin Name	I/O	Description
Power supply	VCC	Input	Power supply pin. Connect it to the system power supply.
	VCL	—	Connect this pin to the VSS pin via the 4.7 μF smoothing capacitor used to stabilize the internal power supply. Place the capacitor close to the pin.
	VSS	Input	Ground pin. Connect it to the system power supply (0 V).
Clock	XTAL	Output	Pins for connecting a crystal. An external clock can be input through the EXTAL pin.
	EXTAL	Input	
	XCIN	Input	Input/output pins for the sub-clock oscillator. Connect a crystal between XCIN and XCOUT.
	XCOUT	Output	
	CLKOUT	Output	Clock output pin.
Operating mode control	MD	Input	Pin for setting the operating mode. The signal levels on this pin must not be changed during operation.
System control	RES#	Input	Reset pin. This MCU enters the reset state when this signal goes low.
CAC	CACREF	Input	Input pin for the clock frequency accuracy measurement circuit.
On-chip emulator	FINED	I/O	FINE interface pin.
Interrupts	NMI	Input	Non-maskable interrupt request pin.
	IRQ0 to IRQ7	Input	Interrupt request pins.
Multi-function timer pulse unit 2	MTIOC0A, MTIOC0B, MTIOC0C, MTIOC0D	I/O	The TGRA0 to TGRD0 input capture input/output compare output/PWM output pins.
	MTIOC1A, MTIOC1B	I/O	The TGRA1 and TGRB1 input capture input/output compare output/PWM output pins.
	MTIOC2A, MTIOC2B	I/O	The TGRA2 and TGRB2 input capture input/output compare output/PWM output pins.
	MTIOC3A, MTIOC3B, MTIOC3C, MTIOC3D	I/O	The TGRA3 to TGRD3 input capture input/output compare output/PWM output pins.
	MTIOC4A, MTIOC4B, MTIOC4C, MTIOC4D	I/O	The TGRA4 to TGRD4 input capture input/output compare output/PWM output pins.
	MTIC5U, MTIC5V, MTIC5W	Input	The TGRU5, TGRV5, and TGRW5 input capture input/external pulse input pins.
	MTCLKA, MTCLKB, MTCLKC, MTCLKD	Input	Input pins for the external clock.
Port output enable 2	POE0# to POE3#, POE8#	Input	Input pins for request signals to place the MTU pins in the high impedance state.
Realtime clock	RTCOUT	Output	Output pin for the 1-Hz/64-Hz clock.
8-bit timer	TMO0 to TMO3	Output	Compare match output pins.
	TMCI0 to TMCI3	Input	Input pins for the external clock to be input to the counter.
	TMRI0 to TMRI3	Input	Counter reset input pins.



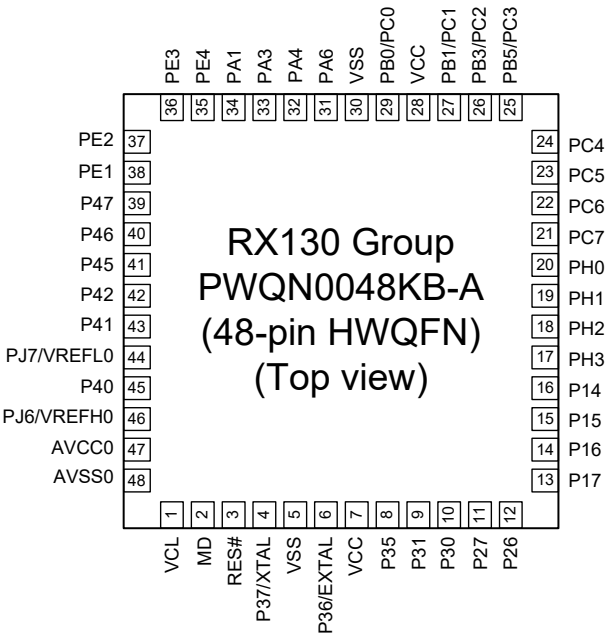
Note: This figure indicates the power supply pins and I/O ports.
For the pin configuration, see the table “List of Pins and Pin Functions (80-Pin LFQFP)”.

Figure 1.4 Pin Assignments of the 80-Pin LFQFP



Note: This figure indicates the power supply pins and I/O ports.
For the pin configuration, see the table “List of Pins and Pin Functions (48-Pin LFQFP/ HWQFN)”.

Figure 1.6 Pin Assignments of the 48-Pin LQFP



Note: It is recommended to connect an exposed die pad to VSS.
Note: This figure indicates the power supply pins and I/O ports.
For the pin configuration, see the table “List of Pins and Pin Functions (48-Pin LFQFP/ HWQFN)”.

Figure 1.7 Pin Assignments of the 48-Pin HWQFN

2.1 General-Purpose Registers (R0 to R15)

This CPU has 16 general-purpose registers (R0 to R15). R0 to R15 can be used as data registers or address registers. R0, a general-purpose register, also functions as the stack pointer (SP). The stack pointer is switched to operate as the interrupt stack pointer (ISP) or user stack pointer (USP) by the value of the stack pointer select bit (U) in the processor status word (PSW).

2.2 Control Registers

(1) Interrupt Stack Pointer (ISP)/User Stack Pointer (USP)

The stack pointer (SP) can be either of two types, the interrupt stack pointer (ISP) or the user stack pointer (USP). Whether the stack pointer operates as the ISP or USP depends on the value of the stack pointer select bit (U) in the processor status word (PSW).
Set the ISP or USP to a multiple of 4, as this reduces the numbers of cycles required to execute interrupt sequences and instructions entailing stack manipulation.

(2) Interrupt Table Register (INTB)

The interrupt table register (INTB) specifies the address where the relocatable vector table starts.

(3) Program Counter (PC)

The program counter (PC) indicates the address of the instruction being executed.

(4) Processor Status Word (PSW)

The processor status word (PSW) indicates the results of instruction execution or the state of the CPU.

(5) Backup PC (BPC)

The backup PC (BPC) is provided to speed up response to interrupts.
After a fast interrupt has been generated, the contents of the program counter (PC) are saved in the BPC register.

(6) Backup PSW (BPSW)

The backup PSW (BPSW) is provided to speed up response to interrupts.
After a fast interrupt has been generated, the contents of the processor status word (PSW) are saved in the BPSW. The allocation of bits in the BPSW corresponds to that in the PSW.

(7) Fast Interrupt Vector Register (FINTV)

The fast interrupt vector register (FINTV) is provided to speed up response to interrupts.
The FINTV register specifies a branch destination address when a fast interrupt has been generated.

2.3 Register Associated with DSP Instructions

(1) Accumulator (ACC)

The accumulator (ACC) is a 64-bit register used for DSP instructions. The accumulator is also used for the multiply and multiply-and-accumulate instructions; EMUL, EMULU, MUL, and RMPA, in which case the prior value in the accumulator is modified by execution of the instruction.
Use the MVTACHI and MVTACLO instructions for writing to the accumulator. The MVTACHI and MVTACLO instructions write data to the higher-order 32 bits (bits 63 to 32) and the lower-order 32 bits (bits 31 to 0), respectively.
Use the MVFACHI and MVFACMI instructions for reading data from the accumulator. The MVFACHI and MVFACMI instructions read data from the higher-order 32 bits (bits 63 to 32) and the middle 32 bits (bits 47 to 16), respectively.

Table 4.1 List of I/O Registers (Address Order) (13 / 18)

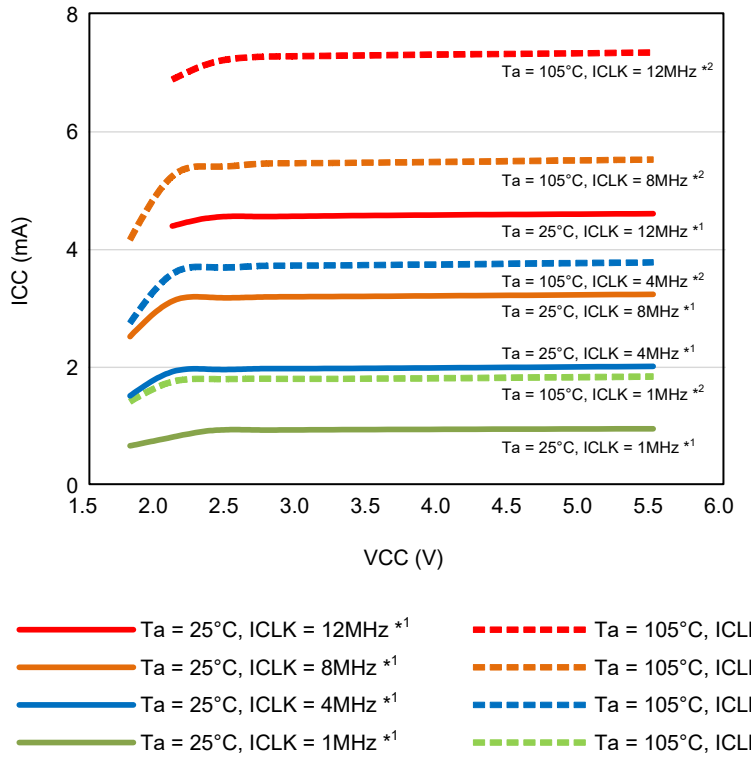
Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles
0008 C065h	PORT5	Port Mode Register	PMR	8	8	2 or 3 PCLKB
0008 C06Ah	PORTA	Port Mode Register	PMR	8	8	2 or 3 PCLKB
0008 C06Bh	PORTB	Port Mode Register	PMR	8	8	2 or 3 PCLKB
0008 C06Ch	PORTC	Port Mode Register	PMR	8	8	2 or 3 PCLKB
0008 C06Dh	PORTD	Port Mode Register	PMR	8	8	2 or 3 PCLKB
0008 C06Eh	PORTE	Port Mode Register	PMR	8	8	2 or 3 PCLKB
0008 C071h	PORTH	Port Mode Register	PMR	8	8	2 or 3 PCLKB
0008 C072h	PORTJ	Port Mode Register	PMR	8	8	2 or 3 PCLKB
0008 C082h	PORT1	Open Drain Control Register 0	ODR0	8	8	2 or 3 PCLKB
0008 C083h	PORT1	Open Drain Control Register 1	ODR1	8	8	2 or 3 PCLKB
0008 C084h	PORT2	Open Drain Control Register 0	ODR0	8	8	2 or 3 PCLKB
0008 C085h	PORT2	Open Drain Control Register 1	ODR1	8	8	2 or 3 PCLKB
0008 C086h	PORT3	Open Drain Control Register 0	ODR0	8	8	2 or 3 PCLKB
0008 C087h	PORT3	Open Drain Control Register 1	ODR1	8	8	2 or 3 PCLKB
0008 C094h	PORTA	Open Drain Control Register 0	ODR0	8	8	2 or 3 PCLKB
0008 C095h	PORTA	Open Drain Control Register 1	ODR1	8	8	2 or 3 PCLKB
0008 C096h	PORTB	Open Drain Control Register 0	ODR0	8	8	2 or 3 PCLKB
0008 C097h	PORTB	Open Drain Control Register 1	ODR1	8	8	2 or 3 PCLKB
0008 C098h	PORTC	Open Drain Control Register 0	ODR0	8	8	2 or 3 PCLKB
0008 C099h	PORTC	Open Drain Control Register 1	ODR1	8	8	2 or 3 PCLKB
0008 C09Ah	PORTD	Open Drain Control Register 0	ODR0	8	8	2 or 3 PCLKB
0008 C09Ch	PORTE	Open Drain Control Register 0	ODR0	8	8	2 or 3 PCLKB
0008 C0A4h	PORTJ	Open Drain Control Register 0	ODR0	8	8	2 or 3 PCLKB
0008 C0C0h	PORT0	Pull-Up Control Register	PCR	8	8	2 or 3 PCLKB
0008 C0C1h	PORT1	Pull-Up Control Register	PCR	8	8	2 or 3 PCLKB
0008 C0C2h	PORT2	Pull-Up Control Register	PCR	8	8	2 or 3 PCLKB
0008 C0C3h	PORT3	Pull-Up Control Register	PCR	8	8	2 or 3 PCLKB
0008 C0C4h	PORT4	Pull-Up Control Register	PCR	8	8	2 or 3 PCLKB
0008 C0C5h	PORT5	Pull-Up Control Register	PCR	8	8	2 or 3 PCLKB
0008 C0CAh	PORTA	Pull-Up Control Register	PCR	8	8	2 or 3 PCLKB
0008 C0CBh	PORTB	Pull-Up Control Register	PCR	8	8	2 or 3 PCLKB
0008 C0CCh	PORTC	Pull-Up Control Register	PCR	8	8	2 or 3 PCLKB
0008 C0CDh	PORTD	Pull-Up Control Register	PCR	8	8	2 or 3 PCLKB
0008 C0CEh	PORTE	Pull-Up Control Register	PCR	8	8	2 or 3 PCLKB
0008 C0D1h	PORTH	Pull-Up Control Register	PCR	8	8	2 or 3 PCLKB
0008 C0D2h	PORTJ	Pull-Up Control Register	PCR	8	8	2 or 3 PCLKB
0008 C0E1h	PORT1	Drive Capacity Control Register	DSCR	8	8	2 or 3 PCLKB
0008 C0E2h	PORT2	Drive Capacity Control Register	DSCR	8	8	2 or 3 PCLKB
0008 C0E3h	PORT3	Drive Capacity Control Register	DSCR	8	8	2 or 3 PCLKB
0008 C0E5h	PORT5	Drive Capacity Control Register	DSCR	8	8	2 or 3 PCLKB
0008 C0EAh	PORTA	Drive Capacity Control Register	DSCR	8	8	2 or 3 PCLKB
0008 C0EBh	PORTB	Drive Capacity Control Register	DSCR	8	8	2 or 3 PCLKB
0008 C0ECh	PORTC	Drive Capacity Control Register	DSCR	8	8	2 or 3 PCLKB
0008 C0EDh	PORTD	Drive Capacity Control Register	DSCR	8	8	2 or 3 PCLKB
0008 C0EEh	PORTE	Drive Capacity Control Register	DSCR	8	8	2 or 3 PCLKB
0008 C0F1h	PORTH	Drive Capacity Control Register	DSCR	8	8	2 or 3 PCLKB
0008 C0F2h	PORTJ	Drive Capacity Control Register	DSCR	8	8	2 or 3 PCLKB
0008 C11Fh	MPC	Write-Protect Register	PWPR	8	8	2 or 3 PCLKB
0008 C120h	PORT	Port Switching Register B	PSRB	8	8	2 or 3 PCLKB
0008 C121h	PORT	Port Switching Register A	PSRA	8	8	2 or 3 PCLKB
0008 C143h	MPC	P03 Pin Function Control Register	P03PFS	8	8	2 or 3 PCLKB
0008 C145h	MPC	P05 Pin Function Control Register	P05PFS	8	8	2 or 3 PCLKB

[Products with 128 Kbytes of flash memory or less (except for 100-pin packages)]

Table 5.7 DC Characteristics (5)

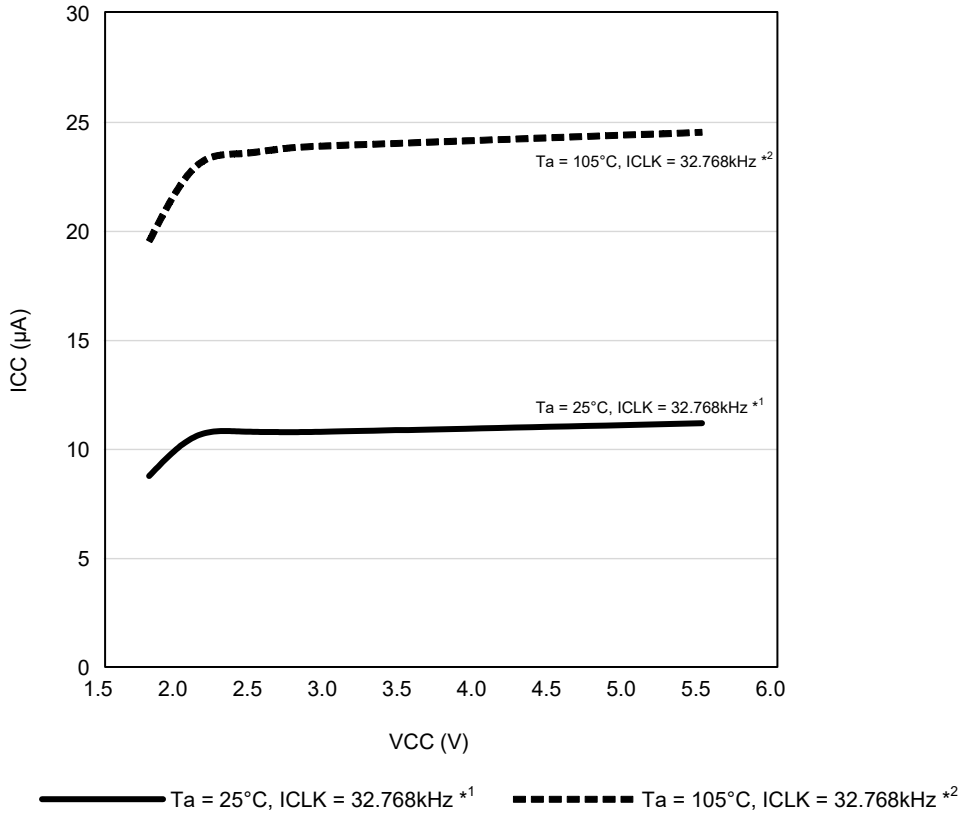
Conditions: 1.8 V ≤ VCC = AVCC0 < 2.0 V, 2.0 V ≤ VCC ≤ 5.5 V, 2.0 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, Ta = –40 to +105°C

Item					Symbol	Typ.	Max.	Unit	Test Conditions
Supply current*1	High-speed operating mode	Normal operating mode	No peripheral operation*2	ICLK = 32MHz	I_{CC}	3.1	—	mA	
				ICLK = 16MHz		2.1	—		
				ICLK = 8MHz		1.6	—		
			All peripheral operation: Normal*3	ICLK = 32MHz		10.0	—		
				ICLK = 16MHz		5.7	—		
				ICLK = 8MHz		3.5	—		
			All peripheral operation: Max.*3	ICLK = 32MHz		—	17.5		
		Sleep mode	No peripheral operation*2	ICLK = 32MHz		1.6	—		
				ICLK = 16MHz		1.2	—		
				ICLK = 8MHz		1.1	—		
			All peripheral operation: Normal*3	ICLK = 32MHz		5.3	—		
				ICLK = 16MHz		3.2	—		
				ICLK = 8MHz		2.0	—		
		Deep sleep mode	No peripheral operation*2	ICLK = 32MHz		1.0	—		
				ICLK = 16MHz		0.9	—		
				ICLK = 8MHz		0.8	—		
			All peripheral operation: Normal*3	ICLK = 32MHz		4.2	—		
				ICLK = 16MHz		2.5	—		
				ICLK = 8MHz		1.7	—		
		Increase during flash rewrite*5				2.5	—		
	Middle-speed operating modes	Normal operating mode	No peripheral operation*6	ICLK = 12MHz	I_{CC}	1.9	—	mA	
				ICLK = 8MHz		1.2	—		
				ICLK = 4MHz		0.6	—		
				ICLK = 1MHz		0.3	—		
			All peripheral operation: Normal*7	ICLK = 12MHz		4.6	—		
				ICLK = 8MHz		3.2	—		
				ICLK = 4MHz		2.0	—		
				ICLK = 1MHz		0.9	—		
			All peripheral operation: Max.*7	ICLK = 12MHz		—	8.2		
		Sleep mode	No peripheral operation*6	ICLK = 12MHz	I_{CC}	1.2	—	mA	
				ICLK = 8MHz		0.8	—		
				ICLK = 4MHz		0.3	—		
				ICLK = 1MHz		0.2	—		
			All peripheral operation: Normal*7	ICLK = 12MHz		2.7	—		
				ICLK = 8MHz		1.9	—		
				ICLK = 4MHz		1.2	—		
				ICLK = 1MHz		0.7	—		



Note 1. All peripheral operation is normal. This does not include BGO operation. Average value of the tested middle samples during product evaluation.
Note 2. All peripheral operation is maximum. This does not include BGO operation. Average value of the tested upper-limit samples during product evaluation.

Figure 5.2 Voltage Dependency in Middle-Speed Operating Mode (Reference Data)



Note 1. All peripheral operation is normal. This does not include BGO operation. Average value of the tested middle samples during product evaluation.
Note 2. All peripheral operation is maximum. This does not include BGO operation. Average value of the tested upper-limit samples during product evaluation.

Figure 5.3 Voltage Dependency in Low-Speed Operating Mode (Reference Data)

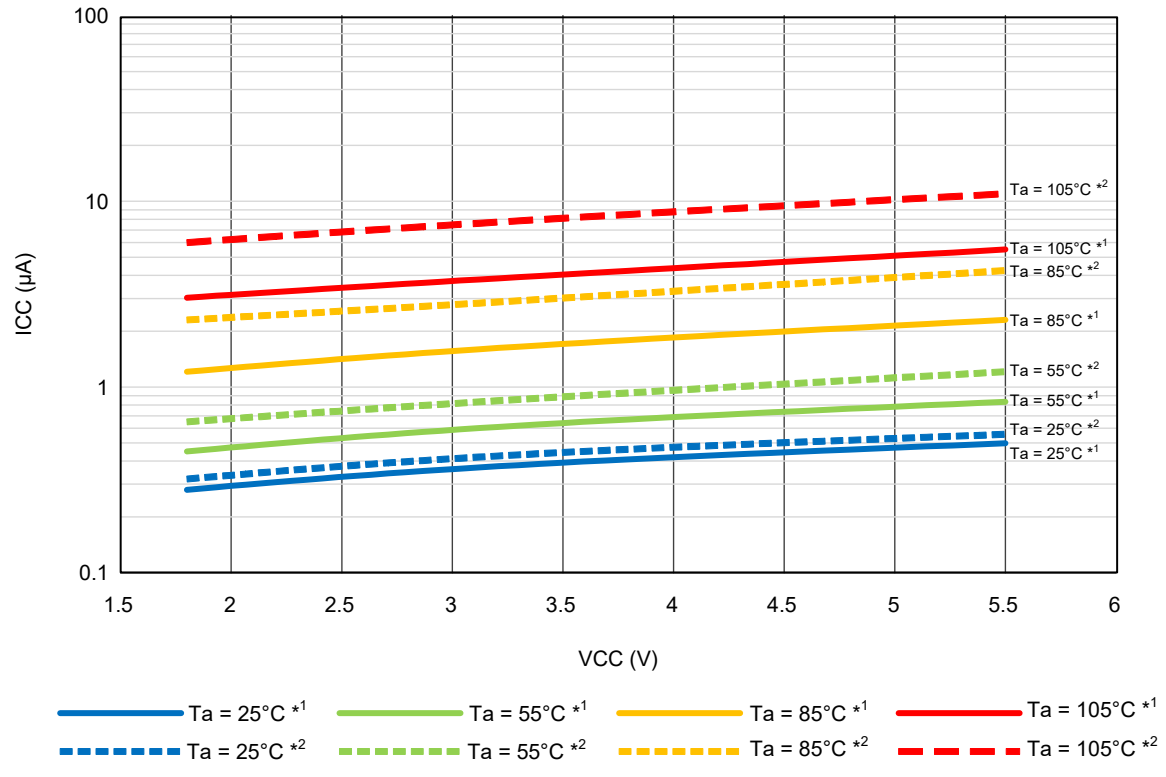
[Products with 128 Kbytes of flash memory or less (except for 100-pin packages)]

Table 5.9 DC Characteristics (6)

Conditions: 1.8 V ≤ VCC = AVCC0 < 2.0 V, 2.0 V ≤ VCC ≤ 5.5 V, 2.0 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, Ta = –40 to +105°C

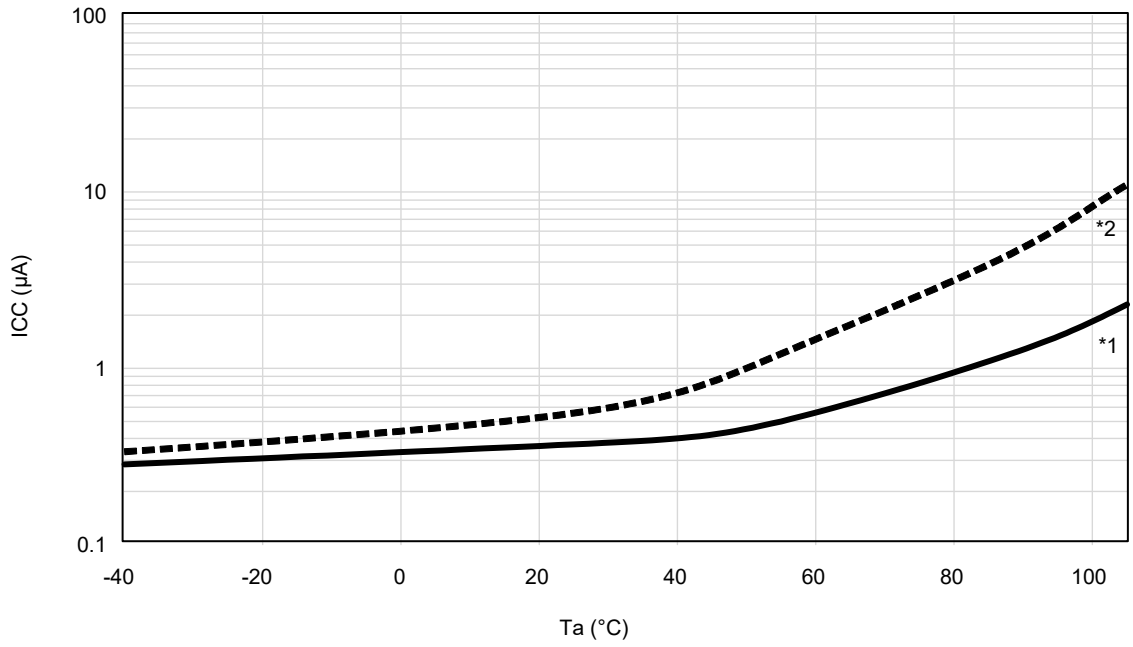
Item			Symbol	Typ.*3	Max.	Unit	Test Conditions
Supply current*1	Software standby mode*2	T_a = 25°C	I_{CC}	0.37	0.71	μA	
		T_a = 55°C		0.50	1.70		
		T_a = 85°C		1.20	8.00		
		T_a = 105°C		2.30	19.60		
	Increment for RTC operation*4			0.40	—		RCR3.RTCDV[2:0] set to low drive capacity
				1.21	—		RCR3.RTCDV[2:0] set to normal drive capacity
	Increment for low-power timer operation			0.37	—		LPTCR1.LPCNTCKSEL set to IWDT-dedicated on-chip oscillator
	Increment for Independent Watchdog Timer operation			0.37	—		

Note 1. Supply current values are with all output pins unloaded and all input pull-up MOSs in the off state.
Note 2. The IWDT, LVD, and CMPB are stopped.
Note 3. VCC = 3.3 V.
Note 4. Includes the oscillation circuit.



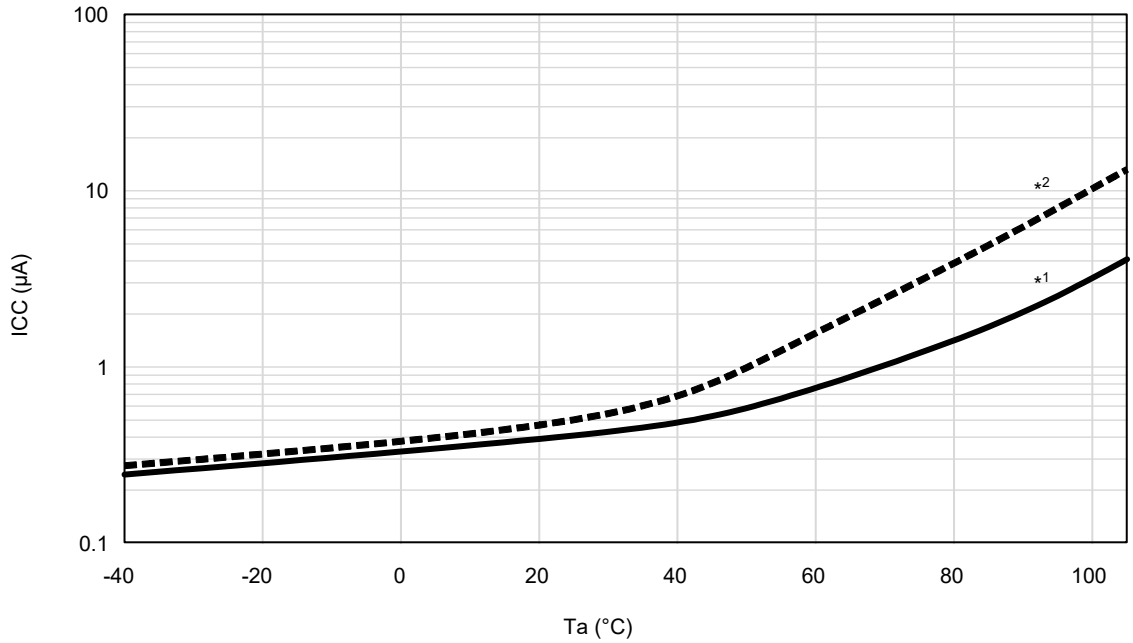
Note 1. Average value of the tested middle samples during product evaluation.
Note 2. Average value of the tested upper-limit samples during product evaluation.

Figure 5.7 Voltage Dependency in Software Standby Mode (Reference Data)



Note 1. Average value of the tested middle samples during product evaluation.
Note 2. Average value of the tested upper-limit samples during product evaluation.

Figure 5.8 Temperature Dependency in Software Standby Mode (Reference Data)



Note 1. Average value of the tested middle samples during product evaluation.
Note 2. Average value of the tested upper-limit samples during product evaluation.

Figure 5.10 Temperature Dependency in Software Standby Mode (Reference Data)

Table 5.11 DC Characteristics (7)

Conditions: 1.8 V ≤ VCC = AVCC0 < 2.0 V, 2.0 V ≤ VCC ≤ 5.5 V, 2.0 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V

Item	Symbol	Typ.	Max.	Unit	Test Conditions
Permissible total power consumption*1	P_d	—	300	mW	D version
		—	105		G version

Note: Please contact a Renesas Electronics sales office for information on the derating of the G-version product. Derating is the systematic reduction of load to improve reliability.
Note 1. Total power dissipated by the entire chip (including output currents)

Table 5.19 Output Values of Voltage (1)

Conditions: 1.8 V ≤ VCC = AVCC0 < 2.0 V, 2.0 V ≤ VCC < 2.7 V, 2.0 V ≤ AVCC0 < 2.7 V, VSS = AVSS0 = 0 V, Ta = –40 to +105°C

Item				Symbol	Min.	Max.	Unit	Test Conditions
Output low	All output ports (except for RIIC)	Normal output mode		V_{OL}	—	0.8	V	I_{OL} = 0.5 mA
		High-drive output mode			—	0.8		I_{OL} = 1.0 mA
Output high	All output ports	Normal output mode	P03 to P07, P40 to P47, PJ6, PJ7	V_{OH}	AVCC0 – 0.5	—	V	I_{OH} = –0.5 mA
			Ports other than above		VCC – 0.5	—		
		High-drive output mode			VCC – 0.5	—		I_{OH} = –1.0 mA

Table 5.20 Output Values of Voltage (2)

Conditions: 2.7 V ≤ VCC < 4.0 V, 2.7 V ≤ AVCC0 < 4.0 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item				Symbol	Min.	Max.	Unit	Test Conditions
Output low	All output ports (except for RIIC)	Normal output mode		V_{OL}	—	0.8	V	I_{OL} = 1.0 mA
		High-drive output mode			—	0.8		I_{OL} = 2.0 mA
	RIIC pins	Standard mode (Normal output mode)			—	0.4		I_{OL} = 3.0 mA
		Fast mode (High-drive output mode)			—	0.4		I_{OL} = 6.0 mA
Output high	All output ports	Normal output mode	P03 to P07, P40 to P47, PJ6, PJ7	V_{OH}	AVCC0 – 0.8	—	V	I_{OH} = –1.0 mA
			Ports other than above		VCC – 0.8	—		
		High-drive output mode			VCC – 0.8	—		I_{OH} = –2.0 mA

Table 5.21 Output Values of Voltage (3)

Conditions: 4.0 V ≤ VCC ≤ 5.5 V, 4.0 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item				Symbol	Min.	Max.	Unit	Test Conditions
Output low	All output ports (except for RIIC)	Normal output mode		V_{OL}	—	0.8	V	I_{OL} = 2.0 mA
		High-drive output mode			—	0.8		I_{OL} = 4.0 mA
	RIIC pins	Standard mode (Normal output mode)			—	0.4		I_{OL} = 3.0 mA
		Fast mode (High-drive output mode)			—	0.6		I_{OL} = 6.0 mA
Output high	All output ports	Normal output mode	P03 to P07, P40 to P47, PJ6, PJ7	V_{OH}	AVCC0 – 0.8	—	V	I_{OH} = –2.0 mA
			Ports other than above		VCC – 0.8	—		
		High-drive output mode			VCC – 0.8	—		I_{OH} = –4.0 mA

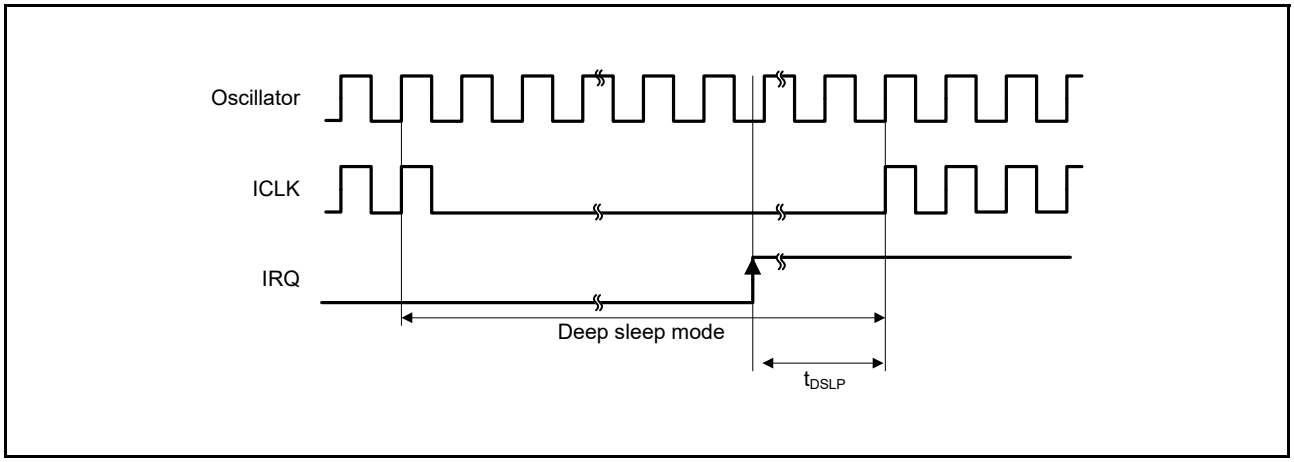


Figure 5.38 Deep Sleep Mode Recovery Timing

Table 5.31 Operating Mode Transition Time

Conditions: 1.8 V ≤ VCC = AVCC0 < 2.0 V, 2.0 V ≤ VCC ≤ 5.5 V, 2.0 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, Ta = –40 to +105°C

Mode before Transition	Mode after Transition	ICLK Frequency	Transition Time			Unit
			Min.	Typ.	Max.	
High-speed operating mode	Middle-speed operating modes	8 MHz	—	10	—	µs
Middle-speed operating modes	High-speed operating mode	8 MHz	—	37.5	—	µs
Low-speed operating mode	Middle-speed operating mode, high-speed operating mode	32.768 kHz	—	215	—	µs
Middle-speed operating mode, high-speed operating mode	Low-speed operating mode	32.768 kHz	—	185	—	µs

Note: Values when the frequencies of PCLKB, PCLKD, and FCLK are not divided.

Table 5.34 Timing of On-Chip Peripheral Modules (2)

Conditions: 1.8 V ≤ VCC = AVCC0 < 2.0 V, 2.0 V ≤ VCC ≤ 5.5 V, 2.0 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, Ta = –40 to +105°C, C = 30 pF, when high-drive output is selected by the drive capacity register

Item				Symbol	Min.	Max.	Unit	Test Conditions
RSPI	RSPCK clock cycle	Master		t_{SPcyc}	2	4096	t_{Pcyc}*1	Figure 5.50
		Slave			8	—		
	RSPCK clock high pulse width	Master		t_{SPCKWH}	$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf})/2 - 3$	—	ns	
		Slave			$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf})/2$	—		
	RSPCK clock low pulse width	Master		t_{SPCKWL}	$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf})/2 - 3$	—	ns	
		Slave			$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf})/2$	—		
	RSPCK clock rise/ fall time	Output	2.7 V or above	t_{SPCKr}, t_{SPCKf}	—	10	ns	
			1.8 V or above		—	15		
		Input			—	0.1	μs/V	
	Data input setup time	Master	2.7 V or above	t_{SU}	10	—	ns	Figure 5.51 to Figure 5.54
			1.8 V or above		30	—		
		Slave			$25 - t_{Pcyc}$	—		
	Data input hold time	Master	RSPCK set to a division ratio other than PCLKB divided by 2	t_H	t_{Pcyc}	—	ns	
			RSPCK set to PCLKB divided by 2	t_{HF}	0	—		
		Slave		t_H	$20 + 2 \times t_{Pcyc}$	—		
	SSL setup time	Master		t_{LEAD}	$–30 + N^{*2} \times t_{SPcyc}$	—	ns	
		Slave			2	—	t_{Pcyc}	
	SSL hold time	Master		t_{LAG}	$–30 + N^{*3} \times t_{SPcyc}$	—	ns	
		Slave			2	—	t_{Pcyc}	
	Data output delay time	Master	2.7 V or above	t_{OD}	—	14	ns	
			1.8 V or above		—	30		
		Slave	2.7 V or above		—	$3 \times t_{Pcyc} + 65$		
			1.8 V or above		—	$3 \times t_{Pcyc} + 105$		
	Data output hold time	Master		t_{OH}	0	—	ns	
		Slave			0	—		
	Successive transmission delay time	Master		t_{TD}	$t_{SPcyc} + 2 \times t_{Pcyc}$	$8 \times t_{SPcyc} + 2 \times t_{Pcyc}$	ns	
		Slave			$4 \times t_{Pcyc}$	—		
	MOSI and MISO rise/ fall time	Output	2.7 V or above	t_{Dr}, t_{Df}	—	10	ns	
			1.8 V or above		—	15		
		Input			—	1	μs	
	SSL rise/fall time	Output	2.7 V or above	t_{SSLr}, t_{SSLf}	—	10	ns	
			1.8 V or above		—	15	ns	
		Input			—	1	μs	
	Slave access time		2.7 V or above	t_{SA}	—	6	t_{Pcyc}	Figure 5.53, Figure 5.54
			1.8 V or above		—	7		
	Slave output release time		2.7 V or above	t_{REL}	—	5	t_{Pcyc}	
			1.8 V or above		—	6		

Note 1. t_{Pcyc}: PCLK cycle
Note 2. N: An integer from 1 to 8 that can be set by the RSPI clock delay register (SPCKD)
Note 3. N: An integer from 1 to 8 that can be set by the RSPI slave select negation delay register (SSLND)

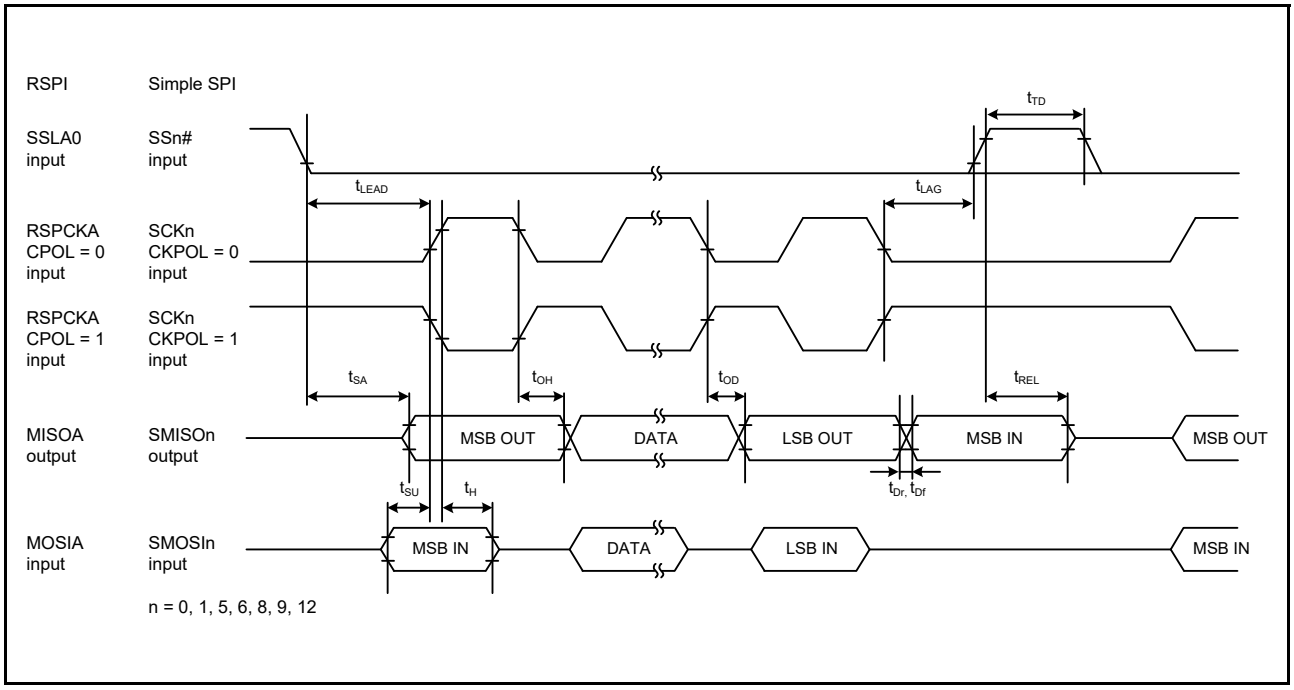


Figure 5.53 RSPI Timing (Slave, CPHA = 0) and Simple SPI Clock Timing (Slave, CKPH = 1)

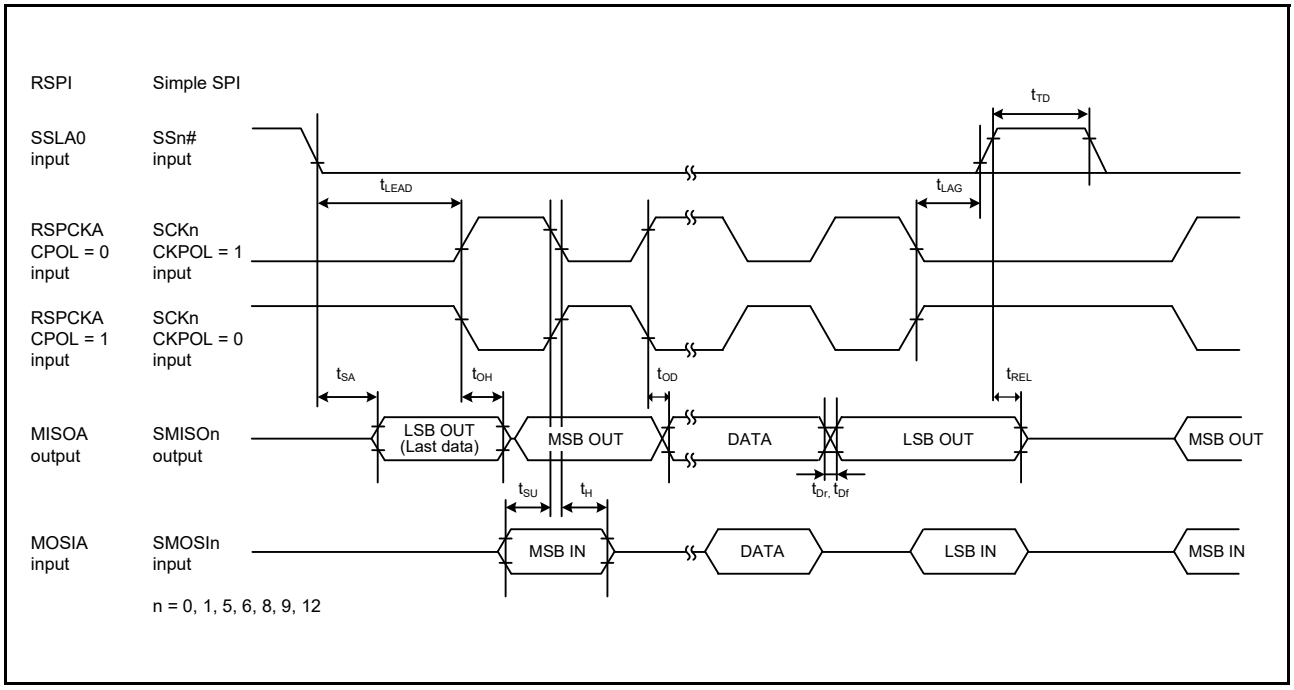


Figure 5.54 RSPI Timing (Slave, CPHA = 1) and Simple SPI Clock Timing (Slave, CKPH = 0)

Table 5.50 Power-On Reset Circuit and Voltage Detection Circuit Characteristics (2)

Conditions: 1.8 V ≤ VCC = AVCC0 < 2.0 V, 2.0 V ≤ VCC ≤ 5.5 V, 2.0 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Wait time after power-on reset cancellation	At normal startup*1	t_{POR}	—	9.1	—	ms	Figure 5.62
	During fast startup time*2	t_{POR}	—	1.6	—		
Wait time after voltage monitoring 0 reset cancellation	Power-on voltage monitoring 0 reset disabled*1	t_{LVD0}	—	568	—	µs	Figure 5.63
	Power-on voltage monitoring 0 reset enabled*2		—	100	—		
Wait time after voltage monitoring 1 reset cancellation		t_{LVD1}	—	100	—	µs	Figure 5.64
Wait time after voltage monitoring 2 reset cancellation		t_{LVD2}	—	100	—	µs	Figure 5.65
Response delay time		t_{det}	—	—	350	µs	Figure 5.61
Minimum VCC down time*3		t_{VOFF}	350	—	—	µs	Figure 5.61, VCC = 1.0 V or above
Power-on reset enable time		$t_{W(POR)}$	1	—	—	ms	Figure 5.62, VCC = below 1.0 V
LVD operation stabilization time (after LVD is enabled)		$t_{d(E-A)}$	—	—	300	µs	Figure 5.64, Figure 5.65
Hysteresis width (power-on rest (POR))		V_{PORH}	—	110	—	mV	
Hysteresis width (LVD0, LVD1, and LVD2)		V_{LVH}	—	70	—	mV	Vdet0_0 to Vdet0_3 selected
			—	70	—		Vdet1_0 to Vdet1_4 selected
			—	60	—		Vdet1_5 to 9 selected
			—	50	—		Vdet1_A to B selected
			—	40	—		Vdet1_C to D selected
			—	60	—		LVD2 selected

Note: These characteristics apply when noise is not superimposed on the power supply. When a setting is made so that the voltage detection level overlaps with that of the voltage detection circuit (LVD1), it cannot be specified which of LVD1 and LVD2 is used for voltage detection.

Note 1. When OFS1.(LVDAS, FASTSTUP) = 11b.

Note 2. When OFS1.(LVDAS, FASTSTUP) ≠ 11b.

Note 3. The minimum VCC down time indicates the time when VCC is below the minimum value of voltage detection levels V_{POR}, V_{det0}, V_{det1}, and V_{det2} for the POR/LVD.

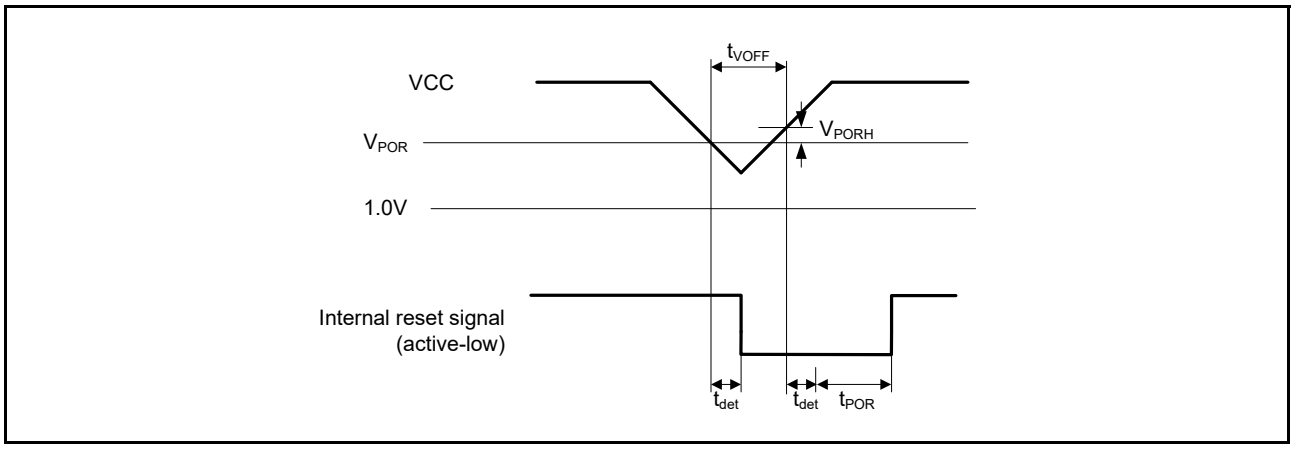


Figure 5.61 Voltage Detection Reset Timing

5.11 ROM (Flash Memory for Code Storage) Characteristics

Table 5.52 ROM (Flash Memory for Code Storage) Characteristics (1)

Item		Symbol	Min.	Typ.	Max.	Unit	Conditions
Reprogramming/erasure cycle*1		N_{PEC}	1000	—	—	Times	
Data retention	After 1000 times of N_{PEC}	t_{DRP}	20*2, *3	—	—	Year	T_a = +85°C

Note 1. Definition of reprogram/erase cycle: The reprogram/erase cycle is the number of erasing for each block. When the reprogram/erase cycle is n times (n = 1000), erasing can be performed n times for each block. For instance, when 4-byte programming is performed 256 times for different addresses in 1-Kbyte block and then the entire block is erased, the reprogram/erase cycle is counted as one. However, programming the same address for several times as one erasing is not enabled (overwriting is prohibited).
Note 2. Characteristic when using the flash memory programmer and the self-programming library provided from Renesas Electronics.
Note 3. This result is obtained from reliability testing.

Table 5.53 ROM (Flash Memory for Code Storage) Characteristics (2) High-Speed Operating Mode

Conditions: 2.7 V ≤ VCC ≤ 5.5 V, 2.7 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V

Temperature range for the programming/erasure operation: T_a = –40 to +105°C

Item		Symbol	FCLK = 1 MHz			FCLK = 32 MHz			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Programming time	4-byte	t_{P4}	—	103	931	—	52	489	µs
Erasure time	1-Kbyte	t_{E1K}	—	8.23	267	—	5.48	214	ms
	256-Kbyte	t_{E256K}	—	407	928	—	39	457	ms
Blank check time	4-byte	t_{BC4}	—	—	48	—	—	15.9	µs
	1-Kbyte	t_{BC1K}	—	—	1.58	—	—	0.127	ms
Erase operation forcible stop time		t_{SED}	—	—	21.6	—	—	12.8	µs
Start-up area switching setting time		t_{SAS}	—	12.6	543	—	6.16	432	ms
Access window setting time		t_{AWS}	—	12.6	543	—	6.16	432	ms
ROM mode transition wait time 1		t_{DIS}	2	—	—	2	—	—	µs
ROM mode transition wait time 2		t_{MS}	5	—	—	5	—	—	µs

Note: Does not include the time until each operation of the flash memory is started after instructions are executed by software.
Note: The lower-limit frequency of FCLK is 1 MHz during programming or erasing of the flash memory. When using FCLK at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.
Note: The frequency accuracy of FCLK should be ±3.5%.

REVISION HISTORY	RX130 Group Datasheet

Classifications

- Items with Technical Update document number: Changes according to the corresponding issued Technical Update
- Items without Technical Update document number: Minor changes that do not require Technical Update to be issued

Rev.	Date	Description		Classification
		Page	Summary	
1.00	Oct 30, 2015	—	First edition, issued	
2.00	Sep 01, 2017	All	Products with at least 256 Kbytes of code flash memory and 100-pin packages added	
		4. I/O Registers		
		42	Table 4.1 List of I/O Registers (Address Order), changed	TN-RX*-A179A/E
		5. Electrical Characteristics		
		49	Table 5.2 Recommended Operating Voltage Conditions Note 3, added	
		57 to 61	The characteristics of products with at least 256 Kbytes of flash memory or 100-pin packages added	
		64, 65	The characteristics of products with at least 256 Kbytes of flash memory or 100-pin packages added	
		90	Table 5.34 Timing of On-Chip Peripheral Modules (2), changed	TN-RX*-A179A/E
		91	Table 5.35 Timing of On-Chip Peripheral Modules (3), changed	
		93	Table 5.38 Timing of On-Chip Peripheral Modules (6), added	
		111	Table 5.48 CTSU Characteristics, item for products with at least 256 Kbytes of flash memory or 100-pin packages added	
		113	Table 5.50 Power-On Reset Circuit and Voltage Detection Circuit Characteristics (2), item with Vdet0_0 to Vdet0_3 selected added	
		117	Table 5.53 ROM (Flash Memory for Code Storage) Characteristics (2) High-Speed Operating Mode, erasure time (128-Kbyte) deleted and erasure time (256-Kbyte) added	
		118	Table 5.54 ROM (Flash Memory for Code Storage) Characteristics (3) Middle-Speed Operating Mode, erasure time (128-Kbyte) deleted and erasure time (256-Kbyte) added	

NOTES FOR CMOS DEVICES

(1) VOLTAGE APPLICATION WAVEFORM AT INPUT PIN: Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between VIL (MAX) and VIH (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between VIL (MAX) and VIH (MIN).

(2) HANDLING OF UNUSED INPUT PINS: Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to VDD or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.

(3) PRECAUTION AGAINST ESD: A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.

(4) STATUS BEFORE INITIALIZATION: Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.

(5) POWER ON/OFF SEQUENCE: In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current. The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.

(6) INPUT OF SIGNAL DURING POWER OFF STATE : Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.