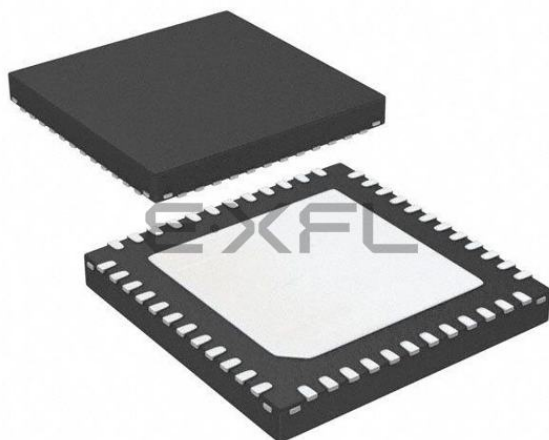




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Details

Product Status	Not For New Designs
Core Processor	RX
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	I ² C, LINbus, SCI, SPI
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	38
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	8K x 8
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 10x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-WFQFN Exposed Pad
Supplier Device Package	48-HWQFN (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f51305adne-u0

1.4 Pin Functions

Table 1.4 lists the pin functions.

Table 1.4 Pin Functions (1/3)

Classifications	Pin Name	I/O	Description
Power supply	VCC	Input	Power supply pin. Connect it to the system power supply.
	VCL	—	Connect this pin to the VSS pin via the 4.7 μ F smoothing capacitor used to stabilize the internal power supply. Place the capacitor close to the pin.
	VSS	Input	Ground pin. Connect it to the system power supply (0 V).
Clock	XTAL	Output	Pins for connecting a crystal. An external clock can be input through the EXTAL pin.
	EXTAL	Input	
	XCIN	Input	Input/output pins for the sub-clock oscillator. Connect a crystal between XCIN and XCOUT.
	XCOUT	Output	
	CLKOUT	Output	Clock output pin.
Operating mode control	MD	Input	Pin for setting the operating mode. The signal levels on this pin must not be changed during operation.
System control	RES#	Input	Reset pin. This MCU enters the reset state when this signal goes low.
CAC	CACREF	Input	Input pin for the clock frequency accuracy measurement circuit.
On-chip emulator	FINED	I/O	FINE interface pin.
Interrupts	NMI	Input	Non-maskable interrupt request pin.
	IRQ0 to IRQ7	Input	Interrupt request pins.
Multi-function timer pulse unit 2	MTIOC0A, MTIOC0B, MTIOC0C, MTIOC0D	I/O	The TGRA0 to TGRD0 input capture input/output compare output/PWM output pins.
	MTIOC1A, MTIOC1B	I/O	The TGRA1 and TGRB1 input capture input/output compare output/PWM output pins.
	MTIOC2A, MTIOC2B	I/O	The TGRA2 and TGRB2 input capture input/output compare output/PWM output pins.
	MTIOC3A, MTIOC3B, MTIOC3C, MTIOC3D	I/O	The TGRA3 to TGRD3 input capture input/output compare output/PWM output pins.
	MTIOC4A, MTIOC4B, MTIOC4C, MTIOC4D	I/O	The TGRA4 to TGRD4 input capture input/output compare output/PWM output pins.
	MTIC5U, MTIC5V, MTIC5W	Input	The TGRU5, TGRV5, and TGRW5 input capture input/external pulse input pins.
	MTCLKA, MTCLKB, MTCLKC, MTCLKD	Input	Input pins for the external clock.
Port output enable 2	POE0# to POE3#, POE8#	Input	Input pins for request signals to place the MTU pins in the high impedance state.
Realtime clock	RTCOUT	Output	Output pin for the 1-Hz/64-Hz clock.
8-bit timer	TMO0 to TMO3	Output	Compare match output pins.
	TMCI0 to TMCI3	Input	Input pins for the external clock to be input to the counter.
	TMRI0 to TMRI3	Input	Counter reset input pins.

1.5 Pin Assignments

Figure 1.3 to Figure 1.7 show the pin assignments. Table 1.5 to Table 1.8 show the lists of pins and pin functions.

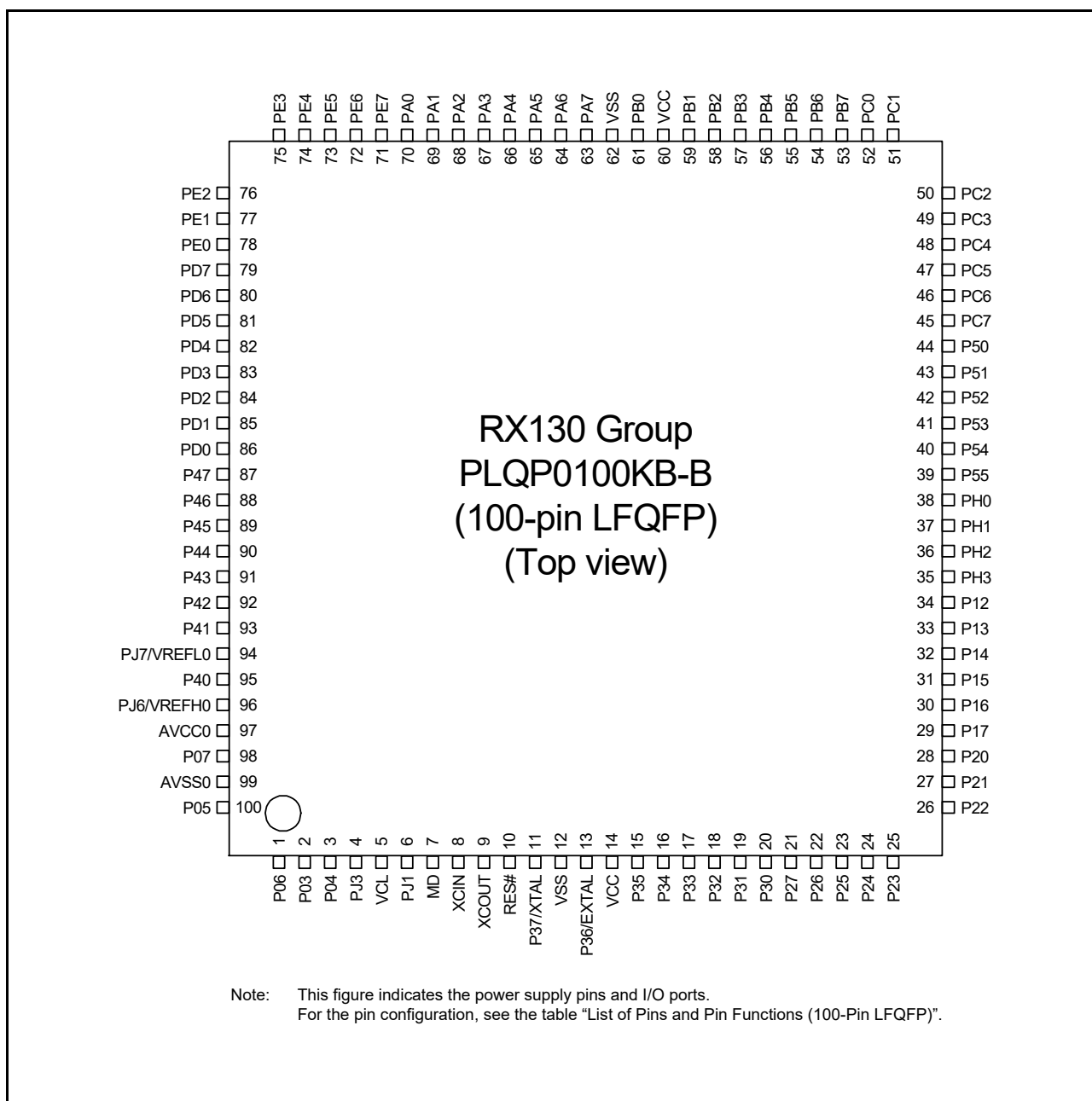


Figure 1.3 Pin Assignments of the 100-Pin LFQFP

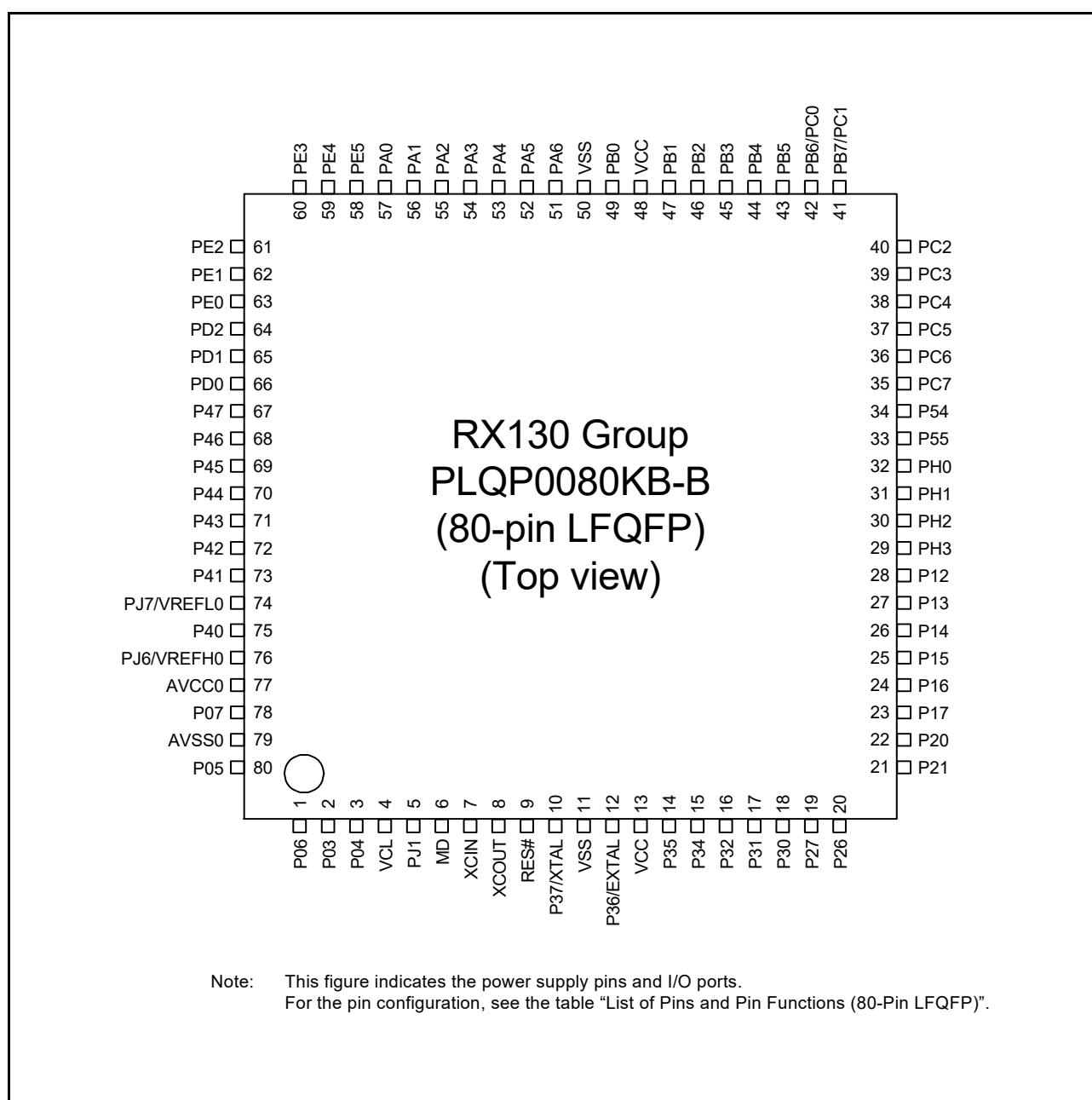
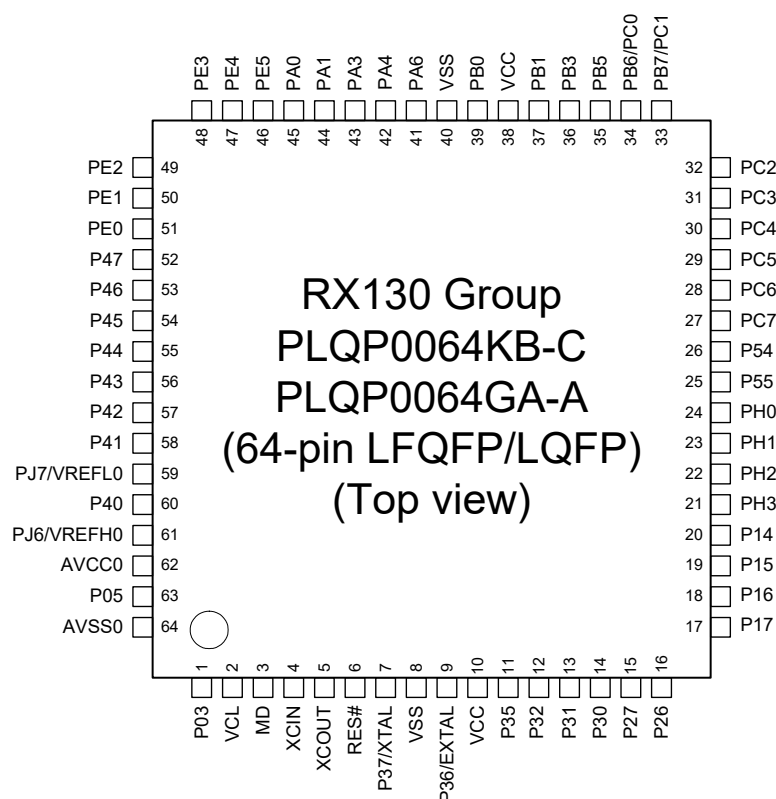


Figure 1.4 Pin Assignments of the 80-Pin LQFP



Note: This figure indicates the power supply pins and I/O ports.
 For the pin configuration, see the table "List of Pins and Pin Functions (64-Pin LFQFP/LQFP)".

Figure 1.5 Pin Assignments of the 64-Pin LFQFP/LQFP

Table 1.5 List of Pins and Pin Functions (100-Pin LFQFP) (2/2)

Pin No.	Power Supply, Clock, System Control	I/O Port	Timers (MTU, TMR, POE)	Communications (SCIg, SCIf, RSPI, IIC, REMC)	Touch sensing	Others
53		PB7	MTIOC3B	TXD9/SMOSI9/SSDA9	TS18	
54		PB6	MTIOC3D	RXD9/SMISO9/SSCL9	TS19	
55		PB5	MTIOC2A/MTIOC1B/TMRI1/POE1#	SCK9	TS20	
56		PB4		CTS9#/RTS9#/SS9#	TS21	
57		PB3	MTIOC0A/MTIOC4A/TMO0/POE3#	SCK6	TS22	
58		PB2		CTS6#/RTS6#/SS6#	TS23	
59		PB1	MTIOC0C/MTIOC4C/TMC10	TXD6/SMOSI6/SSDA6	TS24	IRQ4/CMPOB1
60	VCC					
61		PB0	MTIC5W	RXD6/SMISO6/SSCL6/RSPCKA	TS25	
62	VSS					
63		PA7		MISOA		
64		PA6	MTIC5V/MTCLKB/TMC13/POE2#	CTS5#/RTS5#/SS5#/MOSIA	TS26	
65		PA5		RSPCKA	TS27	
66		PA4	MTIC5U/MTCLKA/TMRI0	TXD5/SMOSI5/SSDA5/SSLA0	TS28	IRQ5/CVREFB1
67		PA3	MTIOC0D/MTCLKD	RXD5/SMISO5/SSCL5	TS29	IRQ6/CMPB1
68		PA2		RXD5/SMISO5/SSCL5/SSLA3	TS30	
69		PA1	MTIOC0B/MTCLKC	SCK5/SSLA2	TS31	
70		PA0	MTIOC4A	SSLA1	TS32	CACREF
71		PE7				IRQ7/AN023
72		PE6				IRQ6/AN022
73		PE5	MTIOC4C/MTIOC2B			IRQ5/AN021/CMPOB0
74		PE4	MTIOC4D/MTIOC1A		TS33	AN020/CMPA2/CLKOUT
75		PE3	MTIOC4B/POE8#	CTS12#/RTS12#/SS12#	TS34	AN019/CLKOUT
76		PE2	MTIOC4A	RXD12/RXD12/SMISO12/SSCL12	TS35	IRQ7/AN018/CVREFB0
77		PE1	MTIOC4C	TXD12/TXD12/SIOX12/SMOSI12/SSDA12		AN017/CMPB0
78		PE0		SCK12		AN016
79		PD7	MTIC5U/POE0#			IRQ7/AN031
80		PD6	MTIC5V/POE1#			IRQ6/AN030
81		PD5	MTIC5W/POE2#			IRQ5/AN029
82		PD4	POE3#			IRQ4/AN028
83		PD3	POE8#			IRQ3/AN027
84		PD2	MTIOC4D	SCK6		IRQ2/AN026
85		PD1	MTIOC4B	RXD6/SMISO6/SSCL6		IRQ1/AN025
86		PD0		TXD6/SMOSI6/SSDA6		IRQ0/AN024
87		P47*1				AN007
88		P46*1				AN006
89		P45*1				AN005
90		P44*1				AN004
91		P43*1				AN003
92		P42*1				AN002
93		P41*1				AN001
94	VREFL0	PJ7*1				
95		P40*1				AN000
96	VREFH0	PJ6*1				
97	AVCC0					
98		P07*1				ADTRG0#
99	AVSS0					
100		P05*1				DA1

Note 1. The power source of the I/O buffer for these pins is AVCC0.

Table 1.7 List of Pins and Pin Functions (64-Pin LFQFP/LQFP) (2/2)

Pin No.	Power Supply, Clock, System Control	I/O Port	Timers (MTU, TMR, POE)	Communications (SCIg, SCIf, RSPI, IIC)	Touch sensing	Others
49		PE2	MTIOC4A	RXD12/RXDX12/SMISO12/SSCL12	TS35	IRQ7/AN018/CVREFB0
50		PE1	MTIOC4C	TXD12/TXDX12/SIOX12/SMOSI12/SSDA12		AN017/CMPB0
51		PE0		SCK12		AN016
52		P47*1				AN007
53		P46*1				AN006
54		P45*1				AN005
55		P44*1				AN004
56		P43*1				AN003
57		P42*1				AN002
58		P41*1				AN001
59	VREFL0	PJ7*1				
60		P40*1				AN000
61	VREFH0	PJ6*1				
62	AVCC0					
63		P05*1				DA1
64	AVSS0					

Note 1. The power source of the I/O buffer for these pins is AVCC0.

Note 2. PC0 and PC1 are valid only when the port switching function is selected.

4.1 I/O Register Addresses (Address Order)

Table 4.1 List of I/O Registers (Address Order) (1 / 18)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles
0008 0000h	SYSTEM	Mode Monitor Register	MDMONR	16	16	3 ICLK
0008 0008h	SYSTEM	System Control Register 1	SYSCR1	16	16	3 ICLK
0008 000Ch	SYSTEM	Standby Control Register	SBYCR	16	16	3 ICLK
0008 0010h	SYSTEM	Module Stop Control Register A	MSTPCRA	32	32	3 ICLK
0008 0014h	SYSTEM	Module Stop Control Register B	MSTPCRB	32	32	3 ICLK
0008 0018h	SYSTEM	Module Stop Control Register C	MSTPCRC	32	32	3 ICLK
0008 001Ch	SYSTEM	Module Stop Control Register D	MSTPCRD	32	32	3 ICLK
0008 0020h	SYSTEM	System Clock Control Register	SCKCR	32	32	3 ICLK
0008 0026h	SYSTEM	System Clock Control Register 3	SCKCR3	16	16	3 ICLK
0008 0028h	SYSTEM	PLL Control Register	PLLCR	16	16	3 ICLK
0008 002Ah	SYSTEM	PLL Control Register 2	PLLCR2	8	8	3 ICLK
0008 0032h	SYSTEM	Main Clock Oscillator Control Register	MOSCCR	8	8	3 ICLK
0008 0033h	SYSTEM	Sub-Clock Oscillator Control Register	SOSCCR	8	8	3 ICLK
0008 0034h	SYSTEM	Low-Speed On-Chip Oscillator Control Register	LOCOCR	8	8	3 ICLK
0008 0035h	SYSTEM	IWDT-Dedicated On-Chip Oscillator Control Register	ILOCOCR	8	8	3 ICLK
0008 0036h	SYSTEM	High-Speed On-Chip Oscillator Control Register	HOCOCR	8	8	3 ICLK
0008 003Ch	SYSTEM	Oscillation Stabilization Flag Register	OSCOVFSR	8	8	3 ICLK
0008 003Dh	SYSTEM	High-Speed On-Chip Oscillator Forced Oscillation Control Register	HOFCR	8	8	3 ICLK
0008 003Eh	SYSTEM	CLKOUT Output Control Register	CKOCR	16	16	3 ICLK
0008 0040h	SYSTEM	Oscillation Stop Detection Control Register	OSTDCR	8	8	3 ICLK
0008 0041h	SYSTEM	Oscillation Stop Detection Status Register	OSTDSR	8	8	3 ICLK
0008 0060h	SYSTEM	Low-Speed On-Chip Oscillator Trimming Register	LOCOTRR	8	8	3 ICLK
0008 0064h	SYSTEM	IWDT-Dedicated On-Chip Oscillator Trimming Register	ILOCOTRR	8	8	3 ICLK
0008 0068h	SYSTEM	High-Speed On-Chip Oscillator Trimming Register 0	HOCOTRR0	8	8	3 ICLK
0008 00A0h	SYSTEM	Operating Power Control Register	OPCCR	8	8	3 ICLK
0008 00A1h	SYSTEM	Sleep Mode Return Clock Source Switching Register	RSTCKCR	8	8	3 ICLK
0008 00A2h	SYSTEM	Main Clock Oscillator Wait Control Register	MOSCWTCR	8	8	3 ICLK
0008 00AAh	SYSTEM	Sub Operating Power Control Register	SOPCCR	8	8	3 ICLK
0008 00B0h	LPT	Low-Power Timer Control Register 1	LPTCR1	8	8	3 ICLK
0008 00B1h	LPT	Low-Power Timer Control Register 2	LPTCR2	8	8	3 ICLK
0008 00B2h	LPT	Low-Power Timer Control Register 3	LPTCR3	8	8	3 ICLK
0008 00B4h	LPT	Low-Power Timer Cycle Setting Register	LPTPRD	16	16	3 ICLK
0008 00B8h	LPT	Low-Power Timer Compare Register 0	LPCMR0	16	16	3 ICLK
0008 00BCh	LPT	Low-Power Timer Standby Wakeup Enable Register	LPWUCR	16	16	3 ICLK
0008 00C0h	SYSTEM	Reset Status Register 2	RSTSR2	8	8	3 ICLK
0008 00C2h	SYSTEM	Software Reset Register	SWRR	16	16	3 ICLK
0008 00E0h	SYSTEM	Voltage Monitoring 1 Circuit Control Register 1	LVD1CR1	8	8	3 ICLK
0008 00E1h	SYSTEM	Voltage Monitoring 1 Circuit Status Register	LVD1SR	8	8	3 ICLK
0008 00E2h	SYSTEM	Voltage Monitoring 2 Circuit Control Register 1	LVD2CR1	8	8	3 ICLK
0008 00E3h	SYSTEM	Voltage Monitoring 2 Circuit Status Register	LVD2SR	8	8	3 ICLK
0008 03FEh	SYSTEM	Protect Register	PRCR	16	16	3 ICLK
0008 1300h	BSC	Bus Error Status Clear Register	BERCLR	8	8	2 ICLK
0008 1304h	BSC	Bus Error Monitoring Enable Register	BEREN	8	8	2 ICLK
0008 1308h	BSC	Bus Error Status Register 1	BERSR1	8	8	2 ICLK
0008 130Ah	BSC	Bus Error Status Register 2	BERSR2	16	16	2 ICLK
0008 1310h	BSC	Bus Priority Control Register	BUSPRI	16	16	2 ICLK
0008 2400h	DTC	DTC Control Register	DTCCR	8	8	2 ICLK
0008 2404h	DTC	DTC Vector Base Register	DTCVBR	32	32	2 ICLK
0008 2408h	DTC	DTC Address Mode Register	DTCADMOD	8	8	2 ICLK

Table 4.1 List of I/O Registers (Address Order) (11 / 18)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles
0008 B119h	ELC	Event Link Setting Register 24	ELSR24	8	8	2 or 3 PCLKB
0008 B11Ah	ELC	Event Link Setting Register 25	ELSR25	8	8	2 or 3 PCLKB
0008 B11Fh	ELC	Event Link Option Setting Register A	ELOPA	8	8	2 or 3 PCLKB
0008 B120h	ELC	Event Link Option Setting Register B	ELOPB	8	8	2 or 3 PCLKB
0008 B121h	ELC	Event Link Option Setting Register C	ELOPC	8	8	2 or 3 PCLKB
0008 B122h	ELC	Event Link Option Setting Register D	ELOPD	8	8	2 or 3 PCLKB
0008 B123h	ELC	Port Group Setting Register 1	PGR1	8	8	2 or 3 PCLKB
0008 B125h	ELC	Port Group Control Register 1	PGC1	8	8	2 or 3 PCLKB
0008 B127h	ELC	Port Buffer Register 1	PDBF1	8	8	2 or 3 PCLKB
0008 B129h	ELC	Event Link Port Setting Register 0	PEL0	8	8	2 or 3 PCLKB
0008 B12Ah	ELC	Event Link Port Setting Register 1	PEL1	8	8	2 or 3 PCLKB
0008 B12Dh	ELC	Event Link Software Event Generation Register	ELSEGR	8	8	2 or 3 PCLKB
0008 B300h	SCI12	Serial Mode Register	SMR	8	8	2 or 3 PCLKB
0008 B301h	SCI12	Bit Rate Register	BRR	8	8	2 or 3 PCLKB
0008 B302h	SCI12	Serial Control Register	SCR	8	8	2 or 3 PCLKB
0008 B303h	SCI12	Transmit Data Register	TDR	8	8	2 or 3 PCLKB
0008 B304h	SCI12	Serial Status Register	SSR	8	8	2 or 3 PCLKB
0008 B305h	SCI12	Receive Data Register	RDR	8	8	2 or 3 PCLKB
0008 B306h	SMCI12	Smart Card Mode Register	SCMR	8	8	2 or 3 PCLKB
0008 B307h	SCI12	Serial Extended Mode Register	SEMR	8	8	2 or 3 PCLKB
0008 B308h	SCI12	Noise Filter Setting Register	SNFR	8	8	2 or 3 PCLKB
0008 B309h	SCI12	I ² C Mode Register 1	SIMR1	8	8	2 or 3 PCLKB
0008 B30Ah	SCI12	I ² C Mode Register 2	SIMR2	8	8	2 or 3 PCLKB
0008 B30Bh	SCI12	I ² C Mode Register 3	SIMR3	8	8	2 or 3 PCLKB
0008 B30Ch	SCI12	I ² C Status Register	SISR	8	8	2 or 3 PCLKB
0008 B30Dh	SCI12	SPI Mode Register	SPMR	8	8	2 or 3 PCLKB
0008 B30Eh	SCI12	Transmit Data Register HL	TDRHL	16	16	2 or 3 PCLKB
0008 B30Eh	SCI12	Transmit Data Register H	TDRH	8	8	2 or 3 PCLKB
0008 B30Fh	SCI12	Transmit Data Register L	TDRL	8	8	2 or 3 PCLKB
0008 B310h	SCI12	Receive Data Register HL	RDRHL	16	16	2 or 3 PCLKB
0008 B310h	SCI12	Receive Data Register H	RDRH	8	8	2 or 3 PCLKB
0008 B311h	SCI12	Receive Data Register L	RDRL	8	8	2 or 3 PCLKB
0008 B312h	SCI12	Modulation Duty Register	MDDR	8	8	2 or 3 PCLKB
0008 B320h	SCI12	Extended Serial Module Enable Register	ESMER	8	8	2 or 3 PCLKB
0008 B321h	SCI12	Control Register 0	CR0	8	8	2 or 3 PCLKB
0008 B322h	SCI12	Control Register 1	CR1	8	8	2 or 3 PCLKB
0008 B323h	SCI12	Control Register 2	CR2	8	8	2 or 3 PCLKB
0008 B324h	SCI12	Control Register 3	CR3	8	8	2 or 3 PCLKB
0008 B325h	SCI12	Port Control Register	PCR	8	8	2 or 3 PCLKB
0008 B326h	SCI12	Interrupt Control Register	ICR	8	8	2 or 3 PCLKB
0008 B327h	SCI12	Status Register	STR	8	8	2 or 3 PCLKB
0008 B328h	SCI12	Status Clear Register	STCR	8	8	2 or 3 PCLKB
0008 B329h	SCI12	Control Field 0 Data Register	CF0DR	8	8	2 or 3 PCLKB
0008 B32Ah	SCI12	Control Field 0 Compare Enable Register	CF0CR	8	8	2 or 3 PCLKB
0008 B32Bh	SCI12	Control Field 0 Receive Data Register	CF0RR	8	8	2 or 3 PCLKB
0008 B32Ch	SCI12	Primary Control Field 1 Data Register	PCF1DR	8	8	2 or 3 PCLKB
0008 B32Dh	SCI12	Secondary Control Field 1 Data Register	SCF1DR	8	8	2 or 3 PCLKB
0008 B32Eh	SCI12	Control Field 1 Compare Enable Register	CF1CR	8	8	2 or 3 PCLKB
0008 B32Fh	SCI12	Control Field 1 Receive Data Register	CF1RR	8	8	2 or 3 PCLKB
0008 B330h	SCI12	Timer Control Register	TCR	8	8	2 or 3 PCLKB
0008 B331h	SCI12	Timer Mode Register	TMR	8	8	2 or 3 PCLKB
0008 B332h	SCI12	Timer Prescaler Register	TPRE	8	8	2 or 3 PCLKB

Table 4.1 List of I/O Registers (Address Order) (12 / 18)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles
0008 B333h	SCI12	Timer Count Register	TCNT	8	8	2 or 3 PCLKB
0008 C000h	PORT0	Port Direction Register	PDR	8	8	2 or 3 PCLKB
0008 C001h	PORT1	Port Direction Register	PDR	8	8	2 or 3 PCLKB
0008 C002h	PORT2	Port Direction Register	PDR	8	8	2 or 3 PCLKB
0008 C003h	PORT3	Port Direction Register	PDR	8	8	2 or 3 PCLKB
0008 C004h	PORT4	Port Direction Register	PDR	8	8	2 or 3 PCLKB
0008 C005h	PORT5	Port Direction Register	PDR	8	8	2 or 3 PCLKB
0008 C00Ah	PORTA	Port Direction Register	PDR	8	8	2 or 3 PCLKB
0008 C00Bh	PORTB	Port Direction Register	PDR	8	8	2 or 3 PCLKB
0008 C00Ch	PORTC	Port Direction Register	PDR	8	8	2 or 3 PCLKB
0008 C00Dh	PORTD	Port Direction Register	PDR	8	8	2 or 3 PCLKB
0008 C00Eh	PORTE	Port Direction Register	PDR	8	8	2 or 3 PCLKB
0008 C011h	PORTH	Port Direction Register	PDR	8	8	2 or 3 PCLKB
0008 C012h	PORTJ	Port Direction Register	PDR	8	8	2 or 3 PCLKB
0008 C020h	PORT0	Port Output Data Register	PODR	8	8	2 or 3 PCLKB
0008 C021h	PORT1	Port Output Data Register	PODR	8	8	2 or 3 PCLKB
0008 C022h	PORT2	Port Output Data Register	PODR	8	8	2 or 3 PCLKB
0008 C023h	PORT3	Port Output Data Register	PODR	8	8	2 or 3 PCLKB
0008 C024h	PORT4	Port Output Data Register	PODR	8	8	2 or 3 PCLKB
0008 C025h	PORT5	Port Output Data Register	PODR	8	8	2 or 3 PCLKB
0008 C02Ah	PORTA	Port Output Data Register	PODR	8	8	2 or 3 PCLKB
0008 C02Bh	PORTB	Port Output Data Register	PODR	8	8	2 or 3 PCLKB
0008 C02Ch	PORTC	Port Output Data Register	PODR	8	8	2 or 3 PCLKB
0008 C02Dh	PORTD	Port Output Data Register	PODR	8	8	2 or 3 PCLKB
0008 C02Eh	PORTE	Port Output Data Register	PODR	8	8	2 or 3 PCLKB
0008 C031h	PORTH	Port Output Data Register	PODR	8	8	2 or 3 PCLKB
0008 C032h	PORTJ	Port Output Data Register	PODR	8	8	2 or 3 PCLKB
0008 C040h	PORT0	Port Input Data Register	PIDR	8	8	3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing
0008 C041h	PORT1	Port Input Data Register	PIDR	8	8	3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing
0008 C042h	PORT2	Port Input Data Register	PIDR	8	8	3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing
0008 C043h	PORT3	Port Input Data Register	PIDR	8	8	3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing
0008 C044h	PORT4	Port Input Data Register	PIDR	8	8	3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing
0008 C045h	PORT5	Port Input Data Register	PIDR	8	8	3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing
0008 C04Ah	PORTA	Port Input Data Register	PIDR	8	8	3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing
0008 C04Bh	PORTB	Port Input Data Register	PIDR	8	8	3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing
0008 C04Ch	PORTC	Port Input Data Register	PIDR	8	8	3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing
0008 C04Dh	PORTD	Port Input Data Register	PIDR	8	8	3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing
0008 C04Eh	PORTE	Port Input Data Register	PIDR	8	8	3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing
0008 C051h	PORTH	Port Input Data Register	PIDR	8	8	3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing
0008 C052h	PORTJ	Port Input Data Register	PIDR	8	8	3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing
0008 C060h	PORT0	Port Mode Register	PMR	8	8	2 or 3 PCLKB
0008 C061h	PORT1	Port Mode Register	PMR	8	8	2 or 3 PCLKB
0008 C062h	PORT2	Port Mode Register	PMR	8	8	2 or 3 PCLKB
0008 C063h	PORT3	Port Mode Register	PMR	8	8	2 or 3 PCLKB
0008 C064h	PORT4	Port Mode Register	PMR	8	8	2 or 3 PCLKB

Item					Symbol	Typ.	Max.	Unit	Test Conditions		
Supply current*1	Middle-speed operating modes	Deep sleep mode	No peripheral operation*6	ICLK = 12 MHz	I _{CC}	1.0	—	mA			
				ICLK = 8 MHz		0.7	—				
				ICLK = 4 MHz		0.2	—				
				ICLK = 1 MHz		0.1	—				
			All peripheral operation: Normal*7	ICLK = 12 MHz		2.3	—				
				ICLK = 8 MHz		1.6	—				
				ICLK = 4 MHz		1.0	—				
				ICLK = 1 MHz		0.7	—				
			Increase during flash rewrite*5				2.5			—	
			Low-speed operating mode	Normal operating mode		No peripheral operation*8	ICLK = 32.768 kHz			I _{CC}	3.8
	All peripheral operation: Normal*10	ICLK = 32.768 kHz			10.9	—					
	All peripheral operation: Max.*10	ICLK = 32.768 kHz			—	29.2					
	Sleep mode	No peripheral operation*8		ICLK = 32.768 kHz	2.1	—					
		All peripheral operation: Normal*9		ICLK = 32.768 kHz	6.0	—					
	Deep sleep mode	No peripheral operation*8		ICLK = 32.768 kHz	1.6	—					
		All peripheral operation: Normal*9		ICLK = 32.768 kHz	5.0	—					

Note 1. Supply current values do not include output charge/discharge current from all pins. The values apply when internal pull-up MOSs are in the off state.

Note 2. Clock supply to the peripheral functions is stopped. This does not include BGO operation. The clock source is PLL. FCLK and PCLK are set to divided by 64.

Note 3. Clocks are supplied to the peripheral functions. This does not include BGO operation. The clock source is PLL. FCLK and PCLK are set to the same frequency as ICLK.

Note 4. Values when VCC = 3.3 V.

Note 5. This is the increase for programming or erasure of the ROM or E2 DataFlash during program execution.

Note 6. Clock supply to the peripheral function is stopped. The clock source is PLL when ICLK is 12 MHz, HOCO when ICLK is 8 MHz, and LOCO otherwise. FCLK and PCLK are set to divided by 64.

Note 7. Clocks are supplied to the peripheral functions. The clock source is PLL when ICLK is 12 MHz, HOCO when ICLK is (MHz, and LOCO otherwise. FCLK and PCLK are set to the same frequency as ICLK.

Note 8. Clock supply to the peripheral functions is stopped. The clock source is the sub-clock oscillator. FCLK and PCLK are set to divided by 64.

Note 9. Clocks are supplied to the peripheral functions. The clock source is the sub-clock oscillator. FCLK and PCLK are set to the same frequency as ICLK.

Note 10. Values when the MSTPCRA.MSTPA17 bit (12-bit A/D converter module stop bit) is set to "transition to the module stop state is made".

Item					Symbol	Typ.	Max.	Unit	Test Conditions		
Supply current*1	Middle-speed operating modes	Deep sleep mode	No peripheral operation*6	ICLK = 12 MHz	I _{CC}	1.1	—	mA			
				ICLK = 8 MHz		0.7	—				
				ICLK = 4 MHz		0.2	—				
				ICLK = 1 MHz		0.1	—				
			All peripheral operation: Normal*7	ICLK = 12 MHz		2.6	—				
				ICLK = 8 MHz		1.8	—				
				ICLK = 4 MHz		1.1	—				
				ICLK = 1 MHz		0.7	—				
			Increase during flash rewrite*5				2.5			—	
			Low-speed operating mode	Normal operating mode		No peripheral operation*8	ICLK = 32.768 kHz			I _{CC}	4.3
	All peripheral operation: Normal*10	ICLK = 32.768 kHz			13.4	—					
	All peripheral operation: Max.*10	ICLK = 32.768 kHz			—	51.3					
	Sleep mode	No peripheral operation*8		ICLK = 32.768 kHz	2.2	—					
		All peripheral operation: Normal*9		ICLK = 32.768 kHz	7.2	—					
	Deep sleep mode	No peripheral operation*8		ICLK = 32.768 kHz	1.7	—					
		All peripheral operation: Normal*9		ICLK = 32.768 kHz	6.0	—					

Note 1. Supply current values do not include output charge/discharge current from all pins. The values apply when internal pull-up MOSs are in the off state.

Note 2. Clock supply to the peripheral functions is stopped. This does not include BGO operation. The clock source is PLL. FCLK and PCLK are set to divided by 64.

Note 3. Clocks are supplied to the peripheral functions. This does not include BGO operation. The clock source is PLL. FCLK and PCLK are set to the same frequency as ICLK.

Note 4. Values when VCC = 3.3 V.

Note 5. This is the increase for programming or erasure of the ROM or E2 DataFlash during program execution.

Note 6. Clock supply to the peripheral function is stopped. The clock source is PLL when ICLK is 12 MHz, HOCO when ICLK is 8 MHz, and LOCO otherwise. FCLK and PCLK are set to divided by 64.

Note 7. Clocks are supplied to the peripheral functions. The clock source is PLL when ICLK is 12 MHz, HOCO when ICLK is (MHz, and LOCO otherwise. FCLK and PCLK are set to the same frequency as ICLK.

Note 8. Clock supply to the peripheral functions is stopped. The clock source is the sub-clock oscillator. FCLK and PCLK are set to divided by 64.

Note 9. Clocks are supplied to the peripheral functions. The clock source is the sub-clock oscillator. FCLK and PCLK are set to the same frequency as ICLK.

Note 10. Values when the MSTPCRA.MSTPA17 bit (12-bit A/D converter module stop bit) is set to "transition to the module stop state is made".

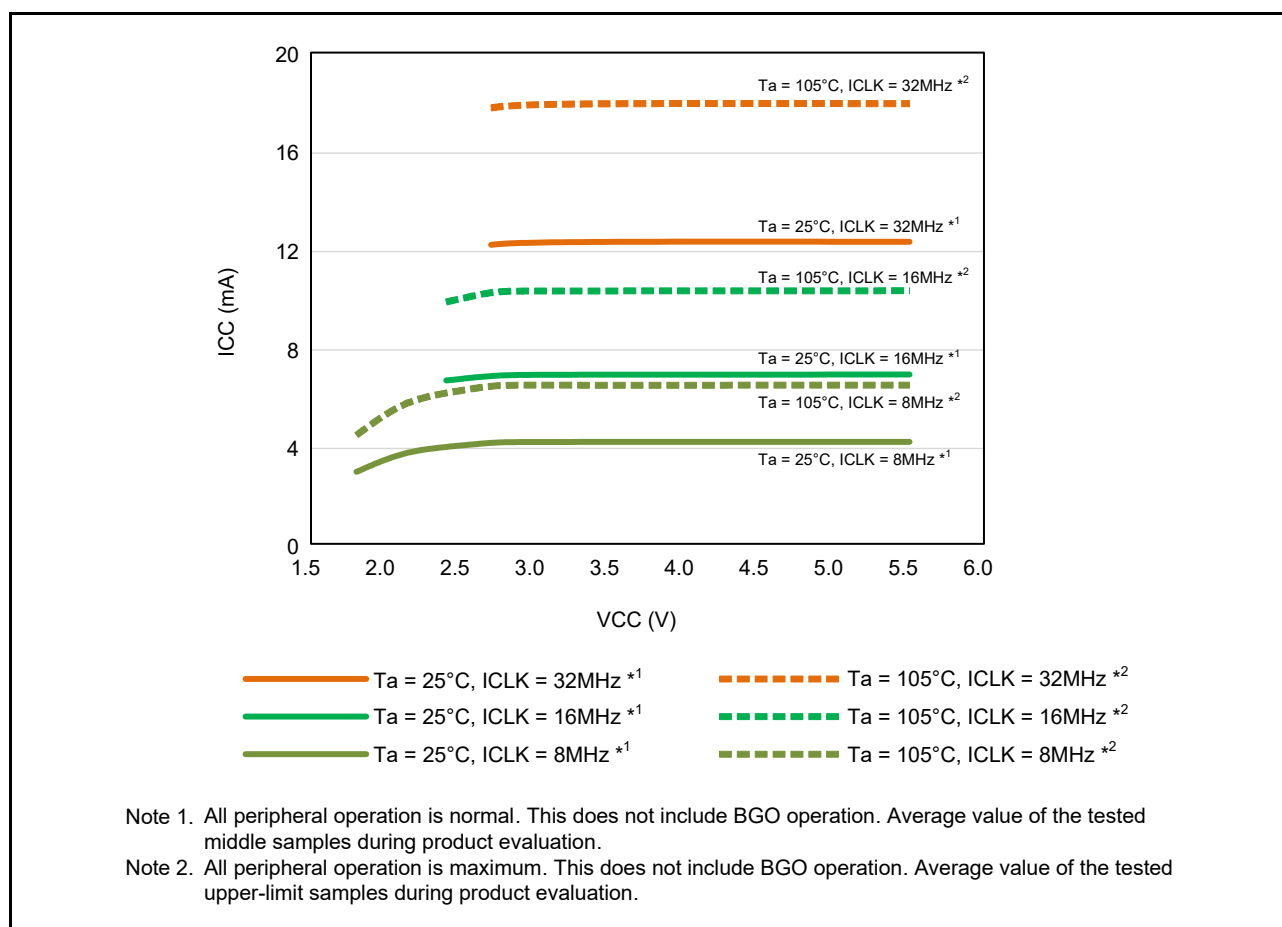


Figure 5.4 Voltage Dependency in High-Speed Operating Mode (Reference Data)

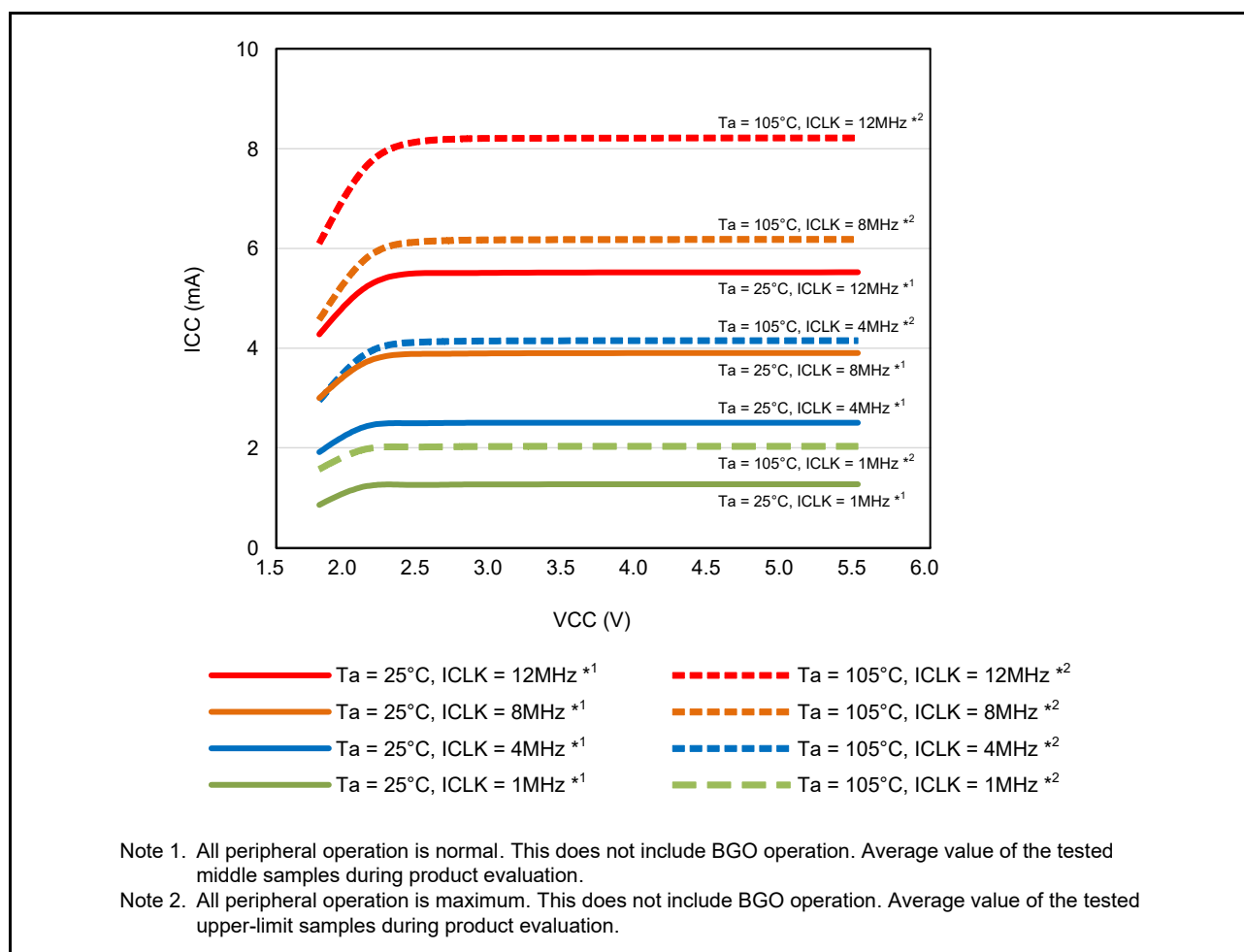


Figure 5.5 Voltage Dependency in Middle-Speed Operating Mode (Reference Data)

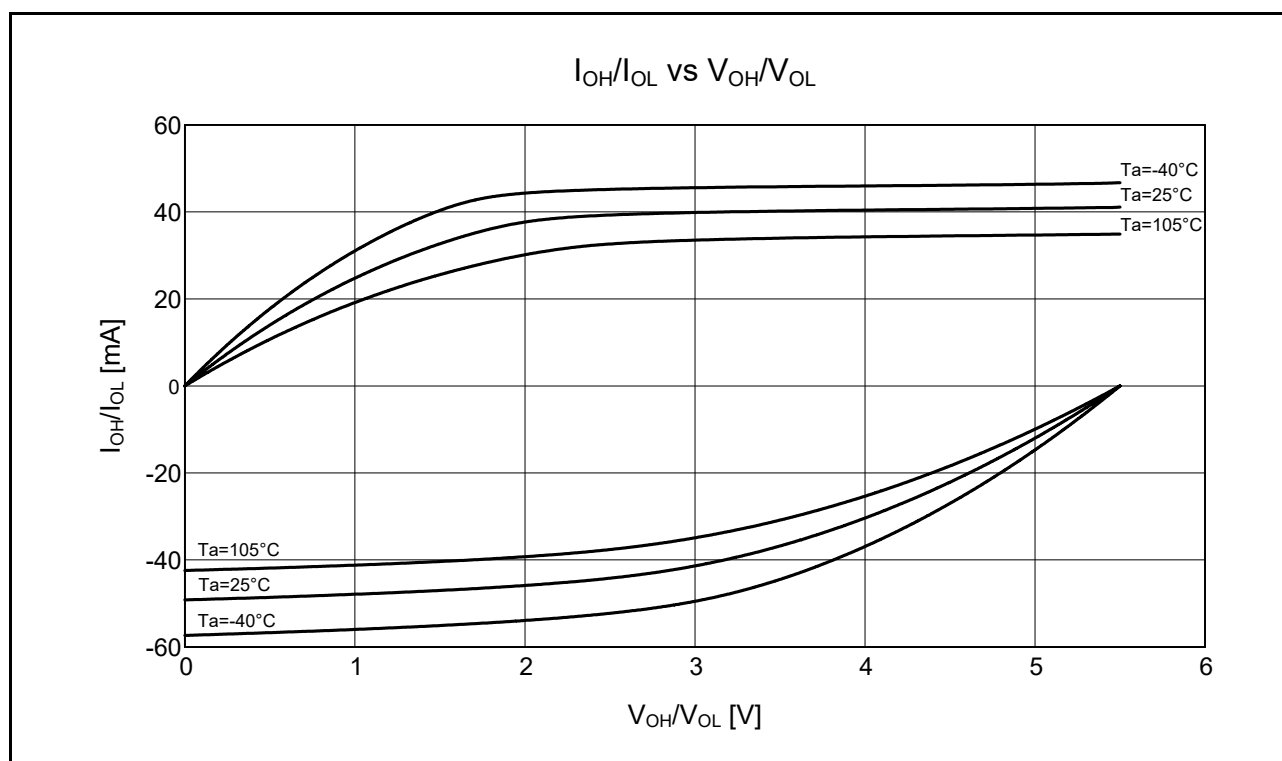


Figure 5.16 V_{OH}/V_{OL} and I_{OH}/I_{OL} Temperature Characteristics at $V_{CC} = 5.5$ V When Normal Output is Selected (Reference Data)

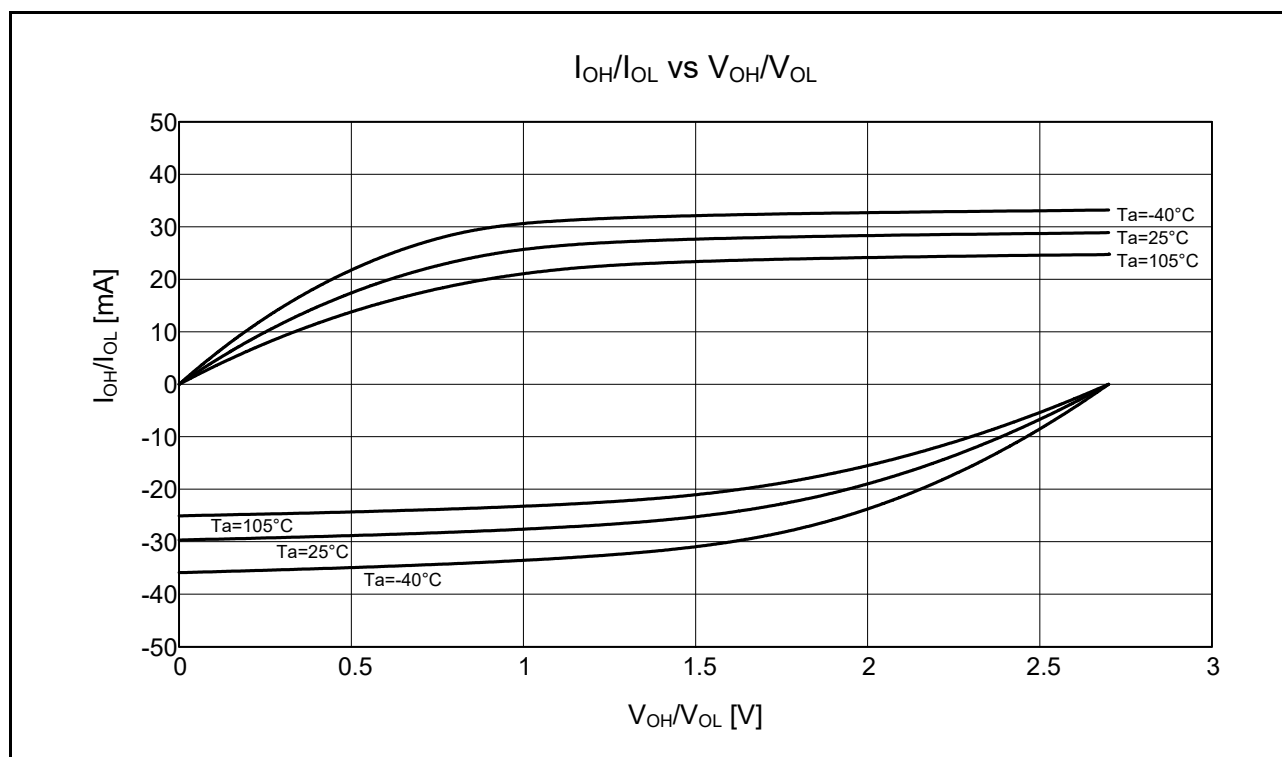


Figure 5.19 V_{OH}/V_{OL} and I_{OH}/I_{OL} Temperature Characteristics at VCC = 2.7 V When High-Drive Output is Selected (Reference Data)

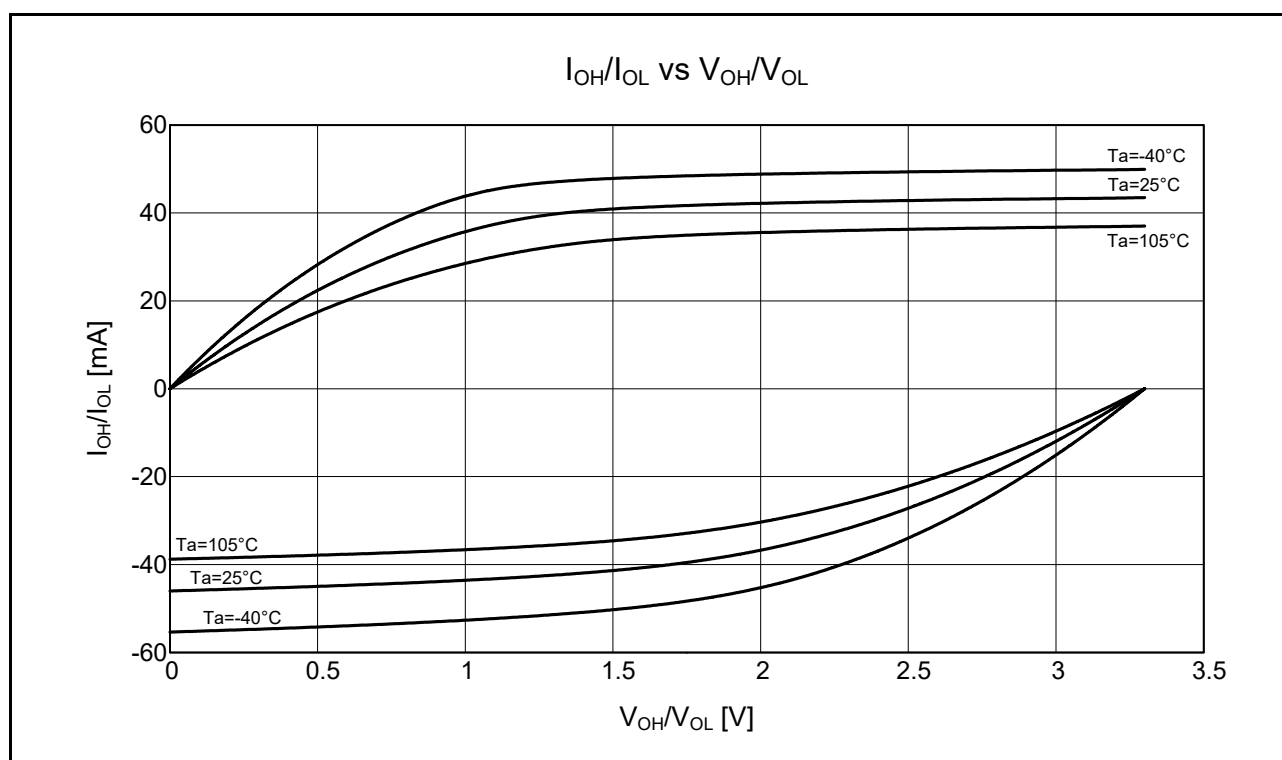


Figure 5.20 V_{OH}/V_{OL} and I_{OH}/I_{OL} Temperature Characteristics at VCC = 3.3 V When High-Drive Output is Selected (Reference Data)

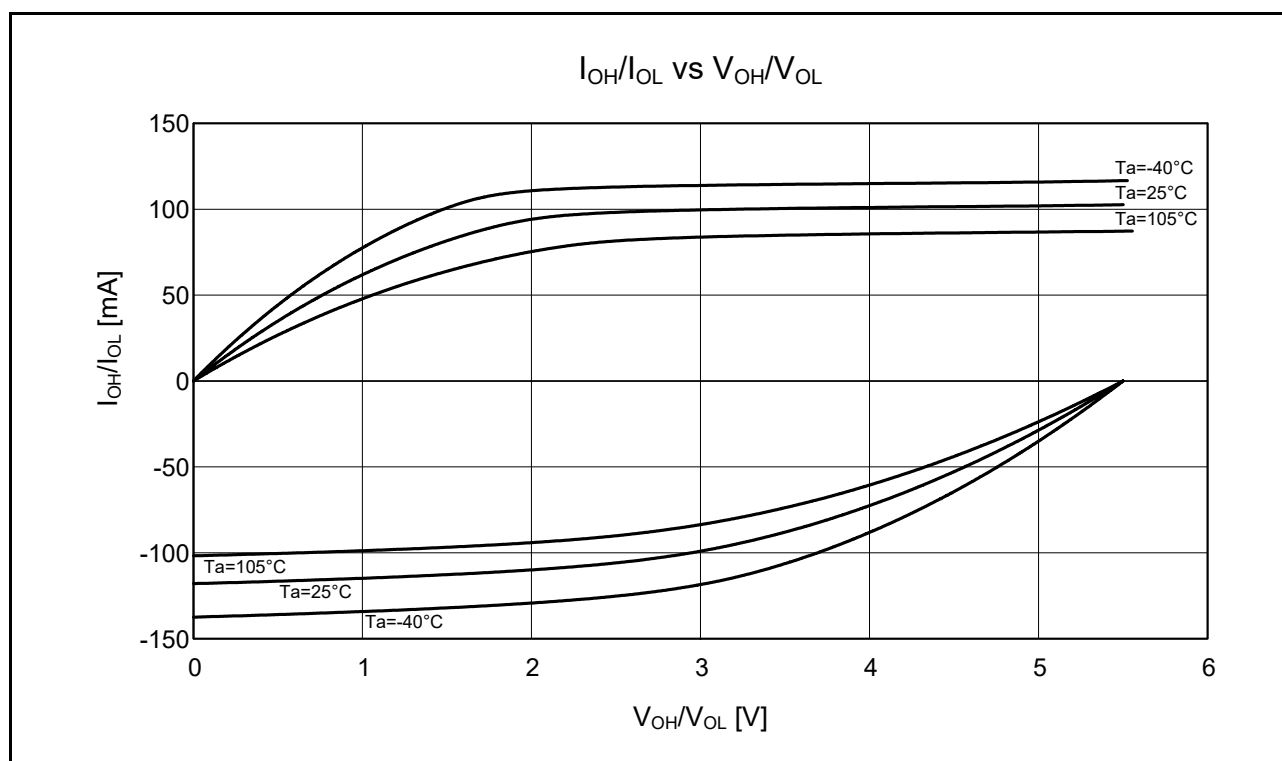


Figure 5.21 V_{OH}/V_{OL} and I_{OH}/I_{OL} Temperature Characteristics at $V_{CC} = 5.5\text{ V}$ When High-Drive Output is Selected (Reference Data)

Table 5.33 Timing of On-Chip Peripheral Modules (1)

Conditions: $1.8\text{ V} \leq VCC = AVCC0 < 2.0\text{ V}$, $2.0\text{ V} \leq VCC \leq 5.5\text{ V}$, $2.0\text{ V} \leq AVCC0 \leq 5.5\text{ V}$, $VSS = AVSS0 = 0\text{ V}$, $T_a = -40$ to $+105^\circ\text{C}$

Item			Symbol	Min.	Max.	Unit *1	Test Conditions
CLKOUT	CLKOUT pin output cycle*4	VCC = 2.7 V or above	t _{Cyc}	62.5	—	ns	Figure 5.49
		VCC = 1.8 V or above		125			
	CLKOUT pin high pulse width*3	VCC = 2.7 V or above	t _{CH}	15	—	ns	
		VCC = 1.8 V or above		30			
	CLKOUT pin low pulse width*3	VCC = 2.7 V or above	t _{CL}	15	—	ns	
		VCC = 1.8 V or above		30			
	CLKOUT pin output rise time	VCC = 2.7 V or above	t _{Cr}	—	12	ns	
		VCC = 1.8 V or above			25		
	CLKOUT pin output fall time	VCC = 2.7 V or above	t _{Cf}	—	12	ns	
		VCC = 1.8 V or above			25		

Note 1. t_{Pcyc} : PCLK cycle

Note 2. t_{cac} : CAC count clock source cycle

Note 3. When the LOCO is selected as the clock output source (CKOCR.CKOSSEL[3:0] bits = 0000b), set the clock output division ratio selection to divided by 2 (CKOCR.CKODIV[2:0] bits = 001b).

Note 4. When the XTAL external clock input or an oscillator is used with divided by 1 (CKOCR.CKOSSEL[3:0] bits = 010b and CKOCR.CKODIV[2:0] bits = 000b) to output from CLKOUT, the above should be satisfied with an input duty cycle of 45 to 55%.

Table 5.36 Timing of On-Chip Peripheral Modules (4)Conditions: $2.7\text{ V} \leq V_{CC} \leq 5.5\text{ V}$, $2.7\text{ V} \leq AV_{CC0} \leq 5.5\text{ V}$, $V_{SS} = AV_{SS0} = 0\text{ V}$, $T_a = -40\text{ to }+105^\circ\text{C}$

Item		Symbol	Min.*1, *2	Max.	Unit	Test Conditions
RIIC (Standard mode, SMBus)	SCL cycle time	t_{SCL}	$6(12) \times t_{IICcyc} + 1300$	—	ns	Figure 5.55
	SCL high pulse width	t_{SCLH}	$3(6) \times t_{IICcyc} + 300$	—	ns	
	SCL low pulse width	t_{SCLL}	$3(6) \times t_{IICcyc} + 300$	—	ns	
	SCL, SDA rise time	t_{Sr}	—	1000	ns	
	SCL, SDA fall time	t_{Sf}	—	300	ns	
	SCL, SDA spike pulse removal time	t_{SP}	0	$1(4) \times t_{IICcyc}$	ns	
	SDA bus free time	t_{BUF}	$3(6) \times t_{IICcyc} + 300$	—	ns	
	START condition hold time	t_{STAH}	$t_{IICcyc} + 300$	—	ns	
	Repeated START condition setup time	t_{STAS}	1000	—	ns	
	STOP condition setup time	t_{STOS}	1000	—	ns	
	Data setup time	t_{SDAS}	$t_{IICcyc} + 50$	—	ns	
	Data hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b	—	400	pF	
RIIC (Fast mode)	SCL cycle time	t_{SCL}	$6(12) \times t_{IICcyc} + 600$	—	ns	Figure 5.55
	SCL high pulse width	t_{SCLH}	$3(6) \times t_{IICcyc} + 300$	—	ns	
	SCL low pulse width	t_{SCLL}	$3(6) \times t_{IICcyc} + 300$	—	ns	
	SCL, SDA rise time	t_{Sr}	—	300	ns	
	SCL, SDA fall time	t_{Sf}	—	300	ns	
	SCL, SDA spike pulse removal time	t_{SP}	0	$1(4) \times t_{IICcyc}$	ns	
	SDA bus free time	t_{BUF}	$3(6) \times t_{IICcyc} + 300$	—	ns	
	START condition hold time	t_{STAH}	$t_{IICcyc} + 300$	—	ns	
	Repeated START condition setup time	t_{STAS}	300	—	ns	
	STOP condition setup time	t_{STOS}	300	—	ns	
	Data setup time	t_{SDAS}	$t_{IICcyc} + 50$	—	ns	
	Data hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b	—	400	pF	

Note: t_{IICcyc} : RIIC internal reference count clock (IIC ϕ) cycle

Note 1. The value in parentheses is used when the ICMR3.NF[1:0] bits are set to 11b while a digital filter is enabled with the ICFER.NFE bit = 1.

Note 2. C_b is the total capacitance of the bus lines.

5.12 E2 DataFlash Characteristics (Flash Memory for Data Storage)

Table 5.55 E2 DataFlash Characteristics (1)

Item		Symbol	Min.	Typ.	Max.	Unit	Conditions
Reprogramming/erasure cycle*1		N _{DPEC}	100000	1000000	—	Times	
Data retention	After 10000 times of N _{DPEC}	t _{DDRP}	20*2, *3	—	—	Year	T _a = +85°C
	After 100000 times of N _{DPEC}		5*2, *3	—	—	Year	
	After 1000000 times of N _{DPEC}		—	1*2, *3	—	Year	T _a = +25°C

Note 1. The reprogram/erase cycle is the number of erasing for each block. When the reprogram/erase cycle is n times (n = 100000), erasing can be performed n times for each block. For instance, when 1-byte programming is performed 1000 times for different addresses in 1-Kbyte block and then the entire block is erased, the reprogram/erase cycle is counted as one. However, programming the same address for several times as one erasing is not enabled (overwriting is prohibited).

Note 2. Characteristic when using the flash memory programmer and the self-programming library provided from Renesas Electronics.

Note 3. These results are obtained from reliability testing.

Table 5.56 E2 DataFlash Characteristics (2): high-speed operating mode

Conditions: 2.7 V ≤ VCC ≤ 5.5 V, 2.7 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V

Temperature range for the programming/erasure operation: T_a = −40 to +105°C

Item		Symbol	FCLK = 1 MHz			FCLK = 32 MHz			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Programming time	1-byte	t _{DP1}	—	86	761	—	40.5	374	μs
Erasure time	1-Kbyte	t _{DE1K}	—	17.4	456	—	6.15	228	ms
	8-Kbyte	t _{DE8K}	—	60.4	499	—	9.3	231	ms
Blank check time	1-byte	t _{DBC1}	—	—	48	—	—	15.9	μs
	1-Kbyte	t _{DBC1K}	—	—	1.58	—	—	0.127	μs
Erase operation forcible stop time		t _{DSED}	—	—	21.5	—	—	12.8	μs
DataFlash STOP recovery time		t _{DSTOP}	5.0	—	—	5	—	—	μs

Note: Does not include the time until each operation of the flash memory is started after instructions are executed by software.

Note: The lower-limit frequency of FCLK is 1 MHz during programming or erasing of the flash memory. When using FCLK at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.

Note: The frequency accuracy of FCLK should be ±3.5%.

Table 5.57 E2 DataFlash Characteristics (3): middle-speed operating mode

Conditions: 1.8 V ≤ VCC = AVCC0 < 2.0 V, 2.0 V ≤ VCC ≤ 5.5 V, 2.0 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V

Temperature range for the programming/erasure operation: T_a = −40 to +85°C

Item		Symbol	FCLK = 1 MHz			FCLK = 8 MHz			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Programming time	1-byte	t _{DP1}	—	126	1160	—	85.4	818	μs
Erasure time	1-Kbyte	t _{DE1K}	—	17.5	457	—	7.76	259	ms
	8-Kbyte	t _{DE8K}	—	60.5	500	—	4.2	66.9	ms
Blank check time	1-byte	t _{DBC1}	—	—	78	—	—	50	μs
	1-Kbyte	t _{DBC1K}	—	—	1.61	—	—	0.369	ms
Erase operation forcible stop time		t _{DSED}	—	—	33.5	—	—	25.5	μs
DataFlash STOP recovery time		t _{DSTOP}	720	—	—	720	—	—	ns

Note: Does not include the time until each operation of the flash memory is started after instructions are executed by software.

Note: The lower-limit frequency of FCLK is 1 MHz during programming or erasing of the flash memory. When using FCLK at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.

Note: The frequency accuracy of FCLK should be ±3.5%.

NOTES FOR CMOS DEVICES

- (1) **VOLTAGE APPLICATION WAVEFORM AT INPUT PIN:** Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (MAX) and V_{IH} (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (MAX) and V_{IH} (MIN).
- (2) **HANDLING OF UNUSED INPUT PINS:** Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to VDD or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.
- (3) **PRECAUTION AGAINST ESD:** A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.
- (4) **STATUS BEFORE INITIALIZATION:** Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.
- (5) **POWER ON/OFF SEQUENCE:** In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current. The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.
- (6) **INPUT OF SIGNAL DURING POWER OFF STATE :** Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.