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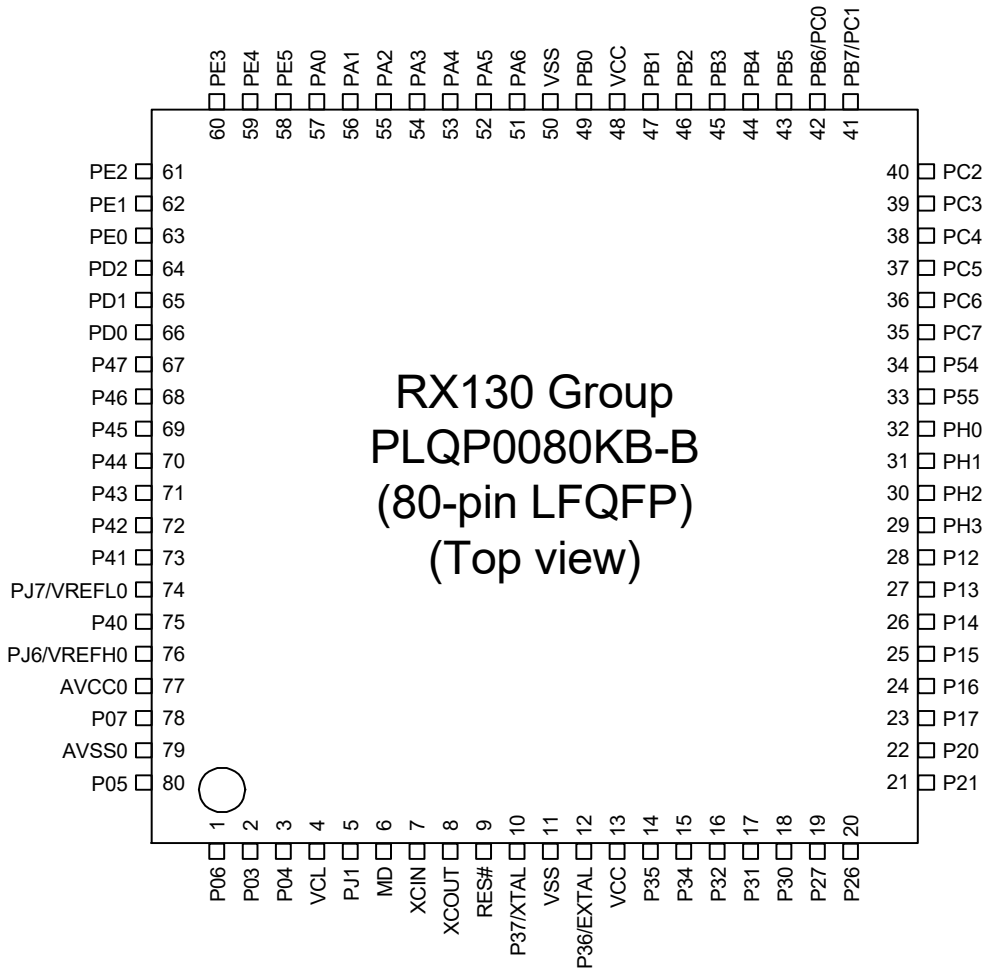
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	RX
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	I²C, LINbus, SCI, SPI
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	52
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	8K x 8
RAM Size	48K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 14x12b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f51308adfk-30

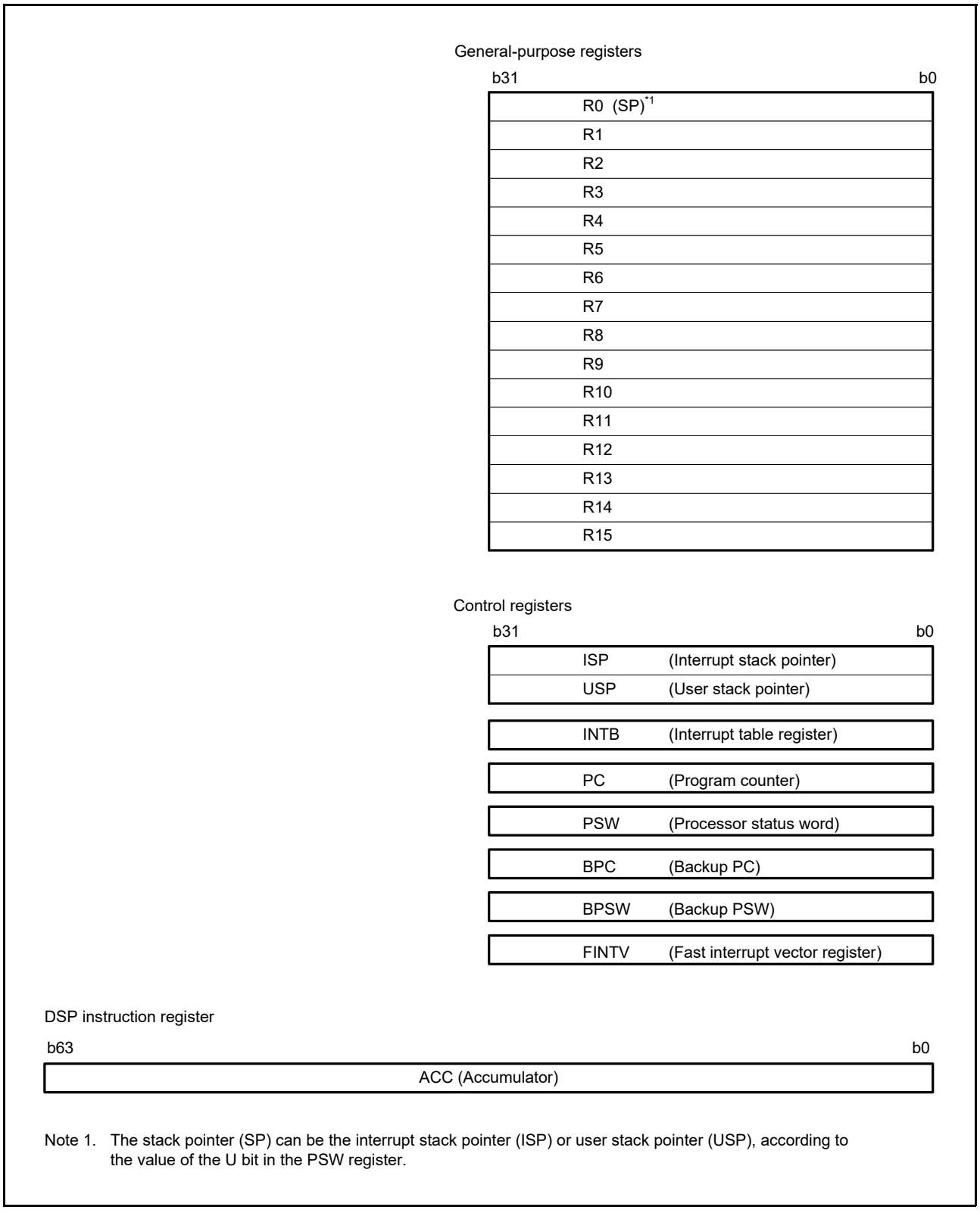


Note: This figure indicates the power supply pins and I/O ports.
For the pin configuration, see the table “List of Pins and Pin Functions (80-Pin LFQFP)”.

Figure 1.4 Pin Assignments of the 80-Pin LFQFP

2. CPU

Figure 2.1 shows the register set of the CPU.



Note 1. The stack pointer (SP) can be the interrupt stack pointer (ISP) or user stack pointer (USP), according to the value of the U bit in the PSW register.

Figure 2.1 Register Set of the CPU

Table 4.1 List of I/O Registers (Address Order) (7 / 18)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles
0008 905Eh	S12AD	A/D Data Register 31	ADDR31	16	16	2 or 3 PCLKB
0008 907Ah	S12AD	A/D Disconnection Detection Control Register	ADDISCR	8	8	2 or 3 PCLKB
0008 907Dh	S12AD	A/D Event Link Control Register	ADELCCR	8	8	2 or 3 PCLKB
0008 9080h	S12AD	A/D Group Scan Priority Control Register	ADGSPCR	16	16	2 or 3 PCLKB
0008 908Ah	S12AD	A/D High-Potential/Low-Potential Reference Voltage Control Register	ADHVREFCNT	8	8	2 or 3 PCLKB
0008 908Ch	S12AD	A/D Compare Function Window A/B Status Monitor Register	ADWINMON	8	8	2 or 3 PCLKB
0008 9090h	S12AD	A/D Compare Function Control Register	ADCMPCR	16	16	2 or 3 PCLKB
0008 9092h	S12AD	A/D Compare Function Window A Extended Input Select Register	ADCMPANSER	8	8	2 or 3 PCLKB
0008 9093h	S12AD	A/D Compare Function Window A Extended Input Comparison Condition Setting Register	ADCMPLER	8	8	2 or 3 PCLKB
0008 9094h	S12AD	A/D Compare Function Window A Channel Select Register 0	ADCMPANSR0	16	16	2 or 3 PCLKB
0008 9096h	S12AD	A/D Compare Function Window A Channel Select Register 1	ADCMPANSR1	16	16	2 or 3 PCLKB
0008 9098h	S12AD	A/D Compare Function Window A Comparison Condition Setting Register 0	ADCMPLR0	16	16	2 or 3 PCLKB
0008 909Ah	S12AD	A/D Compare Function Window A Comparison Condition Setting Register 1	ADCMPLR1	16	16	2 or 3 PCLKB
0008 909Ch	S12AD	A/D Compare Function Window A Lower-Side Level Setting Register	ADCMPDR0	16	16	2 or 3 PCLKB
0008 909Eh	S12AD	A/D Compare Function Window A Upper-Side Level Setting Register	ADCMPDR1	16	16	2 or 3 PCLKB
0008 90A0h	S12AD	A/D Compare Function Window A Channel Status Register 0	ADCMPSR0	16	16	2 or 3 PCLKB
0008 90A2h	S12AD	A/D Compare Function Window A Channel Status Register 1	ADCMPSR1	16	16	2 or 3 PCLKB
0008 90A4h	S12AD	A/D Compare Function Window A Extended Input Channel Status Register	ADCMPSER	8	8	2 or 3 PCLKB
0008 90A6h	S12AD	A/D Compare Function Window B Channel Select Register	ADCMPBNSR	8	8	2 or 3 PCLKB
0008 90A8h	S12AD	A/D Compare Function Window B Lower-Side Level Setting Register	ADWINLLB	16	16	2 or 3 PCLKB
0008 90AAh	S12AD	A/D Compare Function Window B Upper-Side Level Setting Register	ADWINULB	16	16	2 or 3 PCLKB
0008 90ACh	S12AD	A/D Compare Function Window B Status Register	ADCMPBSR	8	8	2 or 3 PCLKB
0008 90B0h	S12AD	A/D Data Storage Buffer Register 0	ADBUF0	16	16	2 or 3 PCLKB
0008 90B2h	S12AD	A/D Data Storage Buffer Register 1	ADBUF1	16	16	2 or 3 PCLKB
0008 90B4h	S12AD	A/D Data Storage Buffer Register 2	ADBUF2	16	16	2 or 3 PCLKB
0008 90B6h	S12AD	A/D Data Storage Buffer Register 3	ADBUF3	16	16	2 or 3 PCLKB
0008 90B8h	S12AD	A/D Data Storage Buffer Register 4	ADBUF4	16	16	2 or 3 PCLKB
0008 90BAh	S12AD	A/D Data Storage Buffer Register 5	ADBUF5	16	16	2 or 3 PCLKB
0008 90BCh	S12AD	A/D Data Storage Buffer Register 6	ADBUF6	16	16	2 or 3 PCLKB
0008 90BEh	S12AD	A/D Data Storage Buffer Register 7	ADBUF7	16	16	2 or 3 PCLKB
0008 90C0h	S12AD	A/D Data Storage Buffer Register 8	ADBUF8	16	16	2 or 3 PCLKB
0008 90C2h	S12AD	A/D Data Storage Buffer Register 9	ADBUF9	16	16	2 or 3 PCLKB
0008 90C4h	S12AD	A/D Data Storage Buffer Register 10	ADBUF10	16	16	2 or 3 PCLKB
0008 90C6h	S12AD	A/D Data Storage Buffer Register 11	ADBUF11	16	16	2 or 3 PCLKB
0008 90C8h	S12AD	A/D Data Storage Buffer Register 12	ADBUF12	16	16	2 or 3 PCLKB
0008 90CAh	S12AD	A/D Data Storage Buffer Register 13	ADBUF13	16	16	2 or 3 PCLKB
0008 90CCh	S12AD	A/D Data Storage Buffer Register 14	ADBUF14	16	16	2 or 3 PCLKB
0008 90CEh	S12AD	A/D Data Storage Buffer Register 15	ADBUF15	16	16	2 or 3 PCLKB
0008 90D0h	S12AD	A/D Data Storage Buffer Enable Register	ADBUFEN	8	8	2 or 3 PCLKB
0008 90D2h	S12AD	A/D Data Storage Buffer Pointer Register	ADBUFPTR	8	8	2 or 3 PCLKB
0008 90DDh	S12AD	A/D Sampling State Register L	ADSSTRL	8	8	2 or 3 PCLKB
0008 90DEh	S12AD	A/D Sampling State Register T	ADSSTRT	8	8	2 or 3 PCLKB
0008 90DFh	S12AD	A/D Sampling State Register O	ADSSTRO	8	8	2 or 3 PCLKB
0008 90E0h	S12AD	A/D Sampling State Register 0	ADSSTR0	8	8	2 or 3 PCLKB
0008 90E1h	S12AD	A/D Sampling State Register 1	ADSSTR1	8	8	2 or 3 PCLKB
0008 90E2h	S12AD	A/D Sampling State Register 2	ADSSTR2	8	8	2 or 3 PCLKB
0008 90E3h	S12AD	A/D Sampling State Register 3	ADSSTR3	8	8	2 or 3 PCLKB

Table 4.1 List of I/O Registers (Address Order) (14 / 18)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles
0008 C147h	MPC	P07 Pin Function Control Register	P07PFS	8	8	2 or 3 PCLKB
0008 C14Ah	MPC	P12 Pin Function Control Register	P12PFS	8	8	2 or 3 PCLKB
0008 C14Bh	MPC	P13 Pin Function Control Register	P13PFS	8	8	2 or 3 PCLKB
0008 C14Ch	MPC	P14 Pin Function Control Register	P14PFS	8	8	2 or 3 PCLKB
0008 C14Dh	MPC	P15 Pin Function Control Register	P15PFS	8	8	2 or 3 PCLKB
0008 C14Eh	MPC	P16 Pin Function Control Register	P16PFS	8	8	2 or 3 PCLKB
0008 C14Fh	MPC	P17 Pin Function Control Register	P17PFS	8	8	2 or 3 PCLKB
0008 C150h	MPC	P20 Pin Function Control Register	P20PFS	8	8	2 or 3 PCLKB
0008 C151h	MPC	P21 Pin Function Control Register	P21PFS	8	8	2 or 3 PCLKB
0008 C152h	MPC	P22 Pin Function Control Register	P22PFS	8	8	2 or 3 PCLKB
0008 C153h	MPC	P23 Pin Function Control Register	P23PFS	8	8	2 or 3 PCLKB
0008 C154h	MPC	P24 Pin Function Control Register	P24PFS	8	8	2 or 3 PCLKB
0008 C155h	MPC	P25 Pin Function Control Register	P25PFS	8	8	2 or 3 PCLKB
0008 C156h	MPC	P26 Pin Function Control Register	P26PFS	8	8	2 or 3 PCLKB
0008 C157h	MPC	P27 Pin Function Control Register	P27PFS	8	8	2 or 3 PCLKB
0008 C158h	MPC	P30 Pin Function Control Register	P30PFS	8	8	2 or 3 PCLKB
0008 C159h	MPC	P31 Pin Function Control Register	P31PFS	8	8	2 or 3 PCLKB
0008 C15Ah	MPC	P32 Pin Function Control Register	P32PFS	8	8	2 or 3 PCLKB
0008 C15Bh	MPC	P33 Pin Function Control Register	P33PFS	8	8	2 or 3 PCLKB
0008 C15Ch	MPC	P34 Pin Function Control Register	P34PFS	8	8	2 or 3 PCLKB
0008 C160h	MPC	P40 Pin Function Control Register	P40PFS	8	8	2 or 3 PCLKB
0008 C161h	MPC	P41 Pin Function Control Register	P41PFS	8	8	2 or 3 PCLKB
0008 C162h	MPC	P42 Pin Function Control Register	P42PFS	8	8	2 or 3 PCLKB
0008 C163h	MPC	P43 Pin Function Control Register	P43PFS	8	8	2 or 3 PCLKB
0008 C164h	MPC	P44 Pin Function Control Register	P44PFS	8	8	2 or 3 PCLKB
0008 C165h	MPC	P45 Pin Function Control Register	P45PFS	8	8	2 or 3 PCLKB
0008 C166h	MPC	P46 Pin Function Control Register	P46PFS	8	8	2 or 3 PCLKB
0008 C167h	MPC	P47 Pin Function Control Register	P47PFS	8	8	2 or 3 PCLKB
0008 C169h	MPC	P51 Pin Function Control Register	P51PFS	8	8	2 or 3 PCLKB
0008 C16Ah	MPC	P52 Pin Function Control Register	P52PFS	8	8	2 or 3 PCLKB
0008 C16Ch	MPC	P54 Pin Function Control Register	P54PFS	8	8	2 or 3 PCLKB
0008 C16Dh	MPC	P55 Pin Function Control Register	P55PFS	8	8	2 or 3 PCLKB
0008 C190h	MPC	PA0 Pin Function Control Register	PA0PFS	8	8	2 or 3 PCLKB
0008 C191h	MPC	PA1 Pin Function Control Register	PA1PFS	8	8	2 or 3 PCLKB
0008 C192h	MPC	PA2 Pin Function Control Register	PA2PFS	8	8	2 or 3 PCLKB
0008 C193h	MPC	PA3 Pin Function Control Register	PA3PFS	8	8	2 or 3 PCLKB
0008 C194h	MPC	PA4 Pin Function Control Register	PA4PFS	8	8	2 or 3 PCLKB
0008 C195h	MPC	PA5 Pin Function Control Register	PA5PFS	8	8	2 or 3 PCLKB
0008 C196h	MPC	PA6 Pin Function Control Register	PA6PFS	8	8	2 or 3 PCLKB
0008 C197h	MPC	PA7 Pin Function Control Register	PA7PFS	8	8	2 or 3 PCLKB
0008 C198h	MPC	PB0 Pin Function Control Register	PB0PFS	8	8	2 or 3 PCLKB
0008 C199h	MPC	PB1 Pin Function Control Register	PB1PFS	8	8	2 or 3 PCLKB
0008 C19Ah	MPC	PB2 Pin Function Control Register	PB2PFS	8	8	2 or 3 PCLKB
0008 C19Bh	MPC	PB3 Pin Function Control Register	PB3PFS	8	8	2 or 3 PCLKB
0008 C19Ch	MPC	PB4 Pin Function Control Register	PB4PFS	8	8	2 or 3 PCLKB
0008 C19Dh	MPC	PB5 Pin Function Control Register	PB5PFS	8	8	2 or 3 PCLKB
0008 C19Eh	MPC	PB6 Pin Function Control Register	PB6PFS	8	8	2 or 3 PCLKB
0008 C19Fh	MPC	PB7 Pin Function Control Register	PB7PFS	8	8	2 or 3 PCLKB
0008 C1A0h	MPC	PC0 Pin Function Control Register	PC0PFS	8	8	2 or 3 PCLKB
0008 C1A1h	MPC	PC1 Pin Function Control Register	PC1PFS	8	8	2 or 3 PCLKB
0008 C1A2h	MPC	PC2 Pin Function Control Register	PC2PFS	8	8	2 or 3 PCLKB
0008 C1A3h	MPC	PC3 Pin Function Control Register	PC3PFS	8	8	2 or 3 PCLKB

Table 5.2 Recommended Operating Voltage Conditions

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Power supply voltages	VCC*1, *2, *3		1.8	—	5.5	V
	VSS		—	0	—	
Analog power supply voltages	AVCC0*1, *2		1.8	—	5.5	V
	AVSS0		—	0	—	
	VREFH0		1.8	—	AVCC0	
	VREFL0		—	0	—	

Note 1. Use AVCC0 and VCC under the following conditions:
AVCC0 and VCC can be set individually within the operating range when VCC ≥ 2.0 V
AVCC0 = VCC when VCC < 2.0 V

Note 2. When powering on the VCC and AVCC0 pins, power them on at the same time or the VCC pin first and then the AVCC0 pin.

Note 3. When VCC < 2.4 V, some functions of the REMC and CTSU are restricted. For details, refer to section 28, Remote Control Signal Receiver (REMC) and section 32, Capacitive Touch Sensing Unit (CTSUa) in the User's Manual: Hardware.

[Products with 128 Kbytes of flash memory or less (except for 100-pin packages)]

Table 5.7 DC Characteristics (5)

Conditions: 1.8 V ≤ VCC = AVCC0 < 2.0 V, 2.0 V ≤ VCC ≤ 5.5 V, 2.0 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, Ta = –40 to +105°C

Item					Symbol	Typ.	Max.	Unit	Test Conditions
Supply current*1	High-speed operating mode	Normal operating mode	No peripheral operation*2	ICLK = 32MHz	I_{CC}	3.1	—	mA	
				ICLK = 16MHz		2.1	—		
				ICLK = 8MHz		1.6	—		
			All peripheral operation: Normal*3	ICLK = 32MHz		10.0	—		
				ICLK = 16MHz		5.7	—		
				ICLK = 8MHz		3.5	—		
			All peripheral operation: Max.*3	ICLK = 32MHz		—	17.5		
		Sleep mode	No peripheral operation*2	ICLK = 32MHz		1.6	—		
				ICLK = 16MHz		1.2	—		
				ICLK = 8MHz		1.1	—		
			All peripheral operation: Normal*3	ICLK = 32MHz		5.3	—		
				ICLK = 16MHz		3.2	—		
				ICLK = 8MHz		2.0	—		
		Deep sleep mode	No peripheral operation*2	ICLK = 32MHz		1.0	—		
				ICLK = 16MHz		0.9	—		
				ICLK = 8MHz		0.8	—		
			All peripheral operation: Normal*3	ICLK = 32MHz		4.2	—		
				ICLK = 16MHz		2.5	—		
				ICLK = 8MHz		1.7	—		
		Increase during flash rewrite*5				2.5	—		
	Middle-speed operating modes	Normal operating mode	No peripheral operation*6	ICLK = 12MHz	I_{CC}	1.9	—	mA	
				ICLK = 8MHz		1.2	—		
				ICLK = 4MHz		0.6	—		
				ICLK = 1MHz		0.3	—		
			All peripheral operation: Normal*7	ICLK = 12MHz		4.6	—		
				ICLK = 8MHz		3.2	—		
				ICLK = 4MHz		2.0	—		
				ICLK = 1MHz		0.9	—		
			All peripheral operation: Max.*7	ICLK = 12MHz		—	8.2		
		Sleep mode	No peripheral operation*6	ICLK = 12MHz	I_{CC}	1.2	—	mA	
				ICLK = 8MHz		0.8	—		
				ICLK = 4MHz		0.3	—		
				ICLK = 1MHz		0.2	—		
			All peripheral operation: Normal*7	ICLK = 12MHz		2.7	—		
				ICLK = 8MHz		1.9	—		
				ICLK = 4MHz		1.2	—		
				ICLK = 1MHz		0.7	—		

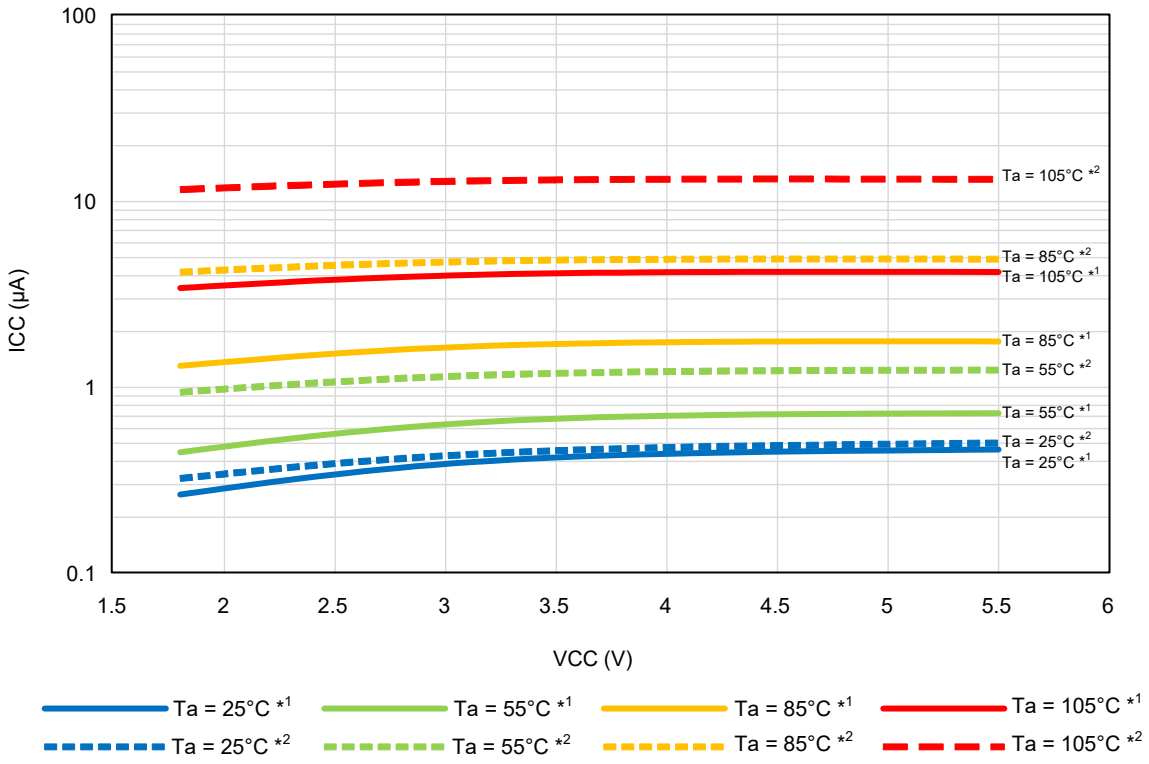
[Products with at least 256 Kbytes of flash memory or 100-pin packages]

Table 5.10 DC Characteristics (6)

Conditions: 1.8 V ≤ VCC = AVCC0 < 2.0 V, 2.0 V ≤ VCC ≤ 5.5 V, 2.0 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, Ta = –40 to +105°C

Item			Symbol	Typ.*3	Max.	Unit	Test Conditions
Supply current*1	Software standby mode*2	T_a = 25°C	I_{CC}	0.41	0.98	μA	
		T_a = 55°C		0.66	2.78		
		T_a = 85°C		1.69	9.65		
		T_a = 105°C		4.08	25.04		
	Increment for RTC operation*4			0.40	—		RCR3.RTCDV[2:0] set to low drive capacity
				1.21	—		RCR3.RTCDV[2:0] set to normal drive capacity
	Increment for low-power timer operation			0.37	—		LPTCR1.LPCNTCKSEL set to IWDT-dedicated on-chip oscillator
	Increment for Independent Watchdog Timer operation			0.37	—		
	Increment for REMC operation			0.44*4	—		REMCON1.CSRC[3:0] set to Sub-clock RCR3.RTCDV[2:0] set to low drive capacity
				1.34*4	—		REMCON1.CSRC[3:0] set to Sub-clock RCR3.RTCDV[2:0] set to normal drive capacity
				235	—		REMCON1.CSRC[3:0] set to HOCO clock/512

Note 1. Supply current values are with all output pins unloaded and all input pull-up MOSs in the off state.
Note 2. The IWDT, LVD, and CMPB are stopped.
Note 3. VCC = 3.3 V.
Note 4. Includes the oscillation circuit.



Note 1. Average value of the tested middle samples during product evaluation.
Note 2. Average value of the tested upper-limit samples during product evaluation.

Figure 5.9 Voltage Dependency in Software Standby Mode (Reference Data)

5.2.1 Normal I/O Pin Output Characteristics (1)

Figure 5.12 to Figure 5.16 show the characteristics when normal output is selected by the drive capacity control register.

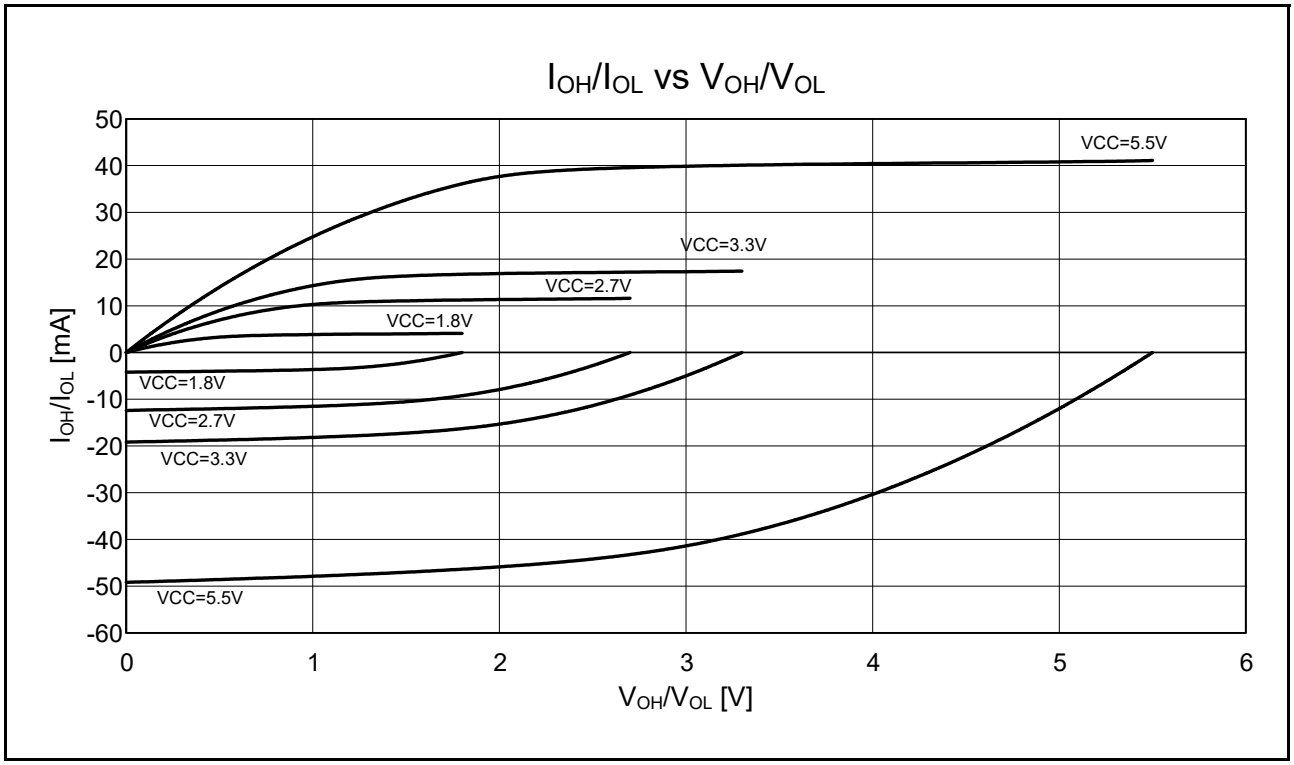


Figure 5.12 V_{OH}/V_{OL} and I_{OH}/I_{OL} Voltage Characteristics at T_a = 25°C When Normal Output is Selected (Reference Data)

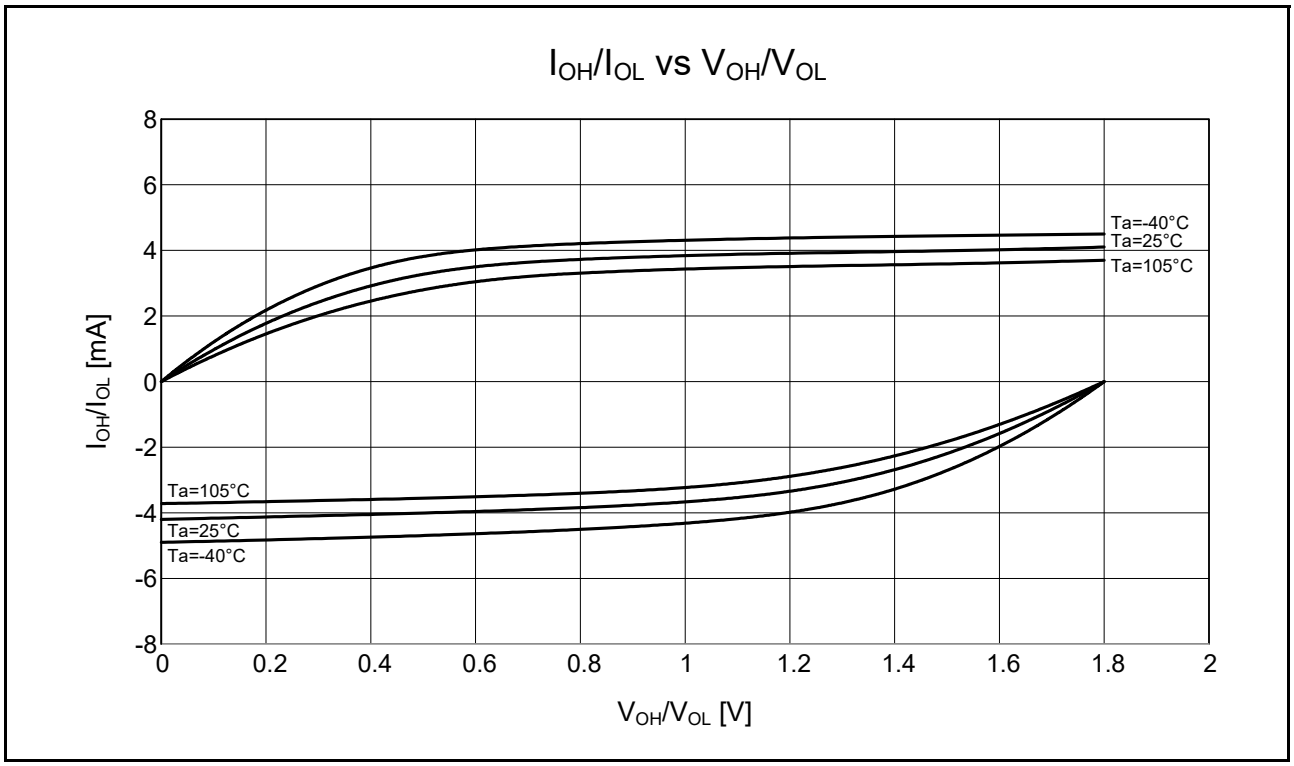


Figure 5.13 V_{OH}/V_{OL} and I_{OH}/I_{OL} Temperature Characteristics at VCC = 1.8 V When Normal Output is Selected (Reference Data)

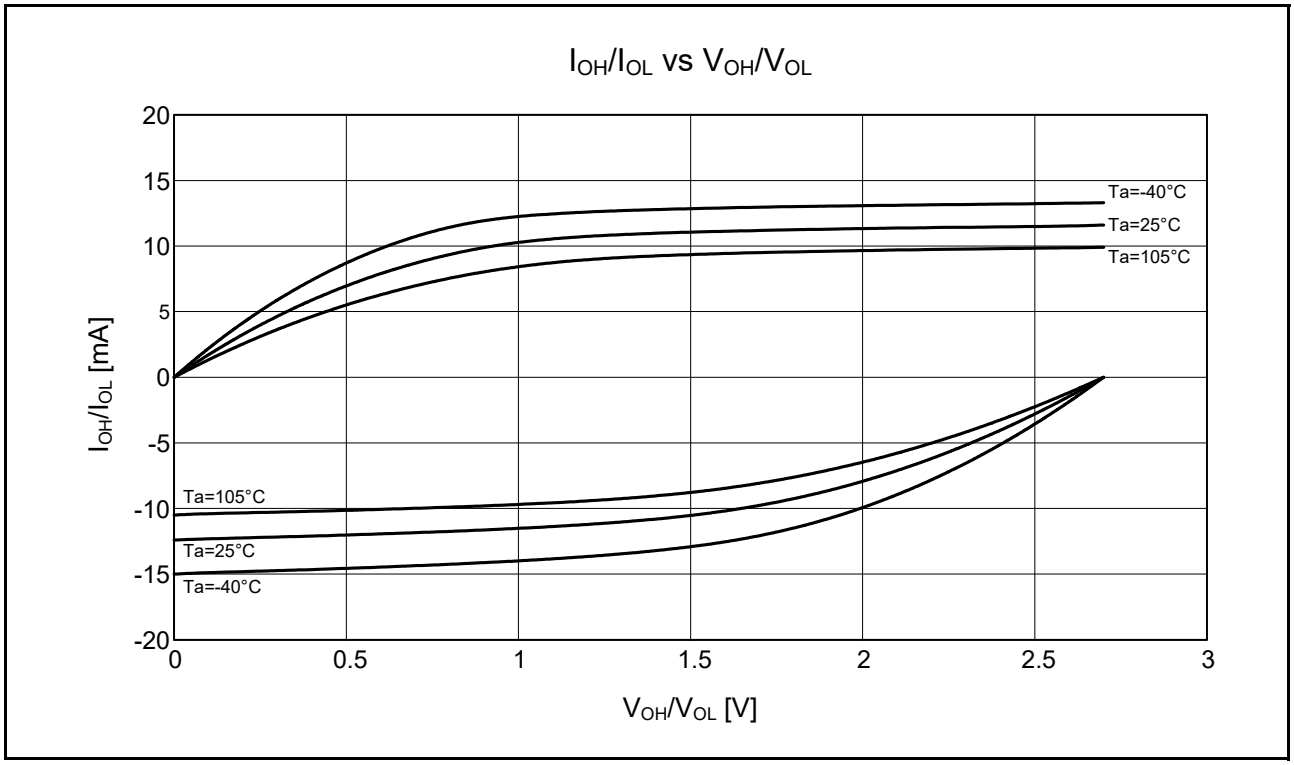


Figure 5.14 V_{OH}/V_{OL} and I_{OH}/I_{OL} Temperature Characteristics at VCC = 2.7 V When Normal Output is Selected (Reference Data)

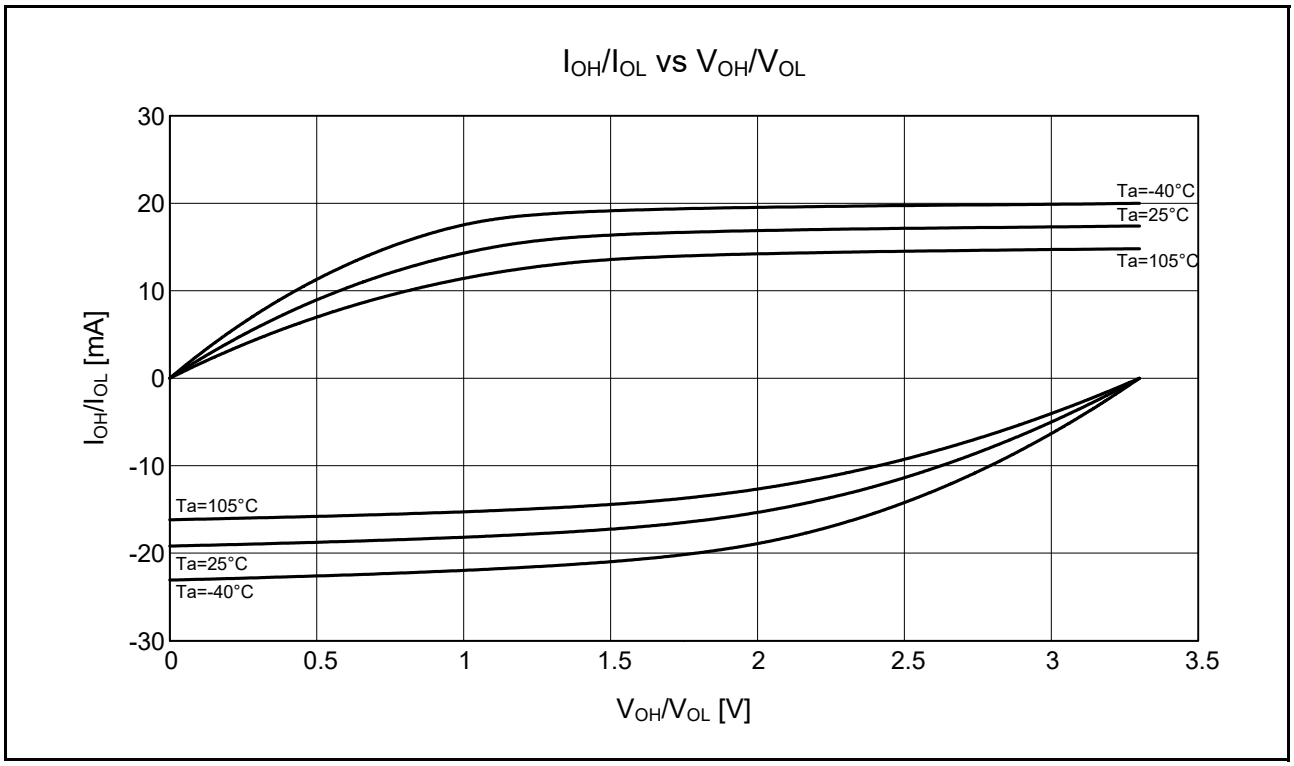


Figure 5.15 V_{OH}/V_{OL} and I_{OH}/I_{OL} Temperature Characteristics at VCC = 3.3 V When Normal Output is Selected (Reference Data)

5.2.3 Normal I/O Pin Output Characteristics (3)

Figure 5.22 to Figure 5.25 show the characteristics of the RIIC output pin.

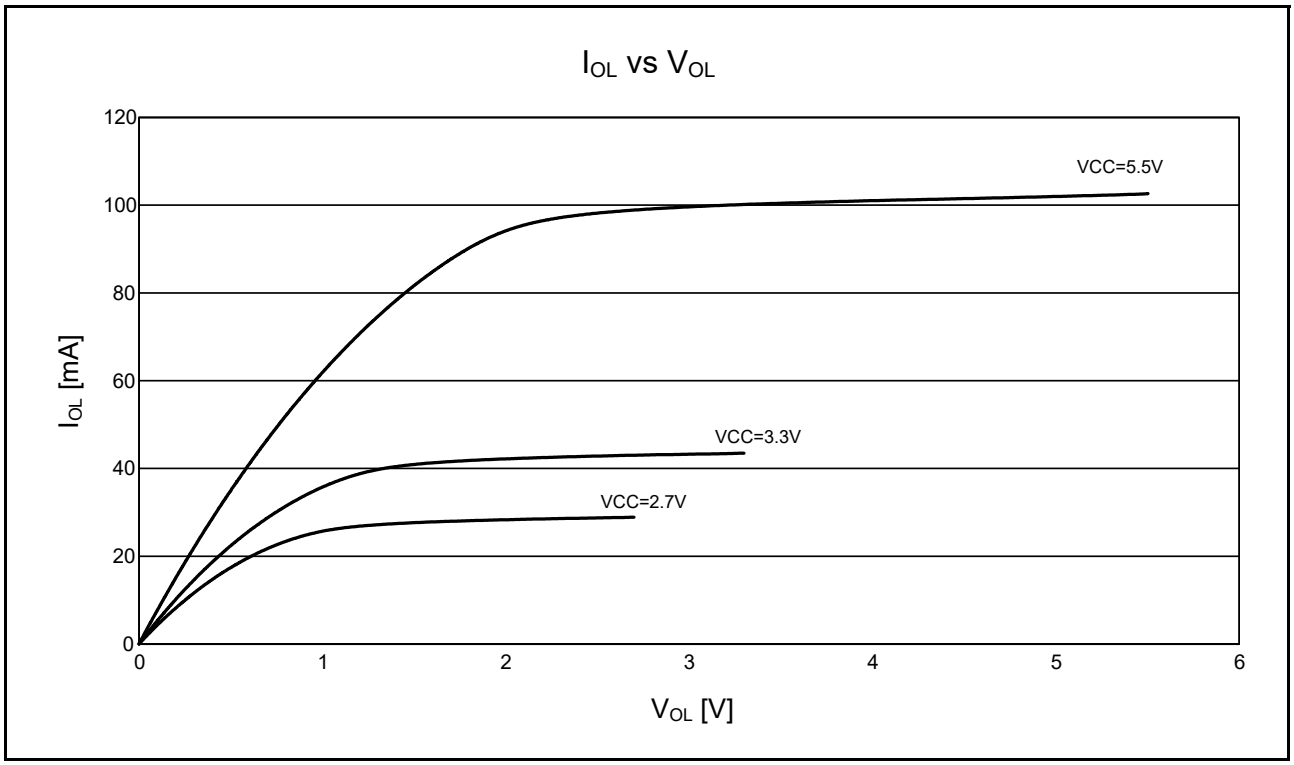


Figure 5.22 V_{OL} and I_{OL} Voltage Characteristics of RIIC Output Pin at T_a = 25°C (Reference Data)

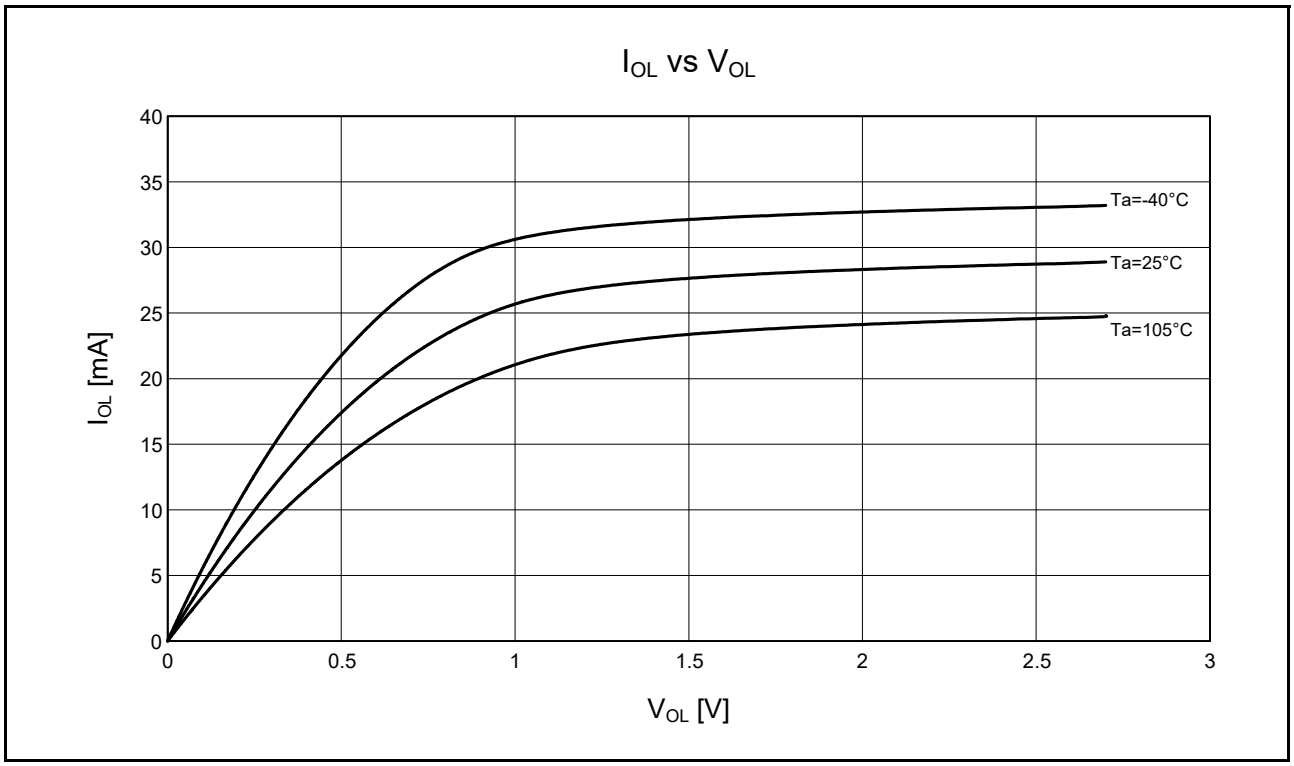


Figure 5.23 V_{OL} and I_{OL} Temperature Characteristics of RIIC Output Pin at VCC = 2.7 V (Reference Data)

5.3 AC Characteristics

5.3.1 Clock Timing

Table 5.22 Operating Frequency Value (High-Speed Operating Mode)

Conditions: 1.8 V ≤ VCC = AVCC0 < 2.0 V, 2.0 V ≤ VCC ≤ 5.5 V, 2.0 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, Ta = –40 to +105°C

Item		Symbol	VCC			Unit
			1.8 V ≤ VCC < 2.4 V	2.4 V ≤ VCC < 2.7 V	2.7 V ≤ VCC ≤ 5.5 V	
Maximum operating frequency*4	System clock (ICLK)	f_{max}	8	16	32	MHz
	FlashIF clock (FCLK)*1, *2		8	16	32	
	Peripheral module clock (PCLKB)		8	16	32	
	Peripheral module clock (PCLKD)*3		8	16	32	

Note 1. The lower-limit frequency of FCLK is 1 MHz during programming or erasing of the flash memory. When using FCLK at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.
Note 2. The frequency accuracy of FCLK should be ±3.5%.
Note 3. The lower-limit frequency of PCLKD is 4 MHz at 2.4 V or above and 1 MHz at below 2.4 V when the A/D converter is in use.
Note 4. The maximum operating frequency does not include HOCO error or PLL jitter. See Table 5.25, Clock Timing.

Table 5.23 Operating Frequency Value (Middle-Speed Operating Mode)

Conditions: 1.8 V ≤ VCC = AVCC0 < 2.0 V, 2.0 V ≤ VCC ≤ 5.5 V, 2.0 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, Ta = –40 to +105°C

Item		Symbol	VCC			Unit
			1.8 V ≤ VCC < 2.4 V	2.4 V ≤ VCC < 2.7 V	2.7 V ≤ VCC ≤ 5.5 V	
Maximum operating frequency*4	System clock (ICLK)	f_{max}	8	12	12	MHz
	FlashIF clock (FCLK)*1, *2		8	12	12	
	Peripheral module clock (PCLKB)		8	12	12	
	Peripheral module clock (PCLKD)*3		8	12	12	

Note 1. The lower-limit frequency of FCLK is 1 MHz during programming or erasing of the flash memory. When using FCLK at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.
Note 2. The frequency accuracy of FCLK should be ±3.5%.
Note 3. The lower-limit frequency of PCLKD is 4 MHz at 2.4 V or above and 1 MHz at below 2.4 V when the A/D converter is in use.
Note 4. The maximum operating frequency does not include HOCO error or PLL jitter. See Table 5.25, Clock Timing

Table 5.24 Operating Frequency Value (Low-Speed Operating Mode)

Conditions: 1.8 V ≤ VCC = AVCC0 < 2.0 V, 2.0 V ≤ VCC ≤ 5.5 V, 2.0 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, Ta = –40 to +105°C

Item		Symbol	VCC			Unit
			1.8 V ≤ VCC < 2.4 V	2.4 V ≤ VCC < 2.7 V	2.7 V ≤ VCC ≤ 5.5 V	
Maximum operating frequency	System clock (ICLK)	f_{max}	32.768			kHz
	FlashIF clock (FCLK)*1		32.768			
	Peripheral module clock (PCLKB)		32.768			
	Peripheral module clock (PCLKD)*2		32.768			

Note 1. Programming and erasing the flash memory is impossible.
Note 2. The A/D converter cannot be used.

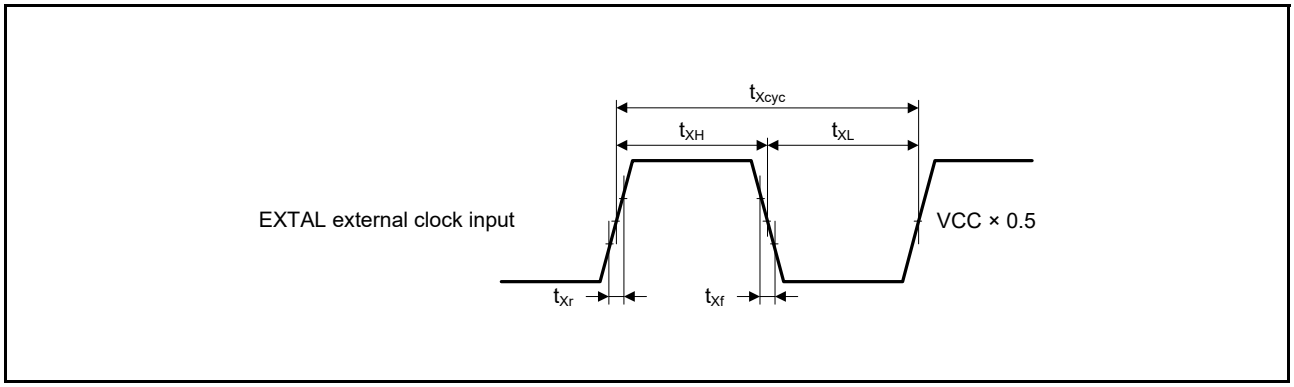


Figure 5.26 EXTAL External Clock Input Timing

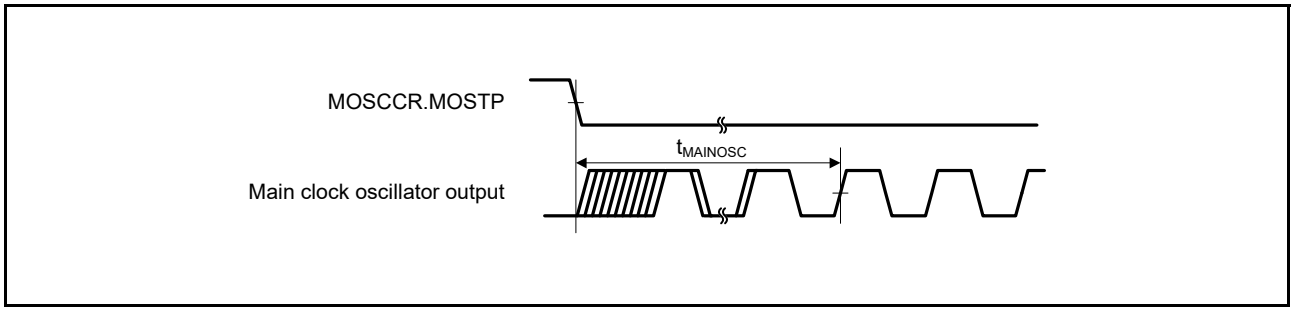


Figure 5.27 Main Clock Oscillation Start Timing

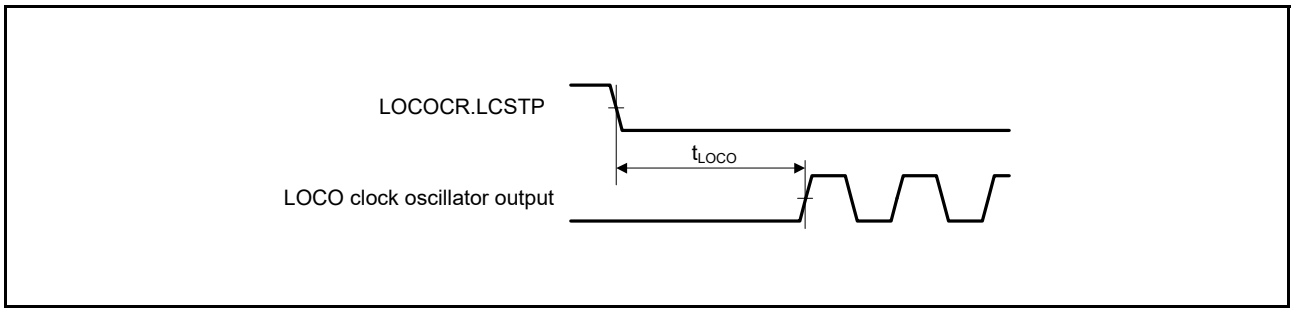


Figure 5.28 LOCO Clock Oscillation Start Timing

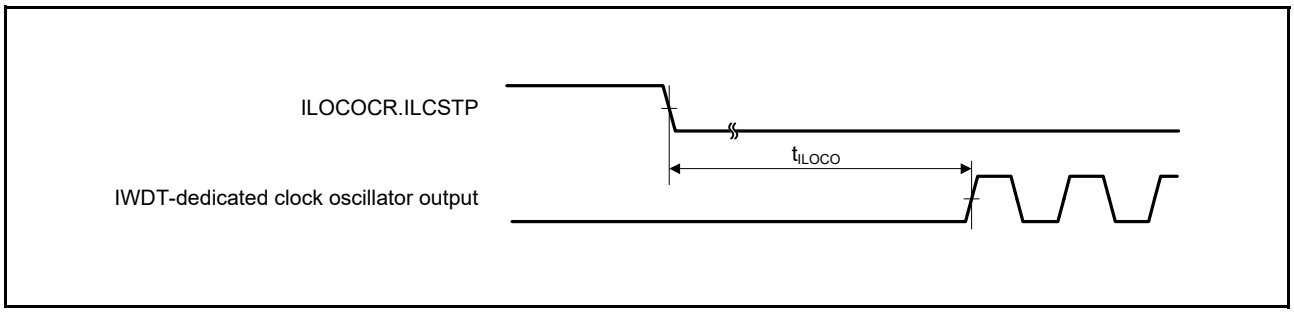


Figure 5.29 IWDT-Dedicated Clock Oscillation Start Timing

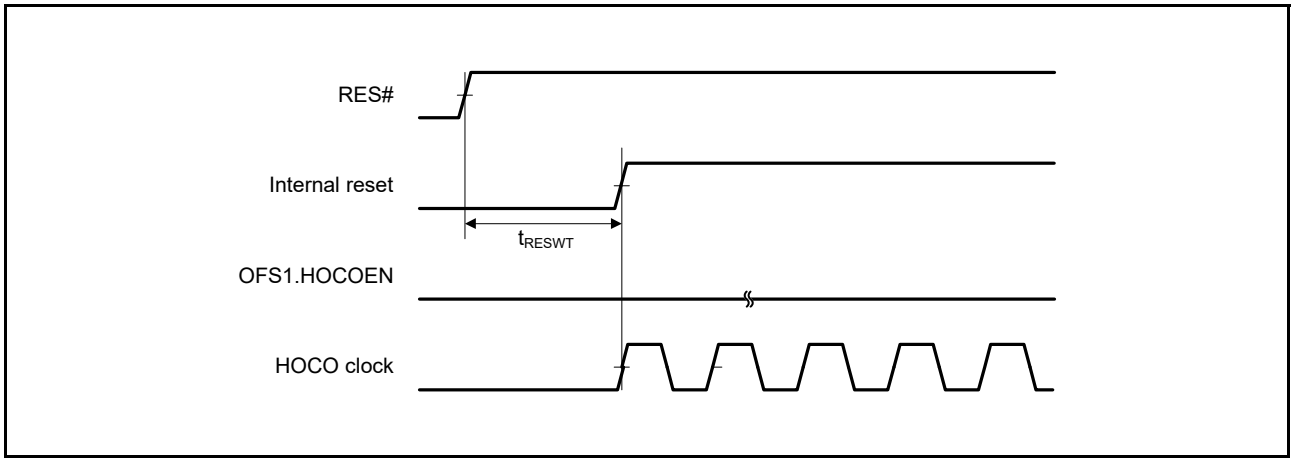


Figure 5.30 HOCO Clock Oscillation Start Timing (After Reset is Canceled by Setting OFS1.HOCOEN Bit to 0)

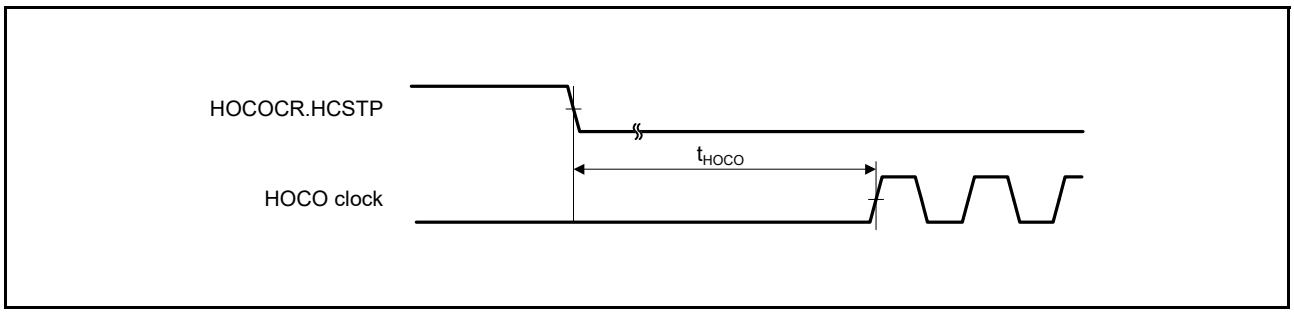


Figure 5.31 HOCO Clock Oscillation Start Timing (Oscillation is Started by Setting HOCOCR.HCSTP Bit)

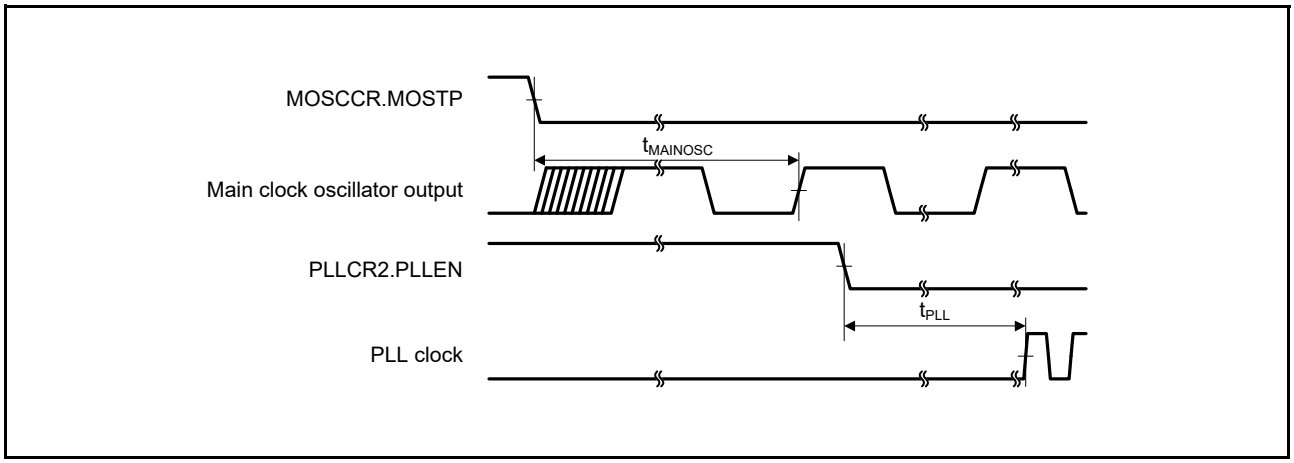


Figure 5.32 PLL Clock Oscillation Start Timing (PLL is Operated after Main Clock Oscillation Has Settled)

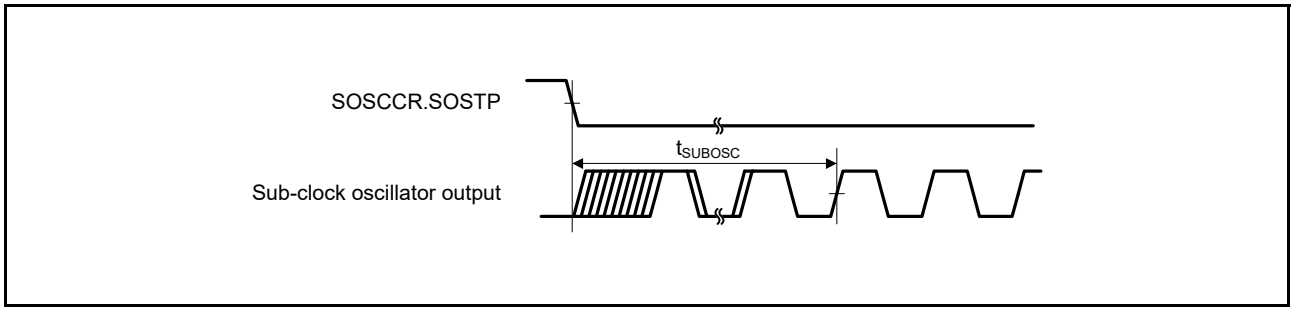


Figure 5.33 Sub-Clock Oscillation Start Timing

Table 5.37 Timing of On-Chip Peripheral Modules (5)

Conditions: 2.7 V ≤ VCC ≤ 5.5 V, 2.7 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item		Symbol	Min.*1	Max.	Unit	Test Conditions
Simple I²C (Standard mode)	SDA rise time	t_{Sr}	—	1000	ns	Figure 5.55
	SDA fall time	t_{Sf}	—	300	ns	
	SDA spike pulse removal time	t_{SP}	0	4 × t_{Pcyc}	ns	
	Data setup time	t_{SDAS}	250	—	ns	
	Data hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b	—	400	pF	
Simple I²C (Fast mode)	SDA rise time	t_{Sr}	—	300	ns	Figure 5.55
	SDA fall time	t_{Sf}	—	300	ns	
	SDA spike pulse removal time	t_{SP}	0	4 × t_{Pcyc}	ns	
	Data setup time	t_{SDAS}	100	—	ns	
	Data hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b	—	400	pF	

Note: t_{Pcyc}: PCLK cycle

Note 1. C_b is the total capacitance of the bus lines.

Table 5.38 Timing of On-Chip Peripheral Modules (6)

Conditions: 2.4 V ≤ VCC ≤ 5.5 V, 2.4 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item		Min.	Max.	Unit	Test Conditions
REMC	Increase of the operating clock frequency at a transition to software standby mode	—	1.5	%	REMCON1.CSRC[3:0] = x101b (with the HOCO clock/512 selected) HOFCR.HOFXIN = 1 (when the HOCO oscillation is set to be continued)
	The period for the change in the operating clock frequency at a transition to software standby mode	—	400	µs	

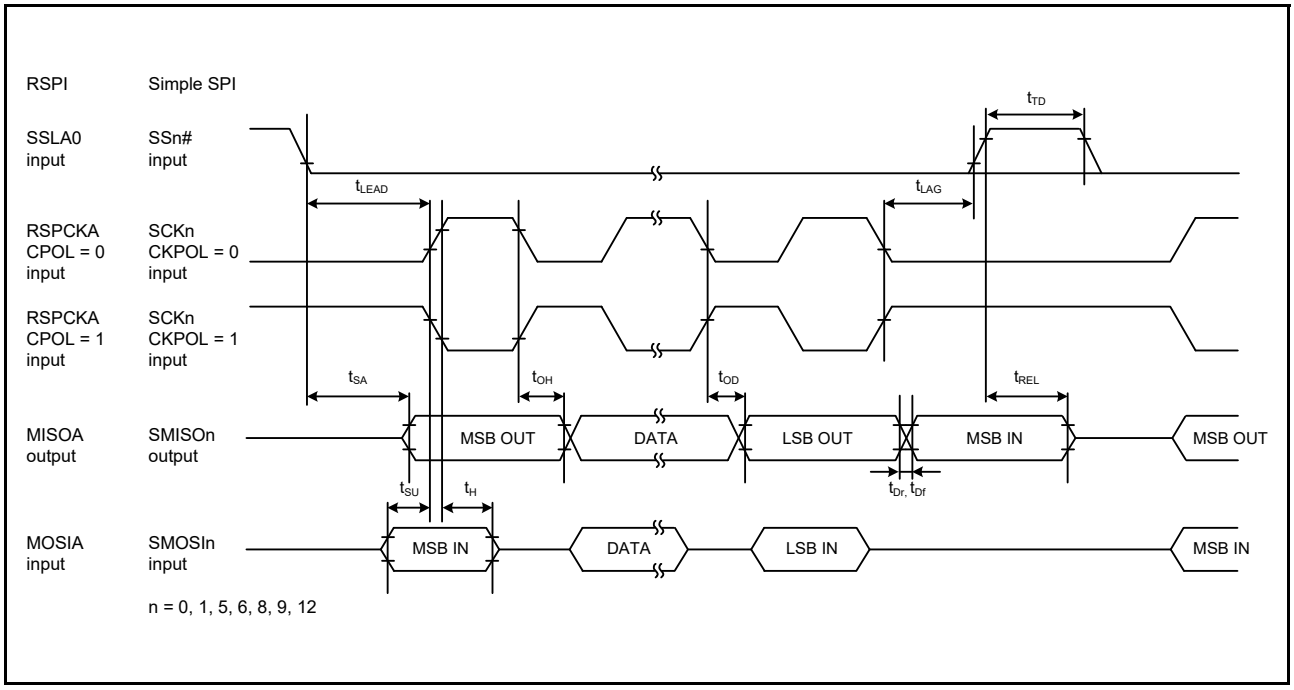


Figure 5.53 RSPI Timing (Slave, CPHA = 0) and Simple SPI Clock Timing (Slave, CKPH = 1)

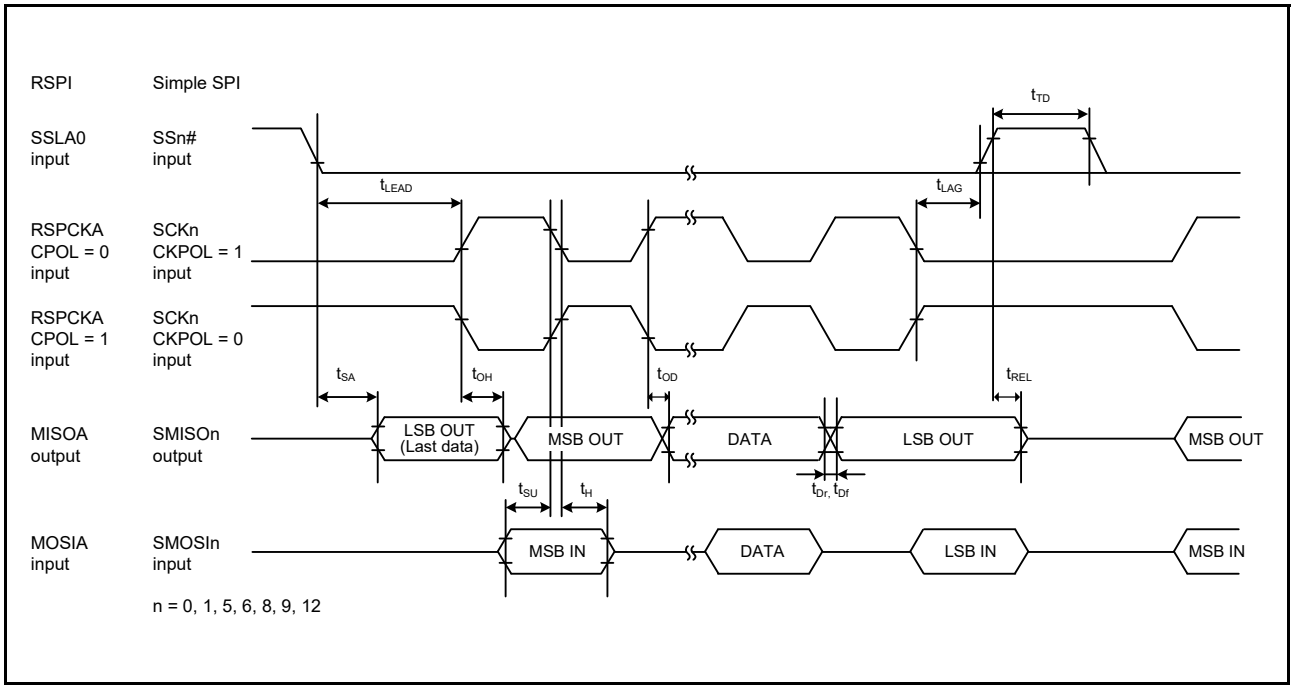
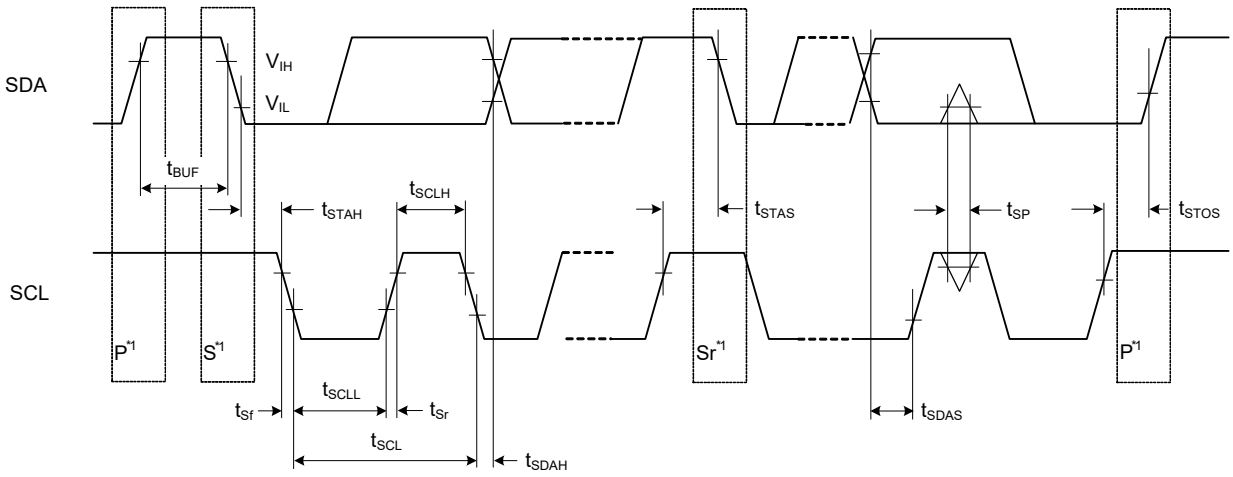


Figure 5.54 RSPI Timing (Slave, CPHA = 1) and Simple SPI Clock Timing (Slave, CKPH = 0)



Note 1. S, P, and Sr indicate the following conditions, respectively.
S: START condition
P: STOP condition
Sr: Repeated START condition

Test conditions
V_{IH} = VCC × 0.7, V_{IL} = VCC × 0.3

Figure 5.55 RIIC Bus Interface Input/Output Timing and Simple I²C Bus Interface Input/Output Timing

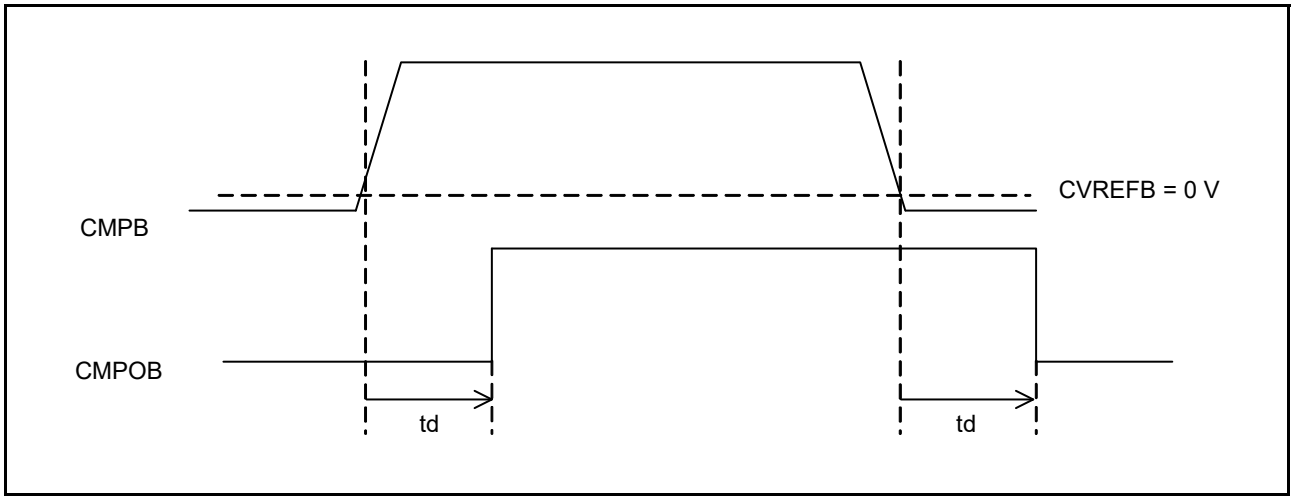


Figure 5.59 Comparator Output Delay Time in Comparator High-Speed Mode and Low-Speed Mode

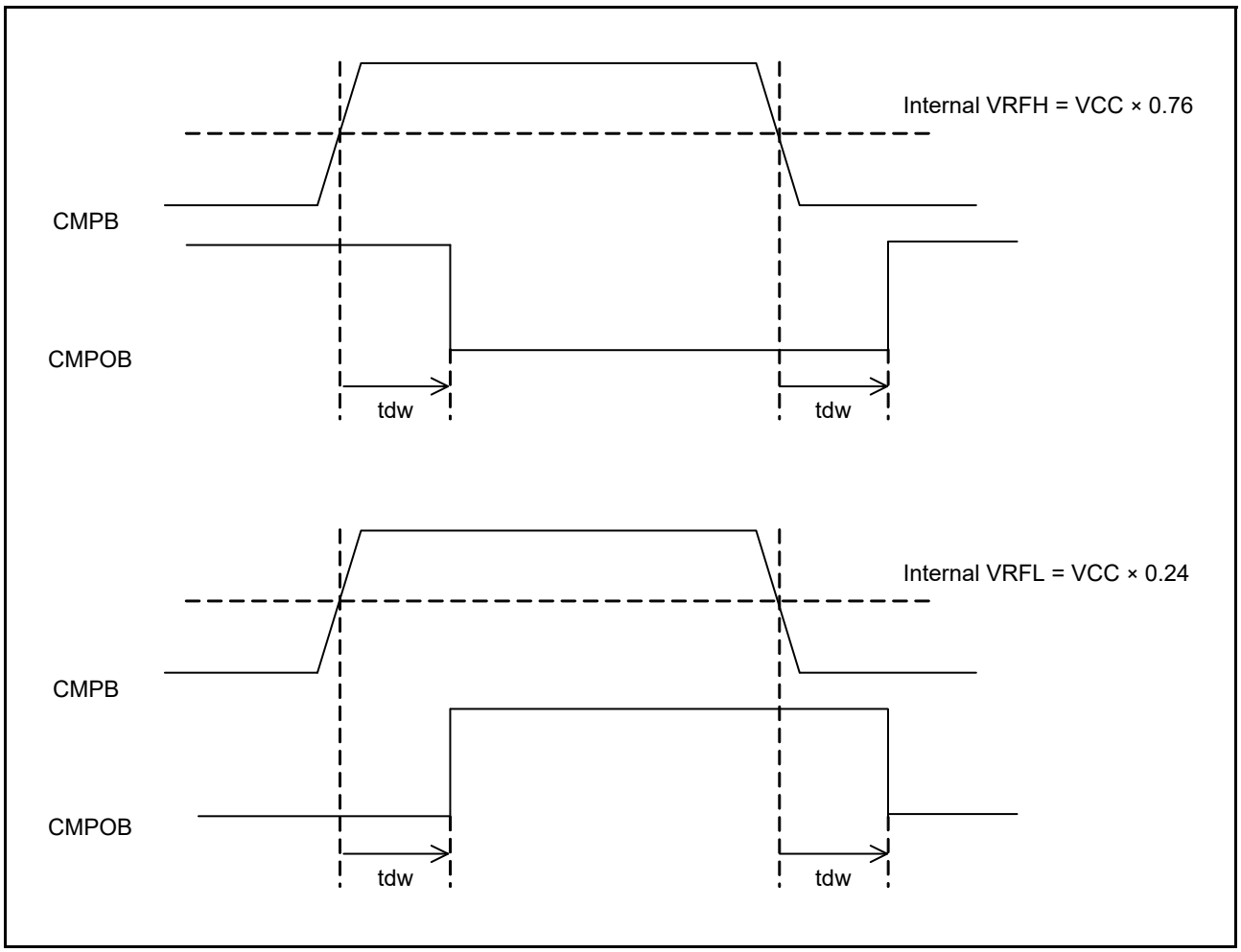


Figure 5.60 Comparator Output Delay Time in High-Speed Mode with Window Function Enabled

5.11 ROM (Flash Memory for Code Storage) Characteristics

Table 5.52 ROM (Flash Memory for Code Storage) Characteristics (1)

Item		Symbol	Min.	Typ.	Max.	Unit	Conditions
Reprogramming/erasure cycle*1		N_{PEC}	1000	—	—	Times	
Data retention	After 1000 times of N_{PEC}	t_{DRP}	20*2, *3	—	—	Year	T_a = +85°C

Note 1. Definition of reprogram/erase cycle: The reprogram/erase cycle is the number of erasing for each block. When the reprogram/erase cycle is n times (n = 1000), erasing can be performed n times for each block. For instance, when 4-byte programming is performed 256 times for different addresses in 1-Kbyte block and then the entire block is erased, the reprogram/erase cycle is counted as one. However, programming the same address for several times as one erasing is not enabled (overwriting is prohibited).
Note 2. Characteristic when using the flash memory programmer and the self-programming library provided from Renesas Electronics.
Note 3. This result is obtained from reliability testing.

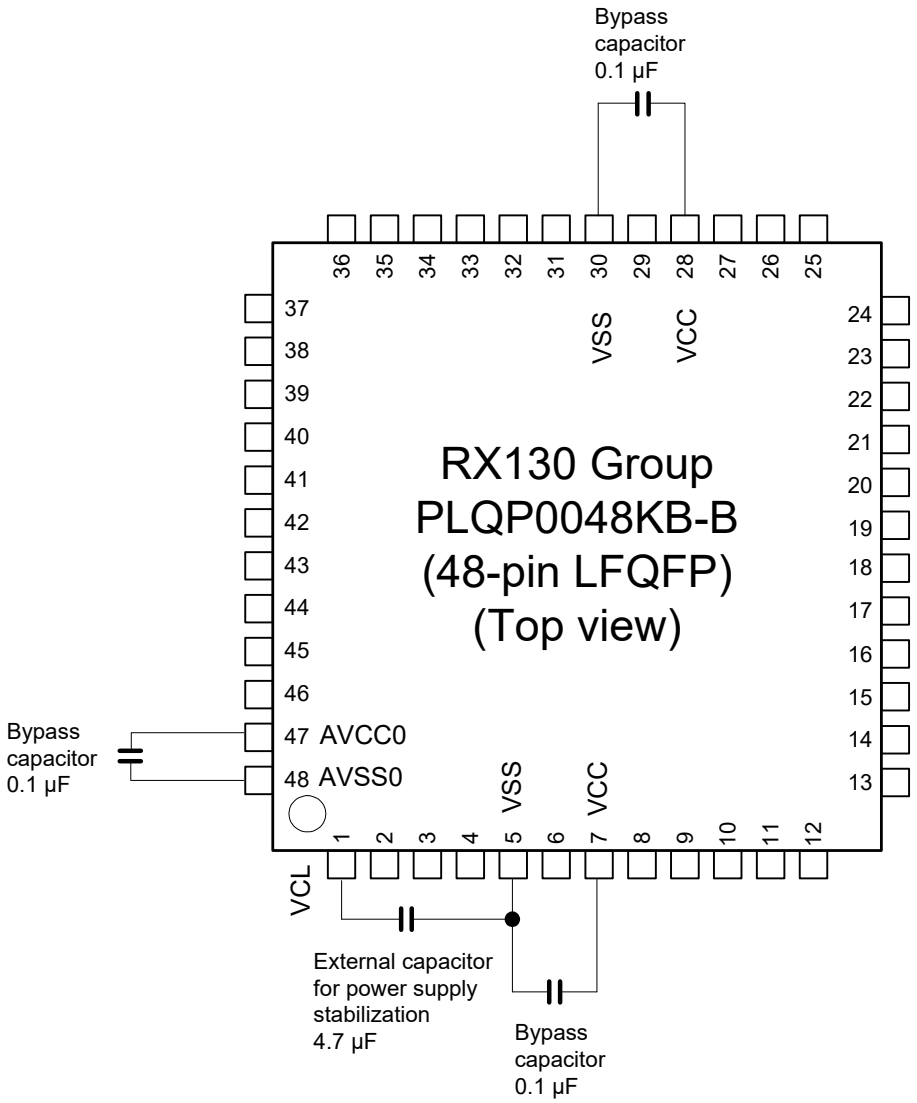
Table 5.53 ROM (Flash Memory for Code Storage) Characteristics (2) High-Speed Operating Mode

Conditions: 2.7 V ≤ VCC ≤ 5.5 V, 2.7 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V

Temperature range for the programming/erasure operation: T_a = –40 to +105°C

Item		Symbol	FCLK = 1 MHz			FCLK = 32 MHz			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Programming time	4-byte	t_{P4}	—	103	931	—	52	489	µs
Erasure time	1-Kbyte	t_{E1K}	—	8.23	267	—	5.48	214	ms
	256-Kbyte	t_{E256K}	—	407	928	—	39	457	ms
Blank check time	4-byte	t_{BC4}	—	—	48	—	—	15.9	µs
	1-Kbyte	t_{BC1K}	—	—	1.58	—	—	0.127	ms
Erase operation forcible stop time		t_{SED}	—	—	21.6	—	—	12.8	µs
Start-up area switching setting time		t_{SAS}	—	12.6	543	—	6.16	432	ms
Access window setting time		t_{AWS}	—	12.6	543	—	6.16	432	ms
ROM mode transition wait time 1		t_{DIS}	2	—	—	2	—	—	µs
ROM mode transition wait time 2		t_{MS}	5	—	—	5	—	—	µs

Note: Does not include the time until each operation of the flash memory is started after instructions are executed by software.
Note: The lower-limit frequency of FCLK is 1 MHz during programming or erasing of the flash memory. When using FCLK at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.
Note: The frequency accuracy of FCLK should be ±3.5%.



Note. Do not apply the power supply voltage to the VCL pin.
Use a 4.7-µF multilayer ceramic for the VCL pin and place it close to the pin.
A recommended value is shown for the capacitance of the bypass capacitors.

Figure 5.70 Connecting Capacitors (48 Pins)

NOTES FOR CMOS DEVICES

(1) VOLTAGE APPLICATION WAVEFORM AT INPUT PIN: Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between VIL (MAX) and VIH (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between VIL (MAX) and VIH (MIN).

(2) HANDLING OF UNUSED INPUT PINS: Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to VDD or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.

(3) PRECAUTION AGAINST ESD: A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.

(4) STATUS BEFORE INITIALIZATION: Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.

(5) POWER ON/OFF SEQUENCE: In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current. The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.

(6) INPUT OF SIGNAL DURING POWER OFF STATE : Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.