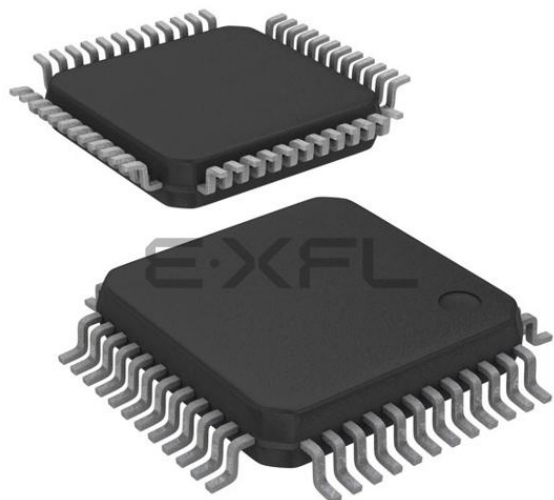




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Details

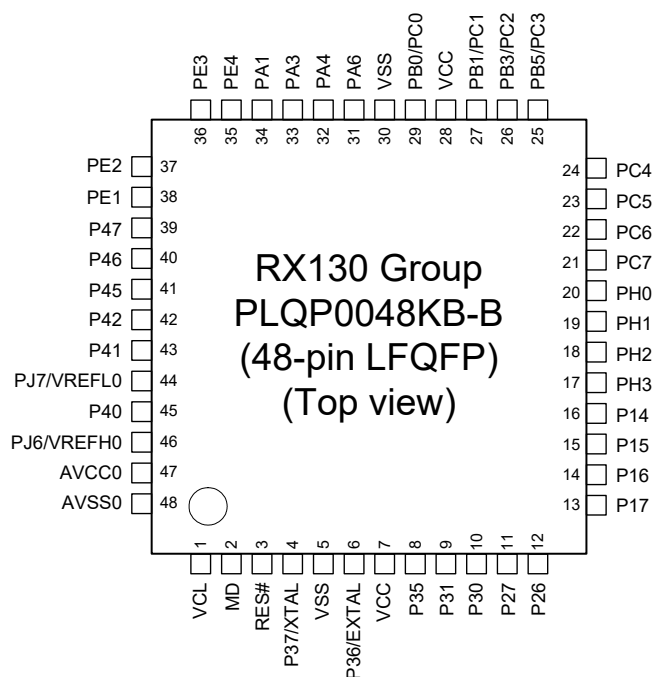
Product Status	Active
Core Processor	RX
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	I ² C, LINbus, SCI, SPI
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	38
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	8K x 8
RAM Size	48K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 10x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LFQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f51308adfl-30

1.2 List of Products

Table 1.3 is a lists of products, and Figure 1.1 shows how to read the product part no., memory capacity, and package type.

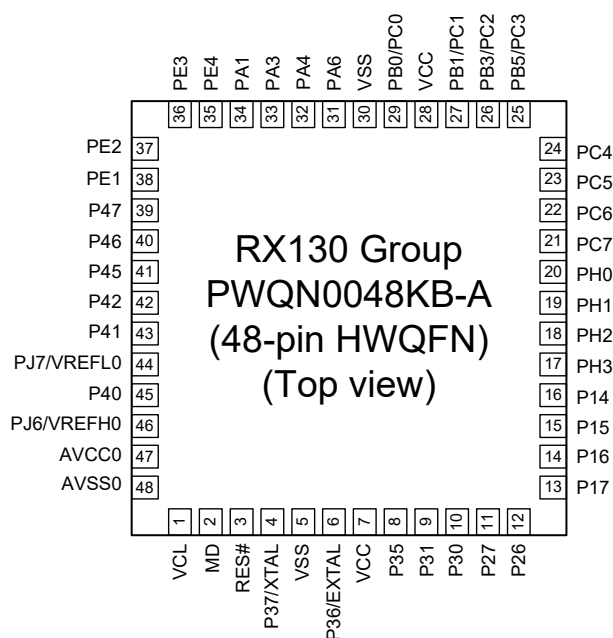
Table 1.3 List of Products (1/2)

Group	Part No.	Part No. (for Orders)	Package	ROM Capacity	RAM Capacity	E2 DataFlash	Operating Frequency (Max.)	Operating Temperature												
RX130	R5F51308ADFP	R5F51308ADFP#30	PLQP0100KB-B	512 Kbytes	48 Kbytes	8 Kbytes	32 MHz	−40 to +85°C												
	R5F51308ADFN	R5F51308ADFN#30	PLQP0080KB-B																	
	R5F51308ADFM	R5F51308ADFM#30	PLQP0064KB-C																	
	R5F51308ADFK	R5F51308ADFK#30	PLQP0064GA-A																	
	R5F51308ADFL	R5F51308ADFL#30	PLQP0048KB-B																	
	R5F51308ADNE	R5F51308ADNE#U0	PWQN0048KB-A																	
	R5F51307ADFP	R5F51307ADFP#30	PLQP0100KB-B	384 Kbytes																
	R5F51307ADFN	R5F51307ADFN#30	PLQP0080KB-B																	
	R5F51307ADFM	R5F51307ADFM#30	PLQP0064KB-C																	
	R5F51307ADFK	R5F51307ADFK#30	PLQP0064GA-A																	
	R5F51307ADFL	R5F51307ADFL#30	PLQP0048KB-B																	
	R5F51307ADNE	R5F51307ADNE#U0	PWQN0048KB-A																	
	R5F51306ADFP	R5F51306ADFP#30	PLQP0100KB-B	256 Kbytes	32 Kbytes															
	R5F51306ADFN	R5F51306ADFN#30	PLQP0080KB-B																	
	R5F51306ADFM	R5F51306ADFM#30	PLQP0064KB-C																	
	R5F51306ADFK	R5F51306ADFK#30	PLQP0064GA-A																	
	R5F51306ADFL	R5F51306ADFL#30	PLQP0048KB-B																	
	R5F51306ADNE	R5F51306ADNE#U0	PWQN0048KB-A																	
	R5F51305ADFP	R5F51305ADFP#30	PLQP0100KB-B	128 Kbytes	16 Kbytes															
	R5F51305ADFN	R5F51305ADFN#30	PLQP0080KB-B																	
	R5F51305ADFM	R5F51305ADFM#30	PLQP0064KB-C																	
	R5F51305ADFK	R5F51305ADFK#30	PLQP0064GA-A																	
	R5F51305ADFL	R5F51305ADFL#30	PLQP0048KB-B																	
	R5F51305ADNE	R5F51305ADNE#U0	PWQN0048KB-A																	
	R5F51303ADFN	R5F51303ADFN#30	PLQP0080KB-B	64 Kbytes	10 Kbytes															
	R5F51303ADFM	R5F51303ADFM#30	PLQP0064KB-C																	
	R5F51303ADFK	R5F51303ADFK#30	PLQP0064GA-A																	
	R5F51303ADFL	R5F51303ADFL#30	PLQP0048KB-B																	
	R5F51303ADNE	R5F51303ADNE#U0	PWQN0048KB-A																	



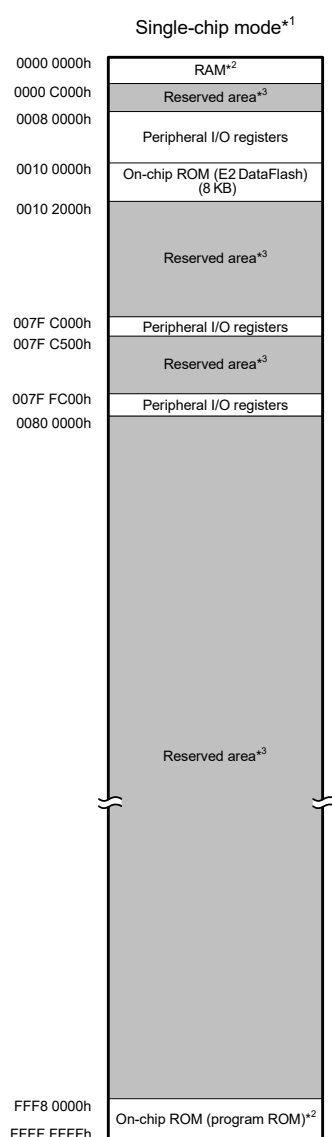
Note: This figure indicates the power supply pins and I/O ports.
For the pin configuration, see the table "List of Pins and Pin Functions (48-Pin LQFP/HWQFN)".

Figure 1.6 Pin Assignments of the 48-Pin LQFP



Note: It is recommended to connect an exposed die pad to VSS.
Note: This figure indicates the power supply pins and I/O ports.
For the pin configuration, see the table "List of Pins and Pin Functions (48-Pin LQFP/HWQFN)".

Figure 1.7 Pin Assignments of the 48-Pin HWQFN



Note 1. The address space in boot mode is the same as the address space in single-chip mode.

Note 2. The capacity of ROM/RAM differs depending on the products.

ROM (bytes)		RAM (bytes)	
Capacity	Address	Capacity	Address
512 Kbytes	FFF8 0000h to FFFF FFFFh	48 Kbytes	0000 0000h to 0000 BFFFh
384 Kbytes	FFFA 8000h to FFFF FFFFh		
256 Kbytes	FFFC 0000h to FFFF FFFFh	32 Kbytes	0000 0000h to 0000 7FFFh
128 Kbytes	FFFE 0000h to FFFF FFFFh	16 Kbytes	0000 0000h to 0000 3FFFh
64 Kbytes	FFFF 0000h to FFFF FFFFh	10 Kbytes	0000 0000h to 0000 27FFh

Note: See Table 1.3, List of Products, for the product type name.

Note 3. Reserved areas should not be accessed.

Figure 3.1 Memory Map in Each Operating Mode

4.1 I/O Register Addresses (Address Order)

Table 4.1 List of I/O Registers (Address Order) (1 / 18)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles
0008 0000h	SYSTEM	Mode Monitor Register	MDMONR	16	16	3 ICLK
0008 0008h	SYSTEM	System Control Register 1	SYSCR1	16	16	3 ICLK
0008 000Ch	SYSTEM	Standby Control Register	SBYCR	16	16	3 ICLK
0008 0010h	SYSTEM	Module Stop Control Register A	MSTPCRA	32	32	3 ICLK
0008 0014h	SYSTEM	Module Stop Control Register B	MSTPCRB	32	32	3 ICLK
0008 0018h	SYSTEM	Module Stop Control Register C	MSTPCRC	32	32	3 ICLK
0008 001Ch	SYSTEM	Module Stop Control Register D	MSTPCRD	32	32	3 ICLK
0008 0020h	SYSTEM	System Clock Control Register	SCKCR	32	32	3 ICLK
0008 0026h	SYSTEM	System Clock Control Register 3	SCKCR3	16	16	3 ICLK
0008 0028h	SYSTEM	PLL Control Register	PLLCR	16	16	3 ICLK
0008 002Ah	SYSTEM	PLL Control Register 2	PLLCR2	8	8	3 ICLK
0008 0032h	SYSTEM	Main Clock Oscillator Control Register	MOSCCR	8	8	3 ICLK
0008 0033h	SYSTEM	Sub-Clock Oscillator Control Register	SOSCCR	8	8	3 ICLK
0008 0034h	SYSTEM	Low-Speed On-Chip Oscillator Control Register	LOCOCR	8	8	3 ICLK
0008 0035h	SYSTEM	IWDT-Dedicated On-Chip Oscillator Control Register	ILOCOCR	8	8	3 ICLK
0008 0036h	SYSTEM	High-Speed On-Chip Oscillator Control Register	HOCOCR	8	8	3 ICLK
0008 003Ch	SYSTEM	Oscillation Stabilization Flag Register	OSCOVFSR	8	8	3 ICLK
0008 003Dh	SYSTEM	High-Speed On-Chip Oscillator Forced Oscillation Control Register	HOFCR	8	8	3 ICLK
0008 003Eh	SYSTEM	CLKOUT Output Control Register	CKOCR	16	16	3 ICLK
0008 0040h	SYSTEM	Oscillation Stop Detection Control Register	OSTDCR	8	8	3 ICLK
0008 0041h	SYSTEM	Oscillation Stop Detection Status Register	OSTDSR	8	8	3 ICLK
0008 0060h	SYSTEM	Low-Speed On-Chip Oscillator Trimming Register	LOCOTRR	8	8	3 ICLK
0008 0064h	SYSTEM	IWDT-Dedicated On-Chip Oscillator Trimming Register	ILOCOTRR	8	8	3 ICLK
0008 0068h	SYSTEM	High-Speed On-Chip Oscillator Trimming Register 0	HOCOTRR0	8	8	3 ICLK
0008 00A0h	SYSTEM	Operating Power Control Register	OPCCR	8	8	3 ICLK
0008 00A1h	SYSTEM	Sleep Mode Return Clock Source Switching Register	RSTCKCR	8	8	3 ICLK
0008 00A2h	SYSTEM	Main Clock Oscillator Wait Control Register	MOSCWTCR	8	8	3 ICLK
0008 00AAh	SYSTEM	Sub Operating Power Control Register	SOPCCR	8	8	3 ICLK
0008 00B0h	LPT	Low-Power Timer Control Register 1	LPTCR1	8	8	3 ICLK
0008 00B1h	LPT	Low-Power Timer Control Register 2	LPTCR2	8	8	3 ICLK
0008 00B2h	LPT	Low-Power Timer Control Register 3	LPTCR3	8	8	3 ICLK
0008 00B4h	LPT	Low-Power Timer Cycle Setting Register	LPTPRD	16	16	3 ICLK
0008 00B8h	LPT	Low-Power Timer Compare Register 0	LPCMR0	16	16	3 ICLK
0008 00BCh	LPT	Low-Power Timer Standby Wakeup Enable Register	LPWUCR	16	16	3 ICLK
0008 00C0h	SYSTEM	Reset Status Register 2	RSTSR2	8	8	3 ICLK
0008 00C2h	SYSTEM	Software Reset Register	SWRR	16	16	3 ICLK
0008 00E0h	SYSTEM	Voltage Monitoring 1 Circuit Control Register 1	LVD1CR1	8	8	3 ICLK
0008 00E1h	SYSTEM	Voltage Monitoring 1 Circuit Status Register	LVD1SR	8	8	3 ICLK
0008 00E2h	SYSTEM	Voltage Monitoring 2 Circuit Control Register 1	LVD2CR1	8	8	3 ICLK
0008 00E3h	SYSTEM	Voltage Monitoring 2 Circuit Status Register	LVD2SR	8	8	3 ICLK
0008 03FEh	SYSTEM	Protect Register	PRCR	16	16	3 ICLK
0008 1300h	BSC	Bus Error Status Clear Register	BERCLR	8	8	2 ICLK
0008 1304h	BSC	Bus Error Monitoring Enable Register	BEREN	8	8	2 ICLK
0008 1308h	BSC	Bus Error Status Register 1	BERSR1	8	8	2 ICLK
0008 130Ah	BSC	Bus Error Status Register 2	BERSR2	16	16	2 ICLK
0008 1310h	BSC	Bus Priority Control Register	BUSPRI	16	16	2 ICLK
0008 2400h	DTC	DTC Control Register	DTCCR	8	8	2 ICLK
0008 2404h	DTC	DTC Vector Base Register	DTCVBR	32	32	2 ICLK
0008 2408h	DTC	DTC Address Mode Register	DTCADMOD	8	8	2 ICLK

Table 4.1 List of I/O Registers (Address Order) (3 / 18)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles
0008 820Bh	TMR1	Timer Counter Control Register	TCCR	8	8	2 or 3 PCLKB
0008 820Ch	TMR0	Timer Counter Start Register	TCSTR	8	8	2 or 3 PCLKB
0008 8210h	TMR2	Timer Control Register	TCR	8	8	2 or 3 PCLKB
0008 8211h	TMR3	Timer Control Register	TCR	8	8	2 or 3 PCLKB
0008 8212h	TMR2	Timer Control/Status Register	TCSR	8	8	2 or 3 PCLKB
0008 8213h	TMR3	Timer Control/Status Register	TCSR	8	8	2 or 3 PCLKB
0008 8214h	TMR2	Time Constant Register A	TCORA	8	8	2 or 3 PCLKB
0008 8214h	TMR23	Time Constant Register A	TCORA	16	16	2 or 3 PCLKB
0008 8215h	TMR3	Time Constant Register A	TCORA	8	8	2 or 3 PCLKB
0008 8216h	TMR2	Time Constant Register B	TCORB	8	8	2 or 3 PCLKB
0008 8216h	TMR23	Time Constant Register B	TCORB	16	16	2 or 3 PCLKB
0008 8217h	TMR3	Time Constant Register B	TCORB	8	8	2 or 3 PCLKB
0008 8218h	TMR2	Timer Counter	TCNT	8	8	2 or 3 PCLKB
0008 8218h	TMR23	Timer Counter	TCNT	16	16	2 or 3 PCLKB
0008 8219h	TMR3	Timer Counter	TCNT	8	8	2 or 3 PCLKB
0008 821Ah	TMR2	Timer Counter Control Register	TCCR	8	8	2 or 3 PCLKB
0008 821Ah	TMR23	Timer Counter Control Register	TCCR	16	16	2 or 3 PCLKB
0008 821Bh	TMR3	Timer Counter Control Register	TCCR	8	8	2 or 3 PCLKB
0008 821Ch	TMR2	Timer Counter Start Register	TCSTR	8	8	2 or 3 PCLKB
0008 8280h	CRC	CRC Control Register	CRCCR	8	8	2 or 3 PCLKB
0008 8281h	CRC	CRC Data Input Register	CRCDIR	8	8	2 or 3 PCLKB
0008 8282h	CRC	CRC Data Output Register	CRCDOR	16	16	2 or 3 PCLKB
0008 8300h	RIIC0	I ² C Bus Control Register 1	ICCR1	8	8	2 or 3 PCLKB
0008 8301h	RIIC0	I ² C Bus Control Register 2	ICCR2	8	8	2 or 3 PCLKB
0008 8302h	RIIC0	I ² C Bus Mode Register 1	ICMR1	8	8	2 or 3 PCLKB
0008 8303h	RIIC0	I ² C Bus Mode Register 2	ICMR2	8	8	2 or 3 PCLKB
0008 8304h	RIIC0	I ² C Bus Mode Register 3	ICMR3	8	8	2 or 3 PCLKB
0008 8305h	RIIC0	I ² C Bus Function Enable Register	ICFER	8	8	2 or 3 PCLKB
0008 8306h	RIIC0	I ² C Bus Status Enable Register	ICSER	8	8	2 or 3 PCLKB
0008 8307h	RIIC0	I ² C Bus Interrupt Enable Register	ICIER	8	8	2 or 3 PCLKB
0008 8308h	RIIC0	I ² C Bus Status Register 1	ICSR1	8	8	2 or 3 PCLKB
0008 8309h	RIIC0	I ² C Bus Status Register 2	ICSR2	8	8	2 or 3 PCLKB
0008 830Ah	RIIC0	Slave Address Register L0	SARL0	8	8	2 or 3 PCLKB
0008 830Bh	RIIC0	Slave Address Register U0	SARU0	8	8	2 or 3 PCLKB
0008 830Ch	RIIC0	Slave Address Register L1	SARL1	8	8	2 or 3 PCLKB
0008 830Dh	RIIC0	Slave Address Register U1	SARU1	8	8	2 or 3 PCLKB
0008 830Eh	RIIC0	Slave Address Register L2	SARL2	8	8	2 or 3 PCLKB
0008 830Fh	RIIC0	Slave Address Register U2	SARU2	8	8	2 or 3 PCLKB
0008 8310h	RIIC0	I ² C Bus Bit Rate Low-Level Register	ICBRL	8	8	2 or 3 PCLKB
0008 8311h	RIIC0	I ² C Bus Bit Rate High-Level Register	ICBRH	8	8	2 or 3 PCLKB
0008 8312h	RIIC0	I ² C Bus Transmit Data Register	ICDRT	8	8	2 or 3 PCLKB
0008 8313h	RIIC0	I ² C Bus Receive Data Register	ICDRR	8	8	2 or 3 PCLKB
0008 8380h	RSPI0	RSPI Control Register	SPCR	8	8	2 or 3 PCLKB
0008 8381h	RSPI0	RSPI Slave Select Polarity Register	SSLP	8	8	2 or 3 PCLKB
0008 8382h	RSPI0	RSPI Pin Control Register	SPPCR	8	8	2 or 3 PCLKB
0008 8383h	RSPI0	RSPI Status Register	SPSR	8	8	2 or 3 PCLKB
0008 8384h	RSPI0	RSPI Data Register	SPDR	32	16, 32	2 or 3 PCLKB/2 ICLK
0008 8388h	RSPI0	RSPI Sequence Control Register	SPSCR	8	8	2 or 3 PCLKB
0008 8389h	RSPI0	RSPI Sequence Status Register	SPSSR	8	8	2 or 3 PCLKB
0008 838Ah	RSPI0	RSPI Bit Rate Register	SPBR	8	8	2 or 3 PCLKB
0008 838Bh	RSPI0	RSPI Data Control Register	SPDCR	8	8	2 or 3 PCLKB
0008 838Ch	RSPI0	RSPI Clock Delay Register	SPCKD	8	8	2 or 3 PCLKB

Table 4.1 List of I/O Registers (Address Order) (4 / 18)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles
0008 838Dh	RSPI0	RSPI Slave Select Negation Delay Register	SSLND	8	8	2 or 3 PCLKB
0008 838Eh	RSPI0	RSPI Next-Access Delay Register	SPND	8	8	2 or 3 PCLKB
0008 838Fh	RSPI0	RSPI Control Register 2	SPCR2	8	8	2 or 3 PCLKB
0008 8390h	RSPI0	RSPI Command Register 0	SPCMD0	16	16	2 or 3 PCLKB
0008 8392h	RSPI0	RSPI Command Register 1	SPCMD1	16	16	2 or 3 PCLKB
0008 8394h	RSPI0	RSPI Command Register 2	SPCMD2	16	16	2 or 3 PCLKB
0008 8396h	RSPI0	RSPI Command Register 3	SPCMD3	16	16	2 or 3 PCLKB
0008 8398h	RSPI0	RSPI Command Register 4	SPCMD4	16	16	2 or 3 PCLKB
0008 839Ah	RSPI0	RSPI Command Register 5	SPCMD5	16	16	2 or 3 PCLKB
0008 839Ch	RSPI0	RSPI Command Register 6	SPCMD6	16	16	2 or 3 PCLKB
0008 839Eh	RSPI0	RSPI Command Register 7	SPCMD7	16	16	2 or 3 PCLKB
0008 8600h	MTU3	Timer Control Register	TCR	8	8	2 or 3 PCLKB
0008 8601h	MTU4	Timer Control Register	TCR	8	8	2 or 3 PCLKB
0008 8602h	MTU3	Timer Mode Register	TMDR	8	8	2 or 3 PCLKB
0008 8603h	MTU4	Timer Mode Register	TMDR	8	8	2 or 3 PCLKB
0008 8604h	MTU3	Timer I/O Control Register H	TIORH	8	8	2 or 3 PCLKB
0008 8605h	MTU3	Timer I/O Control Register L	TIORL	8	8	2 or 3 PCLKB
0008 8606h	MTU4	Timer I/O Control Register H	TIORH	8	8	2 or 3 PCLKB
0008 8607h	MTU4	Timer I/O Control Register L	TIORL	8	8	2 or 3 PCLKB
0008 8608h	MTU3	Timer Interrupt Enable Register	TIER	8	8	2 or 3 PCLKB
0008 8609h	MTU4	Timer Interrupt Enable Register	TIER	8	8	2 or 3 PCLKB
0008 860Ah	MTU	Timer Output Master Enable Registers	TOER	8	8	2 or 3 PCLKB
0008 860Dh	MTU	Timer Gate Control Registers	TGCR	8	8	2 or 3 PCLKB
0008 860Eh	MTU	Timer Output Control Register 1	TOCR1	8	8	2 or 3 PCLKB
0008 860Fh	MTU	Timer Output Control Register 2	TOCR2	8	8	2 or 3 PCLKB
0008 8610h	MTU3	Timer Counter	TCNT	16	16	2 or 3 PCLKB
0008 8612h	MTU4	Timer Counter	TCNT	16	16	2 or 3 PCLKB
0008 8614h	MTU	Timer Cycle Data Register	TCDR	16	16	2 or 3 PCLKB
0008 8616h	MTU	Timer Dead Time Data Register	TDDR	16	16	2 or 3 PCLKB
0008 8618h	MTU3	Timer General Register A	TGRA	16	16	2 or 3 PCLKB
0008 861Ah	MTU3	Timer General Register B	TGRB	16	16	2 or 3 PCLKB
0008 861Ch	MTU4	Timer General Register A	TGRA	16	16	2 or 3 PCLKB
0008 861Eh	MTU4	Timer General Register B	TGRB	16	16	2 or 3 PCLKB
0008 8620h	MTU	Timer Subcounter	TCNTS	16	16	2 or 3 PCLKB
0008 8622h	MTU	Timer Cycle Buffer Register	TCBR	16	16	2 or 3 PCLKB
0008 8624h	MTU3	Timer General Register C	TGRC	16	16	2 or 3 PCLKB
0008 8626h	MTU3	Timer General Register D	TGRD	16	16	2 or 3 PCLKB
0008 8628h	MTU4	Timer General Register C	TGRC	16	16	2 or 3 PCLKB
0008 862Ah	MTU4	Timer General Register D	TGRD	16	16	2 or 3 PCLKB
0008 862Ch	MTU3	Timer Status Register	TSR	8	8	2 or 3 PCLKB
0008 862Dh	MTU4	Timer Status Register	TSR	8	8	2 or 3 PCLKB
0008 8630h	MTU	Timer Interrupt Skipping Set Register	TITCR	8	8	2 or 3 PCLKB
0008 8631h	MTU	Timer Interrupt Skipping Counter	TITCNT	8	8	2 or 3 PCLKB
0008 8632h	MTU	Timer Buffer Transfer Set Register	TBTER	8	8	2 or 3 PCLKB
0008 8634h	MTU	Timer Dead Time Enable Register	TDER	8	8	2 or 3 PCLKB
0008 8636h	MTU	Timer Output Level Buffer Register	TOLBR	8	8	2 or 3 PCLKB
0008 8638h	MTU3	Timer Buffer Operation Transfer Mode Register	TBTM	8	8	2 or 3 PCLKB
0008 8639h	MTU4	Timer Buffer Operation Transfer Mode Register	TBTM	8	8	2 or 3 PCLKB
0008 8640h	MTU4	Timer A/D Converter Start Request Control Register	TADCR	16	16	2 or 3 PCLKB
0008 8644h	MTU4	Timer A/D Converter Start Request Cycle Set Register A	TADCORA	16	16	2 or 3 PCLKB
0008 8646h	MTU4	Timer A/D Converter Start Request Cycle Set Register B	TADCORB	16	16	2 or 3 PCLKB
0008 8648h	MTU4	Timer A/D Converter Start Request Cycle Set Buffer Register A	TADCOBRA	16	16	2 or 3 PCLKB

Table 4.1 List of I/O Registers (Address Order) (7 / 18)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles
0008 905Eh	S12AD	A/D Data Register 31	ADDR31	16	16	2 or 3 PCLKB
0008 907Ah	S12AD	A/D Disconnection Detection Control Register	ADDISCR	8	8	2 or 3 PCLKB
0008 907Dh	S12AD	A/D Event Link Control Register	ADELCCR	8	8	2 or 3 PCLKB
0008 9080h	S12AD	A/D Group Scan Priority Control Register	ADGSPCR	16	16	2 or 3 PCLKB
0008 908Ah	S12AD	A/D High-Potential/Low-Potential Reference Voltage Control Register	ADHVREFCNT	8	8	2 or 3 PCLKB
0008 908Ch	S12AD	A/D Compare Function Window A/B Status Monitor Register	ADWINMON	8	8	2 or 3 PCLKB
0008 9090h	S12AD	A/D Compare Function Control Register	ADCMPCR	16	16	2 or 3 PCLKB
0008 9092h	S12AD	A/D Compare Function Window A Extended Input Select Register	ADCMPSER	8	8	2 or 3 PCLKB
0008 9093h	S12AD	A/D Compare Function Window A Extended Input Comparison Condition Setting Register	ADCMPLER	8	8	2 or 3 PCLKB
0008 9094h	S12AD	A/D Compare Function Window A Channel Select Register 0	ADCMPSR0	16	16	2 or 3 PCLKB
0008 9096h	S12AD	A/D Compare Function Window A Channel Select Register 1	ADCMPSR1	16	16	2 or 3 PCLKB
0008 9098h	S12AD	A/D Compare Function Window A Comparison Condition Setting Register 0	ADCMPLR0	16	16	2 or 3 PCLKB
0008 909Ah	S12AD	A/D Compare Function Window A Comparison Condition Setting Register 1	ADCMPLR1	16	16	2 or 3 PCLKB
0008 909Ch	S12AD	A/D Compare Function Window A Lower-Side Level Setting Register	ADCMPSR0	16	16	2 or 3 PCLKB
0008 909Eh	S12AD	A/D Compare Function Window A Upper-Side Level Setting Register	ADCMPSR1	16	16	2 or 3 PCLKB
0008 90A0h	S12AD	A/D Compare Function Window A Channel Status Register 0	ADCMPSR0	16	16	2 or 3 PCLKB
0008 90A2h	S12AD	A/D Compare Function Window A Channel Status Register 1	ADCMPSR1	16	16	2 or 3 PCLKB
0008 90A4h	S12AD	A/D Compare Function Window A Extended Input Channel Status Register	ADCMPSER	8	8	2 or 3 PCLKB
0008 90A6h	S12AD	A/D Compare Function Window B Channel Select Register	ADCMPSR0	8	8	2 or 3 PCLKB
0008 90A8h	S12AD	A/D Compare Function Window B Lower-Side Level Setting Register	ADWINLLB	16	16	2 or 3 PCLKB
0008 90AAh	S12AD	A/D Compare Function Window B Upper-Side Level Setting Register	ADWINULB	16	16	2 or 3 PCLKB
0008 90ACh	S12AD	A/D Compare Function Window B Status Register	ADCMPSR	8	8	2 or 3 PCLKB
0008 90B0h	S12AD	A/D Data Storage Buffer Register 0	ADBUF0	16	16	2 or 3 PCLKB
0008 90B2h	S12AD	A/D Data Storage Buffer Register 1	ADBUF1	16	16	2 or 3 PCLKB
0008 90B4h	S12AD	A/D Data Storage Buffer Register 2	ADBUF2	16	16	2 or 3 PCLKB
0008 90B6h	S12AD	A/D Data Storage Buffer Register 3	ADBUF3	16	16	2 or 3 PCLKB
0008 90B8h	S12AD	A/D Data Storage Buffer Register 4	ADBUF4	16	16	2 or 3 PCLKB
0008 90BAh	S12AD	A/D Data Storage Buffer Register 5	ADBUF5	16	16	2 or 3 PCLKB
0008 90BCh	S12AD	A/D Data Storage Buffer Register 6	ADBUF6	16	16	2 or 3 PCLKB
0008 90BEh	S12AD	A/D Data Storage Buffer Register 7	ADBUF7	16	16	2 or 3 PCLKB
0008 90C0h	S12AD	A/D Data Storage Buffer Register 8	ADBUF8	16	16	2 or 3 PCLKB
0008 90C2h	S12AD	A/D Data Storage Buffer Register 9	ADBUF9	16	16	2 or 3 PCLKB
0008 90C4h	S12AD	A/D Data Storage Buffer Register 10	ADBUF10	16	16	2 or 3 PCLKB
0008 90C6h	S12AD	A/D Data Storage Buffer Register 11	ADBUF11	16	16	2 or 3 PCLKB
0008 90C8h	S12AD	A/D Data Storage Buffer Register 12	ADBUF12	16	16	2 or 3 PCLKB
0008 90CAh	S12AD	A/D Data Storage Buffer Register 13	ADBUF13	16	16	2 or 3 PCLKB
0008 90CCh	S12AD	A/D Data Storage Buffer Register 14	ADBUF14	16	16	2 or 3 PCLKB
0008 90CEh	S12AD	A/D Data Storage Buffer Register 15	ADBUF15	16	16	2 or 3 PCLKB
0008 90D0h	S12AD	A/D Data Storage Buffer Enable Register	ADBUFEN	8	8	2 or 3 PCLKB
0008 90D2h	S12AD	A/D Data Storage Buffer Pointer Register	ADBUFPTR	8	8	2 or 3 PCLKB
0008 90DDh	S12AD	A/D Sampling State Register L	ADSSTRL	8	8	2 or 3 PCLKB
0008 90DEh	S12AD	A/D Sampling State Register T	ADSSTRT	8	8	2 or 3 PCLKB
0008 90DFh	S12AD	A/D Sampling State Register O	ADSSTRO	8	8	2 or 3 PCLKB
0008 90E0h	S12AD	A/D Sampling State Register 0	ADSSTR0	8	8	2 or 3 PCLKB
0008 90E1h	S12AD	A/D Sampling State Register 1	ADSSTR1	8	8	2 or 3 PCLKB
0008 90E2h	S12AD	A/D Sampling State Register 2	ADSSTR2	8	8	2 or 3 PCLKB
0008 90E3h	S12AD	A/D Sampling State Register 3	ADSSTR3	8	8	2 or 3 PCLKB

Table 4.1 List of I/O Registers (Address Order) (11 / 18)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles
0008 B119h	ELC	Event Link Setting Register 24	ELSR24	8	8	2 or 3 PCLKB
0008 B11Ah	ELC	Event Link Setting Register 25	ELSR25	8	8	2 or 3 PCLKB
0008 B11Fh	ELC	Event Link Option Setting Register A	ELOPA	8	8	2 or 3 PCLKB
0008 B120h	ELC	Event Link Option Setting Register B	ELOPB	8	8	2 or 3 PCLKB
0008 B121h	ELC	Event Link Option Setting Register C	ELOPC	8	8	2 or 3 PCLKB
0008 B122h	ELC	Event Link Option Setting Register D	ELOPD	8	8	2 or 3 PCLKB
0008 B123h	ELC	Port Group Setting Register 1	PGR1	8	8	2 or 3 PCLKB
0008 B125h	ELC	Port Group Control Register 1	PGC1	8	8	2 or 3 PCLKB
0008 B127h	ELC	Port Buffer Register 1	PDBF1	8	8	2 or 3 PCLKB
0008 B129h	ELC	Event Link Port Setting Register 0	PEL0	8	8	2 or 3 PCLKB
0008 B12Ah	ELC	Event Link Port Setting Register 1	PEL1	8	8	2 or 3 PCLKB
0008 B12Dh	ELC	Event Link Software Event Generation Register	ELSEGR	8	8	2 or 3 PCLKB
0008 B300h	SCI12	Serial Mode Register	SMR	8	8	2 or 3 PCLKB
0008 B301h	SCI12	Bit Rate Register	BRR	8	8	2 or 3 PCLKB
0008 B302h	SCI12	Serial Control Register	SCR	8	8	2 or 3 PCLKB
0008 B303h	SCI12	Transmit Data Register	TDR	8	8	2 or 3 PCLKB
0008 B304h	SCI12	Serial Status Register	SSR	8	8	2 or 3 PCLKB
0008 B305h	SCI12	Receive Data Register	RDR	8	8	2 or 3 PCLKB
0008 B306h	SMCI12	Smart Card Mode Register	SCMR	8	8	2 or 3 PCLKB
0008 B307h	SCI12	Serial Extended Mode Register	SEMR	8	8	2 or 3 PCLKB
0008 B308h	SCI12	Noise Filter Setting Register	SNFR	8	8	2 or 3 PCLKB
0008 B309h	SCI12	I ² C Mode Register 1	SIMR1	8	8	2 or 3 PCLKB
0008 B30Ah	SCI12	I ² C Mode Register 2	SIMR2	8	8	2 or 3 PCLKB
0008 B30Bh	SCI12	I ² C Mode Register 3	SIMR3	8	8	2 or 3 PCLKB
0008 B30Ch	SCI12	I ² C Status Register	SISR	8	8	2 or 3 PCLKB
0008 B30Dh	SCI12	SPI Mode Register	SPMR	8	8	2 or 3 PCLKB
0008 B30Eh	SCI12	Transmit Data Register HL	TDRHL	16	16	2 or 3 PCLKB
0008 B30Eh	SCI12	Transmit Data Register H	TDRH	8	8	2 or 3 PCLKB
0008 B30Fh	SCI12	Transmit Data Register L	TDRL	8	8	2 or 3 PCLKB
0008 B310h	SCI12	Receive Data Register HL	RDRHL	16	16	2 or 3 PCLKB
0008 B310h	SCI12	Receive Data Register H	RDRH	8	8	2 or 3 PCLKB
0008 B311h	SCI12	Receive Data Register L	RDRL	8	8	2 or 3 PCLKB
0008 B312h	SCI12	Modulation Duty Register	MDDR	8	8	2 or 3 PCLKB
0008 B320h	SCI12	Extended Serial Module Enable Register	ESMER	8	8	2 or 3 PCLKB
0008 B321h	SCI12	Control Register 0	CR0	8	8	2 or 3 PCLKB
0008 B322h	SCI12	Control Register 1	CR1	8	8	2 or 3 PCLKB
0008 B323h	SCI12	Control Register 2	CR2	8	8	2 or 3 PCLKB
0008 B324h	SCI12	Control Register 3	CR3	8	8	2 or 3 PCLKB
0008 B325h	SCI12	Port Control Register	PCR	8	8	2 or 3 PCLKB
0008 B326h	SCI12	Interrupt Control Register	ICR	8	8	2 or 3 PCLKB
0008 B327h	SCI12	Status Register	STR	8	8	2 or 3 PCLKB
0008 B328h	SCI12	Status Clear Register	STCR	8	8	2 or 3 PCLKB
0008 B329h	SCI12	Control Field 0 Data Register	CF0DR	8	8	2 or 3 PCLKB
0008 B32Ah	SCI12	Control Field 0 Compare Enable Register	CF0CR	8	8	2 or 3 PCLKB
0008 B32Bh	SCI12	Control Field 0 Receive Data Register	CF0RR	8	8	2 or 3 PCLKB
0008 B32Ch	SCI12	Primary Control Field 1 Data Register	PCF1DR	8	8	2 or 3 PCLKB
0008 B32Dh	SCI12	Secondary Control Field 1 Data Register	SCF1DR	8	8	2 or 3 PCLKB
0008 B32Eh	SCI12	Control Field 1 Compare Enable Register	CF1CR	8	8	2 or 3 PCLKB
0008 B32Fh	SCI12	Control Field 1 Receive Data Register	CF1RR	8	8	2 or 3 PCLKB
0008 B330h	SCI12	Timer Control Register	TCR	8	8	2 or 3 PCLKB
0008 B331h	SCI12	Timer Mode Register	TMR	8	8	2 or 3 PCLKB
0008 B332h	SCI12	Timer Prescaler Register	TPRE	8	8	2 or 3 PCLKB

Item					Symbol	Typ.	Max.	Unit	Test Conditions		
Supply current*1	Middle-speed operating modes	Deep sleep mode	No peripheral operation*6	ICLK = 12 MHz	I _{CC}	1.0	—	mA			
				ICLK = 8 MHz		0.7	—				
				ICLK = 4 MHz		0.2	—				
				ICLK = 1 MHz		0.1	—				
			All peripheral operation: Normal*7	ICLK = 12 MHz		2.3	—				
				ICLK = 8 MHz		1.6	—				
				ICLK = 4 MHz		1.0	—				
				ICLK = 1 MHz		0.7	—				
			Increase during flash rewrite*5				2.5			—	
			Low-speed operating mode	Normal operating mode		No peripheral operation*8	ICLK = 32.768 kHz			I _{CC}	3.8
	All peripheral operation: Normal*10	ICLK = 32.768 kHz			10.9	—					
	All peripheral operation: Max.*10	ICLK = 32.768 kHz			—	29.2					
	Sleep mode	No peripheral operation*8		ICLK = 32.768 kHz	2.1	—					
		All peripheral operation: Normal*9		ICLK = 32.768 kHz	6.0	—					
	Deep sleep mode	No peripheral operation*8		ICLK = 32.768 kHz	1.6	—					
		All peripheral operation: Normal*9		ICLK = 32.768 kHz	5.0	—					

Note 1. Supply current values do not include output charge/discharge current from all pins. The values apply when internal pull-up MOSs are in the off state.

Note 2. Clock supply to the peripheral functions is stopped. This does not include BGO operation. The clock source is PLL. FCLK and PCLK are set to divided by 64.

Note 3. Clocks are supplied to the peripheral functions. This does not include BGO operation. The clock source is PLL. FCLK and PCLK are set to the same frequency as ICLK.

Note 4. Values when VCC = 3.3 V.

Note 5. This is the increase for programming or erasure of the ROM or E2 DataFlash during program execution.

Note 6. Clock supply to the peripheral function is stopped. The clock source is PLL when ICLK is 12 MHz, HOCO when ICLK is 8 MHz, and LOCO otherwise. FCLK and PCLK are set to divided by 64.

Note 7. Clocks are supplied to the peripheral functions. The clock source is PLL when ICLK is 12 MHz, HOCO when ICLK is (MHz, and LOCO otherwise. FCLK and PCLK are set to the same frequency as ICLK.

Note 8. Clock supply to the peripheral functions is stopped. The clock source is the sub-clock oscillator. FCLK and PCLK are set to divided by 64.

Note 9. Clocks are supplied to the peripheral functions. The clock source is the sub-clock oscillator. FCLK and PCLK are set to the same frequency as ICLK.

Note 10. Values when the MSTPCRA.MSTPA17 bit (12-bit A/D converter module stop bit) is set to "transition to the module stop state is made".

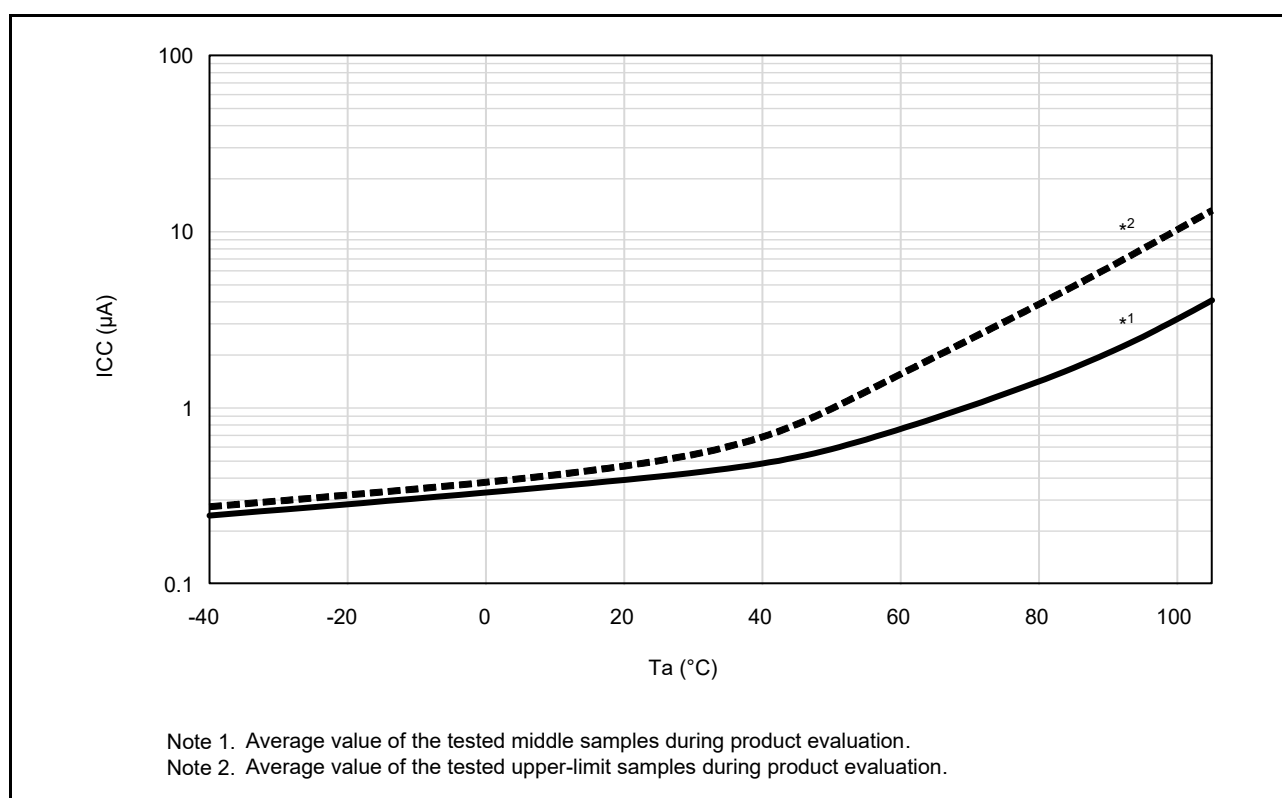


Figure 5.10 Temperature Dependency in Software Standby Mode (Reference Data)

Table 5.11 DC Characteristics (7)

Conditions: $1.8\text{ V} \leq \text{VCC} = \text{AVCC0} < 2.0\text{ V}$, $2.0\text{ V} \leq \text{VCC} \leq 5.5\text{ V}$, $2.0\text{ V} \leq \text{AVCC0} \leq 5.5\text{ V}$, $\text{VSS} = \text{AVSS0} = 0\text{ V}$

Item	Symbol	Typ.	Max.	Unit	Test Conditions
Permissible total power consumption*1	P_d	—	300	mW	D version
		—	105		G version

Note: Please contact a Renesas Electronics sales office for information on the derating of the G-version product. Derating is the systematic reduction of load to improve reliability.

Note 1. Total power dissipated by the entire chip (including output currents)

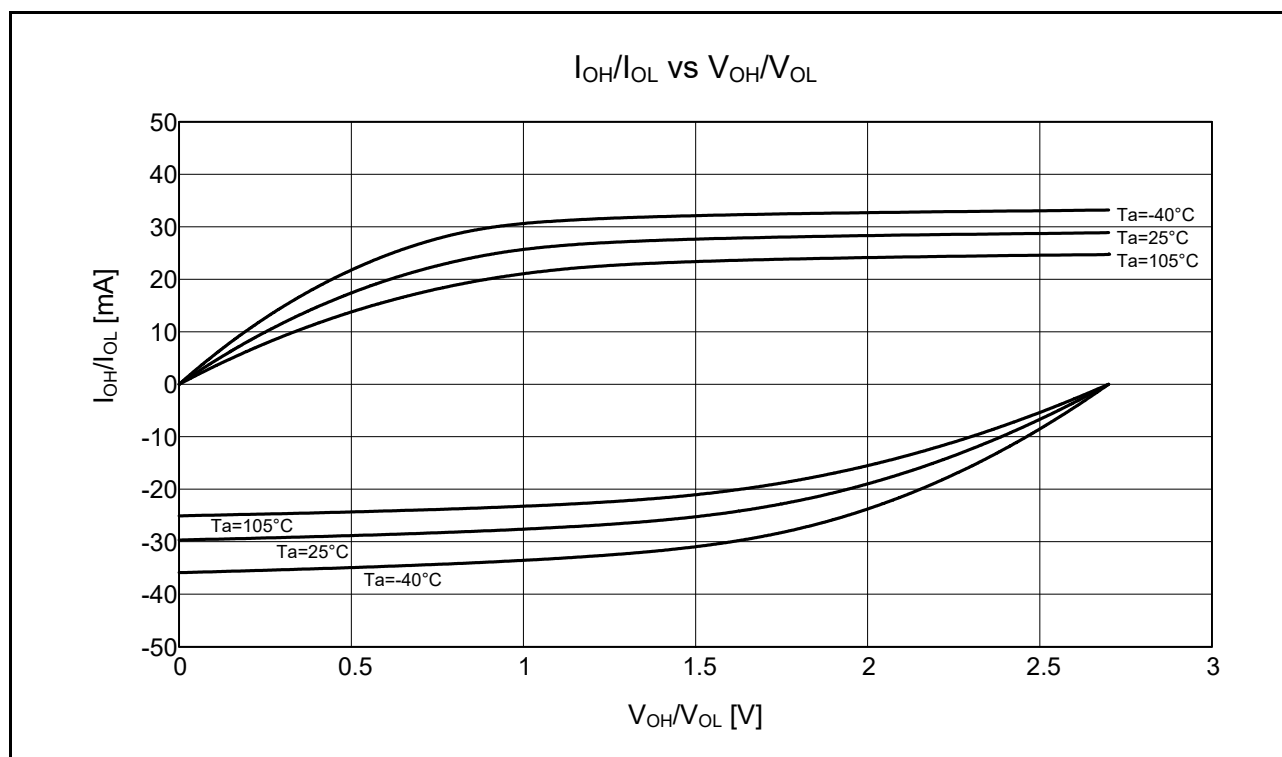


Figure 5.19 V_{OH}/V_{OL} and I_{OH}/I_{OL} Temperature Characteristics at $V_{CC} = 2.7$ V When High-Drive Output is Selected (Reference Data)

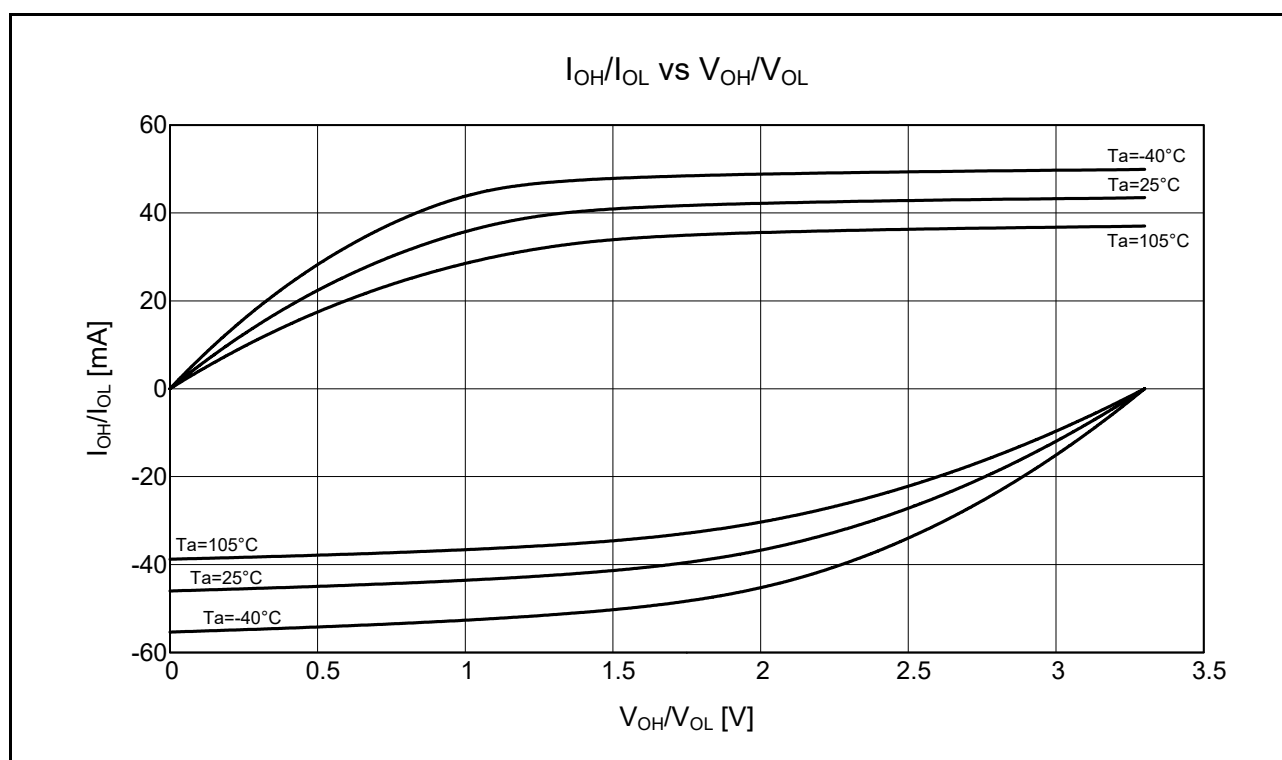


Figure 5.20 V_{OH}/V_{OL} and I_{OH}/I_{OL} Temperature Characteristics at $V_{CC} = 3.3$ V When High-Drive Output is Selected (Reference Data)

Table 5.37 Timing of On-Chip Peripheral Modules (5)Conditions: $2.7\text{ V} \leq \text{VCC} \leq 5.5\text{ V}$, $2.7\text{ V} \leq \text{AVCC0} \leq 5.5\text{ V}$, $\text{VSS} = \text{AVSS0} = 0\text{ V}$, $T_a = -40\text{ to }+105^\circ\text{C}$

Item		Symbol	Min.*1	Max.	Unit	Test Conditions
Simple I ² C (Standard mode)	SDA rise time	t_{Sr}	—	1000	ns	Figure 5.55
	SDA fall time	t_{Sf}	—	300	ns	
	SDA spike pulse removal time	t_{SP}	0	$4 \times t_{Pcyc}$	ns	
	Data setup time	t_{SDAS}	250	—	ns	
	Data hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b	—	400	pF	
Simple I ² C (Fast mode)	SDA rise time	t_{Sr}	—	300	ns	Figure 5.55
	SDA fall time	t_{Sf}	—	300	ns	
	SDA spike pulse removal time	t_{SP}	0	$4 \times t_{Pcyc}$	ns	
	Data setup time	t_{SDAS}	100	—	ns	
	Data hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b	—	400	pF	

Note: t_{Pcyc} : PCLK cycleNote 1. C_b is the total capacitance of the bus lines.**Table 5.38 Timing of On-Chip Peripheral Modules (6)**Conditions: $2.4\text{ V} \leq \text{VCC} \leq 5.5\text{ V}$, $2.4\text{ V} \leq \text{AVCC0} \leq 5.5\text{ V}$, $\text{VSS} = \text{AVSS0} = 0\text{ V}$, $T_a = -40\text{ to }+105^\circ\text{C}$

Item		Min.	Max.	Unit	Test Conditions
REMC	Increase of the operating clock frequency at a transition to software standby mode	—	1.5	%	REMCON1.CSRC[3:0] = x101b (with the HOCO clock/512 selected) HOFCR.HOFXIN = 1 (when the HOCO oscillation is set to be continued)
	The period for the change in the operating clock frequency at a transition to software standby mode	—	400	μs	

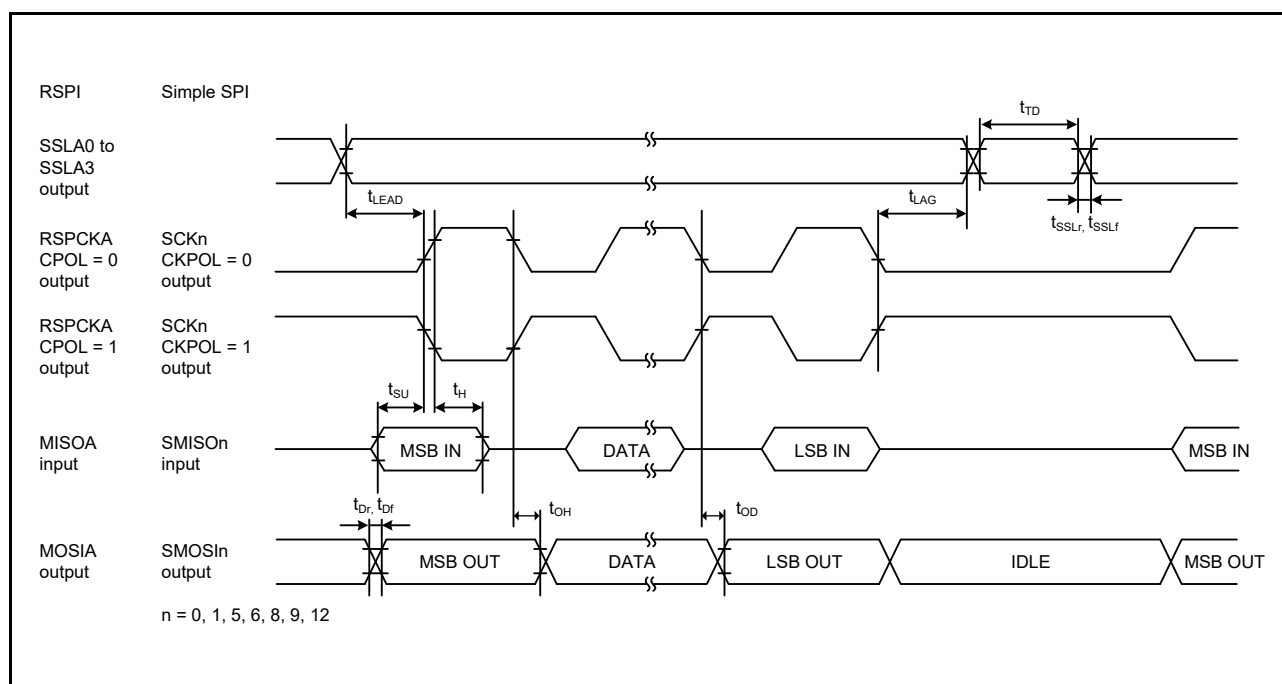


Figure 5.51 RSPI Timing (Master, CPHA = 0) and Simple SPI Clock Timing (Master, CKPH = 1)

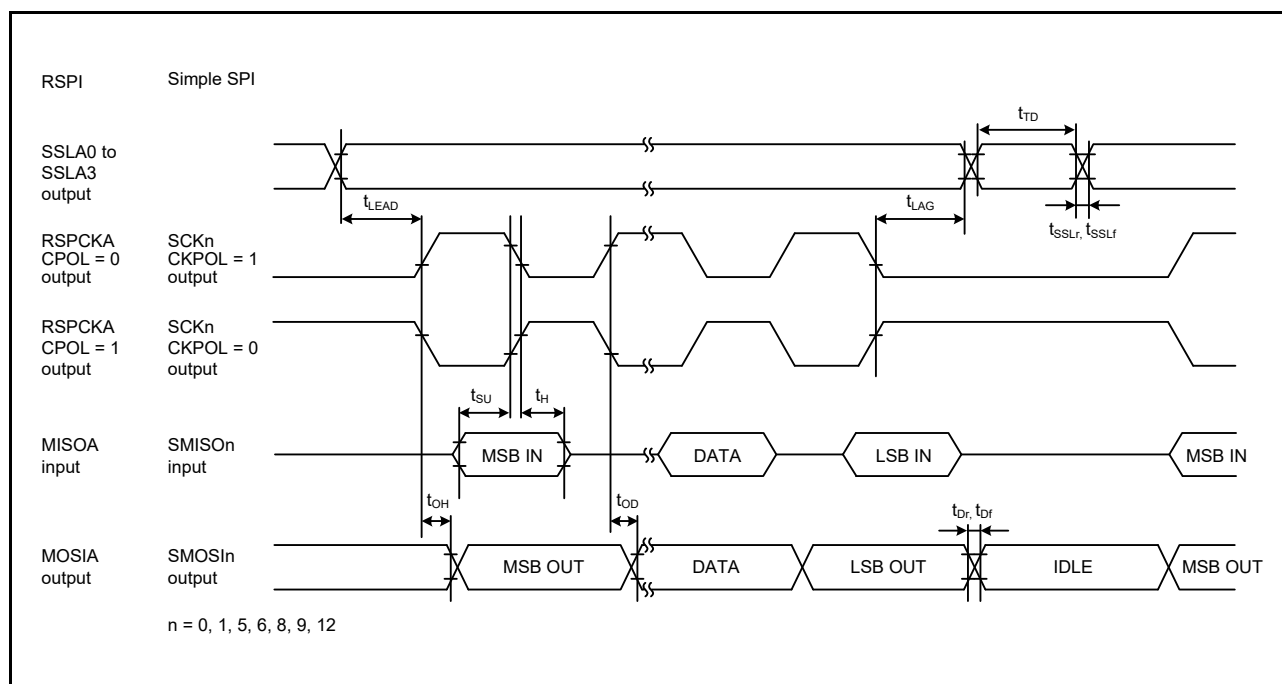


Figure 5.52 RSPI Timing (Master, CPHA = 1) and Simple SPI Clock Timing (Master, CKPH = 0)

Table 5.42 A/D Conversion Characteristics (4)

Conditions: $2.4\text{ V} \leq V_{CC} \leq 5.5\text{ V}$, $2.4\text{ V} \leq AV_{CC0} \leq 5.5\text{ V}$, $2.4\text{ V} \leq V_{REFH0} \leq AV_{CC0}$, Reference voltage = V_{REFH0} ,
 $V_{SS} = AV_{SS0} = 0\text{ V}$, $T_a = -40\text{ to }+105^\circ\text{C}$

Item		Min.	Typ.	Max.	Unit	Test Conditions
Frequency		1	—	16	MHz	
Resolution		—	—	12	Bit	
Conversion time*1 (Operation at PCLKD = 16 MHz)	Permissible signal source impedance (Max.) = 2.2 kΩ	3.38	—	—	μs	High-precision channel ADCSR.ADHSC bit = 1 ADSSTRn = 0Dh
		5.06	—	—		Normal-precision channel ADCSR.ADHSC bit = 1 ADSSTRn = 28h
Analog input capacitance	Cs	—	—	15	pF	Pin capacitance included
Analog input resistance	Rs	—	—	2.5	kΩ	
Analog input effective range		0	—	VREFH0	V	
Offset error		—	±0.5	±4.5	LSB	
Full-scale error		—	±0.75	±4.5	LSB	
Quantization error		—	±0.5	—	LSB	
Absolute accuracy		—	±1.25	±5.0	LSB	High-precision channel
				±8.0	LSB	Other than above
DNL differential nonlinearity error		—	±1.0	—	LSB	
INL integral nonlinearity error		—	±1.0	±3.0	LSB	

Note: The characteristics apply when no pin functions other than A/D converter input are used. Absolute accuracy includes quantization errors. Offset error, full-scale error, DNL differential nonlinearity error, and INL integral nonlinearity error do not include quantization errors.

Note 1. The conversion time is the sum of the sampling time and the comparison time. As the test conditions, the number of sampling states is indicated.

5.7 Comparator Characteristics

Table 5.47 Comparator Characteristics

Conditions: $1.8\text{ V} \leq V_{CC} = AV_{CC0} < 2.0\text{ V}$, $2.0\text{ V} \leq V_{CC} \leq 5.5\text{ V}$, $2.0\text{ V} \leq AV_{CC0} \leq 5.5\text{ V}$, $V_{SS} = AV_{SS0} = 0\text{ V}$, $T_a = -40$ to $+105^\circ\text{C}$

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
CVREFB0 to CVREFB1 input reference voltage		VREF	0	—	$V_{CC} - 1.4$	V	
CMPB0 to CMPB1 input voltage		VI	-0.3	—	$V_{CC} + 0.3$	V	
Offset	Comparator high-speed mode	—	—	—	50	mV	
	Comparator high-speed mode Window function enabled	—	—	—	60	mV	
	Comparator low-speed mode	—	—	—	40	mV	
Comparator output delay time	Comparator high-speed mode	Td	—	—	1.2	μs	$V_{CC} = 3\text{ V}$, input slew rate $\geq 50\text{ mV}/\mu\text{s}$
	Comparator high-speed mode Window function enabled	Tdw	—	—	2.0	μs	
	Comparator low-speed mode	Td	—	—	5.0	μs	
High-side reference voltage (comparator high-speed mode, window function enabled)		VRFH	—	$V_{CC} \times 0.76$	—	V	
Low-side reference voltage (comparator high-speed mode, window function enabled)		VRFL	—	$V_{CC} \times 0.24$	—	V	
Operation stabilization wait time		Tcmp	100	—	—	μs	

Table 5.54 ROM (Flash Memory for Code Storage) Characteristics (3) Middle-Speed Operating ModeConditions: $1.8\text{ V} \leq V_{CC} = AV_{CC0} < 2.0\text{ V}$, $2.0\text{ V} \leq V_{CC} \leq 5.5\text{ V}$, $2.0\text{ V} \leq AV_{CC0} \leq 5.5\text{ V}$, $V_{SS} = AV_{SS0} = 0\text{ V}$ Temperature range for the programming/erasure operation: $T_a = -40$ to $+85^\circ\text{C}$

Item		Symbol	FCLK = 1 MHz			FCLK = 8 MHz			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Programming time	4-byte	t_{P4}	—	143	1330	—	96.8	932	μs
Erasure time	1-Kbyte	t_{E1K}	—	8.3	269	—	5.85	219	ms
	256-Kbyte	t_{E256K}	—	407	928	—	93	520	ms
Blank check time	4-byte	t_{BC4}	—	—	78	—	—	50	μs
	1-Kbyte	t_{BC1K}	—	—	1.61	—	—	0.369	ms
Erase operation forcible stop time		t_{SED}	—	—	33.6	—	—	25.6	μs
Start-up area switching setting time		t_{SAS}	—	13.2	549	—	7.6	445	ms
Access window setting time		t_{AWS}	—	13.2	549	—	7.6	445	ms
ROM mode transition wait time 1		t_{DIS}	2	—	—	2	—	—	μs
ROM mode transition wait time 2		t_{MS}	3	—	—	3	—	—	μs

Note: Does not include the time until each operation of the flash memory is started after instructions are executed by software.

Note: The lower-limit frequency of FCLK is 1 MHz during programming or erasing of the flash memory. When using FCLK at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.

Note: The frequency accuracy of FCLK should be $\pm 3.5\%$.

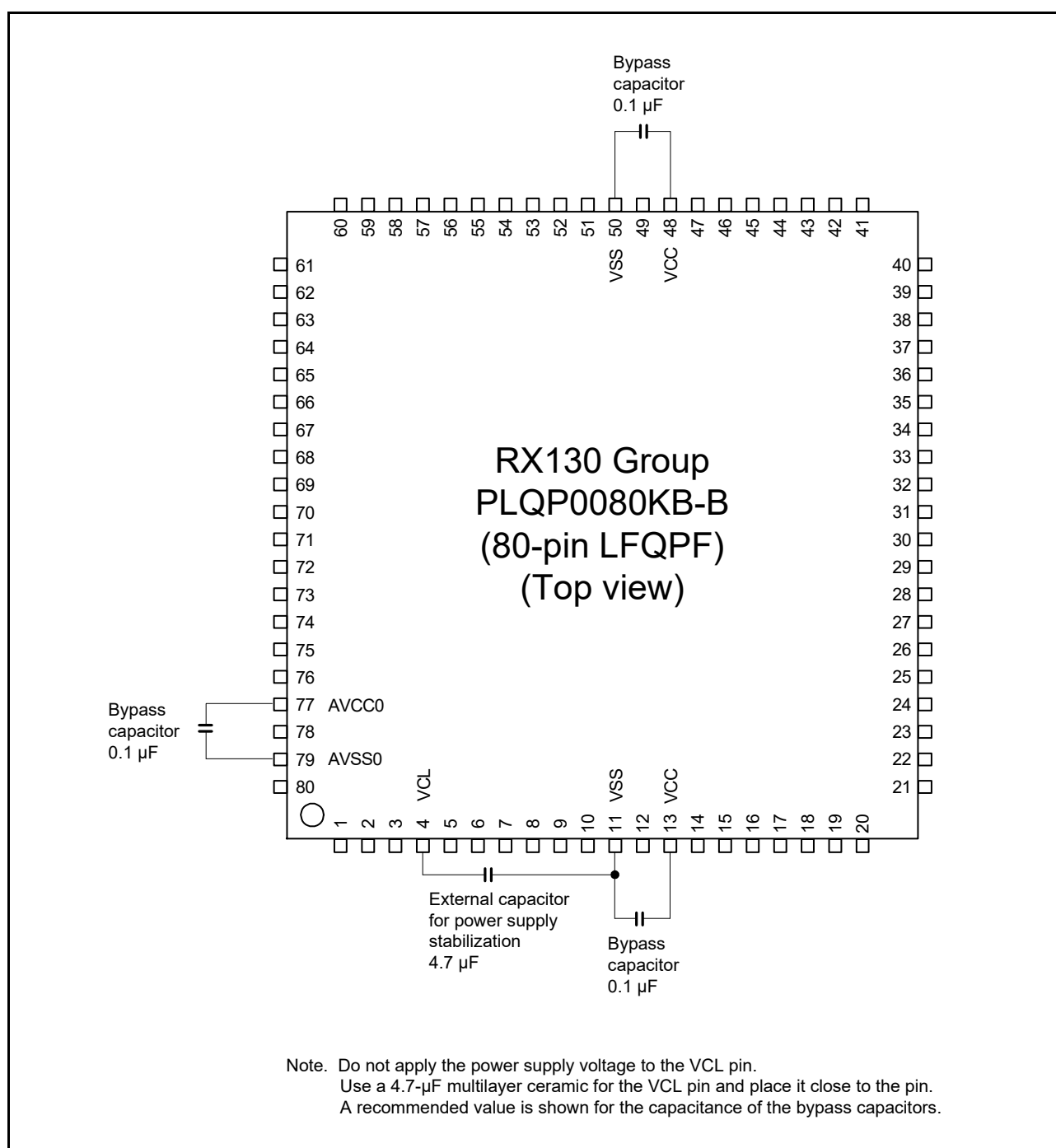
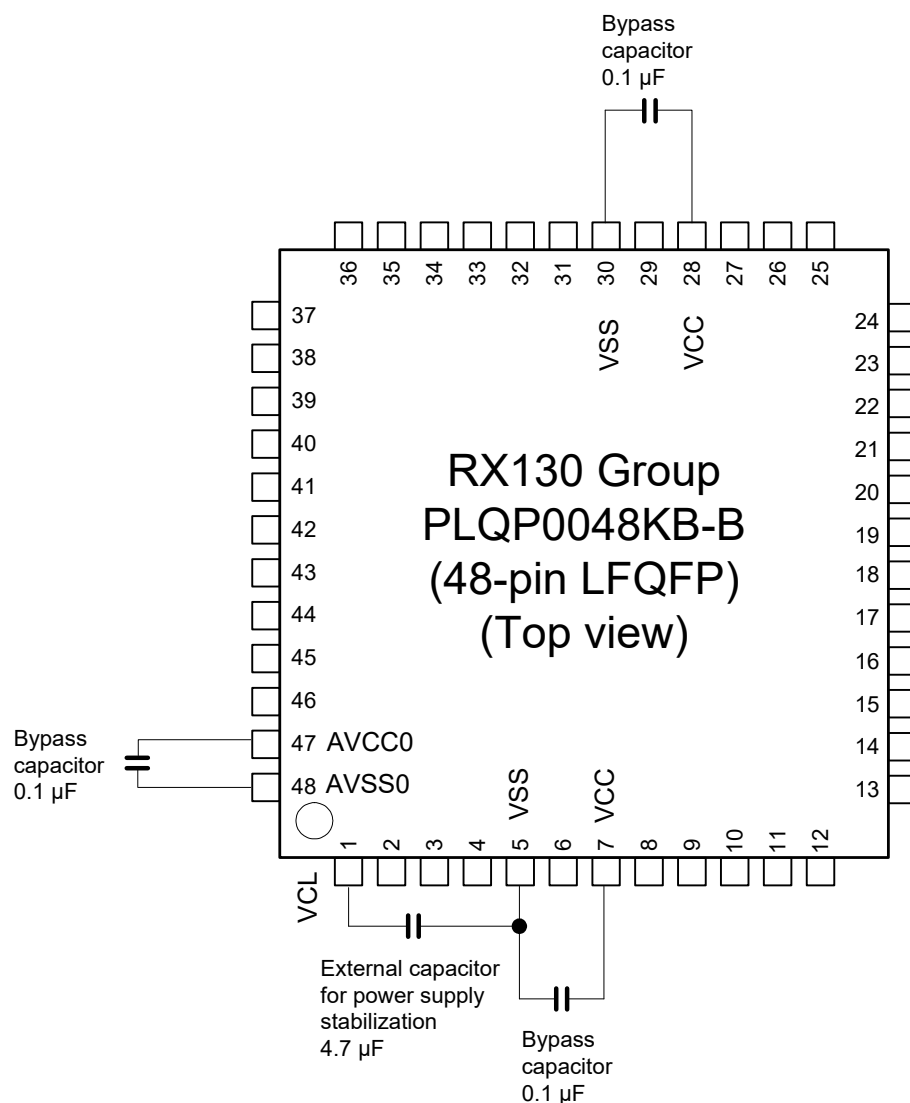


Figure 5.68 Connecting Capacitors (80 Pins)



Note. Do not apply the power supply voltage to the VCL pin.
Use a 4.7- μ F multilayer ceramic for the VCL pin and place it close to the pin.
A recommended value is shown for the capacitance of the bypass capacitors.

Figure 5.70 Connecting Capacitors (48 Pins)

Appendix 1. Package Dimensions

Information on the latest version of the package dimensions or mountings has been displayed in “Packages” on Renesas Electronics Corporation website.

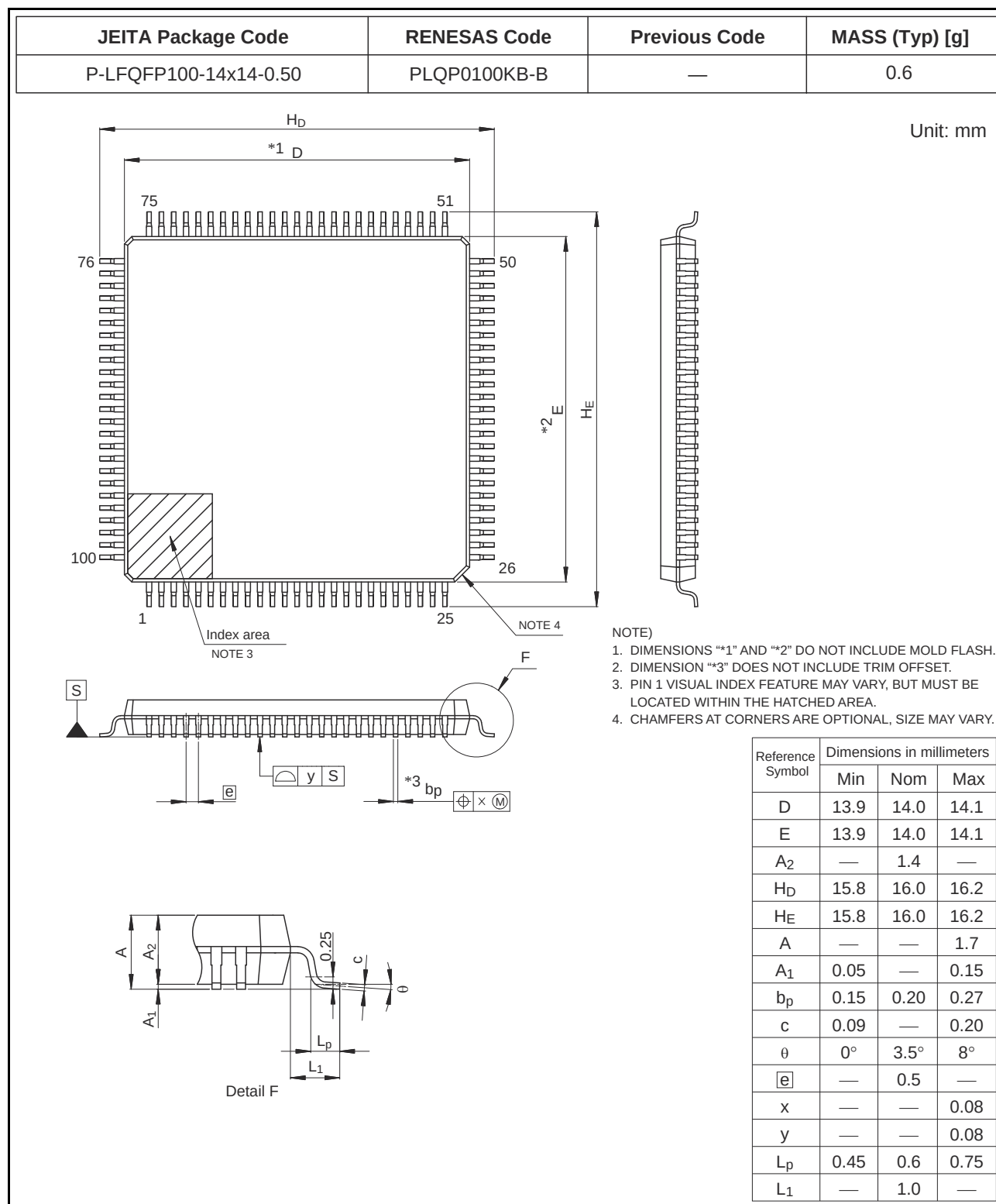


Figure A 100-Pin LFQFP (PLQP0100KB-B)

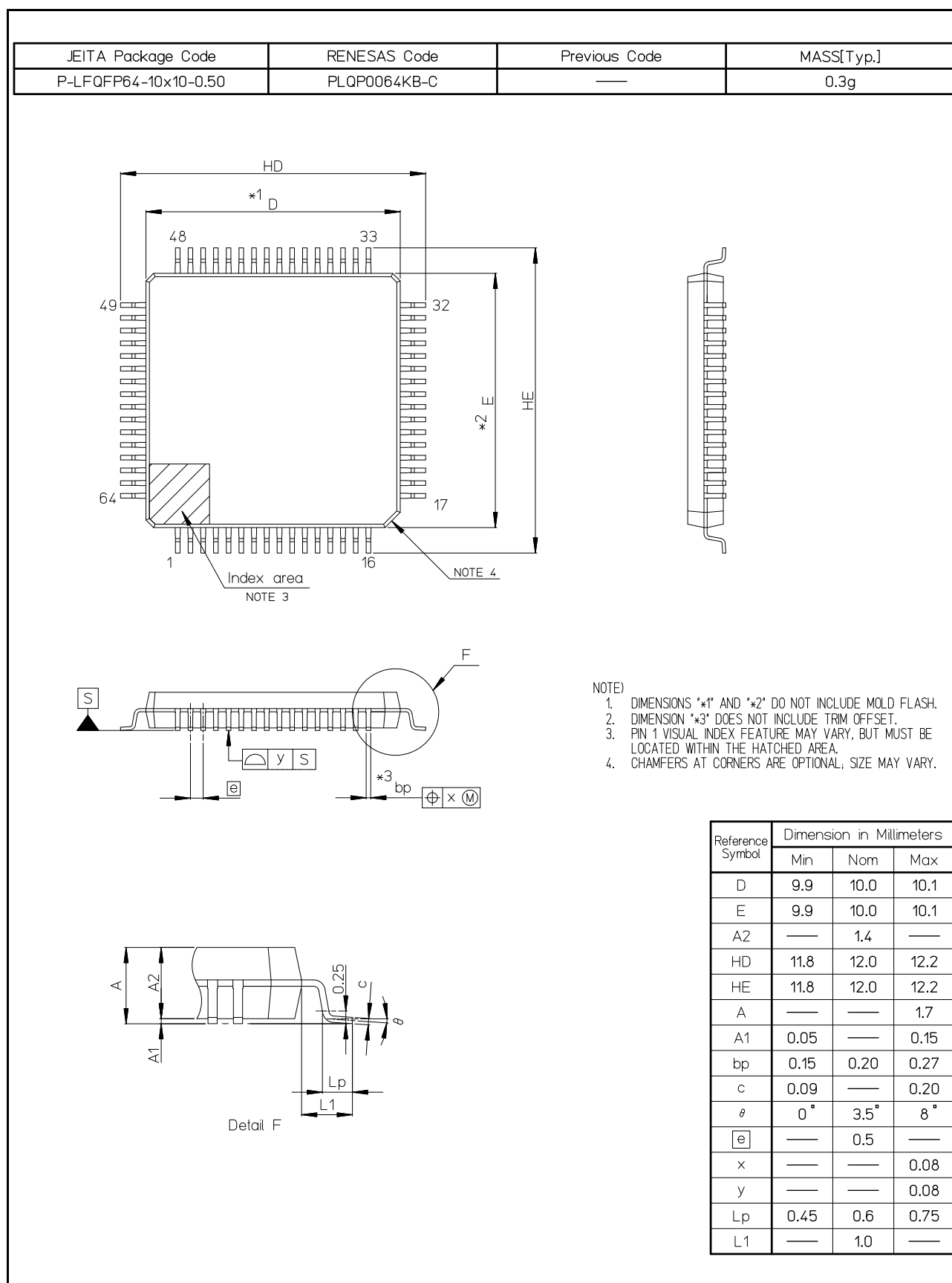


Figure D 64-Pin LFQFP (PLQP0064KB-C)