Renesas Electronics America Inc - R5F51308ADFM#30 Datasheet

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

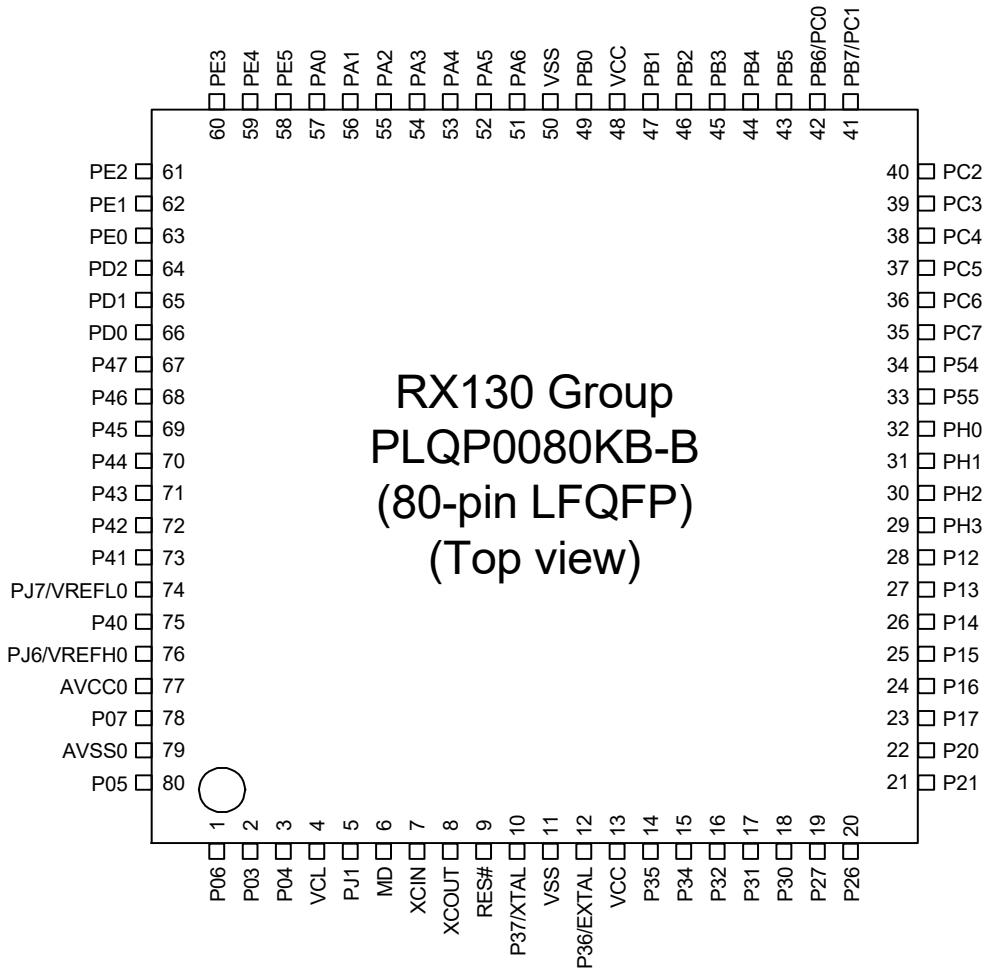
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	RX
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	I²C, LINbus, SCI, SPI
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	52
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	8K x 8
RAM Size	48K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 14x12b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LFQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f51308adfm-30

Table 1.1 Outline of Specifications (3/3)

Classification	Module/Function	Description
Communication functions	Serial peripheral interface (RSPIa)	• 1 channel • Transfer facility Using the MOSI (master out, slave in), MISO (master in, slave out), SSL (slave select), and RSPCK (RSPI clock) signals enables serial transfer through SPI operation (four lines) or clock-synchronous operation (three lines) • Capable of handling serial transfer as a master or slave • Data formats • Choice of LSB-first or MSB-first transfer The number of bits in each transfer can be changed to 8, 9, 10, 11, 12, 13, 14, 15, 16, 20, 24, or 32 bits. 128-bit buffers for transmission and reception Up to four frames can be transmitted or received in a single transfer operation (with each frame having up to 32 bits) • Double buffers for both transmission and reception
	Remote control signal receiver (REMC)	• 2 channels • Four pattern matching (header, data 0, data 1, and special data detection) • 8-byte receive buffer per unit • The operating clock can be selected from among the PCLK, sub-clock, HOCO, IWDTCLK, and TMR.
12-bit A/D converter (S12ADE)		• 12 bits (24 channels × 1 unit) • 12-bit resolution • Minimum conversion time: 1.4 µs per channel when the ADCLK is operating at 32 MHz • Operating modes Scan mode (single scan mode, continuous scan mode, and group scan mode) Group A priority control (only for group scan mode) • Sampling variable Sampling time can be set up for each channel. • Self-diagnostic function • Double trigger mode (A/D conversion data duplicated) • Detection of analog input disconnection • Conversion results compare features • A/D conversion start conditions A software trigger, a trigger from a timer (MTU), an external trigger signal, or ELC • Event linking by the ELC
Temperature sensor (TEMPSA)		• 1 channel • The voltage output from the temperature sensor is converted into a digital value by the 12-bit A/D converter.
D/A converter (DA)		• 2 channels • 8-bit resolution • Output voltage: 0V to AVCC0
CRC calculator (CRC)		• CRC code generation for arbitrary amounts of data in 8-bit units • Select any of three generating polynomials: $X^8 + X^2 + X + 1$, $X^{16} + X^{15} + X^2 + 1$, or $X^{16} + X^{12} + X^5 + 1$ • Generation of CRC codes for use with LSB-first or MSB-first communications is selectable.
Comparator B (CMPBa)		• 2 channels • Function to compare the reference voltage and the analog input voltage • Window comparator operation or standard comparator operation is selectable
Capacitive touch sensing unit (CTSUa)		Detection pin: 36 channels
Data operation circuit (DOC)		Comparison, addition, and subtraction of 16-bit data
Unique ID		32-byte ID code for the MCU
Power supply voltages/Operating frequencies		VCC = 1.8 to 2.4 V: 8 MHz, VCC = 2.4 to 2.7 V: 16 MHz, VCC = 2.7 to 5.5 V: 32 MHz
Operating temperature range		D version: –40 to +85°C, G version: –40 to +105°C
Packages		100-pin LFQFP (PLQP0100KB-B) 14 × 14 mm, 0.5 mm pitch 80-pin LFQFP (PLQP0080KB-B) 12 × 12 mm, 0.5 mm pitch 64-pin LFQFP (PLQP0064KB-C) 10 × 10 mm, 0.5 mm pitch 64-pin LQFP (PLQP0064GA-A) 14 × 14 mm, 0.8 mm pitch 48-pin LFQFP (PLQP0048KB-B) 7 × 7 mm, 0.5 mm pitch 48-pin HWQFN (PWQN0048KB-A) 7 × 7 mm, 0.5 mm pitch
On-chip debugging system		E1 emulator (FINE interface)

Note 1. When the realtime clock is not to be used, refer to section 24.5.7, Initialization Procedure When the Realtime Clock is Not to be Used.

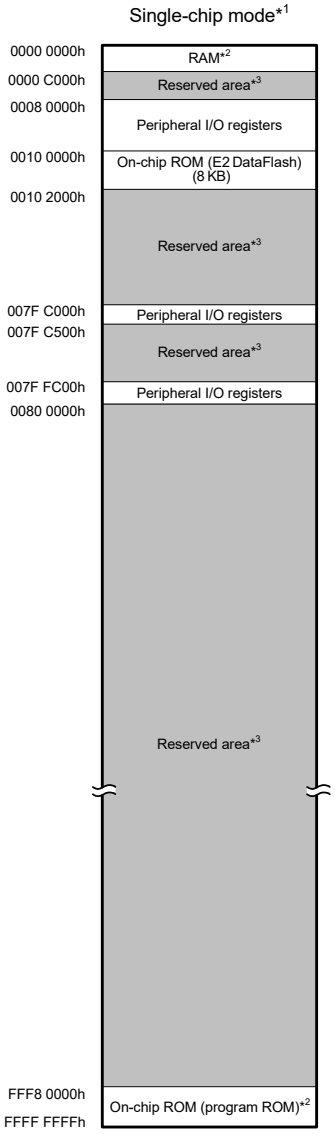


Note: This figure indicates the power supply pins and I/O ports.
For the pin configuration, see the table “List of Pins and Pin Functions (80-Pin LFQFP)”.

Figure 1.4 Pin Assignments of the 80-Pin LFQFP

Table 1.5 List of Pins and Pin Functions (100-Pin LFQFP) (1/2)

Pin No.	Power Supply, Clock, System Control	I/O Port	Timers (MTU, TMR, POE)	Communications (SCIg, SCIh, RSPI, RIIC, REMC)	Touch sensing	Others
1		P06*1				
2		P03*1				DA0
3		P04*1				
4		PJ3	MTIOC3C	CTS6#/RTS6#/SS6#		
5	VCL					
6		PJ1	MTIOC3A			
7	MD					FINED
8	XCIN					
9	XCOUT					
10	RES#					
11	XTAL	P37				
12	VSS					
13	EXTAL	P36				
14	VCC					
15		P35				NMI
16		P34	MTIOC0A/TMCI3/POE2#	SCK6		IRQ4
17		P33	MTIOC0D/TMRI3/POE3#	RXD6/SMISO6/SSCL6		IRQ3
18		P32	MTIOC0C/TMO3	TXD6/SMOSI6/SSDA6	TS0	IRQ2/RTCOUT
19		P31	MTIOC4D/TMCI2	CTS1#/RTS1#/SS1#	TS1	IRQ1
20		P30	MTIOC4B/POE8#/TMRI3	RXD1/SMISO1/SSCL1	TS2	IRQ0
21		P27	MTIOC2B/TMCI3	SCK1	TS3	
22		P26	MTIOC2A/TMO1	TXD1/SMOSI1/SSDA1	TS4	
23		P25	MTIOC4C/MTCLKB			ADTRG0#
24		P24	MTIOC4A/MTCLKA/TMRI1			
25		P23	MTIOC3D/MTCLKD	CTS0#/RTS0#/SS0#		
26		P22	MTIOC3B/MTCLKC/TMO0	SCK0		
27		P21	MTIOC1B/TMCI0	RXD0/SMISO0/SSCL0		
28		P20	MTIOC1A/TMRI0	TXD0/SMOSI0/SSDA0		
29	(5V tolerant)	P17	MTIOC3A/MTIOC3B/TMO1/ POE8#	SCK1/MISOA/SDA		IRQ7
30	(5V tolerant)	P16	MTIOC3C/MTIOC3D/TMO2	TXD1/SMOSI1/SSDA1/MOSIA/SCL		IRQ6/RTCOUT/ ADTRG0#
31		P15	MTIOC0B/MTCLKB/TMCI2	RXD1/SMISO1/SSCL1	TS5	IRQ5
32		P14	MTIOC3A/MTCLKA/TMRI2	CTS1#/RTS1#/SS1#	TS6	IRQ4
33	(5V tolerant)	P13	MTIOC0B/TMO3	SDA		IRQ3
34	(5V tolerant)	P12	TMCI1	SCL		IRQ2
35		PH3	TMCI0		TS7	
36		PH2	TMRI0		TS8	IRQ1
37		PH1	TMO0		TS9	IRQ0
38		PH0			TS10	CACREF
39		P55	MTIOC4D/TMO3		TS11	
40		P54	MTIOC4B/TMCI1		TS12	
41		P53				
42		P52		PMC1		
43		P51		PMC0		
44		P50				
45		PC7	MTIOC3A/MTCLKB/TMO2	TXD8/SMOSI8/SSDA8/MISOA	TS13	CACREF
46		PC6	MTIOC3C/MTCLKA/TMCI2	RXD8/SMISO8/SSCL8/MOSIA	TS14	
47		PC5	MTIOC3B/MTCLKD/TMRI2	SCK8/RSPCKA	TS15	
48		PC4	MTIOC3D/MTCLKC/TMCI1/ POE0#	SCK5/CTS8#/RTS8#/SS8#/SSLA0	TSCAP	
49		PC3	MTIOC4D	TXD5/SMOSI5/SSDA5	TS16	
50		PC2	MTIOC4B	RXD5/SMISO5/SSCL5/SSLA3	TS17	
51		PC1	MTIOC3A	SCK5/SSLA2		
52		PC0	MTIOC3C	CTS5#/RTS5#/SS5#/SSLA1		



Note 1. The address space in boot mode is the same as the address space in single-chip mode.
Note 2. The capacity of ROM/RAM differs depending on the products.

ROM (bytes)		RAM (bytes)	
Capacity	**Address**	**Capacity**	**Address**
512 Kbytes	FFF8 0000h to FFFF FFFFh	48 Kbytes	0000 0000h to 0000 BFFFh
384 Kbytes	FFFA 8000h to FFFF FFFFh		
256 Kbytes	FFFC 0000h to FFFF FFFFh	32 Kbytes	0000 0000h to 0000 7FFFh
128 Kbytes	FFFE 0000h to FFFF FFFFh	16 Kbytes	0000 0000h to 0000 3FFFh
64 Kbytes	FFFF 0000h to FFFF FFFFh	10 Kbytes	0000 0000h to 0000 27FFh

Note: See Table 1.3, List of Products, for the product type name.

Note 3. Reserved areas should not be accessed.

Figure 3.1 Memory Map in Each Operating Mode

Table 4.1 List of I/O Registers (Address Order) (10 / 18)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles
0008 A10Fh	SCI8	Transmit Data Register L	TDRL	8	8	2 or 3 PCLKB
0008 A110h	SCI8	Receive Data Register HL	RDRHL	16	16	2 or 3 PCLKB
0008 A110h	SCI8	Receive Data Register H	RDRH	8	8	2 or 3 PCLKB
0008 A111h	SCI8	Receive Data Register L	RDRL	8	8	2 or 3 PCLKB
0008 A112h	SCI8	Modulation Duty Register	MDDR	8	8	2 or 3 PCLKB
0008 A120h	SCI9	Serial Mode Register	SMR	8	8	2 or 3 PCLKB
0008 A121h	SCI9	Bit Rate Register	BRR	8	8	2 or 3 PCLKB
0008 A122h	SCI9	Serial Control Register	SCR	8	8	2 or 3 PCLKB
0008 A123h	SCI9	Transmit Data Register	TDR	8	8	2 or 3 PCLKB
0008 A124h	SCI9	Serial Status Register	SSR	8	8	2 or 3 PCLKB
0008 A125h	SCI9	Receive Data Register	RDR	8	8	2 or 3 PCLKB
0008 A126h	SMCI9	Smart Card Mode Register	SCMR	8	8	2 or 3 PCLKB
0008 A127h	SCI9	Serial Extended Mode Register	SEMR	8	8	2 or 3 PCLKB
0008 A128h	SCI9	Noise Filter Setting Register	SNFR	8	8	2 or 3 PCLKB
0008 A129h	SCI9	I^2C Mode Register 1	SIMR1	8	8	2 or 3 PCLKB
0008 A12Ah	SCI9	I^2C Mode Register 2	SIMR2	8	8	2 or 3 PCLKB
0008 A12Bh	SCI9	I^2C Mode Register 3	SIMR3	8	8	2 or 3 PCLKB
0008 A12Ch	SCI9	I^2C Status Register	SISR	8	8	2 or 3 PCLKB
0008 A12Dh	SCI9	SPI Mode Register	SPMR	8	8	2 or 3 PCLKB
0008 A12Eh	SCI9	Transmit Data Register HL	TDRHL	16	16	2 or 3 PCLKB
0008 A12Eh	SCI9	Transmit Data Register H	TDRH	8	8	2 or 3 PCLKB
0008 A12Fh	SCI9	Transmit Data Register L	TDRL	8	8	2 or 3 PCLKB
0008 A130h	SCI9	Receive Data Register HL	RDRHL	16	16	2 or 3 PCLKB
0008 A130h	SCI9	Receive Data Register H	RDRH	8	8	2 or 3 PCLKB
0008 A131h	SCI9	Receive Data Register L	RDRL	8	8	2 or 3 PCLKB
0008 A132h	SCI9	Modulation Duty Register	MDDR	8	8	2 or 3 PCLKB
0008 B000h	CAC	CAC Control Register 0	CACR0	8	8	2 or 3 PCLKB
0008 B001h	CAC	CAC Control Register 1	CACR1	8	8	2 or 3 PCLKB
0008 B002h	CAC	CAC Control Register 2	CACR2	8	8	2 or 3 PCLKB
0008 B003h	CAC	CAC Interrupt Request Enable Register	CAICR	8	8	2 or 3 PCLKB
0008 B004h	CAC	CAC Status Register	CASTR	8	8	2 or 3 PCLKB
0008 B006h	CAC	CAC Upper-Limit Value Setting Register	CAULVR	16	16	2 or 3 PCLKB
0008 B008h	CAC	CAC Lower-Limit Value Setting Register	CALLVR	16	16	2 or 3 PCLKB
0008 B00Ah	CAC	CAC Counter Buffer Register	CACNTBR	16	16	2 or 3 PCLKB
0008 B080h	DOC	DOC Control Register	DOCR	8	8	2 or 3 PCLKB
0008 B082h	DOC	DOC Data Input Register	DODIR	16	16	2 or 3 PCLKB
0008 B084h	DOC	DOC Data Setting Register	DODSR	16	16	2 or 3 PCLKB
0008 B100h	ELC	Event Link Control Register	ELCR	8	8	2 or 3 PCLKB
0008 B102h	ELC	Event Link Setting Register 1	ELSR1	8	8	2 or 3 PCLKB
0008 B103h	ELC	Event Link Setting Register 2	ELSR2	8	8	2 or 3 PCLKB
0008 B104h	ELC	Event Link Setting Register 3	ELSR3	8	8	2 or 3 PCLKB
0008 B105h	ELC	Event Link Setting Register 4	ELSR4	8	8	2 or 3 PCLKB
0008 B108h	ELC	Event Link Setting Register 7	ELSR7	8	8	2 or 3 PCLKB
0008 B109h	ELC	Event Link Setting Register 8	ELSR8	8	8	2 or 3 PCLKB
0008 B10Bh	ELC	Event Link Setting Register 10	ELSR10	8	8	2 or 3 PCLKB
0008 B10Dh	ELC	Event Link Setting Register 12	ELSR12	8	8	2 or 3 PCLKB
0008 B10Fh	ELC	Event Link Setting Register 14	ELSR14	8	8	2 or 3 PCLKB
0008 B110h	ELC	Event Link Setting Register 15	ELSR15	8	8	2 or 3 PCLKB
0008 B111h	ELC	Event Link Setting Register 16	ELSR16	8	8	2 or 3 PCLKB
0008 B113h	ELC	Event Link Setting Register 18	ELSR18	8	8	2 or 3 PCLKB
0008 B115h	ELC	Event Link Setting Register 20	ELSR20	8	8	2 or 3 PCLKB
0008 B117h	ELC	Event Link Setting Register 22	ELSR22	8	8	2 or 3 PCLKB

Table 4.1 List of I/O Registers (Address Order) (11 / 18)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles
0008 B119h	ELC	Event Link Setting Register 24	ELSR24	8	8	2 or 3 PCLKB
0008 B11Ah	ELC	Event Link Setting Register 25	ELSR25	8	8	2 or 3 PCLKB
0008 B11Fh	ELC	Event Link Option Setting Register A	ELOPA	8	8	2 or 3 PCLKB
0008 B120h	ELC	Event Link Option Setting Register B	ELOPB	8	8	2 or 3 PCLKB
0008 B121h	ELC	Event Link Option Setting Register C	ELOPC	8	8	2 or 3 PCLKB
0008 B122h	ELC	Event Link Option Setting Register D	ELOPD	8	8	2 or 3 PCLKB
0008 B123h	ELC	Port Group Setting Register 1	PGR1	8	8	2 or 3 PCLKB
0008 B125h	ELC	Port Group Control Register 1	PGC1	8	8	2 or 3 PCLKB
0008 B127h	ELC	Port Buffer Register 1	PDBF1	8	8	2 or 3 PCLKB
0008 B129h	ELC	Event Link Port Setting Register 0	PEL0	8	8	2 or 3 PCLKB
0008 B12Ah	ELC	Event Link Port Setting Register 1	PEL1	8	8	2 or 3 PCLKB
0008 B12Dh	ELC	Event Link Software Event Generation Register	ELSEGR	8	8	2 or 3 PCLKB
0008 B300h	SCI12	Serial Mode Register	SMR	8	8	2 or 3 PCLKB
0008 B301h	SCI12	Bit Rate Register	BRR	8	8	2 or 3 PCLKB
0008 B302h	SCI12	Serial Control Register	SCR	8	8	2 or 3 PCLKB
0008 B303h	SCI12	Transmit Data Register	TDR	8	8	2 or 3 PCLKB
0008 B304h	SCI12	Serial Status Register	SSR	8	8	2 or 3 PCLKB
0008 B305h	SCI12	Receive Data Register	RDR	8	8	2 or 3 PCLKB
0008 B306h	SMCI12	Smart Card Mode Register	SCMR	8	8	2 or 3 PCLKB
0008 B307h	SCI12	Serial Extended Mode Register	SEMR	8	8	2 or 3 PCLKB
0008 B308h	SCI12	Noise Filter Setting Register	SNFR	8	8	2 or 3 PCLKB
0008 B309h	SCI12	I^2C Mode Register 1	SIMR1	8	8	2 or 3 PCLKB
0008 B30Ah	SCI12	I^2C Mode Register 2	SIMR2	8	8	2 or 3 PCLKB
0008 B30Bh	SCI12	I^2C Mode Register 3	SIMR3	8	8	2 or 3 PCLKB
0008 B30Ch	SCI12	I^2C Status Register	SISR	8	8	2 or 3 PCLKB
0008 B30Dh	SCI12	SPI Mode Register	SPMR	8	8	2 or 3 PCLKB
0008 B30Eh	SCI12	Transmit Data Register HL	TDRHL	16	16	2 or 3 PCLKB
0008 B30Eh	SCI12	Transmit Data Register H	TDRH	8	8	2 or 3 PCLKB
0008 B30Fh	SCI12	Transmit Data Register L	TDRL	8	8	2 or 3 PCLKB
0008 B310h	SCI12	Receive Data Register HL	RDRHL	16	16	2 or 3 PCLKB
0008 B310h	SCI12	Receive Data Register H	RDRH	8	8	2 or 3 PCLKB
0008 B311h	SCI12	Receive Data Register L	RDRL	8	8	2 or 3 PCLKB
0008 B312h	SCI12	Modulation Duty Register	MDDR	8	8	2 or 3 PCLKB
0008 B320h	SCI12	Extended Serial Module Enable Register	ESMER	8	8	2 or 3 PCLKB
0008 B321h	SCI12	Control Register 0	CR0	8	8	2 or 3 PCLKB
0008 B322h	SCI12	Control Register 1	CR1	8	8	2 or 3 PCLKB
0008 B323h	SCI12	Control Register 2	CR2	8	8	2 or 3 PCLKB
0008 B324h	SCI12	Control Register 3	CR3	8	8	2 or 3 PCLKB
0008 B325h	SCI12	Port Control Register	PCR	8	8	2 or 3 PCLKB
0008 B326h	SCI12	Interrupt Control Register	ICR	8	8	2 or 3 PCLKB
0008 B327h	SCI12	Status Register	STR	8	8	2 or 3 PCLKB
0008 B328h	SCI12	Status Clear Register	STCR	8	8	2 or 3 PCLKB
0008 B329h	SCI12	Control Field 0 Data Register	CF0DR	8	8	2 or 3 PCLKB
0008 B32Ah	SCI12	Control Field 0 Compare Enable Register	CF0CR	8	8	2 or 3 PCLKB
0008 B32Bh	SCI12	Control Field 0 Receive Data Register	CF0RR	8	8	2 or 3 PCLKB
0008 B32Ch	SCI12	Primary Control Field 1 Data Register	PCF1DR	8	8	2 or 3 PCLKB
0008 B32Dh	SCI12	Secondary Control Field 1 Data Register	SCF1DR	8	8	2 or 3 PCLKB
0008 B32Eh	SCI12	Control Field 1 Compare Enable Register	CF1CR	8	8	2 or 3 PCLKB
0008 B32Fh	SCI12	Control Field 1 Receive Data Register	CF1RR	8	8	2 or 3 PCLKB
0008 B330h	SCI12	Timer Control Register	TCR	8	8	2 or 3 PCLKB
0008 B331h	SCI12	Timer Mode Register	TMR	8	8	2 or 3 PCLKB
0008 B332h	SCI12	Timer Prescaler Register	TPRE	8	8	2 or 3 PCLKB

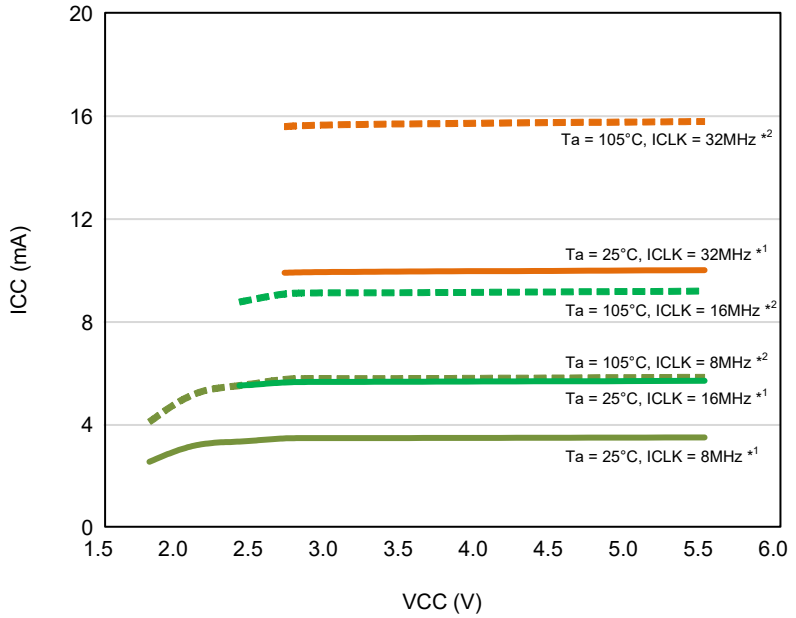
Table 5.2 Recommended Operating Voltage Conditions

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Power supply voltages	VCC*1, *2, *3		1.8	—	5.5	V
	VSS		—	0	—	
Analog power supply voltages	AVCC0*1, *2		1.8	—	5.5	V
	AVSS0		—	0	—	
	VREFH0		1.8	—	AVCC0	
	VREFL0		—	0	—	

Note 1. Use AVCC0 and VCC under the following conditions:
AVCC0 and VCC can be set individually within the operating range when VCC ≥ 2.0 V
AVCC0 = VCC when VCC < 2.0 V

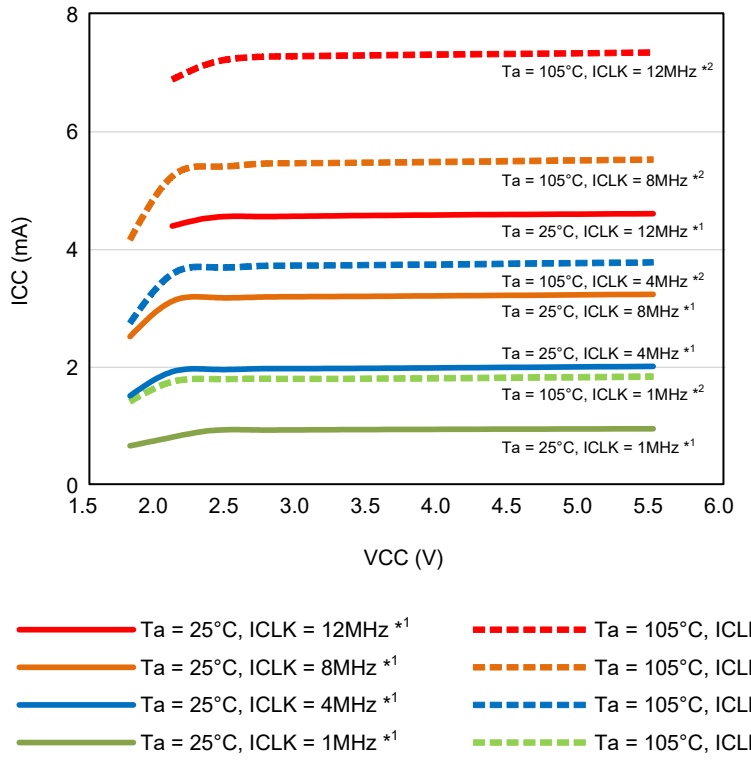
Note 2. When powering on the VCC and AVCC0 pins, power them on at the same time or the VCC pin first and then the AVCC0 pin.

Note 3. When VCC < 2.4 V, some functions of the REMC and CTSU are restricted. For details, refer to section 28, Remote Control Signal Receiver (REMC) and section 32, Capacitive Touch Sensing Unit (CTSUa) in the User's Manual: Hardware.



Note 1. All peripheral operation is normal. This does not include BGO operation. Average value of the tested middle samples during product evaluation.
Note 2. All peripheral operation is maximum. This does not include BGO operation. Average value of the tested upper-limit samples during product evaluation.

Figure 5.1 Voltage Dependency in High-Speed Operating Mode (Reference Data)



Note 1. All peripheral operation is normal. This does not include BGO operation. Average value of the tested middle samples during product evaluation.
Note 2. All peripheral operation is maximum. This does not include BGO operation. Average value of the tested upper-limit samples during product evaluation.

Figure 5.2 Voltage Dependency in Middle-Speed Operating Mode (Reference Data)

[Products with at least 256 Kbytes of flash memory or 100-pin packages]

Table 5.8 DC Characteristics (5)

Conditions: 1.8 V ≤ VCC = AVCC0 < 2.0 V, 2.0 V ≤ VCC ≤ 5.5 V, 2.0 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, Ta = –40 to +105°C

Item					Symbol	Typ.	Max.	Unit	Test Conditions
Supply current*1	High-speed operating mode	Normal operating mode	No peripheral operation*2	ICLK = 32MHz	I_{CC}	3.5	—	mA	
				ICLK = 16MHz		2.4	—		
				ICLK = 8MHz		1.8	—		
			All peripheral operation: Normal*3	ICLK = 32MHz		12.4	—		
				ICLK = 16MHz		7.0	—		
				ICLK = 8MHz		4.3	—		
			All peripheral operation: Max.*3	ICLK = 32MHz		—	25.4		
		Sleep mode	No peripheral operation*2	ICLK = 32MHz		1.8	—		
				ICLK = 16MHz		1.4	—		
				ICLK = 8MHz		1.2	—		
			All peripheral operation: Normal*3	ICLK = 32MHz		6.5	—		
				ICLK = 16MHz		3.8	—		
				ICLK = 8MHz		2.5	—		
		Deep sleep mode	No peripheral operation*2	ICLK = 32MHz		1.1	—		
				ICLK = 16MHz		0.9	—		
				ICLK = 8MHz		0.8	—		
			All peripheral operation: Normal*3	ICLK = 32MHz		5.2	—		
				ICLK = 16MHz		3.0	—		
				ICLK = 8MHz		1.9	—		
		Increase during flash rewrite*5				2.5	—		
	Middle-speed operating modes	Normal operating mode	No peripheral operation*6	ICLK = 12MHz	I_{CC}	2.1	—	mA	
				ICLK = 8MHz		1.4	—		
				ICLK = 4MHz		0.7	—		
				ICLK = 1MHz		0.3	—		
			All peripheral operation: Normal*7	ICLK = 12MHz		5.5	—		
				ICLK = 8MHz		3.9	—		
				ICLK = 4MHz		2.4	—		
				ICLK = 1MHz		1.1	—		
			All peripheral operation: Max.*7	ICLK = 12MHz		—	11.6		
		Sleep mode	No peripheral operation*6	ICLK = 12MHz	I_{CC}	1.4	—	mA	
				ICLK = 8MHz		0.8	—		
				ICLK = 4MHz		0.3	—		
				ICLK = 1MHz		0.2	—		
			All peripheral operation: Normal*7	ICLK = 12MHz		3.2	—		
				ICLK = 8MHz		2.2	—		
				ICLK = 4MHz		1.4	—		
				ICLK = 1MHz		0.8	—		

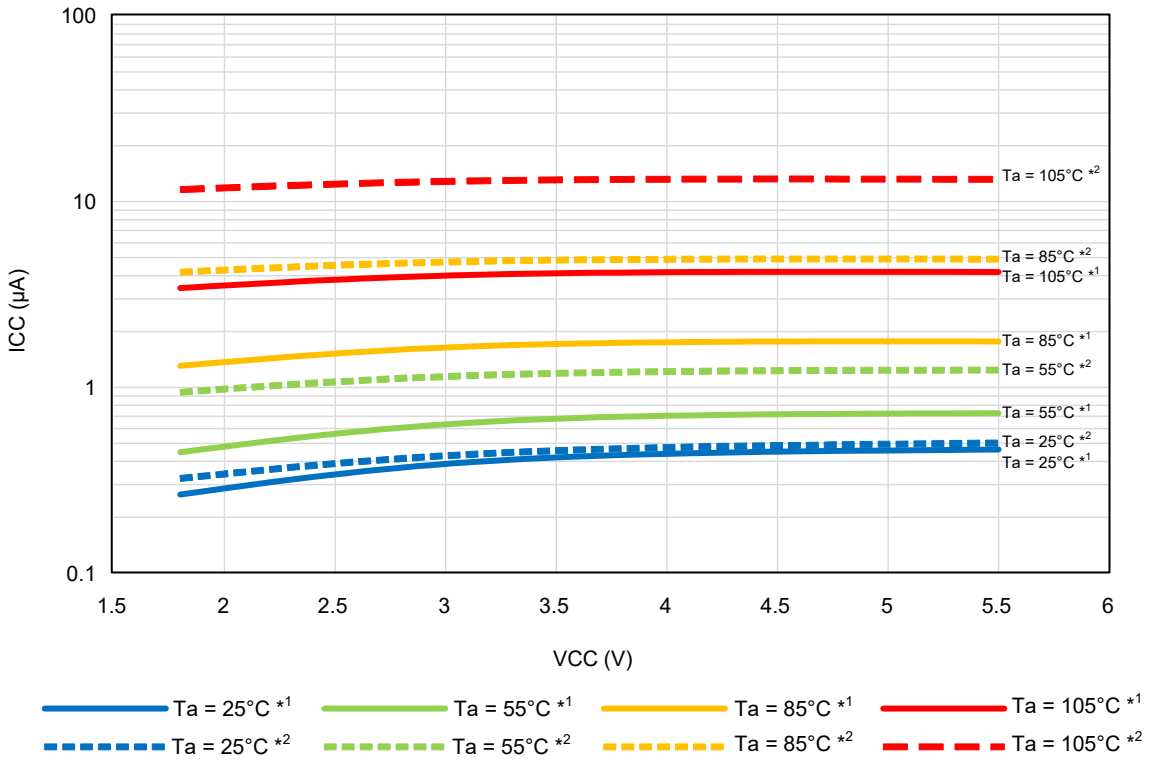
[Products with at least 256 Kbytes of flash memory or 100-pin packages]

Table 5.10 DC Characteristics (6)

Conditions: 1.8 V ≤ VCC = AVCC0 < 2.0 V, 2.0 V ≤ VCC ≤ 5.5 V, 2.0 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, Ta = –40 to +105°C

Item			Symbol	Typ.*3	Max.	Unit	Test Conditions
Supply current*1	Software standby mode*2	T_a = 25°C	I_{CC}	0.41	0.98	μA	
		T_a = 55°C		0.66	2.78		
		T_a = 85°C		1.69	9.65		
		T_a = 105°C		4.08	25.04		
	Increment for RTC operation*4			0.40	—		RCR3.RTCDV[2:0] set to low drive capacity
				1.21	—		RCR3.RTCDV[2:0] set to normal drive capacity
	Increment for low-power timer operation			0.37	—		LPTCR1.LPCNTCKSEL set to IWDT-dedicated on-chip oscillator
	Increment for Independent Watchdog Timer operation			0.37	—		
	Increment for REMC operation			0.44*4	—		REMCON1.CSRC[3:0] set to Sub-clock RCR3.RTCDV[2:0] set to low drive capacity
				1.34*4	—		REMCON1.CSRC[3:0] set to Sub-clock RCR3.RTCDV[2:0] set to normal drive capacity
				235	—		REMCON1.CSRC[3:0] set to HOCO clock/512

Note 1. Supply current values are with all output pins unloaded and all input pull-up MOSs in the off state.
Note 2. The IWDT, LVD, and CMPB are stopped.
Note 3. VCC = 3.3 V.
Note 4. Includes the oscillation circuit.



Note 1. Average value of the tested middle samples during product evaluation.
Note 2. Average value of the tested upper-limit samples during product evaluation.

Figure 5.9 Voltage Dependency in Software Standby Mode (Reference Data)

Table 5.12 DC Characteristics (8)

Conditions: 1.8 V ≤ VCC = AVCC0 < 2.0 V, 2.0 V ≤ VCC ≤ 5.5 V, 2.0 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, Ta = –40 to +105°C

Item		Symbol	Min.	Typ.*4	Max.	Unit	Test Conditions
Analog power supply current	During A/D conversion (at high-speed conversion)	I_{AVCC}	—	0.7	1.7	mA	
	During A/D conversion (at low-speed conversion)		—	0.6	1.0		
	During D/A conversion (per channel)*1		—	—	1.5		
	Waiting for A/D and D/A conversion (all units)		—	—	0.4	µA	
Reference power supply current	During A/D conversion (at high-speed conversion)	I_{REFH0}	—	25	150	µA	
	Waiting for A/D conversion (all units)		—	—	60	nA	
LVD0	—	I_{LVD}	—	0.1	—	µA	
LVD1, 2	Per channel		—	0.15	—	µA	
Temperature sensor*3	—	I_{TEMP}	—	75	—	µA	
Comparator B operating current*3	Window function enabled	I_{CMP}*2	—	12.5	28.6	µA	
	Comparator high-speed mode (per channel)		—	3.2	16.2	µA	
	Comparator low-speed mode (per channel)		—	1.7	4.4	µA	
CUSU operating current	During measurement (CPU is in sleep mode) Base clock: 2 MHz Pin capacity: 50 pF	I_{CTSU}	—	150	—	µA	

Note 1. The value of the D/A converter is the value of the power supply current including the reference current.
Note 2. Current consumed only by the comparator B module.
Note 3. ICurrent consumed by the power supply (VCC).
Note 4. When VCC = AVCC0 = 3.3 V.

Table 5.13 DC Characteristics (9)

Conditions: 1.8 V ≤ VCC = AVCC0 < 2.0 V, 2.0 V ≤ VCC ≤ 5.5 V, 2.0 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, Ta = –40 to +105°C

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
RAM standby voltage	V_{RAM}	1.8	—	—	V	

Table 5.14 DC Characteristics (10)

Conditions: 1.8 V ≤ VCC = AVCC0 < 2.0 V, 2.0 V ≤ VCC ≤ 5.5 V, 2.0 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, Ta = –40 to +105°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Power-on VCC rising gradient	At normal startup*1	SrVCC	0.02	—	20	ms/V	
	During fast startup time*2		0.02	—	2		
	Voltage monitoring 0 reset enabled at startup*3, *4		0.02	—	—		

Note 1. When OFS1.(FASTSTUP, LVDAS) = 11b.
Note 2. When OFS1.(FASTSTUP, LVDAS) = 01b.
Note 3. When OFS1.LVDAS = 0.
Note 4. Turn on the power supply voltage according to the normal startup rising gradient because the register settings set by OFS1 are not read in boot mode.

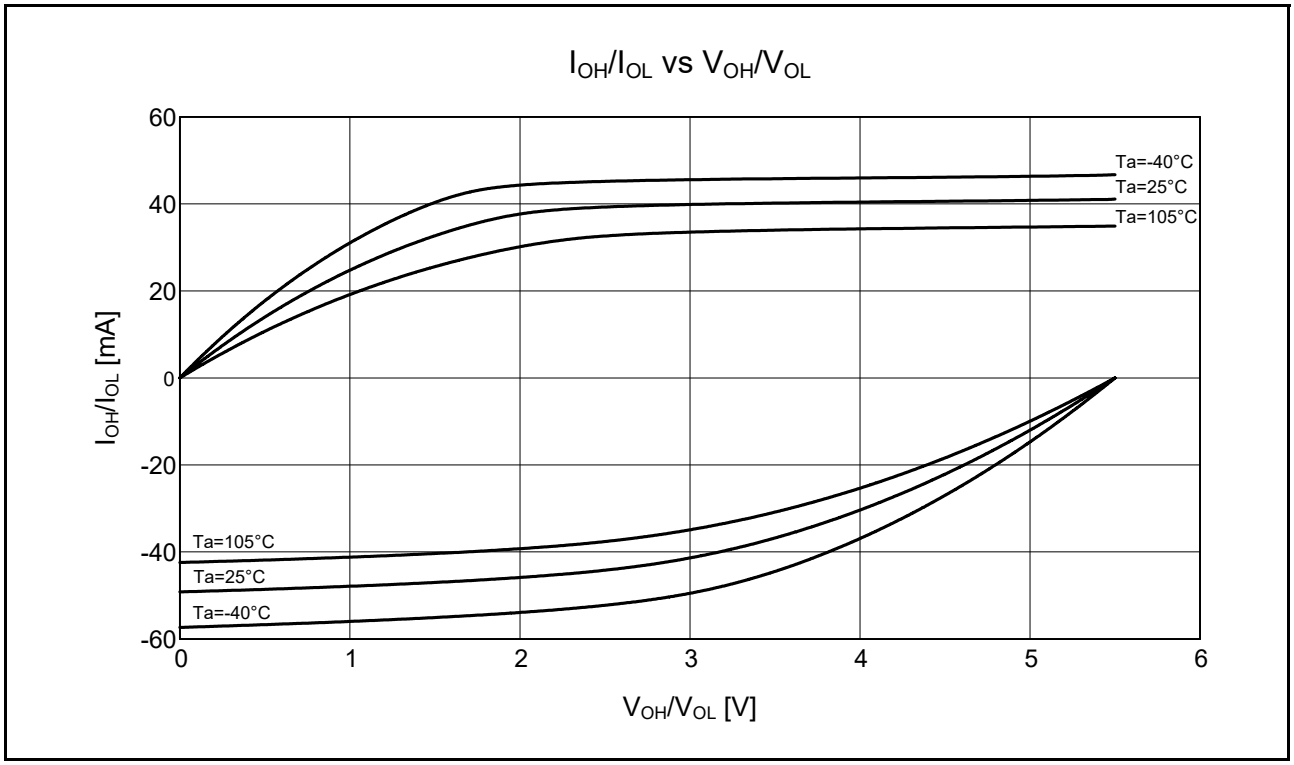


Figure 5.16 V_{OH}/V_{OL} **and** I_{OH}/I_{OL} **Temperature Characteristics at VCC = 5.5 V When Normal Output is Selected (Reference Data)**

5.3 AC Characteristics

5.3.1 Clock Timing

Table 5.22 Operating Frequency Value (High-Speed Operating Mode)

Conditions: 1.8 V ≤ VCC = AVCC0 < 2.0 V, 2.0 V ≤ VCC ≤ 5.5 V, 2.0 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, Ta = –40 to +105°C

Item		Symbol	VCC			Unit
			1.8 V ≤ VCC < 2.4 V	2.4 V ≤ VCC < 2.7 V	2.7 V ≤ VCC ≤ 5.5 V	
Maximum operating frequency*4	System clock (ICLK)	f_{max}	8	16	32	MHz
	FlashIF clock (FCLK)*1, *2		8	16	32	
	Peripheral module clock (PCLKB)		8	16	32	
	Peripheral module clock (PCLKD)*3		8	16	32	

Note 1. The lower-limit frequency of FCLK is 1 MHz during programming or erasing of the flash memory. When using FCLK at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.
Note 2. The frequency accuracy of FCLK should be ±3.5%.
Note 3. The lower-limit frequency of PCLKD is 4 MHz at 2.4 V or above and 1 MHz at below 2.4 V when the A/D converter is in use.
Note 4. The maximum operating frequency does not include HOCO error or PLL jitter. See Table 5.25, Clock Timing.

Table 5.23 Operating Frequency Value (Middle-Speed Operating Mode)

Conditions: 1.8 V ≤ VCC = AVCC0 < 2.0 V, 2.0 V ≤ VCC ≤ 5.5 V, 2.0 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, Ta = –40 to +105°C

Item		Symbol	VCC			Unit
			1.8 V ≤ VCC < 2.4 V	2.4 V ≤ VCC < 2.7 V	2.7 V ≤ VCC ≤ 5.5 V	
Maximum operating frequency*4	System clock (ICLK)	f_{max}	8	12	12	MHz
	FlashIF clock (FCLK)*1, *2		8	12	12	
	Peripheral module clock (PCLKB)		8	12	12	
	Peripheral module clock (PCLKD)*3		8	12	12	

Note 1. The lower-limit frequency of FCLK is 1 MHz during programming or erasing of the flash memory. When using FCLK at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.
Note 2. The frequency accuracy of FCLK should be ±3.5%.
Note 3. The lower-limit frequency of PCLKD is 4 MHz at 2.4 V or above and 1 MHz at below 2.4 V when the A/D converter is in use.
Note 4. The maximum operating frequency does not include HOCO error or PLL jitter. See Table 5.25, Clock Timing

Table 5.24 Operating Frequency Value (Low-Speed Operating Mode)

Conditions: 1.8 V ≤ VCC = AVCC0 < 2.0 V, 2.0 V ≤ VCC ≤ 5.5 V, 2.0 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, Ta = –40 to +105°C

Item		Symbol	VCC			Unit
			1.8 V ≤ VCC < 2.4 V	2.4 V ≤ VCC < 2.7 V	2.7 V ≤ VCC ≤ 5.5 V	
Maximum operating frequency	System clock (ICLK)	f_{max}	32.768			kHz
	FlashIF clock (FCLK)*1		32.768			
	Peripheral module clock (PCLKB)		32.768			
	Peripheral module clock (PCLKD)*2		32.768			

Note 1. Programming and erasing the flash memory is impossible.
Note 2. The A/D converter cannot be used.

When the main clock oscillator wait control register (MOSCWTCR) is set to 00h.

Table 5.29 Timing of Recovery from Low Power Consumption Modes (3)

Conditions: 1.8 V ≤ VCC = AVCC0 < 2.0 V, 2.0 V ≤ VCC ≤ 5.5 V, 2.0 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, Ta = –40 to +105°C

Item			Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Recovery time from software standby mode*1	Low-speed mode	Sub-clock oscillator operating	t_{SBYSC}	—	600	750	µs	Figure 5.37

Note: Note Values when the frequencies of PCLKB, PCLKD, and FCLK are not divided.
Note 1. The sub-clock continues oscillating in software standby mode during low-speed mode.

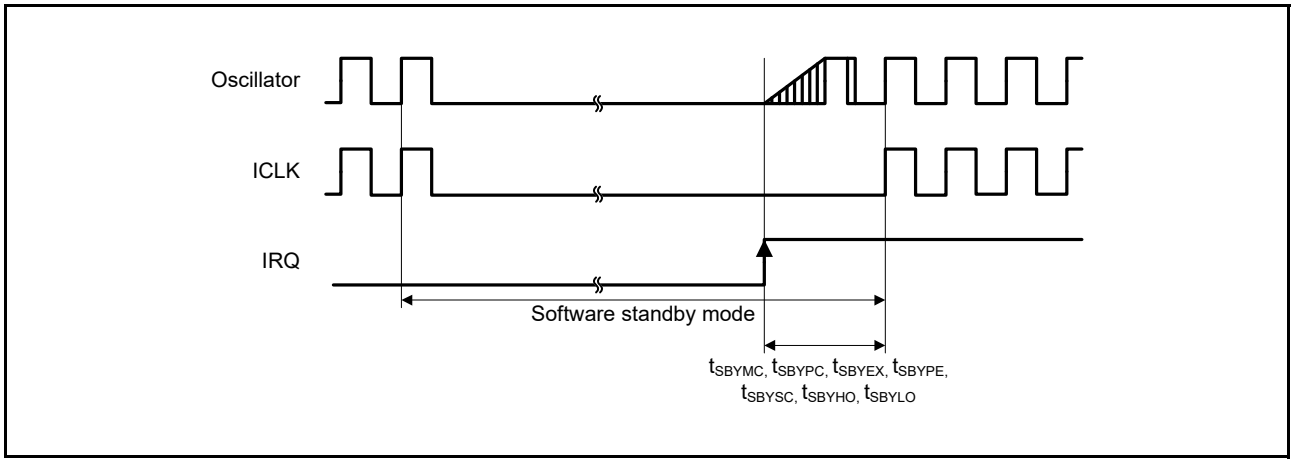


Figure 5.37 Software Standby Mode Recovery Timing

Table 5.30 Timing of Recovery from Low Power Consumption Modes (4)

Conditions: 1.8 V ≤ VCC = AVCC0 < 2.0 V, 2.0 V ≤ VCC ≤ 5.5 V, 2.0 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, Ta = –40 to +105°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Recovery time from deep sleep mode*1	High-speed mode*2	t_{DSLP}	—	2	3.5	µs	Figure 5.38
	Middle-speed mode*3	t_{DSLP}	—	3	4	µs	
	Low-speed mode*4	t_{DSLP}	—	400	500	µs	

Note: Note Values when the frequencies of PCLKB, PCLKD, and FCLK are not divided.
Note 1. Oscillators continue oscillating in deep sleep mode.
Note 2. When the frequency of the system clock is 32 MHz.
Note 3. When the frequency of the system clock is 12 MHz.
Note 4. When the frequency of the system clock is 32.768 kHz.

Table 5.35 Timing of On-Chip Peripheral Modules (3)

Conditions: 1.8 V ≤ VCC = AVCC0 < 2.0 V, 2.0 V ≤ VCC ≤ 5.5 V, 2.0 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, Ta = –40 to +105°C

Item			Symbol	Min.	Max.	Unit*1	Test Conditions
Simple SPI	SCK clock cycle output (master)		t_{SPcyc}	4	65536	t_{Pcyc}	Figure 5.50
	SCK clock cycle input (slave)			6	—	t_{Pcyc}	
	SCK clock high pulse width		t_{SPCKWH}	0.4	0.6	t_{SPcyc}	
	SCK clock low pulse width		t_{SPCKWL}	0.4	0.6	t_{SPcyc}	
	SCK clock rise/fall time		t_{SPCKr}, t_{SPCKf}	—	20	ns	
	Data input setup time (master)	2.7 V or above	t_{SU}	65	—	ns	Figure 5.51, Figure 5.52
		1.8 V or above		95	—		
	Data input setup time (slave)			40	—		
	Data input hold time		t_H	40	—	ns	
	SSL input setup time		t_{LEAD}	3	—	t_{SPcyc}	
	SSL input hold time		t_{LAG}	3	—	t_{SPcyc}	
	Data output delay time (master)		t_{OD}	—	40	ns	
	Data output delay time (slave)	2.7 V or above		—	65		
		1.8 V or above		—	100		
	Data output hold time (master)	2.7 V or above	t_{OH}	–10	—	ns	
		1.8 V or above		–20	—		
	Data output hold time (slave)			–10	—		
	Data rise/fall time		t_{Dr}, t_{Df}	—	20	ns	
	SSL input rise/fall time		t_{SSLr}, t_{SSLf}	—	20	ns	
	Slave access time		t_{SA}	—	6	t_{Pcyc}	Figure 5.53, Figure 5.54
	Slave output release time		t_{REL}	—	6	t_{Pcyc}	

Note 1. t_{Pcyc}: PCLK cycle

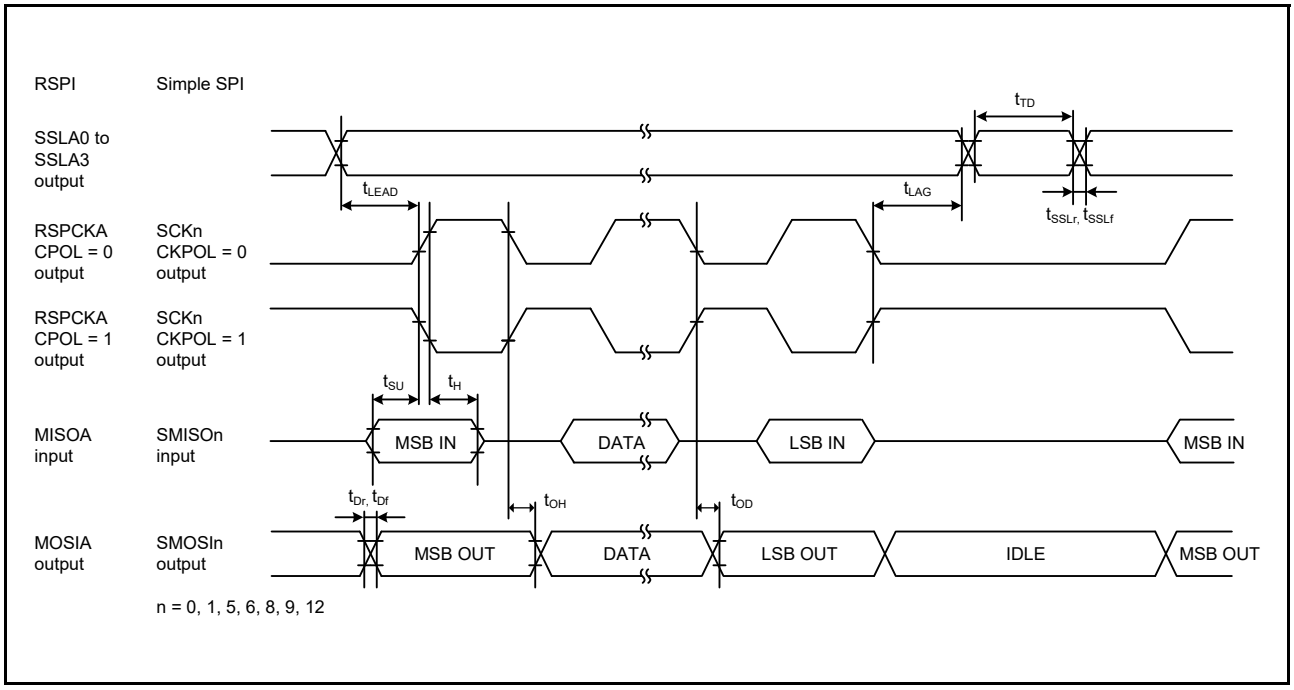


Figure 5.51 RSPI Timing (Master, CPHA = 0) and Simple SPI Clock Timing (Master, CKPH = 1)

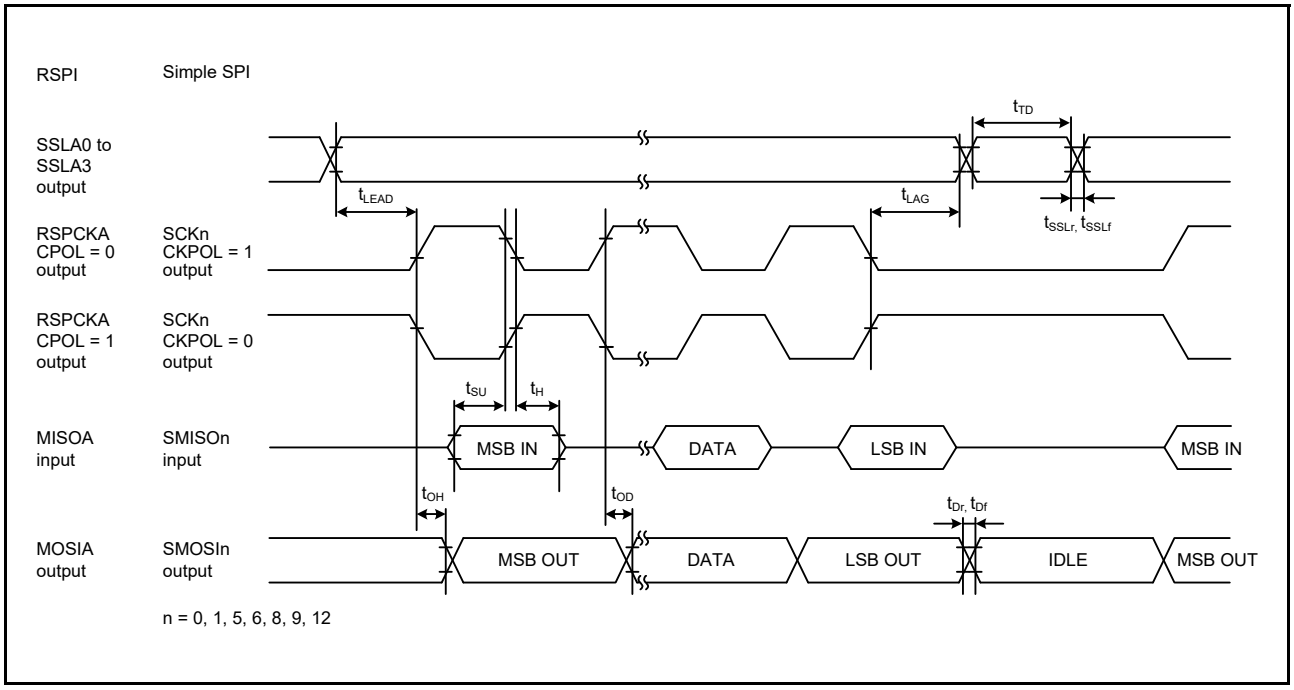


Figure 5.52 RSPI Timing (Master, CPHA = 1) and Simple SPI Clock Timing (Master, CKPH = 0)

Absolute accuracy

Absolute accuracy is the difference between output code based on the theoretical A/D conversion characteristics, and the actual A/D conversion result. When measuring absolute accuracy, the voltage at the midpoint of the width of analog input voltage (1-LSB width), that can meet the expectation of outputting an equal code based on the theoretical A/D conversion characteristics, is used as an analog input voltage. For example, if 12-bit resolution is used and if reference voltage (VREFH0 = 3.072 V), then 1-LSB width becomes 0.75 mV, and 0 mV, 0.75 mV, 1.5 mV, ... are used as analog input voltages.
If analog input voltage is 6 mV, absolute accuracy = ±5 LSB means that the actual A/D conversion result is in the range of 003h to 00Dh though an output code, 008h, can be expected from the theoretical A/D conversion characteristics.

Integral nonlinearity error (INL)

Integral nonlinearity error is the maximum deviation between the ideal line when the measured offset and full-scale errors are zeroed, and the actual output code.

Differential nonlinearity error (DNL)

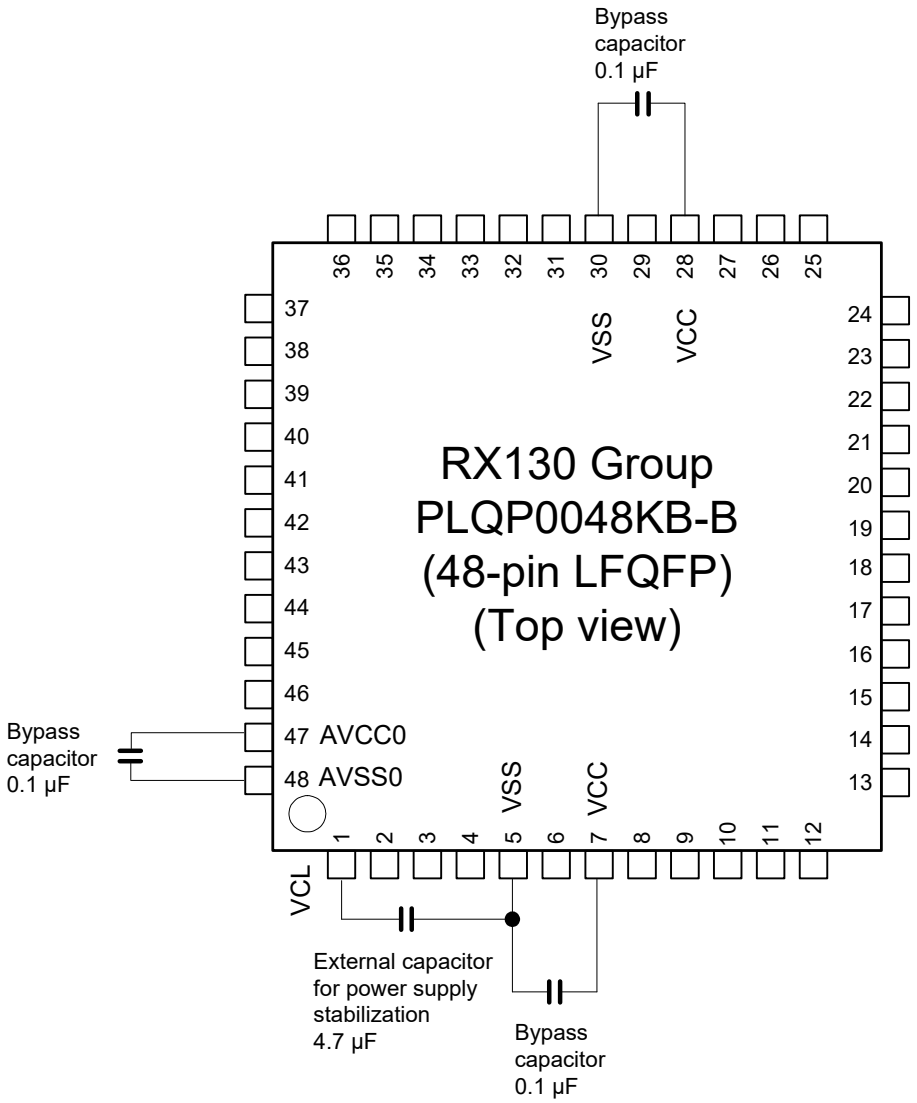
Differential nonlinearity error is the difference between 1-LSB width based on the ideal A/D conversion characteristics and the width of the actual output code.

Offset error

Offset error is the difference between a transition point of the ideal first output code and the actual first output code.

Full-scale error

Full-scale error is the difference between a transition point of the ideal last output code and the actual last output code.



Note. Do not apply the power supply voltage to the VCL pin.
Use a 4.7-µF multilayer ceramic for the VCL pin and place it close to the pin.
A recommended value is shown for the capacitance of the bypass capacitors.

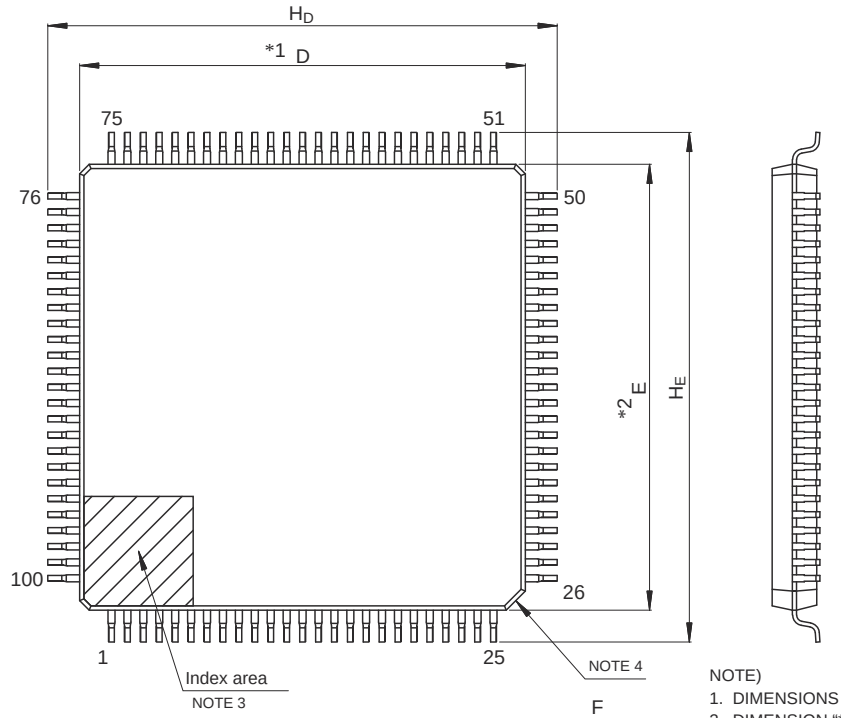
Figure 5.70 Connecting Capacitors (48 Pins)

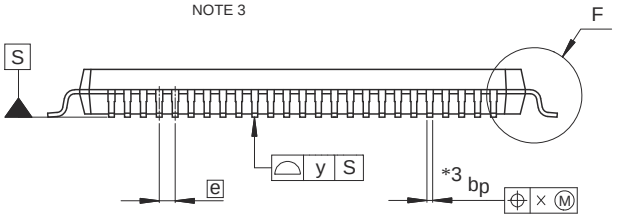
Appendix 1. Package Dimensions

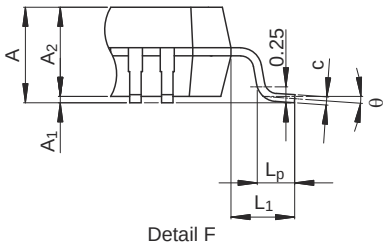
Information on the latest version of the package dimensions or mountings has been displayed in “Packages” on Renesas Electronics Corporation website.

JEITA Package Code	RENESAS Code	Previous Code	MASS (Typ) [g]
P-LFQFP100-14x14-0.50	PLQP0100KB-B	—	0.6

Unit: mm







NOTE)
1. DIMENSIONS “*1” AND “*2” DO NOT INCLUDE MOLD FLASH.
2. DIMENSION “*3” DOES NOT INCLUDE TRIM OFFSET.
3. PIN 1 VISUAL INDEX FEATURE MAY VARY, BUT MUST BE LOCATED WITHIN THE HATCHED AREA.
4. CHAMFERS AT CORNERS ARE OPTIONAL, SIZE MAY VARY.

Reference Symbol	Dimensions in millimeters		
	Min	Nom	Max
D	13.9	14.0	14.1
E	13.9	14.0	14.1
A_2	—	1.4	—
H_D	15.8	16.0	16.2
H_E	15.8	16.0	16.2
A	—	—	1.7
A_1	0.05	—	0.15
b_p	0.15	0.20	0.27
c	0.09	—	0.20
θ	0°	3.5°	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
L_p	0.45	0.6	0.75
L_1	—	1.0	—

Figure A 100-Pin LFQFP (PLQP0100KB-B)