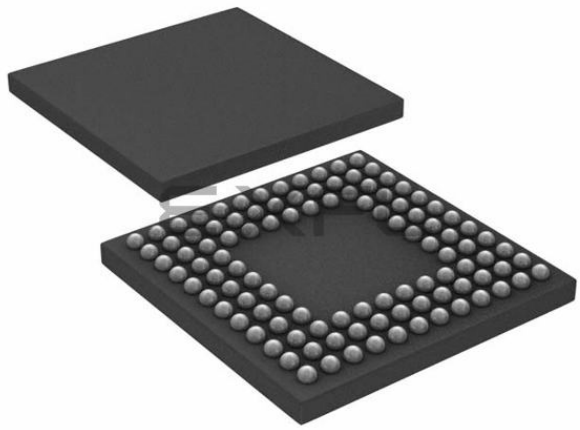

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM7®
Core Size	16/32-Bit
Speed	41.78MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	32
Program Memory Size	126KB (63K x 16)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 32
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 13x12b; D/A 12x12b
Oscillator Type	Internal
Operating Temperature	-10°C ~ 95°C (TA)
Mounting Type	Surface Mount
Package / Case	108-LFBGA, CSPBGA
Supplier Device Package	108-CSPBGA (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/aduc7122bbcz

TIMING SPECIFICATIONS

Table 2. I²C Timing in Fast Mode (400 kHz)

		Slave			Master			
Parameter	**Description**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
t_L	SCLx low pulse width	200				1360		ns
t_H	SCLx high pulse width	100				1140		ns
t_{SHD}	Start condition hold time	300						ns
t_{DSU}	Data setup time	100				740		ns
t_{DHD}	Data hold time	0				400		ns
t_{RSU}	Setup time for repeated start	100						ns
t_{PSU}	Stop condition setup time	100				800		ns
t_{BUF}	Bus-free time between a stop condition and a start condition	1.3						µs
t_R	Rise time for both SCLx and SDAx			300		200		ns
t_F	Fall time for both SCLx and SDAx			300				ns

Table 3. I²C Timing in Standard Mode (100 kHz)

		Slave		
Parameter	**Description**	**Min**	**Typ**	**Max**	**Unit**
t_L	SCLx low pulse width	4.7			µs
t_H	SCLx high pulse width	4.0			ns
t_{SHD}	Start condition hold time	4.0			µs
t_{DSU}	Data setup time	250			ns
t_{DHD}	Data hold time	0		3.45	µs
t_{RSU}	Setup time for repeated start	4.7			µs
t_{PSU}	Stop condition setup time	4.0			µs
t_{BUF}	Bus-free time between a stop condition and a start condition	4.7			µs
t_R	Rise time for both SCLx and SDAx			1	µs
t_F	Fall time for both SCLx and SDAx			300	ns

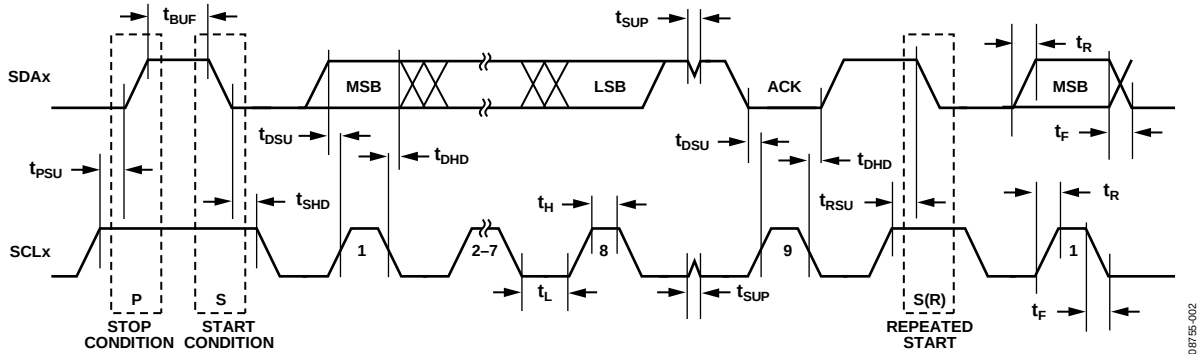

Figure 2. I²C-Compatible Interface Timing

Table 4. SPI Master Mode Timing (SPICPH = 1)

Parameter	Description	Min	Typ	Max	Unit
t_{SL}	SCLOCK low pulse width		(SPIDIV + 1) × t_{UCLK}		ns
t_{SH}	SCLOCK high pulse width		(SPIDIV + 1) × t_{UCLK}		ns
t_{DAV}	Data output valid after SCLOCK edge			25	ns
t_{DSU}	Data input setup time before SCLOCK edge[1]	1 × t_{UCLK}			ns
t_{DHD}	Data input hold time after SCLOCK edge	2 × t_{UCLK}			ns
t_{DF}	Data output fall time		5	12.5	ns
t_{DR}	Data output rise time		5	12.5	ns
t_{SR}	SCLOCK rise time		5	12.5	ns
t_{SF}	SCLOCK fall time		5	12.5	ns

[1] t_{UCLK} = 23.9 ns. It corresponds to the 41.78 MHz internal clock from the PLL before the clock divider.

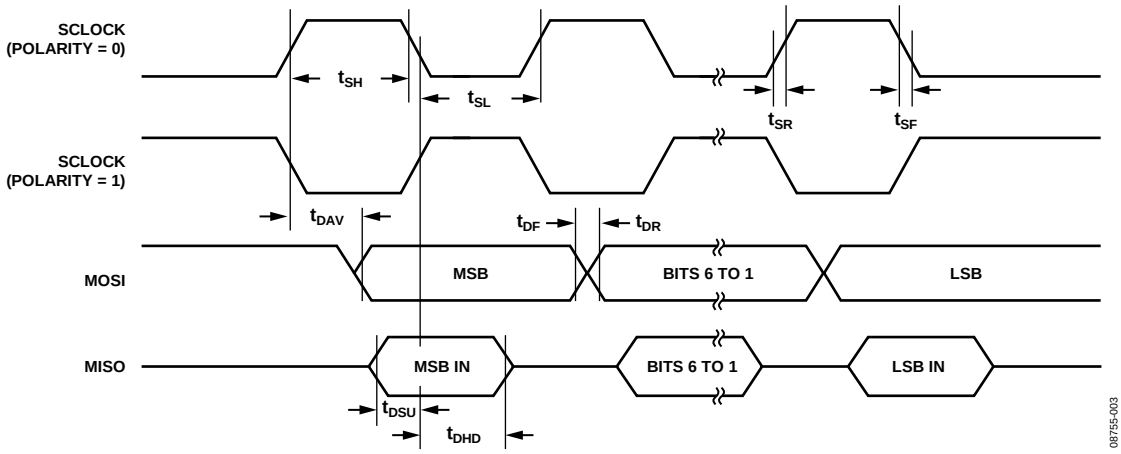

Figure 3. SPI Master Mode Timing (SPICPH = 1)

Table 22. PLA Base Address = 0xFFFF0B00

Address	Name	Byte	Access Type	Cycle
0x0B00	PLAELM0	2	R/W	2
0x0B04	PLAELM1	2	R/W	2
0x0B08	PLAELM2	2	R/W	2
0x0B0C	PLAELM3	2	R/W	2
0x0B10	PLAELM4	2	R/W	2
0x0B14	PLAELM5	2	R/W	2
0x0B18	PLAELM6	2	R/W	2
0x0B1C	PLAELM7	2	R/W	2
0x0B20	PLAELM8	2	R/W	2
0x0B24	PLAELM9	2	R/W	2
0x0B28	PLAELM10	2	R/W	2
0x0B2C	PLAELM11	2	R/W	2
0x0B30	PLAELM12	2	R/W	2
0x0B34	PLAELM13	2	R/W	2
0x0B38	PLAELM14	2	R/W	2
0x0B3C	PLAELM15	2	R/W	2
0x0B40	PLACLK	1	R/W	2
0x0B44	PLAIRQ	4	R/W	2
0x0B48	PLAADC	4	R/W	2
0x0B4C	PLADIN	4	R/W	2
0x0B50	PLADOUT	4	R	2

Table 23. GPIO Base Address = 0xFFFF0D00

Address	Name	Byte	Access Type	Cycle
0x0D00	GP0CON	4	R/W	1
0x0D04	GP1CON	4	R/W	1
0x0D08	GP2CON	4	R/W	1
0x0D0C	GP3CON	4	R/W	1
0x0D20	GP0DAT	4	R/W	1
0x0D24	GP0SET	1	W	1
0x0D28	GP0CLR	1	W	1
0x0D2C	GP0PAR	4	R/W	1
0x0D30	GP1DAT	4	R/W	1
0x0D34	GP1SET	1	W	1
0x0D38	GP1CLR	1	W	1
0x0D3C	GP1PAR	4	R/W	1
0x0D40	GP2DAT	4	R/W	1
0x0D44	GP2SET	1	W	1
0x0D48	GP2CLR	1	W	1
0x0D4C	GP2PAR	4	R/W	1
0x0D50	GP3DAT	4	R/W	1
0x0D54	GP3SET	1	W	1
0x0D58	GP3CLR	1	W	1
0x0D5C	GP3PAR	4	R/W	1
0x0D70	GP1OCE	1	W	1
0x0D74	GP2OCE	1	W	1
0x0D78	GP3OCE	1	W	1

Table 24. Flash/EE Block 0 Base Address = 0xFFFF0E00

Address	Name	Byte	Access Type	Cycle
0x0E00	FEE0STA	1	R	1
0x0E04	FEE0MOD	1	R/W	1
0x0E08	FEE0CON	1	R/W	1
0x0E0C	FEE0DAT	2	R/W	1
0x0E10	FEE0ADR	2	R/W	1
0x0E18	FEE0SGN	3	R	1
0x0E1C	FEE0PRO	4	R/W	1
0x0E20	FEE0HID	4	R/W	1

Table 25. Flash/EE Block 1 Base Address = 0xFFFF0E80

Address	Name	Byte	Access Type	Cycle
0x0E80	FEE1STA	1	R	1
0x0E84	FEE1MOD	1	R/W	1
0x0E88	FEE1CON	1	R/W	1
0x0E8C	FEE1DAT	2	R/W	1
0x0E90	FEE1ADR	2	R/W	1
0x0E98	FEE1SGN	3	R	1
0x0E9C	FEE1PRO	4	R/W	1
0x0EA0	FEE1HID	4	R/W	1

Table 26. PWM Base Address= 0xFFFF0F80

Address	Name	Byte	Access Type	Cycle
0x0F80	PWMCON1	2	R/W	2
0x0F84	PWM1COM1	2	R/W	2
0x0F88	PWM1COM2	2	R/W	2
0x0F8C	PWM1COM3	2	R/W	2
0x0F90	PWM1LEN	2	R/W	2
0x0F94	PWM2COM1	2	R/W	2
0x0F98	PWM2COM2	2	R/W	2
0x0F9C	PWM2COM3	2	R/W	2
0x0FA0	PWM2LEN	2	R/W	2
0x0FA4	PWM3COM1	2	R/W	2
0x0FA8	PWM3COM2	2	R/W	2
0x0FAC	PWM3COM3	2	R/W	2
0x0FB0	PWM3LEN	2	R/W	2
0x0FB4	PWMCON2	2	R/W	2
0x0FB8	PWMICLR	2	W	2

ADC CIRCUIT OVERVIEW

The analog-to-digital converter (ADC) incorporates a fast, multichannel, 12-bit ADC. It can operate from 3.0 V to 3.6 V supplies and is capable of providing a throughput of up to 1 MSPS when the clock source is 41.78 MHz. This block provides the user with a multichannel multiplexer, differential track-and-hold, on-chip reference, and ADC.

The ADC consists of a 12-bit successive approximation converter based around two capacitor DACs. Depending on the input signal configuration, the ADC can operate in one of the following three modes:

- Fully differential mode for small and balanced signals
- Single-ended mode for any single-ended signals
- Pseudo differential mode for any single-ended signals, taking advantage of the common-mode rejection offered by the pseudo differential input

The converter accepts an analog input range of 0 to V_{REF} when operating in single-ended mode or pseudo differential mode. In fully differential mode, the input signal must be balanced around a common-mode voltage, V_{CM}, in the range 0 V to AV_{DD}, and with maximum amplitude of 2 V_{REF} (see Figure 12).

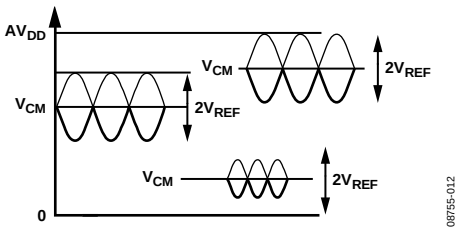

Figure 12. Examples of Balanced Signals for Fully Differential Mode

A high precision, low drift, and factory-calibrated 2.5 V reference is provided on chip. An external reference can also be connected as described in the Band Gap Reference section.

Single or continuous conversion modes can be initiated in software. An external $\overline{\text{CONVST}}$ pin, an output generated from the on-chip PLA, or a Timer0 or Timer1 overflow can also be used to generate a repetitive trigger for ADC conversions.

If the signal has not been deasserted by the time the ADC conversion is complete, a second conversion begins automatically.

A voltage output from an on-chip band gap reference proportional to absolute temperature can also be routed through the front-end ADC multiplexer, effectively an additional ADC channel input. This facilitates an internal temperature sensor channel, measuring die temperature to an accuracy of ±3°C.

For the ADuC7122, a number of modifications have been made to the ADC input structure that appears in the ADuC702x family.

The PADC0 and PADC1 inputs connect to a PGA in pseudo differential mode and allow for selectable gains from 1 to 5 with 32 steps. The remaining ADC channels can be configured as single, differential, or pseudo differential. A buffer is provided before the ADC for measuring internal channels.

ADC TRANSFER FUNCTION

Pseudo Differential and Single-Ended Modes

In pseudo differential or single-ended mode, the input range is 0 V to V_{REF}. The output coding is straight binary in pseudo differential and single-ended modes with

1 LSB = FS/4096 or
2.5 V/4096 = 0.61 mV or
610 µV when V_{REF} = 2.5 V

The ideal code transitions occur midway between successive integer LSB values (that is, 1/2 LSB, 3/2 LSBs, 5/2 LSBs, …, FS – 3/2 LSBs). The ideal input/output transfer characteristic is shown in Figure 13.

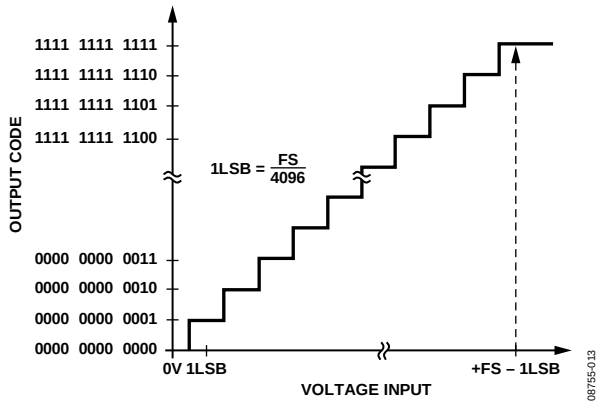

Figure 13. ADC Transfer Function in Pseudo Differential Mode or Single-Ended Mode

Fully Differential Mode

The amplitude of the differential signal is the difference between the signals applied to the V_{IN+} and V_{IN-} inputs (that is, V_{IN+} – V_{IN-}) of the currently enabled differential channel. The maximum amplitude of the differential signal is, therefore, $-V_{REF}$ to $+V_{REF}$ p-p ($2 \times V_{REF}$). This is regardless of the common mode (CM). The common mode is the average of the two signals (V_{IN+} + V_{IN-})/2, and is, therefore, the voltage that the two inputs are centered on. This results in the span of each input being CM ± V_{REF}/2. This voltage must be set up externally, and its range varies with V_{REF} (see the Driving the Analog Inputs section).

The output coding is twos complement in fully differential mode with 1 LSB = 2 V_{REF}/4096 or 2 × 2.5 V/4096 = 1.22 mV when V_{REF} = 2.5 V. The output result is ±11 bits, but this is shifted by one to the right, which allows the result in ADCDAT to be declared as a signed integer when writing C code. The designed code transitions occur midway between successive integer LSB values (that is, 1/2 LSB, 3/2 LSBs, 5/2 LSBs, …, FS – 3/2 LSBs). The ideal input/output transfer characteristic is shown in Figure 14.

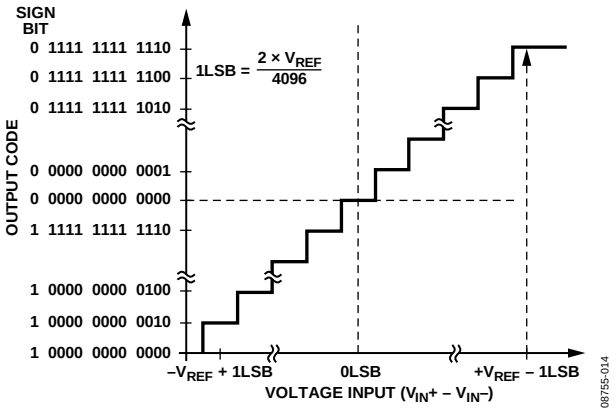

Figure 14. ADC Transfer Function in Differential Mode

ADC Input Channels

The ADuC7122 provides 11 fixed gain ADC input pins. Each of these pins can be separately configured as a differential input pair, single-ended input, or positive side pseudo differential input (the negative side must be the AINCM channel). The buffer and ADC are configured independently from input channel selection. Note that the input range of the ADC input buffer is from 0.15 V to AV_{DD} – 0.15 V. If the input signal range exceeds this range, the input buffer must be bypassed.

The ADC mux can be configured to select an internal channel like IOVDD_MON or the temperature sensor. When converting on an internal channel, the input buffer must be enabled.

In addition, an on-chip diode can be selected to provide chip temperature monitoring. The ADC can also select V_{REF} and AGND as the input for calibration purposes.

PGA and Input Buffer

The ADuC7122 contains two programmable gain channels that operate in pseudo differential mode. The PGA is a one-stage positive gain amplifier that is able to accept an input from 0.1 V to AV_{DD} – 1.2 V. The PGA output can swing up to 2.5 V. The PGA is designed to handle 10 mV minimum input.

The gain of the PGA is from 1 to 5 with 32 linear steps. The PGA cannot be bypassed for the PADC0 and PADC1 channels.

The PGAs use a PMOS input to minimize nonlinearity and noise. The input level for PGA is limited from AV_{DD} – 1.2 V to 0.1 V to make sure the amplifiers are not saturated. The input buffer is a rail-to-rail buffer. It can accept signals from 0.15 V to AV_{DD} – 0.15 V. Each of the input buffers can be bypassed independently.

To minimize noise, the PADC input buffer can be bypassed.

PADCxN is driven by a buffer to 0.15 V to keep the PGA from saturation when the input current drops to 0. The buffer can be disabled by setting ADCCON[14] so that the PADCxN can be connected to GND as well.

The PADCx channels are only specified to operate in pseudo differential mode and this assumes the negative input is close to ground.

POWER SUPPLY MONITOR

The power supply monitor on the ADuC7122 indicates when the IOV_{DD} supply pin drops below one of two supply trip points. The monitor function is controlled via the PSMCON register. If enabled in the IRQEN or FIQEN register, the monitor interrupts the core using the PSMI bit in the PSMCON MMR. This bit is cleared immediately when CMP goes high. Note that if the interrupt generated is exited before CMP goes high (IOV_{DD} is above the trip point), no further interrupts are generated until CMP returns high. The user should ensure that code execution remains within the ISR until CMP returns high.

This monitor function allows the user to save working registers to avoid possible data loss due to the low supply or brownout conditions. It also ensures that normal code execution does not resume until a safe supply level has been established.

When the ADC channel selection bits are configured to IOVDD_MON (ADCCP[4:0] = 10011), this permits the ADC to convert the voltage available at the input of the power supply monitor comparator. When measuring an internal channel, the internal buffer must be enabled. The internal buffer should be enabled to isolate from external interference when sampling any of the internal channels. Before measuring this voltage, the following sequence is required:

1. Measure VREF using the ADC.
2. Set ADCCP = IOVDD_MON channel.
3. Set a typical delay of 60 µs.
4. Perform ADC conversion on the IOVDD_MON channel (use an ADCCON value of 0x2AA3 for optimum results).

The delay between the ADC mux select switching and the initiation of the conversion is required to allow the voltage on the ADC sampling capacitor to settle to the divided down supply voltage.

Table 36. REFCON MMR Bit Designations (Address = 0xFFFF0480, Default Value = 0x01)

Bit	Description
7:1	Reserved.
2	Reserved. Always set to 1. This bit outputs the buffered version of the internal 2.5 V reference onto BUF_VREF1 and BUF_VREF2. To disable this buffer, the user must disable the internal reference by clearing REFCON = 0x00.
1	Internal 2.5 V reference output enable. Set by the user to connect the internal 2.5 V reference to the V_{REF}_2.5 pin. Cleared by the user to disconnect the reference from the V_{REF}_2.5 pin. This pin should also be cleared to connect an external reference source to the V_{REF}_2.5 pin.
0	Internal 1.2 V reference output enable. Set by the user to connect the internal 1.2 V reference to the V_{REF}_1.2 pin. Cleared by the user to disconnect the reference from the V_{REF}_1.2 pin.

Table 37. PSMCON MMR Bit Designations (Address = 0xFFFF0440, Default Value = 0x08 or 0x00 (Dependent on Device Supply Level)

Bit	Name	Description
7:4	Reserved	Reserved bits. Clear to 0.
3	CMP	Comparator bit. This is a read-only bit that directly reflects the state of the comparator. Read 1 indicates the IOV_{DD} supply is above its selected trip point or the PSM is in power-down mode. Read 0 indicates the IOV_{DD} supply is below its selected trip point. This bit should be set before leaving the interrupt service routine.
2	TP	Trip point selection bit. 0 = 2.79 V 1 = 3.07 V
1	PSMEN	Power supply monitor enable bit. Set to 1 by the user to enable the power supply monitor circuit. Cleared to 0 by the user to disable the power supply monitor circuit.
0	PSMI	Power supply monitor interrupt bit. This bit is set high by the ADuC7122 if CMP is low, indicating low I/O supply. The PSMI bit can be used to interrupt the processor. When CMP returns high, the PSMI bit can be cleared by writing a 1 to this location. A write of 0 has no effect. There is no timeout delay. PSMI can be cleared immediately when CMP goes high.

RSTCFG Register

Name: RSTCFG

Address: 0xFFFF024C

Default value: 0x00

Access: Read/write

Table 62. RSTCFG MMR Bit Designations

Bit	Description
7 to 3	Reserved. Always set to 0.
2	This bit is set to 1 to configure the DAC outputs to retain their state after a watchdog or software reset. This bit is cleared for the DAC pins and registers to return to their default state.
1	Reserved. Always set to 0.
0	This bit is set to 1 to configure the GPIO pins to retain their state after a watchdog or software reset. This bit is cleared for the GPIO pins and registers to return to their default state.

RSTKEY1 Register

Name: RSTKEY1

Address: 0xFFFF0248

Default Value: N/A

Access Write

RSTKEY2 Register

Name: RSTKEY2

Address: 0xFFFF0250

Default Value: N/A

Access: Write

Table 63. RSTCFG Write Sequence

Name	Code
RSTKEY1	0x76
RSTCFG	User value
RSTKEY2	0xB1

Table 85. GPxPAR Register

Name	Address	Default Value	Access
GP0PAR	0xFFFF0D2C	0x20000000	R/W
GP1PAR	0xFFFF0D3C	0x00000000	R/W
GP2PAR	0xFFFF0D4C	0x00000000	R/W
GP3PAR	0xFFFF0D5C	0x00222222	R/W

GPxPAR programs the parameters for Port 0, Port 1, Port 2, and Port 3. Note that the GPxDAT MMR must always be written after changing the GPxPAR MMR.

Table 86. GPxPAR MMR Bit Designations

Bit	Description
31:29	Reserved
28	Pull-up disable Px.7 pin
27:25	Reserved
24	Pull-up disable Px.6 pin
23:21	Reserved
20	Pull-up disable Px.5 pin
19:17	Reserved
16	Pull-up disable Px.4 pin
15:13	Reserved
12	Pull-up disable Px.3 pin
11:9	Reserved
8	Pull-up disable Px.2 pin
7:5	Reserved
4	Pull-up disable Px.1 pin
3:1	Reserved
0	Pull-up disable Px.0 pin

Table 87. GPxDAT Register

Name	Address	Default Value	Access
GP0DAT	0xFFFF0D20	0x000000XX	R/W
GP1DAT	0xFFFF0D30	0x000000XX	R/W
GP2DAT	0xFFFF0D40	0x000000XX	R/W
GP3DAT	0xFFFF0D50	0x000000XX	R/W

GPxDAT is a Port x configuration and data register. It configures the direction of the GPIO pins of Port x, sets the output value for the pins configured as outputs, and receives and stores the input value of the pins configured as inputs.

Table 88. GPxDAT MMR Bit Designations

Bit	Description
31:24	Direction of the data. Set to 1 by the user to configure the GPIO pin as an output. Cleared to 0 by user to configure the GPIO pin as an input.
23:16	Port x data output.
15:8	Reflect the state of Port x pins at reset (read only).
7:0	Port x data input (read only).

Table 89. GPxSET Register

Name	Address	Default Value	Access
GP0SET	0xFFFF0D24	0x000000XX	W
GP1SET	0xFFFF0D34	0x000000XX	W
GP2SET	0xFFFF0D44	0x000000XX	W
GP3SET	0xFFFF0D54	0x000000XX	W

Table 90. GPxSET MMR Bit Designations

Bit	Description
31: 24	Reserved.
23:16	Data Port x set bit. Set to 1 by the user to set bit on Port x; also sets the corresponding bit in the GPxDAT MMR. Cleared to 0 by the user; does not affect the data output.
15: 0	Reserved.

GPxSET is a data set Port x register.

Table 91. GPxCLR Register

Name	Address	Default Value	Access
GP0CLR	0xFFFF0D28	0x000000XX	W
GP1CLR	0xFFFF0D38	0x000000XX	W
GP2CLR	0xFFFF0D48	0x000000XX	W
GP3CLR	0xFFFF0D58	0x000000XX	W

GPxCLR is a data clear Port x register.

Table 92. GPxCLR MMR Bit Designations

Bit	Description
31:24	Reserved.
23:16	Data Port x clear bit. Set to 1 by the user to clear bit on Port x; also clears the corresponding bit in the GPxDAT MMR. Cleared to 0 by the user; does not affect the data output.
15:0	Reserved.

Open-collector functionality is available on the following GPIO pins: P1.7, P1.6, P2.x, and P3.x. Open-collector functionality can be configured using GP1OCE[7:6], GP2OCE[7:0], and GP3OCE[7:0].

Table 93. GPxOCE MMR Bit Designations

Bit	Description
31:8	Reserved.
7	GPIO Px.7 open-collector enable Set to 1 by the user to enable open-collector Set to 0 by the user to disable open collector
6	GPIO Px.6 open-collector enable Set to 1 by the user to enable open-collector Set to 0 by the user to disable open-collector
5	GPIO Px.5 open-collector enable Set to 1 by the user to enable open-collector Set to 0 by the user to disable open-collector
4	GPIO Px.4 open-collector enable Set to 1 by the user to enable open-collector Set to 0 by the user to disable open-collector
3	GPIO Px.3 open-collector enable Set to 1 by the user to enable open-collector Set to 0 by the user to disable open-collector
2	GPIO Px.2 open-collector enable Set to 1 by the user to enable open-collector Set to 0 by the user to disable open-collector
1	GPIO Px.1 open-collector enable Set to 1 by the user to enable open-collector Set to 0 by the user to disable open-collector
0	GPIO Px.0 open-collector enable Set to 1 by the user to enable open-collector Set to 0 by the user to disable open-collector

UART SERIAL INTERFACE

The ADuC7122 features a 16450-compatible UART. The UART is a full-duplex, universal, asynchronous receiver/transmitter. A UART performs serial-to-parallel conversion on data characters received from a peripheral device, and parallel-to-serial conversion on data characters received from the ARM7TDMI. The UART features a fractional divider that facilitates high accuracy baud rate generation and a network addressable mode. The UART functionality is available on the P1.0 and P1.1 pins of the ADuC7122.

The serial communication adopts an asynchronous protocol that supports various word length, stop bits, and parity generation options selectable in the configuration register.

BAUD RATE GENERATION

The ADuC7122 features two methods of generating the UART baud rate: normal 450 UART baud rate generation and ADuC7122 fractional divider.

Normal 450 UART Baud Rate Generation

The baud rate is a divided version of the core clock using the value in COMDIV0 and COMDIV1 MMRs (16-bit value, DL). The standard baud rate generator formula is

$$Baud\ rate = \frac{41.78\ \text{MHz}}{16 \times 2 \times DL} \quad (1)$$

Table 94 lists common baud rate values.

Table 94. Baud Rate Using the Standard Baud Rate Generator

Baud Rate	DL	Actual Baud Rate	% Error
9600	0x88	9600	0%
19,200	0x44	19,200	0%
115,200	0x0B	118,691	3%

ADuC7122 Fractional Divider

The fractional divider combined with the normal baud rate generator allows the generating of a wider range of more accurate baud rates.

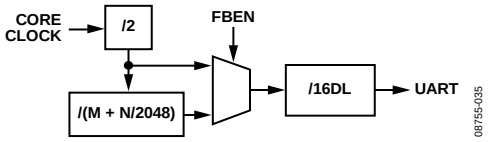

Figure 34. Baud Rate Generation Options

Calculation of the baud rate using fractional divider is as follows:

$$Baud\ Rate = \frac{41.78\ \text{MHz}}{16 \times DL \times 2 \times (M + \frac{N}{2048})} \quad (2)$$

$$M + \frac{N}{2048} = \frac{41.78\ \text{MHz}}{Baud\ Rate \times 16 \times DL \times 2}$$

For example, generation of 19,200 baud

$$M + \frac{N}{2048} = \frac{41.78\ \text{MHz}}{19{,}200 \times 16 \times 67 \times 2}$$

$$M + \frac{N}{2048} = 1.015$$

where:
$M = 1$.
$N = 0.015 \times 2048 = 30$.

$$Baud\ Rate = \frac{41.78\ \text{MHz}}{16 \times 67 \times 2 \times \left(1 + \frac{30}{2048}\right)}$$

where *Baud Rate* = 19,219 bps.

UART REGISTER DEFINITION

The UART interface consists of the following ten registers:

COMTX: 8-bit transmit register
COMRX: 8-bit receive register
COMDIV0: divisor latch (low byte)
COMDIV1: divisor latch (high byte)
COMCON0: line control register
COMCON1: line control register
COMSTA0: line status register
COMIEN0: interrupt enable register
COMIID0: interrupt identification register
COMDIV2: 16-bit fractional baud divide register

COMTX, COMRX, and COMDIV0 share the same address location. COMTX, COMRX, and COMIEN0 can be accessed when Bit 7 in the COMCON0 register is cleared. COMDIVx can be accessed when Bit 7 of COMCON0 is set

UART TX Register

Write to this 8-bit register to transmit data using the UART.

Name: COMTX

Address: 0xFFFF0800

Access: Write only

UART RX Register

This 8-bit register is read from to receive data transmitted using the UART.

Name: COMRX

Address: 0xFFFF0800

Default Value: 0x00

Access: Read only

UART Divisor Latch Register 0

This 8-bit register contains the least significant byte of the divisor latch that controls the baud rate at which the UART operates.

Name: COMDIV0

Address: 0xFFFF0800

Default Value: 0x00

Access: Read/write

UART Divisor Latch Register 1

This 8-bit register contains the most significant byte of the divisor latch that controls the baud rate at which the UART operates.

Name: COMDIV1

Address: 0xFFFF0804

Default Value: 0x00

Access: Read/write

UART Control Register 0

This 8-bit register controls the operation of the UART in conjunction with COMCON1.

Name: COMCON0

Address: 0xFFFF080C

Default Value: 0x00

Access: Read/write

Table 95. COMCON0 MMR Bit Designations

Bit	Name	Description
7	DLAB	Divisor latch access. Set by the user to enable access to COMDIV0 and COMDIV1 registers. Cleared by the user to disable access to COMDIV0 and COMDIV1 and enable access to COMRX, COMTX, and COMIEN0.
6	BRK	Set break. Set by the user to force TxD to 0. Cleared to operate in normal mode.
5	SP	Stick parity. Set by the user to force parity to defined values. 1 if EPS = 1 and PEN = 1. 0 if EPS = 0 and PEN = 1.
4	EPS	Even parity select bit. Set for even parity. Cleared for odd parity.
3	PEN	Parity enable bit. Set by the user to transmit and check the parity bit. Cleared by the user for no parity transmission or checking.
2	STOP	Stop bit. Set by the user to transmit 1.5 stop bits if the word length is 5 bits, or 2 stop bits if the word length is 6, 7, or 8 bits. The receiver checks the first stop bit only, regardless of the number of stop bits selected. Cleared by the user to generate one stop bit in the transmitted data.
1 to 0	WLS	Word length select. 00 = 5 bits. 01 = 6 bits. 10 = 7 bits. 11 = 8 bits.

UART Control Register 1

This 8-bit register controls the operation of the UART in conjunction with COMCON0.

Name: COMCON1

Address: 0xFFFF0810

Default Value: 0x00

Access: Read/write

Table 96. COMCON1 MMR Bit Designations

Bit	Name	Description
7:5		Reserved bits. Not used.
4	Loopback	Set by the user to enable loopback mode. In loopback mode, the TxD is forced high.
3:2		Reserved bits. Not used.
1	RTS	Request to send. Set by the user to force the RTS output to 0. Cleared by the user to force the RTS output to 1.
0	DTR	Data terminal ready. Set by the user to force the DTR output to 0. Cleared by the user to force the DTR output to 1.

I²C

The ADuC7122 incorporates two I²C peripherals that can be separately configured as a fully I²C-compatible I²C bus master device or as a fully I²C bus-compatible slave device. Because both peripherals are identical, only one is explained here.

The two pins used for data transfer, SDA and SCL, are configured in a wire-AND'ed format that allows arbitration in a multimaster system. These pins require external pull-up resistors. Typical pull-up values are between 4.7 kΩ and 10 kΩ.

The I²C bus peripheral address in the I²C bus system is programmed by the user. This ID can be modified any time a transfer is not in progress. The user can configure the interface to respond to four slave addresses.

The transfer sequence of an I²C system consists of a master device initiating a transfer by generating a start condition while the bus is idle. The master transmits the slave device address and the direction of the data transfer (read or write) during the initial address transfer. If the master does not lose arbitration and the slave acknowledges the last byte, the data transfer is initiated. This continues until the master issues a stop condition, and the bus becomes idle.

The I²C peripheral can only be configured as a master or slave at any given time. The same I²C channel cannot simultaneously support master and slave modes.

The I²C interface on the ADuC7122 includes the following features:

- Support for repeated start conditions. In master mode, the ADuC7122 can be programmed to generate a repeated start. In slave mode, the ADuC7122 recognizes repeated start conditions.
- In master and slave mode, the part recognizes both 7-bit and 10-bit bus addresses.
- In I²C master mode, the ADuC7122 supports continuous reads from a single slave up to 512 bytes in a single transfer sequence.
- Clock stretching can be enabled by other devices on the bus without causing any issues with the ADuC7122. However, the ADuC7122 cannot enable clock stretching.
- In slave mode, the ADuC7122 can be programmed to return a NACK (no acknowledge). This allows the validiation of checksum bytes at the end of I²C transfers.
- Bus arbitration in master mode is supported.
- Internal and external loopback modes are supported for I²C hardware testing. In loopback mode.
- The transmit and receive circuits in both master and slave mode contain 2-byte FIFOs. Status bits are available to the user to control these FIFOs.

Configuring External Pins for I²C Functionality

The I²C pins of the ADuC7122 device are P0.0 and P0.1 for I2C0, and P1.0 and P1.1 for I2C1.

P0.0 and P1.0 are the I²C clock signals, and P0.1 and P1.1 are the I²C data signals. For instance, to configure the I2C0 pins (SCL1, SDA1), Bit 0 and Bit 4 of the GP0CON register must be set to 1 to enable I²C mode. Alternatively, to configure the I2C1 pins (SCL2, SDA2), Bit 1 and Bit 5 of the GP1CON register must be set to 1 to enable I²C mode.

SERIAL CLOCK GENERATION

The I²C master in the system generates the serial clock for a transfer. The master channel can be configured to operate in fast mode (400 kHz) or standard mode (100 kHz).

The bit rate is defined in the I2CxDIV MMR as follows:

$$f_{SERIAL\ CLOCK} = \frac{f_{UCLK}}{(2 + DIVH) + (2 + DIVL)}$$

where:
f_{UCLK} is the clock before the clock divider.
DIVH is the high period of the clock.
DIVL is the low period of the clock.

Thus, for 100 kHz operation,

DIVH = *DIVL* = 0xCF

and for 400 kHz,

DIVH = 0x28, DIVL = 0x3C

The I2CxDIV register corresponds to DIVH:DIVL.

I²C BUS ADDRESSES

Slave Mode

In slave mode, the I2CxID0, I2CxID1, I2CxID2, and I2xCID3 registers contain the device IDs. The device compares the four I2CxIDx registers to the address byte received from the bus Master. To be correctly addressed, the seven MSBs of either ID register must be identical to that of the seven MSBs of the first received address byte. The LSB of the ID registers (the transfer direction bit) is ignored in the process of address recognition.

The ADuC7122 also supports 10-bit addressing mode. When Bit 1 of I2CxSCTL (ADR10EN bit) is set to 1, then one 10-bit address is supported in slave mode and is stored in the I2CxID0 and I2CxID1 registers. The 10-bit address is derived as follows:

I2CxID0[0] is the read/write bit and is not part of the I²C address.

I2CxID0[7:1] = Address Bits[6:0].

I2CxID1[2:0] = Address Bits[9:7].

I2CxID1[7:3] must be set to 11110b.

I²C Master Receive Register

Name: I2C0MRX, I2C1MRX

Address: 0xFFFF0888, 0xFFFF0908

Default Value: 0x00, 0x00

Access: Read only

Function: This 8-bit MMR is the I²C master receive register.

I²C Master Transmit Register

Name: I2C0MTX, I2C1MTX

Address: 0xFFFF088C, 0xFFFF090C

Default Value: 0x00, 0x00

Access: Read/write

Function: This 8-bit MMR is the I²C master transmit register.

I²C Master Read Count Register

Name: I2C0MCNT0, I2C1MCNT0

Address: 0xFFFF0890, 0xFFFF0910

Default Value: 0x0000, 0x0000

Access: Read/write

Function: This 16-bit MMR holds the required number of bytes when the master begins a read sequence from a slave device.

I²C Master Current Read Count Register

Name: I2C0MCNT1, I2C1MCNT1

Address: 0xFFFF0894, 0xFFFF0914

Default Value: 0x00, 0x00

Access: Read

Function: This 8-bit MMR holds the number of bytes received so far during a read sequence with a slave device.

Table 103. I2CxMCNT0 MMR Bit Descriptions (Address = 0xFFFF0890, 0xFFFF0910, Default Value = 0x0000)

Bit	Name	Description
15:9		Reserved.
8	I2CRECNT	Set this bit if greater than 256 bytes are required from the slave. Clear this bit when reading 256 bytes or less.
7:0	I2CRCNT	These eight bits hold the number of bytes required during a slave read sequence, minus 1. If only a single byte is required, these bits should be set to 0.

PROGRAMMABLE LOGIC ARRAY (PLA)

The ADuC7122 integrates a fully programmable logic array (PLA) that consists of two, independent but interconnected PLA blocks. Each block consists of eight PLA elements, giving each part a total of 16 PLA elements.

Each PLA element contains a two-input look-up table that can be configured to generate any logic output function based on two inputs and a flip-flop. This is represented in Figure 35.

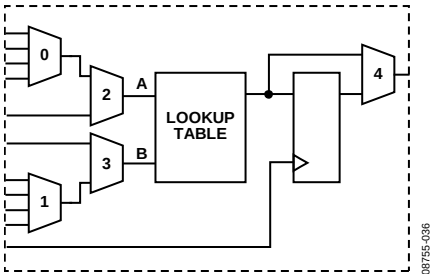

Figure 35. PLA Element

In total, 32 GPIO pins are available on each ADuC7122 for the PLA. These include 16 input pins and 16 output pins that need to be configured in the GPxCON register as PLA pins before using the PLA. Note that the comparator output is also included as one of the 16 input pins.

The PLA is configured via a set of user MMRs. The output(s) of the PLA can be routed to the internal interrupt system, to the $\overline{\text{CONVST}}$ signal of the ADC, to an MMR, or to any of the 16 PLA output pins.

The two blocks can be interconnected as follows:

- Output of Element 15 (Block 1) can be fed back to Input 0 of Mux 0 of Element 0 (Block 0)
- Output of Element 7 (Block 0) can be fed back to the Input 0 of Mux 0 of Element 8 (Block 1)

Table 113. Element Input/Output

PLA Block 0			PLA Block 1		
Element	**Input**	**Output**	**Element**	**Input**	**Output**
0	P2.7	P3.0	8	P1.4	P3.4
1	P2.2	P3.1	9	P1.5	P3.5
2	P0.6	P3.2	10	P0.5	P3.6
3	P0.7	P3.3	11	P0.4	P3.7
4	P0.1	P1.7	12	P2.1	P0.3
5	P0.0	P1.6	13	P2.0	P0.2
6	P1.1	P2.5	14	P2.3	P1.3
7	P1.0	P2.4	15	P2.6	P1.2

PLA MMRs Interface

The PLA peripheral interface consists of the 21 MMRs described in Table 114 to Table 128.

Table 114. PLAELMx Registers

Name	Address	Default Value	Access
PLAELM0	0xFFFF0B00	0x0000	R/W
PLAELM1	0xFFFF0B04	0x0000	R/W
PLAELM2	0xFFFF0B08	0x0000	R/W
PLAELM3	0xFFFF0B0C	0x0000	R/W
PLAELM4	0xFFFF0B10	0x0000	R/W
PLAELM5	0xFFFF0B14	0x0000	R/W
PLAELM6	0xFFFF0B18	0x0000	R/W
PLAELM7	0xFFFF0B1C	0x0000	R/W
PLAELM8	0xFFFF0B20	0x0000	R/W
PLAELM9	0xFFFF0B24	0x0000	R/W
PLAELM10	0xFFFF0B28	0x0000	R/W
PLAELM11	0xFFFF0B2C	0x0000	R/W
PLAELM12	0xFFFF0B30	0x0000	R/W
PLAELM13	0xFFFF0B34	0x0000	R/W
PLAELM14	0xFFFF0B38	0x0000	R/W
PLAELM15	0xFFFF0B3C	0x0000	R/W

PLAELMx are Element 0 to Element 15 control registers. They configure the input and output mux of each element, select the function in the look-up table, and bypass/use the flip-flop. See Table 115 and Table 118.

IRQ

The IRQ is the exception signal to enter the IRQ mode of the processor. It services general-purpose interrupt handling of internal and external events.

All 32 bits are logically OR'ed to create a single IRQ signal to the ARM7TDMI core. The four 32-bit registers dedicated to IRQ are IRQSIG, IRQEN, IRQCLR, and IRQSTA.

IRQSIG

IRQSIG reflects the status of the different IRQ sources. If a peripheral generates an IRQ signal, the corresponding bit in the IRQSIG is set; otherwise, it is cleared. The IRQSIG bits clear when the interrupt in the particular peripheral is cleared. All IRQ sources can be masked in the IRQEN MMR. IRQSIG is read only.

IRQSIG Register

Name: IRQSIG

Address: 0xFFFF0004

Default Value: 0x00000000

Access: Read only

IRQEN

IRQEN provides the value of the current enable mask. When a bit is set to 1, the corresponding source request is enabled to create an IRQ exception. When a bit is set to 0, the corresponding source request is disabled or masked, which does not create an IRQ exception. The IRQEN register cannot be used to disable an interrupt.

IRQEN Register

Name: IRQEN

Address: 0xFFFF0008

Default Value: 0x00000000

Access: Read/write

IRQCLR

IRQCLR is a write-only register that allows the IRQEN register to clear to mask an interrupt source. Each bit that is set to 1 clears the corresponding bit in the IRQEN register without affecting the remaining bits. The pair of registers, IRQEN and IRQCLR, allows independent manipulation of the enable mask without requiring an atomic read-modify-write.

IRQCLR Register

Name: IRQCLR

Address: 0xFFFF000C

Default Value: 0x00000000

Access: Write only

IRQSTA

IRQSTA is a read-only register that provides the current enabled IRQ source status (effectively a logic AND of the IRQSIG and IRQEN bits). When set to 1, that source generates an active IRQ request to the ARM7TDMI core. There is no priority encoder or interrupt vector generation. This function is implemented in software in a common interrupt handler routine.

IRQSTA Register

Name: IRQSTA

Address: 0xFFFF0000

Default Value: 0x00000000

Access: Read only

FAST INTERRUPT REQUEST (FIQ)

The fast interrupt request (FIQ) is the exception signal to enter the FIQ mode of the processor. It is provided to service data transfer or communication channel tasks with low latency. The FIQ interface is identical to the IRQ interface and provides the second level interrupt (highest priority). Four 32-bit registers are dedicated to FIQ: FIQSIG, FIQEN, FIQCLR, and FIQSTA.

Bit 31 to Bit 1 of FIQSTA are logically OR'ed to create the FIQ signal to the core and to Bit 0 of both the FIQ and IRQ registers (FIQ source).

The logic for FIQEN and FIQCLR does not allow an interrupt source to be enabled in both IRQ and FIQ masks. A bit set to 1 in FIQEN clears, as a side effect, the same bit in IRQEN. Likewise, a bit set to 1 in IRQEN clears, as a side effect, the same bit in FIQEN. An interrupt source can be disabled in both IRQEN and FIQEN masks.

FIQSIG

FIQSIG reflects the status of the different FIQ sources. If a peripheral generates an FIQ signal, the corresponding bit in the FIQSIG is set; otherwise, it is cleared. The FIQSIG bits are cleared when the interrupt in the particular peripheral is cleared. All FIQ sources can be masked in the FIQEN MMR. FIQSIG is read only.

FIQSIG Register

Name: FIQSIG

Address: 0xFFFF0104

Default Value: 0x00000000

Access: Read only

Table 133. IRQP1 MMR Bit Designations

Bit	Name	Description
31	Reserved	Reserved bit.
30:28	I2C0MPI	A priority level of 0 to 7 can be set for the I2C0 master.
27	Reserved	Reserved bit.
26:24	SPIPI	A priority level of 0 to 7 can be set for the SPI.
23	Reserved	Reserved bit.
22:20	UARTPI	A priority level of 0 to 7 can be set for the UART.
19	Reserved	Reserved bit.
18:16	ADCPI	A priority level of 0 to 7 can be set for the ADC interrupt source.
15	Reserved	Reserved bit.
14:12	Flash1PI	A priority level of 0 to 7 can be set for the Flash Block 1 controller interrupt source.
11	Reserved	Reserved bit.
10:8	Flash0PI	A priority level of 0 to 7 can be set for the Flash Block 0 controller interrupt source.
7:3	Reserved	Reserved bits.
2:0	PSMPI	A priority level of 0 to 7 can be set for the Power supply monitor interrupt source.

IRQP2 Register

Name: IRQP2

Address: 0xFFFF0028

Default Value: 0x00000000

Access: Read and write

Table 134. IRQP2 MMR Bit Designations

Bit	Name	Description
31	Reserved	Reserved bit.
30:28	PWMPI	A priority level of 0 to 7 can be set for PWM.
27	Reserved	Reserved bit.
26:24	IRQ3PI	A priority level of 0 to 7 can be set for IRQ3.
23	Reserved	Reserved bit.
22:20	IRQ2PI	A priority level of 0 to 7 can be set for IRQ2.
19	Reserved	Reserved bit.
18:16	IRQ1PI	A priority level of 0 to 7 can be set for IRQ1.
15	Reserved	Reserved bit.
14:12	IRQ0PI	A priority level of 0 to 7 can be set for IRQ0.
11	Reserved	Reserved bit.
10:8	I2C1SPI	A priority level of 0 to 7 can be set for I2C1 slave.
7	Reserved	Reserved bit.
6:4	I2C1MPI	A priority level of 0 to 7 can be set for I2C1 master.
3	Reserved	Reserved bit.
2:0	I2C0SPI	A priority level of 0 to 7 can be set for I2C0 slave.

IRQP3 Register

Name: IRQP3

Address: 0xFFFF002C

Default Value: 0x00000000

Access: Read and write

Table 135. IRQP3 MMR Bit Designations

Bit	Name	Description
31:15	Reserved	Reserved bit.
14:12	PLA1PI	A priority level of 0 to 7 can be set for PLA0.
11	Reserved	Reserved bit.
10:8	PLA0PI	A priority level of 0 to 7 can be set for PLA0.
7	Reserved	Reserved bit.
6:4	IRQ5PI	A priority level of 0 to 7 can be set for IRQ5.
3	Reserved	Reserved bit.
2:0	IRQ4PI	A priority level of 0 to 7 can be set for IRQ4.

IRQCONN Register

The IRQCONN register is the IRQ and FIQ control register. It contains two active bits. The first enables nesting and prioritization of IRQ interrupts and the other enables nesting and prioritization of FIQ interrupts.

If these bits are cleared, then FIQs and IRQs can still be used, but it is not possible to nest IRQs or FIQs. Neither is it possible to set an interrupt source priority level. In this default state, an FIQ does have a higher priority than an IRQ.

Name: IRQCONN

Address: 0xFFFF0030

Default Value: 0x00000000

Access: Read and write

Table 136. IRQCONN MMR Bit Designations

Bit	Name	Description
31:2	Reserved	These bits are reserved and should not be written to.
1	ENFIQN	Setting this bit to 1 enables nesting of FIQ interrupts. Clearing this bit means no nesting or prioritization of FIQs is allowed.
0	ENIRQN	Setting this bit to 1 enables nesting of IRQ interrupts. Clearing this bit means no nesting or prioritization of IRQs is allowed.

TIMER1—GENERAL-PURPOSE TIMER

Timer1 is a 32-bit general-purpose timer, count down or count up, with a programmable prescaler. The prescaler source can be from the 32 kHz internal oscillator, the 32 kHz external crystal, the core clock, or from the undivided PLL clock output. This source can be scaled by a factor of 1, 16, 256, or 32,768. This gives a minimum resolution of 42 ns when operating at CD = 0, the core is operating at 41.78 MHz, and with a prescaler of 1.

The counter can be formatted as a standard 32-bit value or as hours:minutes:seconds:hundredths.

Timer1 has a capture register (T1CAP) that can be triggered by a selected IRQ's source initial assertion. When triggered, the current timer value is copied to T1CAP, and the timer keeps running. This feature can be used to determine the assertion of an event with increased accuracy.

The Timer1 interface consists of five MMRs, as shown in Table 151.

Table 151. Timer1 Interface Registers

Register	Description
T1LD	32-bit register. Holds 32-bit unsigned integers. This register is read only.
T1VAL	32-bit register. Holds 32-bit unsigned integers.
T1CAP	32-bit register. Holds 32-bit unsigned integers. This register is read only.
T1CLRI	8-bit register. Writing any value to this register clears the Timer1 interrupt.
T1CON	Configuration MMR.

Note that if the part is in a low power mode, and Timer1 is clocked from the GPIO or low power oscillator source, then Timer1 continues to operate.

Timer1 reloads the value from T1LD either when Timer1 overflows or immediately when T1ICLR is written.

Table 152. Timer1 Load Registers

Name	Address	Default Value	Access
T1LD	0xFFFF0320	0x00000	R/W

T1LD is a 32-bit register that holds the 32-bit value that is loaded into the counter.

Table 153. Timer1 Clear Register

Name	Address	Default Value	Access
T1CLRI	0xFFFF032C	0x00	W

This 8-bit, write-only MMR is written (with any value) by user code to refresh (reload) Timer1.

Table 154. Timer1 Value Register

Name	Address	Default Value	Access
T1VAL	0xFFFF0324	0x0000	R

T1VAL is a 32-bit register that holds the current value of Timer1.

Table 155. Timer1 Capture Register

Name	Address	Default Value	Access
T1CAP	0xFFFF0330	0x00	R

This is a 32-bit register that holds the 32-bit value captured by an enabled IRQ event.

Table 156. Timer1 Control Register.

Name	Address	Default Value	Access
T1CON	0xFFFF0328	0x0000	R/W

This 32-bit MMR configures the mode of operation of Timer1.

Table 169. T3CON MMR Bit Designations

Bit	Value	Description
16:9		These bits are reserved and should be written as 0s by user code.
8		Count up/down enable.
	1	Set by user code to configure Timer3 to count up.
	0	Cleared by user code to configure Timer3 to count down.
7		Timer3 enable.
	1	Set by user code to enable Timer3.
	0	Cleared by user code to disable Timer3.
6		Timer3 operating mode.
	1	Set by user code to configure Timer3 to operate in periodic mode.
	0	Cleared by user to configure Timer3 to operate in free-running mode.
5		Watchdog timer mode enable.
	1	Set by user code to enable watchdog mode.
	0	Cleared by user code to disable watchdog mode.
4		Secure clear bit.
	1	Set by the user to use the secure clear option.
	0	Cleared by the user to disable the secure clear option by default.
3:2		Timer3 clock (32.768 kHz) prescaler.
	00	Source clock/1 (default).
	01	Reserved.
	10	Reserved.
	11	Reserved.
1		Watchdog timer IRQ enable.
	1	Set by the user code to produce an IRQ instead of a reset when the watchdog reaches 0.
	0	Cleared by the user code to disable the IRQ option.
0		PD_OFF.
	1	Set by user code to stop Timer3 when the peripherals are powered down via Bits[6:4] in the POWCON MMR.
	0	Cleared by user code to enable Timer3 when the peripherals are powered down via Bits[6:4] in the POWCON MMR.

Table 175. T4CON MMR Bit Designations

Bit	Value	Description
31:18		Reserved. Set by user to 0.
17		Event select bit.
	1	Set by the user to enable time capture of an event.
	0	Cleared by the user to disable time capture of an event.
16:12		Event select range, 0 to 31. The events are as described in the Timers section.
11:9		Clock select.
	000	32.768 kHz oscillator.
	001	Core clock.
	010	UCLK.
	011	UCLK.
8		Count up.
	1	Set by the user for Timer4 to count up.
	0	Cleared by the user for Timer4 to count down (default).
7		Timer4 enable bit.
	1	Set by the user to enable Timer4.
	0	Cleared by the user to disable Timer4 (default).
6		Timer4 mode.
	1	Set by the user to operate in periodic mode.
	0	Cleared by the user to operate in free-running mode (default).
5:4		Format.
	00	Binary (default).
	01	Reserved.
	10	Hr:min:sec:hundredths: 23 hours to 0 hours.
	11	Hr:min:sec:hundredths: 255 hours to 0 hours.
3:0		Prescaler.
	0000	Source clock/1 (default).
	0100	Source clock/16.
	1000	Source clock/256.
	1111	Source clock/32,768.

OUTLINE DIMENSIONS

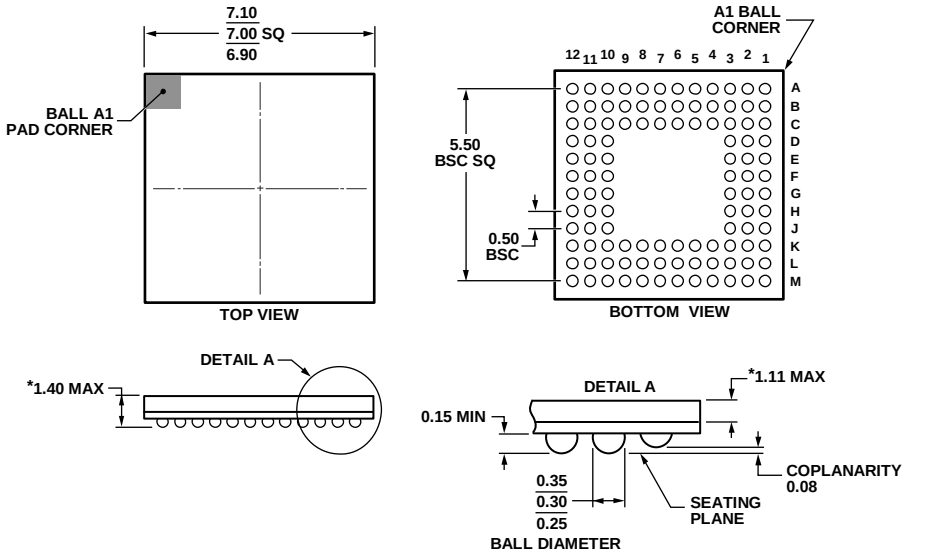

Figure 46. 108-Ball Chip Scale Package Ball Grid Array [CSP_BGA]
(BC-108-4)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
ADuC7122BBCZ	−10°C to +95°C	108-Ball Chip Scale Package Ball Grid Array [CSP_BGA]	BC-108-4
ADuC7122BBCZ-RL	−10°C to +95°C	108-Ball Chip Scale Package Ball Grid Array [CSP_BGA], 13″ Tape and Reel	BC-108-4
EVAL-ADUC7122QSPZ		ADuC7122 Quickstart Plus Development System	

[1] Z = RoHS Compliant Part.

I²C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).