Welcome to E-XFL.COM

Embedded - Microcontrollers - Application Specific: Tailored Solutions for Precision and Performance

Embedded - Microcontrollers - Application Specific represents a category of microcontrollers designed with unique features and capabilities tailored to specific application needs. Unlike general-purpose microcontrollers, application-specific microcontrollers are optimized for particular tasks, offering enhanced performance, efficiency, and functionality to meet the demands of specialized applications.

What Are Embedded - Microcontrollers - Application Specific?

Application-specific microcontrollers are engineered to

Details	
Product Status	Active
Applications	Power Line Communications
Core Processor	External
Program Memory Type	-
Controller Series	-
RAM Size	-
Interface	SPI
Number of I/O	-
Voltage - Supply	3V ~ 3.6V
Operating Temperature	-40°C ~ 85°C
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	80-LQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atpl250a-aku-r

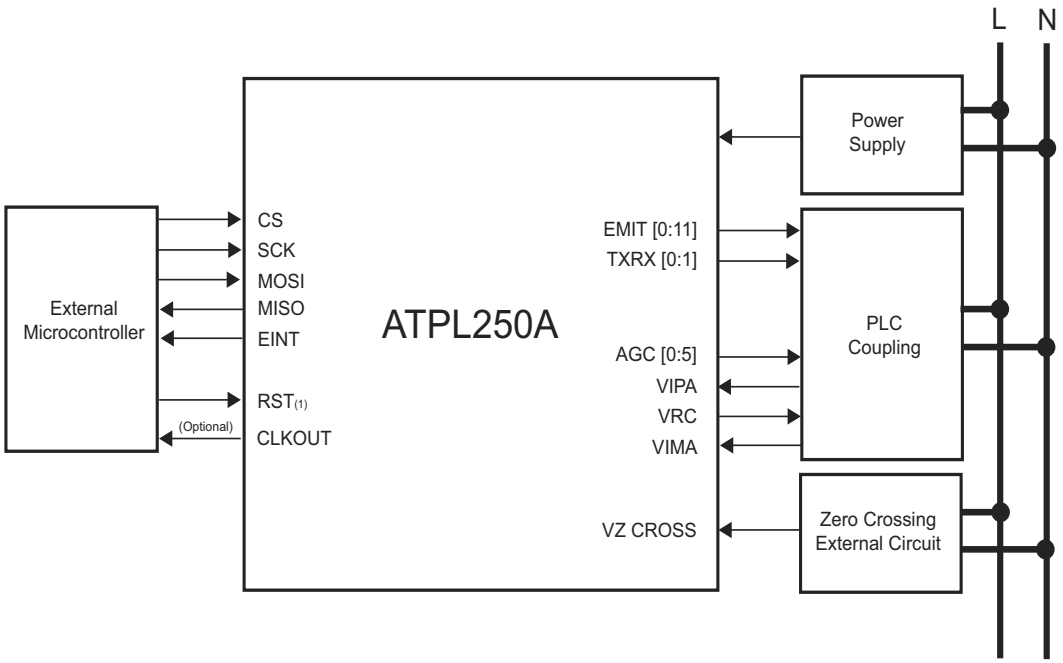
1. Features

- G3-PLC modem
  - Implements G3 CENELEC-A, FCC and ARIB profiles (ITU-T G.9903, June ´14)
  - Power Line Carrier Modem for 50 Hz and 60 Hz mains
  - G3-PLC coherent and differential modulation schemes available
- Automatic Gain Control and continuous amplitude tracking in signal reception
- 1 SPI peripheral (slave) to external MCU
- Zero cross detection
- Embedded PLC Analog Front End (AFE), requires only external discrete high efficient Class D Line Driver for signal injection
- TA range -40ºC to +85ºC
- Package
  - 80-lead LQFP

1.1 ATPL250A Application Block Diagram

ATPL250A has been conceived to be easily managed by an external microcontroller through a 5-line interface. This interface is comprised of a 4-line standard Serial Peripheral Interface (SPI) and an additional line used as interrupt from the ATPL250A to the external microcontroller. The external microcontroller can fully manage and control the ATPL250A (Phy layer, MAC coprocessing, etc.) by accessing the internal peripheral registers.

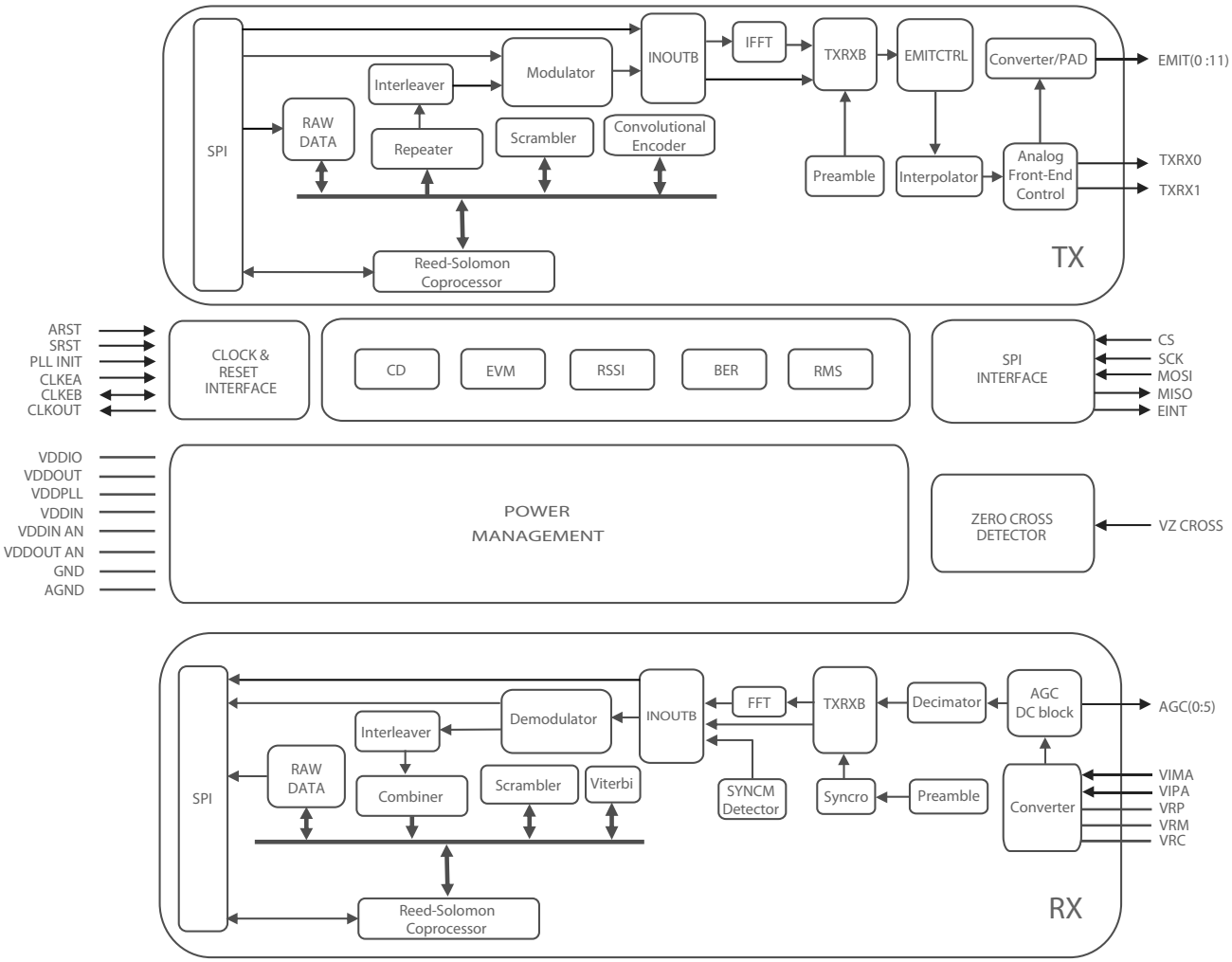
Figure 1-1. ATPL250A application example



Note: 1. There are several RST signals (ARST, SRST and PLL INIT), for more details see Section 3. ”Signal Description”.

2. Block Diagram

Figure 2-1. ATPL250A Functional Block Diagram



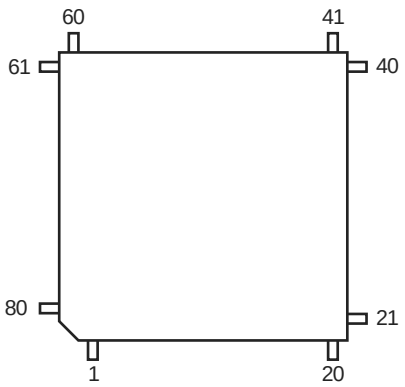
4. Package and Pinout

4.1 80-Lead LQFP Package Outline

The 80-lead LQFP package has a 0.5 mm pitch and respects Green standards.

Figure 4-1 shows the orientation of the 80-lead LQFP package. Refer to the section “Mechanical Characteristics” for the 80-lead LQFP package mechanical drawing.

Figure 4-1. Orientation of the 80-Lead LQFP Package



4.2 80-Lead LQFP Pinout

Table 4-1. 80 - Lead LQFP Pinout

1	NC	21	VDDIO	41	GND	61	GND
2	NC	22	NC	42	EMIT8	62	AGND
3	NC	23	CLKOUT	43	EMIT9	63	VDDOUT AN
4	ARST	24	CS	44	EMIT10	64	VIMA
5	PLL INIT	25	SCK	45	EMIT11	65	VIPA
6	GND	26	MOSI	46	VDDIO	66	VDDOUT AN
7	CLKEA	27	MISO	47	GND	67	AGND
8	GND	28	VDDIO	48	VDDOUT	68	VRP
9	CLKEB	29	GND	49	TXRX0	69	VRM
10	VDDIO	30	EMIT0	50	TXRX1	70	VRC
11	GND	31	EMIT1	51	GND	71	VDDIN AN
12	VDDPLL	32	EMIT2	52	AGC2	72	AGND
13	GND	33	EMIT3	53	AGC5	73	AGND
14	VDDIN	34	VDDIO	54	AGC1	74	VDDIN AN
15	VDDIN	35	GND	55	AGC4	75	GND
16	GND	36	EMIT4	56	AGC0	76	VDDIO
17	VDDOUT	37	EMIT5	57	AGC3	77	VZ CROSS
18	GND	38	EMIT6	58	VDDIO	78	NC
19	NC	39	EMIT7	59	GND	79	NC
20	SRST	40	VDDIO	60	EINT	80	NC

5.1.2 Filtering Stage

The filtering stage is composed by band-pass filters which have been designed to achieve high performance in field deployments complying at the same time with the proper normative and standards.

The in-band flat response filtering stage does not distort the injected signal, reduces spurious emission to the limits set by the corresponding regulation and blocks potential interferences from other transmission channels.

The Filtering stage has three aims:

- Band-pass filtering of high frequency components of the square waveform generated by the Transmission Stage.
- Adapt Input/Output impedances for optimal reception/transmission. This is controlled by TXRX signal.
- In some cases, Band-pass filtering for received signals.

When the system is intended to be connected to a physical channel with high voltage or which is not electrically referenced to the same point then the filtering stage must be always followed by a coupling stage.

5.1.3 Coupling Stage

The coupling stage blocks the DC component of the line to/from which the signal is injected/received (i.e.: 50/60 Hz of the mains). This is carried out by a high voltage capacitor.

Coupling stage could also electrically isolate the coupling circuitry from the external world by means of a 1:1 transformer.

5.1.4 Reception Stage

The reception stage adapts the received analog signal to be properly captured by the ATPL250A internal reception chain. Reception circuit is independent of the PLC channel which is being used. It basically consists of:

- Anti aliasing filter (RC Filter)
- Automatic Gain Control (AGC) circuit
- Driver of the internal ADC

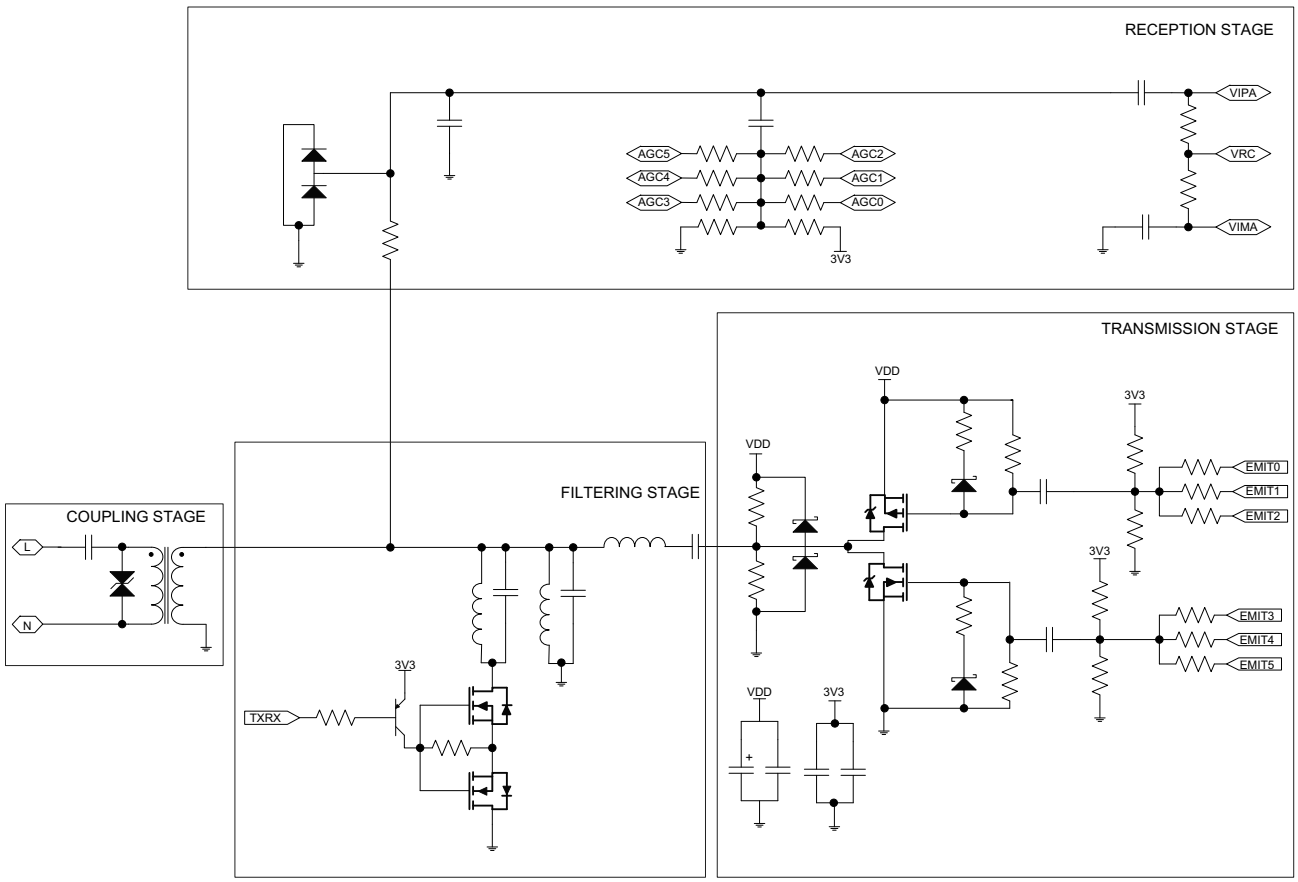
The AGC circuit avoids distortion on the received signal that may arise when the input signal is high enough to polarize the protective diodes in direct region.

The driver to the internal ADC comprises a couple of resistors and a couple of capacitors. This driver provides a DC component and adapts the received signal to be properly converted by the internal reception chain.

5.1.5 Generic PLC Coupling

Please consider that this is a generic PLC Coupling design for a particular application please refer to Atmel doc43052 “PLC Coupling Reference Designs”.

Figure 5-2. PLC Coupling block diagram detailed



5.2 ATPLCOUP reference designs

Atmel provides PLC coupling reference designs for different applications and frequency bands up to 500 kHz. Please refer to Atmel doc43052 “PLC Coupling Reference Designs” for a detailed description.

5.3 Zero-crossing detector

5.3.1 Overview

Zero Crossing Detector block works predicting future zero crossing in function of the past zero crossings. To achieve this, the system embeds a configurable Input Signal Management (ISM) block and a PLL, both of which manage Zero Crossing Detector Input Signal to calculate Zero Crossing Output Flag. The zero-cross detection of waves of 50 Hz and 60 Hz with ±10% of error is supported.

The PLL block interprets its input signal such a way that it indicates a zero cross in the middle of a positive pulse. It is important to note that depending on the external circuit which implements the Zero Crossing Detector Input Signal this interpretation is not always correct. So for these cases it is required to transform the Input Signal in a signal where the middle of a positive pulse corresponds to a truly zero cross. This transformation is implemented through the Input Signal Management (ISM) configured by MODE_INV and MODE_REP fields in ZC_CONFIG register.

Zero Crossing Detector Input Signal (VZ CROSS) must fulfil some requirements. The first requirement is that VZ CROSS signal must be a pulse train which its duty cycle must be >60% or <40% (polarity is configurable). In addition, if we have to detect Ascent or Descent zero-crossing, Zero Crossing Detector Input Signal period must be equal than period of the wave we need to obtain zero-crossing. Ascent and Descent Zero Crossing Detection are configured by setting MODE_MUX and MODE_ASC fields in ZC_CONFIG register.

Figure 5-3. Typical circuit, using a bidirectional optocoupler and a Schmitt trigger

The input signal “VZ CROSS”(wider line) generated by this circuit for Zero Cross Detection of the wave “L”-“N” (finer line) is plotted in next figure. The digital signal at output of Input Signal Management (ISM) is plotted in Figure 5-4.

Figure 5-4. Digital signal (dashed line) at output of Input Signal Management (ISM) internal block

6. Electrical characteristics

6.1 Absolute Maximum Ratings

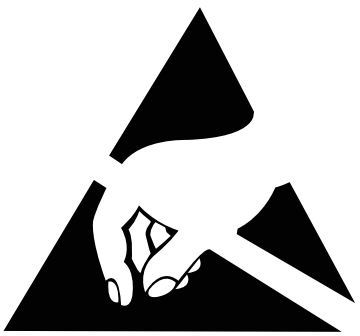
Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions given in the Recommended Operating Conditions section. Exposure to the Absolute Maximum Conditions for extended periods may affect device reliability.

Table 6-1. Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply Voltage	VDDIO	-0.5 to 4.0	V
Input Voltage	VI	-0.5 to VDDIO +0.5 (≤ 4.0V)	
Output Voltage	VO	-0.5 to VDDIO +0.5 (<4.0V)	
Storage Temperature	T_{ST}	-55 to 125	ºC
Junction Temperature	T_J	-40 to 125	
Output Current(1)	IO	±10(2)	mA

Notes: 1. DC current that continuously flows for 10 ms or more, or average DC current.
2. Applies to all the pins except EMIT pins. EMIT pins should be only used according to circuit configurations recommended by Atmel.

ATTENTION observe EDS precautions



Precautions for handling electrostatic sensitive devices should be taken into account to avoid malfunction. Charged devices and circuit boards can discharge without detection.

6.2 Recommended Operating Conditions

Table 6-2. Recommended Operating Conditions

Parameter	Symbol	Rating			Unit
		Min	Typ	Max	
Supply Voltage	VDDIO	3.00	3.30	3.60	V
	VDDIN AN	3.00	3.30	3.60	
	VDDIN	3.00	3.30	3.60	
	VDDPLL	1.08	1.20	1.32	
Junction Temperature	T_J	-40	25	125	ºC
Ambient Temperature	T_A	-40	-	85	

Table 6-3. Thermal Data

Parameter	Symbol	Conditions		LQFP80	Unit
		PCB Layers	Air Speed		
Thermal resistance junction-to-ambient steady state	$R_{Theta-ja}$	2	0 m/s	64	ºC/W
			1 m/s	56	
			3 m/s	48	
		4	0 m/s	43	
			1 m/s	40	
			3 m/s	36	

Theta-ja is calculated based on a standard JEDEC defined environment and is not reliable indicator of a device's thermal performance in a non-JEDEC environment. The customer should always perform their own calculations/simulations to ensure that their system's thermal performance is sufficient.

6.3 Electrical Pinout

Table 6-4. 80 - Lead LQFP Electrical Pinout

Pin No	Pin Name	I/O	I(mA)	Res	HY	Pin No	Pin Name	I/O	I(mA)	Res	HY
1	NC	-	-	-	-	41	GND	P	-	-	-
2	NC	-	-	-	-	42	EMIT8	OT	± 16	-	-
3	NC	-	-	-	-	43	EMIT9	OT	± 16	-	-
4	ARST	I	-	PU	Y	44	EMIT10	OT	± 16	-	-
5	PLL INIT	I	-	PU	Y	45	EMIT11	OT	± 16	-	-
6	GND	P	-	-	-	46	VDDIO	P	-	-	-
7	CLKEA	I	-	-	-	47	GND	P	-	-	-
8	GND	P	-	-	-	48	VDDOUT	P	-	-	-
9	CLKEB	I/O	-	-	-	49	TXRX0	O	± 8	-	-
10	VDDIO	P	-	-	-	50	TXRX1	O	± 8	-	-
11	GND	P	-	-	-	51	GND	P	-	-	-
12	VDDPLL	P	-	-	-	52	AGC2	OT	± 16	-	Y
13	GND	P	-	-	-	53	AGC5	OT	± 16	-	Y
14	VDDIN	P	-	-	-	54	AGC1	OT	± 6	-	Y
15	VDDIN	P	-	-	-	55	AGC4	OT	± 6	-	Y
16	GND	P	-	-	-	56	AGC0	OT	± 4	-	Y
17	VDDOUT	P	-	-	-	57	AGC3	OT	± 4	-	Y
18	GND	P	-	-	-	58	VDDIO	P	-	-	-
19	NC	-	-	-	-	59	GND	P	-	-	-
20	SRST	I	-	PU	Y	60	EINT	O	± 4	-	-
21	VDDIO	P	-	-	-	61	GND	P	-	-	-
22	NC	-	-	-	-	62	AGND	P	-	-	-
23	CLKOUT	O	± 8	-	-	63	VDDOUT AN	P	-	-	-
24	CS	I	-	PU	Y	64	VIMA	I	-	-	-
25	SCK	I	-	PU	Y	65	VIPA	I	-	-	-
26	MOSI	I	-	PU	Y	66	VDDOUT AN	P	-	-	-
27	MISO	O	± 6	-	-	67	AGND	P	-	-	-
28	VDDIO	P	-	-	-	68	VRP	O	-	-	-
29	GND	P	-	-	-	69	VRM	O	-	-	-
30	EMIT0	OT	± 16	-	-	70	VRC	O	-	-	-
31	EMIT1	OT	± 16	-	-	71	VDDIN AN	P	-	-	-
32	EMIT2	OT	± 16	-	-	72	AGND	P	-	-	-
33	EMIT3	OT	± 16	-	-	73	AGND	P	-	-	-
34	VDDIO	P	-	-	-	74	VDDIN AN	P	-	-	-
35	GND	P	-	-	-	75	GND	P	-	-	-
36	EMIT4	OT	± 16	-	-	76	VDDIO	P	-	-	-
37	EMIT5	OT	± 16	-	-	77	VZ CROSS	I	-	PD	Y
38	EMIT6	OT	± 16	-	-	78	NC	-	-	-	-
39	EMIT7	OT	± 16	-	-	79	NC	-	-	-	-
40	VDDIO	P	-	-	-	80	NC	-	-	-	-

I/O = pin direction: I = input, O = output, T = tri-state, P = power

I(mA) = nominal current: + = source, - = sink, X = fixed by external resistor. See “V-I curves”

Res = pin pull up/pull down resistor: PU = pull up, PD = pull down (15 - 70 kΩ, typical 33 kΩ)

HY = Input Hysteresis: Y = yes

Apply to pins CLKOUT, TXRX0, TXRX1

Condition:	MIN	Process = Slow	T_J = 125°C	VDDIO = 3.0V
	TYP	Process = Typical	T_J = 25°C	VDDIO = 3.3V
	MAX	Process = Fast	T_J = -40°C	VDDIO = 3.6V

Figure 6-3. V-I curves for pins CLKOUT, TXRX0, TXRX1

Apply to pins EMIT [0:11], AGC2, AGC5

Condition:	MIN	Process = Slow	T_J = 125°C	VDDIO = 3.0V
	TYP	Process = Typical	T_J = 25°C	VDDIO = 3.3V
	MAX	Process = Fast	T_J = -40°C	VDDIO = 3.6V

Figure 6-4. V-I curves for pins EMIT [0:11], AGC2, AGC5

6.5 Power Consumption

Table 6-6. Power Consumption

Parameter	Condition	Symbol	Rating			Unit
			Min	Typ	Max	
Power Consumption	T_J = 25ºC VDDIO = 3.3V VDDIN = 3.3V VDDIN AN = 3.3V	P_{25}	-	245	-	mW
Power Consumption (worst case)	T_J = 125ºC VDDIO = 3.6V VDDIN = 3.6V VDDIN AN = 3.6V	P_{125}	-	-	330	

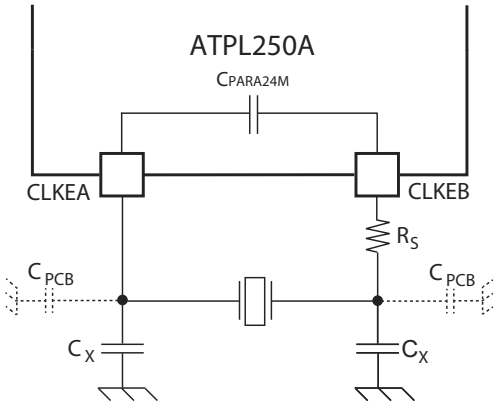
6.6 Oscillator

Table 6-7. ATPL250A 24 MHz Crystal Oscillator Characteristics

Parameter	Test Condition	Symbol	Rating			Unit
			Min	Typ	Max	
Crystal Oscillator frequency	Fundamental	X_{tal}		24		MHz
External Oscillator Capacitance(2)(3)		C_{XTAL}	-	18	-	pF
External capacitor on CLKEA and CLKEB(2)(3)		C_X	-	27	-	
Internal parasitic capacitance	Between CLKEA and CLKEB	$C_{PARA24M}$	-	4	-	
H-level Input Voltage		XVIH	2	-	VDDIO +0.3	V
L-level Input Voltage		XVIL	-0.3	-	0.8	
External Oscillator Parallel Resistance		Rp		not needed		Ω
External Oscillator Series Resistance		Rs	-	220	-	

Notes:
1. The crystal should be located as close as possible to CLKEB and CLKEA pins.
2. Recommended value for Cx is 27 pF and Rs 220 Ω. These values may depend on the specific crystal characteristics and PCB layout. See example below. For further information please refer to Atmel doc43084 “Crystal Selection Guidelines” application note.
3. As a requirement of G3 specification, the System Clock tolerance from which transmit frequency and symbol timing are derived shall be ± 25 ppm maximum. Crystal Stability/Tolerance/Ageing values must be selected according to standard G3 requirements.

Figure 6-5. 24 MHz Crystal Oscillator Schematic



$$C_X = 2 \times (C_{XTAL} - C_{PARA24M} - C_{PCB} / 2)$$

where C_{PCB} is the ground referenced parasitic capacitance of the printed circuit board (PCB) on CLKEA and CLKEB tracks.

As a practical example, taking the following crystal part number:

Manufacturer: TXC CORPORATION

PartNumber: 9C-24.000MEEJ-T

Frequency: 24.000 MHz

Tolerance: 10 ppm (as low as possible to fullfil G3 specification requirements)

C_{XTAL} = 18 pF

Working in a typical layout / substrate with C_{PCB} = 1 pF

The value of the external capacitors on CLKEA and CLKEB should be $C_X = 2 \times (18 - 4 - 0.5) = 27$ pF

It is strongly recommended to use capacitors with the lowest temperature stability possible. In this practical example, a suitable part number could be:

Manufacturer: MURATA

PartNumber: GRM1885C1H270FA01D

Capacitance: 27 pF

Tolerance: 1 %

Dielectric: C0G / NP0 (0 drift)

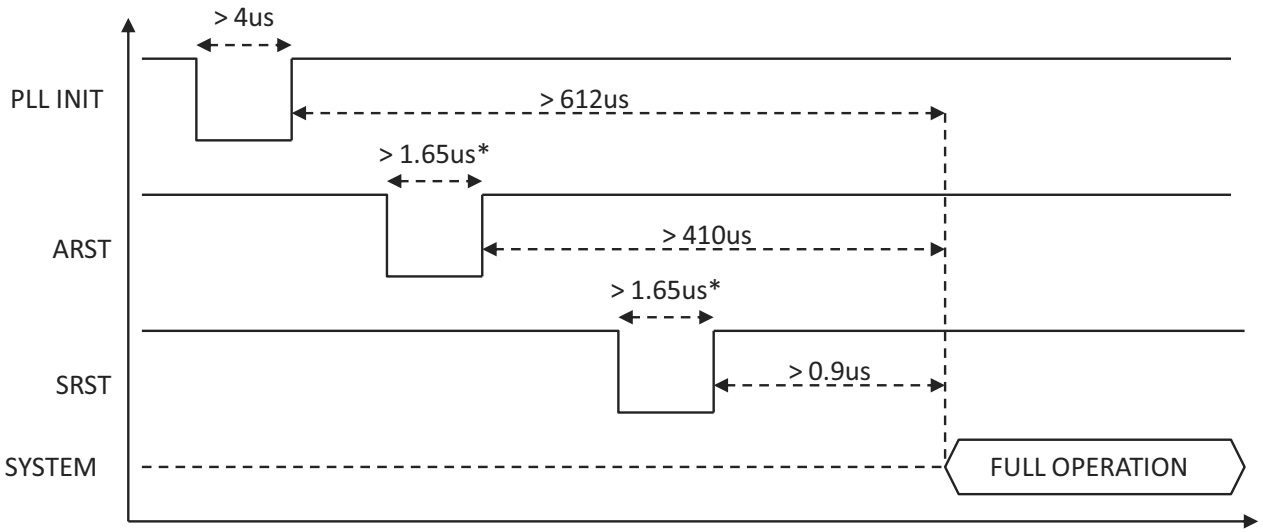
6.7 Power On Considerations

During power-on, PLL INIT pin should be tied to ground during 4 µs at least, in order to ensure proper system start up. After releasing PLL INIT, the system will start no later than 612 µs.

After power-up system can be restarted by means of low active pulse (min 1.65 µs) in ARST or SRST. System full operation starts after 410 µs (ARST pulse) or after 0.9 µs (SRST pulse).

In case of simultaneous tie down of more than one initialization pin the longest time for operation must be respected.

Figure 6-6. Power On timing diagram

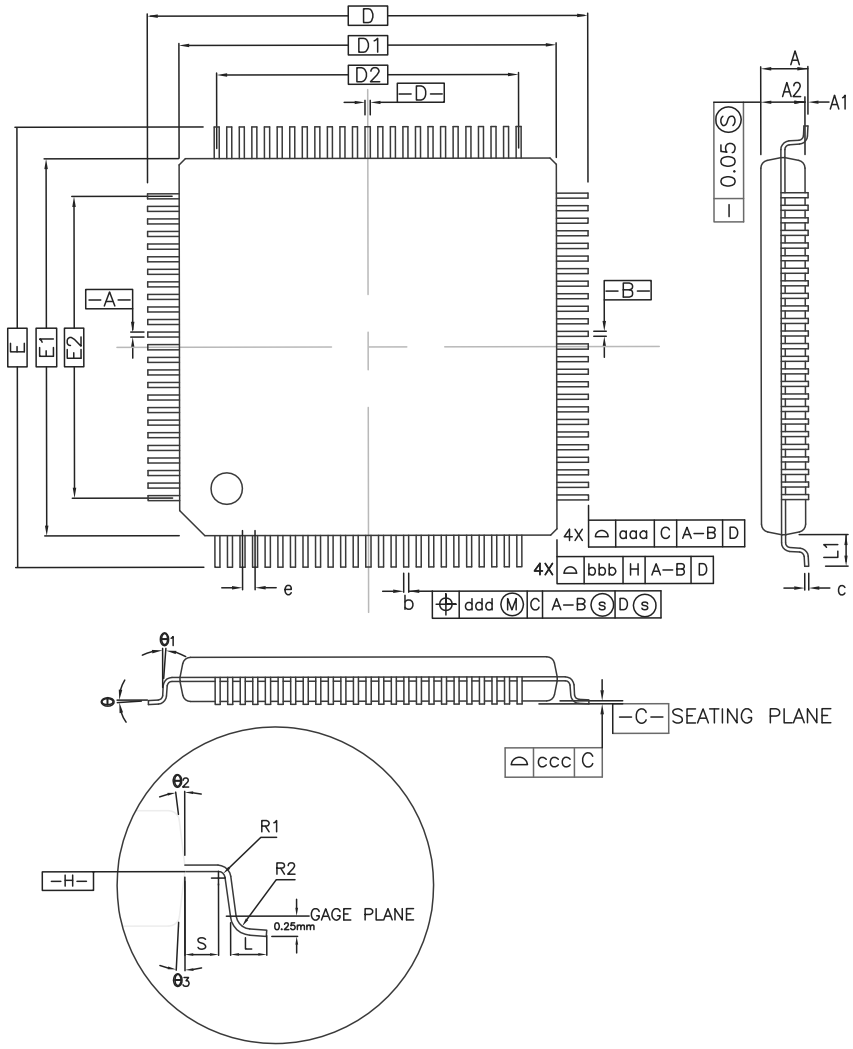


(*) 1.65us = 33*tclk

7. Mechanical Characteristics

7.1 LQFP80 Mechanical Characteristics

Figure 7-1. 80 LQFP package dimensions



CONTROL DIMENSIONS ARE IN MILLIMETERS.

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	1.60	—	—	0.063
A_1	0.05	—	0.15	0.002	—	0.006
A_2	1.35	1.40	1.45	0.053	0.055	0.057
D	14.00 BSC.			0.551 BSC.		
D_1	12.00 BSC.			0.472 BSC.		
E	14.00 BSC.			0.551 BSC.		
E_1	12.00 BSC.			0.472 BSC.		
R_2	0.08	—	0.20	0.003	—	0.008
R_1	0.08	—	—	0.003	—	—
θ	0°	3.5°	7°	0°	3.5°	7°
$θ_1$	0°	—	—	0°	—	—
$θ_2$	11°	12°	13°	11°	12°	13°
$θ_3$	11°	12°	13°	11°	12°	13°
c	0.09	—	0.20	0.004	—	0.008
L	0.45	0.60	0.75	0.018	0.024	0.030
L_1	1.00 REF			0.039 REF		
S	0.20	—	—	0.008	—	—

SYMBOL	80L					
	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
b	0.17	0.20	0.27	0.007	0.008	0.011
e	0.50 BSC.			0.020 BSC.		
D2	9.50			0.374		
E2	9.50			0.374		
TOLERANCES OF FORM AND POSITION						
aaa	0.20			0.008		
bbb	0.20			0.008		
ccc	0.08			0.003		
ddd	0.08			0.003		

Table 7-1. LQFP Package Reference

JEDEC Drawing Reference	MS-026

Table 7-2. LQFP Package Characteristics

Moisture Sensitivity Level	3

This package respects the recommendations of the NEMI User Group.

8. Recommended mounting conditions

8.1 Conditions of Standard Reflow

Table 8-1. Recommended mounting conditions of Standard Reflow

Items	Contents	
Method	IR (Infrared Reflow) / Convection	
Times	2	
Floor Life	Before unpacking	Please use within 2 years after production
	From unpacking to second reflow	Within 8 days
	In case over period of floor life	Baking with 125ºC +/- 3ºC for 24hrs +2hrs/-0hrs is required. Then please use within 8 days (please remember baking is up to 2 times).
Floor Life Condition	Between 5ºC and 30ºC and also below 70% RH required. (It is preferred lower humidity in the required temp. range).	

Figure 8-1. LQFP80 package soldering profile

Note: H rank: 260ºC Max

a: Average ramp-up rate:	1ºC/s to 4ºC/s
b: Preheat & Soak:	170ºC to 190ºC, 60s to 180s
c: Average ramp-up rate:	1ºC/s to 4ºC/s
d: Peak temperature:	260ºC Max, up to 255ºC within 10s
d': Liquidous temperature:	Up to 230ºC within 40s or
	Up to 225ºC within 60s or
	Up to 220ºC within 80s
e: Cooling:	Natural cooling or forced cooling

8.2 Manual Soldering

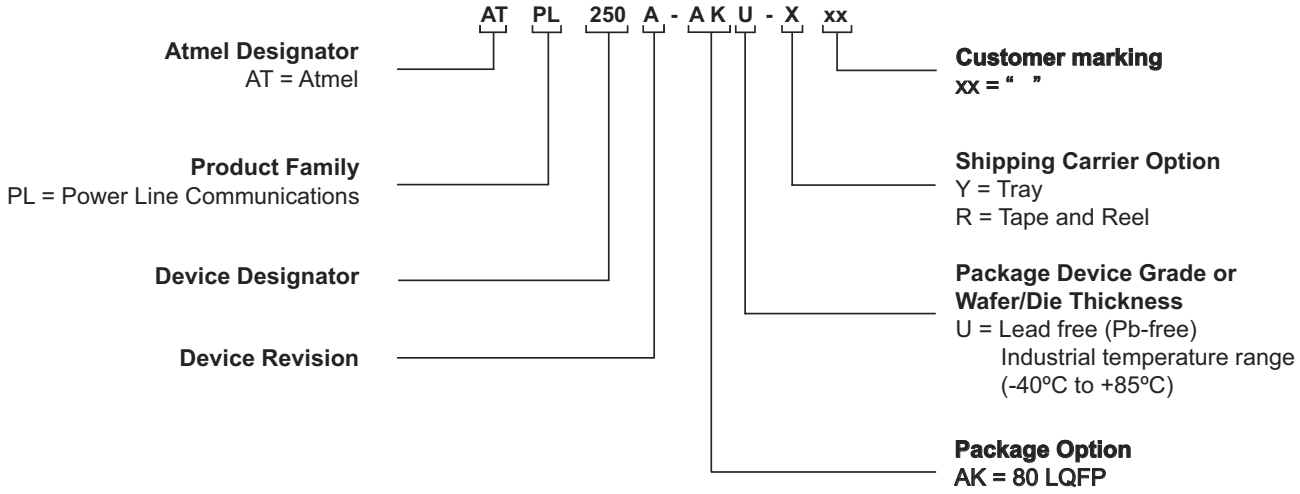
Table 8-2. Recommended mounting conditions of Manual Soldering

Items	Contents	
Floor life	Before unpacking	Please use within 2 years after production
	From unpacking to Manual Soldering	Within 2 years after production (No control required for moisture adsorption because it is partial heating)
Floor life condition	Between 5°C and 30°C and also below 70% RH required. (It is preferred lower humidity in the required temp. range).	
Solder Condition	Temperature of soldering iron: Max 400°C, Time: Within 5 seconds/pin. *Be careful for touching package body with iron.	

9. Ordering Information

Table 9-1. Ordering Information

Atmel Ordering Code	Package	Package Type	Temperature Range
ATPL250A-AKU-Y	80 LQFP	Pb-Free	Industrial (-40ºC to 85ºC)
ATPL250A-AKU-R	80 LQFP	Pb-Free	Industrial (-40ºC to 85ºC)



10. Revision History

In the table that follows, the most recent version of the document appears first.

Doc. Rev. 43079	Comments	Change Request Ref.
F	Figure 5-3 and Figure 5-5: updated.	
E	Section 5.3 ”Zero-crossing detector”: updated.	
D	Format changes according to new templates.	
C	Section 6.6 ”Oscillator” updated: modified Figure 6-5, added equation and information after the figure. Table 6-7 updated: added the values of C_{XTAL} and $C_{PARA24M}$. Modified the notes below the table.	
B	Chapters order redefined. Modified Section 1.1 ”ATPL250A Application Block Diagram” (was Section 8. “Application information”). Figure 1-1 updated: RST and CLKOUT signals introduced. Table 6-6 updated the values of Power Consumption and Power Consumption (worst case). Modified Section 5. ”Analog Front-End” (was “PLC coupling circuitry description”). Deleted Section “Power Considerations”: the information of this section is in Section 3. ”Signal Description”.	
A	First Issue.	

Table of Contents

Atmel | Enabling Unlimited Possibilities®

Atmel Corporation 1600 Technology Drive, San Jose, CA 95110 USA **T:** (+1)(408) 441.0311 **F:** (+1)(408) 436.4200 | **www.atmel.com**