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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-A5/M4/M0+
Core Size	32-Bit Tri-Core
Speed	80MHz, 160MHz, 320MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, LINbus, SPI
Peripherals	DMA, LCD, LVD/HVD, POR, PWM, WDT
Number of I/O	-
Program Memory Size	4MB (4M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2.3M x 8
Voltage - Supply (Vcc/Vdd)	3.15V ~ 5.5V
Data Converters	A/D 24x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	208-LQFP Exposed Pad
Supplier Device Package	208-LQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/sac57d54hcvlt

- Graphics interfaces
  - Vivante GC355 GPU supporting OpenVG 1.1
  - 2 x 2D-ACE Display Controllers (with inline Head-Up-Display warping)
  - Digital RGB, TCON_0 (RSDS), TCON_1 and OpenLDI/LVDS output options
  - Digital Video Input (VIU4)
  - RLE Decoder for memory-memory decompression
  - 40x4 segment LCD driver, reconfigurable as 38x6 or 36x8
- Cluster peripherals
  - Sound Generator Module (SGM)
  - 6 Stepper Motor Drivers with Stepper Stall Detect
- Communication
  - Ethernet 10/100 + AVB (ENET)
  - MLB50
  - FlexCAN x 3
  - DSPI x 5
  - LINFlexD x 3 (1 x Master/Slave, 2 x Master only)
  - I2C x 2
- eDMA controller with multiple transfer request sources using DMAMUX
- Boot Assist Flash (BAF) supports internal flash programming

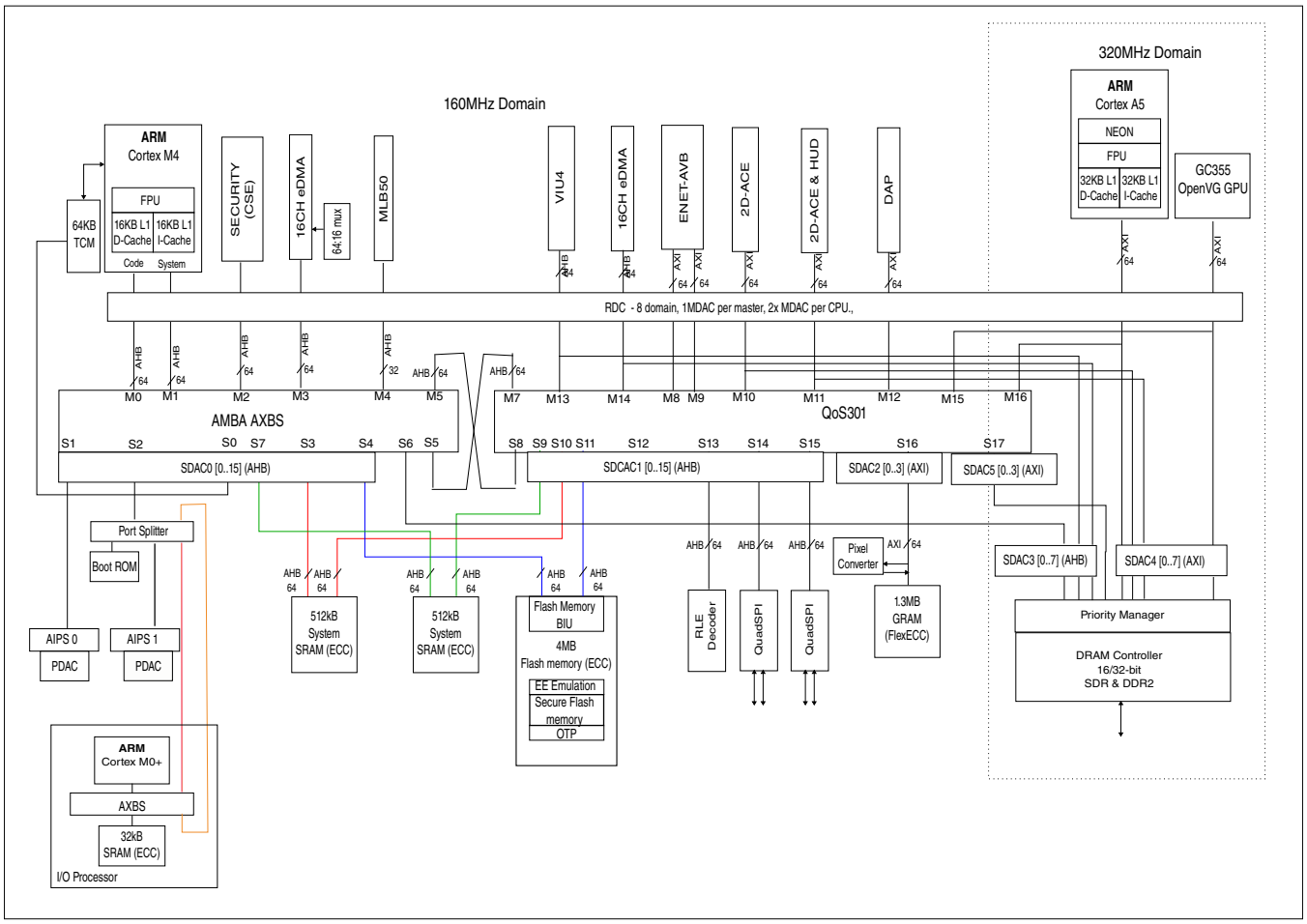

Figure 2. Detailed block diagram

2 Family comparison

The table below provides a summary of the different members of the SAC57D5xx Low/ Mid-Line Instrument Cluster family and their features. Note that not all features are available simultaneously on all packages.

Table 1. Feature sets

Product Features		SAC57D54H	SAC57D53M	SAC57D52L
Cores	Cortex-A5 (320 MHz, 32 KB/32 KB L1 Caches, FPU, MMU, NEON)	Yes	Yes	Yes
	Cortex-M4 (160 MHz, 16 KB/16 KB L1 Caches, FPU)	Yes	Yes	Yes

Table continues on the next page...

Table 1. Feature sets (continued)

Product Features		SAC57D54H	SAC57D53M	SAC57D52L
	Cortex - M0+ I/O Processor (IOP) (80 MHz)	Yes	Yes	Yes
Internal Memory	ECC Flash Memory	4 MB	3 MB	2 MB
	Graphics SRAM[1]	1.3 MB	1.3 MB	1.3 MB
	System SRAM (ECC)	2 x 512 KB	2 x 512 KB	2 x 512 KB
	IOP local SRAM (ECC)	32 KB	32 KB	32 KB
External Memory Interfaces	Dual DDR QuadSPI	2 x Dual DDR QuadSPI	2 x Dual DDR QuadSPI	2 x Dual DDR QuadSPI
	16 bit SDR DRAM (160MHz)	Yes	Yes	Yes
	32-Bit DDR2 DRAM (320MHz)[2]	Yes	Yes	-
System and General Purpose	Memory / Peripheral Protection (xDRC - Extended Resource Domain Controller)	Yes	Yes	Yes
	Security (CSE)	Yes	Yes	Yes
	eDMA	16ch x 2	16ch x 2	16ch x 2
Graphics/Video/Display/ Audio	2D-ACE	x2	x2	x2
	HUD Warping Engine	Yes	Yes	Yes
	TCON_0/RSDS	Yes	Yes	Yes
	TCON_1	Yes	Yes	Yes
	OpenLDI/LVDS	Yes	Yes	-
	GPU	GC355 : OpenVG 1.1 / TinyUI	GC355 : OpenVG 1.1 / TinyUI	GC355 : OpenVG 1.1 / TinyUI
	Video Input Unit	Yes	Yes	Yes
	Sound Generator	Yes	Yes	Yes
	Segment LCD	Yes	Yes	Yes
System Connectivity	FlexCAN	x3	x3	x3
	I2C	x2	x2	x2
	LINFlexD	x3	x3	x3
	SPI	x5	x5	x5
	MLB50	Yes	Yes	Yes
	10/100 Ethernet + AVB	Yes	Yes	Yes
Analog Connectivity	SMC/SSD	x6	x6	x6
	12 Bit ADC	Yes	Yes	Yes
	Analog Comparator	2 x 8ch	2 x 8ch	2 x 8ch
Timer/PWM	PIT	8ch	8ch	8ch
	SWT	3	3	3
	ARTC	Yes	Yes	Yes
	FlexTimer	4 x 8ch	4 x 8ch	4 x 8ch
Package Options	LQFP	208 LQFP	208 LQFP	208 LQFP

Table continues on the next page...

1. All parameters are with reference to V_{ss} unless otherwise specified.
2. A crossover current of up to 2 mA may be experienced if V_{DD12} is ramped up before V_{DDE_A} supply. This current is only an electrical crossover but has no functional implications, and should be removed when V_{DDE_A} ramps up to its functional operating range.
3. Not available for input voltage, only for decoupling internal regulators.
4. V_{DDA_REF} is only available on the 516 BGA package.
5. DDR_VREF is expected to be equal to 0.5 × V_{DDE_DDR} and to track V_{DDE_DDR} DC variations as measured at the device pins. Ensure V_{DD_LV} supply ramps up before V_{DDE_DDR}. In Standby mode, it should be ensured that V_{DDE_DDR} supply should be cut off.
6. Tj=125°C. Assumes Ta=105°C. Assumes maximum θJA of 2s2p board. See Thermal attributes section for details.

4.2 Recommended operating conditions

The following table describes the operating conditions for the device, and for which all specifications in the data sheet are valid, except where explicitly noted. The device operating conditions must not be exceeded in order to guarantee proper operation and reliability. The ranges in this table are design targets and actual data may vary in the given range.

For normal device operations, V_{DDE_A}, V_{DDA}, V_{DDA_REF}, V_{DDEH_ADC} and V_{DD12} supplies must be within operating range corresponding to the range mentioned in following tables. This is required even if some of the features are not used. If using the ADC to convert SSD channels then V_{DDA} should always be >= V_{DDM_SMC}.

V_{DD12} should be supplied externally. V_{DDA_REF}, the supply port to 516 BGA is shorted to V_{DDA} inside lower pin packages. Stepper Stall Detect module (SSD) should only be operated in the 4.5 V to 5.5 V range and so cannot be used if V_{DDM_SMD} is in 3.3 V range.

Design may experience up to 30 mA additional crossover current (on VDDE_A) if the high voltage flash supply is powered before the low voltage core supply. This additional current will be removed once VDD12 supply rises to its operating range. There is no reliability concern to the device due to this additional current.

Table 3. Recommended operating conditions

Symbol [1]	Parameter	Conditions	Min[2]	Max	Unit
V_{DDE_A} V_{DDE_B}[3] V_{DDE_SDR}[3]	Input/output supply voltage	—	3.15	3.6	V
V_{SSA}	ADC supply ground, relative to VSS	—	-0.1	0.1	V
V_{DDA}	ADC supply voltage	V_{DDA},V_{DDA_REF} and V_{DDEH_ADC} should be within +/-25 mV of each other	3.15	5.5	V
V_{DDEH_ADC}	ADC I/O supply voltage		3.15	5.5	V
V_{DDA_REF}	ADC reference voltage		3.15	5.5	V
V_{DDM_SMD}	SMD supply voltage	—	3.15	5.5	V

Table continues on the next page...

- For V_{DD12}, 0.1 µF close to each V_{DD}/V_{SS} pin pair is required.

4.4 Voltage monitor electrical specifications

Table 5. Voltage monitor electrical specifications

Symbol	Parameter	State	Conditions	Configuration			Threshold			Unit
				Power Up [1]	Mask Opt	Reset Type	Min	Typ	Max	
V_{POR_LV}	LV supply power on reset detector	Fall	Untrimmed	Yes	No	Destructive	0.9300	0.9790	1.0280	V
			Trimmed				-	-	-	V
		Rise	Untrimmed				0.9800	1.0290	1.0780	V
			Trimmed				-	-	-	V
$V_{HVD\_LV\_cold}$	LV supply high voltage monitoring, detecting at the device pin	Fall	Untrimmed	No	Yes	Functional	Disabled at Start			
			Trimmed				1.3250	1.3450	1.3750	V
		Rise	Untrimmed				Disabled at Start			
			Trimmed				1.3450	1.3650	1.3950	V
$V_{LVD\_LV\_PD2\_hot}$	LV supply low voltage monitoring, detecting in the PD2 core (hot) area	Fall	Untrimmed	Yes	No	Destructive	1.0800	1.1200	1.1600	V
			Trimmed				1.1250	1.1425	1.1600	V
		Rise	Untrimmed				1.1000	1.1400	1.1800	V
			Trimmed				1.1450	1.1625	1.1800	V
$V_{LVD\_LV\_PD1\_hot}$	LV supply low voltage monitoring, detecting in the PD1 core (hot) area	Fall	Untrimmed	Yes	No	Destructive	1.0800	1.1200	1.1600	V
			Trimmed				1.1140	1.1370	1.1600	V
		Rise	Untrimmed				1.1000	1.1400	1.1800	V
			Trimmed				1.1340	1.1570	1.1800	V
$V_{LVD\_LV\_PD0\_hot}$	LV supply low voltage monitoring, detecting in the PD0 core (hot) area	Fall	Untrimmed	Yes	No	Destructive	1.0800	1.1200	1.1600	V
			Trimmed				1.1140	1.1370	1.1600	V
		Rise	Untrimmed				1.1000	1.1400	1.1800	V
			Trimmed				1.1340	1.1570	1.1800	V
V_{POR_HV}	HV supply power on reset detector	Fall	Untrimmed	Yes	No	Destructive	2.7000	2.8500	3.0000	V
			Trimmed				-	-	-	V
		Rise	Untrimmed				2.7500	2.9000	3.0500	V
			Trimmed				-	-	-	V
$V_{LVD\_IO\_A\_LO}$	HV IO_A supply low voltage monitoring - low range	Fall	Untrimmed	Yes	No	Destructive	2.7500	2.9230	3.0950	V
			Trimmed				2.9780	3.0390	3.1000	V
		Rise	Untrimmed				2.7800	2.9530	3.1250	V
			Trimmed				3.0080	3.0690	3.1300	V
$V_{LVD\_LV\_PD2\_COLD}$	LV supply low voltage monitoring, detecting at the device pin	Fall	Untrimmed	No	Yes	Functional	Disabled at Start			
			Trimmed				1.1400	1.1550	1.1750	V
		Rise	Untrimmed				Disabled at Start			
			Trimmed				1.1600	1.1750	1.1950	V

Table 7. ESD ratings (continued)

Symbol	Parameter	Conditions[1]	Class	Max value[2]	Unit
		conforming to AEC-Q100-002			
$V_{ESD(CDM)}$	Electrostatic discharge (Charged Device Model)	T_A = 25 °C conforming to AEC-Q100-011	C3A	500 750 (corners)	V

1. All ESD testing is in conformity with CDF-AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits.
2. Data based on characterization results, not tested in production.

4.7 Electromagnetic Compatibility (EMC) specifications

EMC measurements to IC-level IEC standards are available from NXP on request.

5 I/O parameters

5.1 AC specifications @ 3.3 V range

Table 8. Functional Pad AC Specifications @ 3.3 V range

Symbol	Rise/Fall Edge (ns)		Drive Load (pF)	Drive/Slew Rate Select
	Min	Max		MSB, LSB
pad_sr_hv (output)		1.75/1.5	25	11 (Recommended setting)
	0.8/0.8	3.25/3	50	
	3.5/2.5	12/12	200	
	0.6/0.8	3.75/3.5	25	10
	1/1	7/6.5	50	
	7.7/5	25/21	200	
	4/3.5	25/25	50	01
	6.3/6.2	30/30	200	
	6.8/6	40/40	50	00[1]
	11/11	51/51	200	
pad_i_hv/pad_sr_hv (input)[2]		0.5/0.5	0.5	NA
pad_fc_hv (output)	0.6/0.6	1.5/1.5	30	11
		2.4/2.4	50	
	0.6/0.6	1.5/1.5	20	10
	0.6/0.6	1.85/1.85	10	01
	12/11	36/45	50	00

5.3 AC specifications @ 5 V range

Table 10. Functional pad AC specifications @ 5 V range

Symbol	Rise/Fall Edge (ns)		Drive Load (pF)	Drive/Slew Rate Select
	Min	Max		MSB, LSB
pad_sr_hv (output)		1.2/1.2	25	11 (Recommended setting)
		2.5/2	50	
		8/8	200	
		3/2	25	10
		5/4	50	
		18/16	200	
		13/13	50	01
		24/24	200	
		24/24	50	00[1]
		50/50	200	
pad_fc_hv (output)		1.8/1.7	50	11
		6.6/6.1	200	
		2.7/2.5	50	10
		10.3/9.3	200	
		5.6/4.8	50	01
		21/19	200	
		41/41	50	00
		151/151	200	

1. Slew rate control modes

5.4 DC electrical specifications @ 5 V range

Table 11. DC electrical specifications @ 5 V range

Symbol	Parameter	Value		Unit
		Min	Max	
V_{dde}	I/O Supply Voltage	4.5	5.5	V
V_{ih}	CMOS Input Buffer High Voltage (with hysteresis disabled)	0.55 × Vdde	Vdde + 0.3	V
V_{il}	CMOS Input Buffer Low Voltage (with hysteresis disabled)	Vss – 0.3	0.40 × Vdde	V
V_{ih_hys}	CMOS Input Buffer High Voltage (with hysteresis enabled)	0.65 × Vdde	Vdde + 0.3	V
V_{il_hys}	CMOS Input Buffer Low Voltage (with hysteresis enabled)	Vss – 0.3	0.35 × Vdde	V

Table continues on the next page...

Table 15. SMC 5V IO DC specifications(4.5V<vdde<5.5V) (continued)

Symbol	Characteristic	Min	Typ	Max	Unit
V_{oh}	High level output voltage (I_{oh}=-20 mA)	vdde – 0.32			V
V_{sum}	Vsum (| Vol | + | Voh |) (I_{ol}=+40 mA and I_{oh}=-40 mA)			1.0	V
V_{oh} delta / V_{ol} delta	Delta V_{oh} across one motor segment and Delta V_{ol} across one motor segment	–50		50	mV
R_{dsonh}	Pad drive active high impedance (test load I_{oh} = 30 mA)	4		13	Ω
R_{dsonl}	Pad drive active low impedance (test load I_{ol} = 30 mA)	2.75		9	Ω

5.6.1.2 SMC 5V pads IO AC specifications

Table 16. SMC 5V IO functional pad AC specifications (4.5V<vdde<5.5V)

Name	Symbol	Symbol	Rise/Fall Edge (ns)		Drive Load (pF)	Drive/Slew Rate Select
			Min	Max		ipp_sre_lv
CMOS input				0.5/0.5	0.5	NA

5.6.2 SMC 3.3 V pads IO specifications

NOTE

In Table 17, Table 18, the "V_{DDE}" refers to the V_{DDM_SMD} supply.

5.6.2.1 SMC 3.3 V pads IO DC specifications

Table 17. SMC 3.3 V pads IO DC specifications (3.0V<vdde<3.6V)

Symbol	Characteristic	Min	Typ	Max	Unit
V_{il}	Low level input voltage	-0.3		0.35 × vdde	V
V_{ih}	High level input voltage	0.65 × vdde		vdde + 0.3	V
V_{hyst}	Schmitt trigger hysteresis	0.1 × vdde			V
I_{pu}	Internal pull up device current (V_{in}=V_{il})	-130			µA
I_{pu}	Internal pull up device current (V_{in}=V_{ih})			-10	µA
I_{pd}	Internal pull down device current (V_{in}=V_{il})	10			µA

Table continues on the next page...

Table 17. SMC 3.3 V pads IO DC specifications (3.0V<vdde<3.6V) (continued)

Symbol	Characteristic	Min	Typ	Max	Unit
I_{pd}	Internal pull down device current (V_{in}=V_{ih})			130	µA
I_{in}	Input leakage current (ipp_pue=0)	-2.5		+2.5	µA
V_{ol}	Low level output voltage (I_{ol}=+10 mA)			0.32	V
V_{oh}	High level output voltage (I_{oh}=-10 mA)	vdde – 0.32			V

5.6.2.2 SMC 3.3 V pads IO AC specifications

Table 18. SMC 3.3 V functional pads IO DC specifications (3.0V<vdde<3.6V)

Name	Symbol	Symbol	Rise/Fall Edge (ns)		Drive Load (pF)	Drive/Slew Rate Select
			Min	Max		ipp_sre_lv
CMOS input				0.5/0.5	0.5	NA

5.7 RSDS pads electrical specifications

Table 19. RSDS pads electrical specifications

Symbol	Parameter	Min	Typ	Max	Unit
Supply Voltages					
	V_{dde}[1]	3	3.3	-	V
RSDS_Tx					
	Normal mode (V_{dde})	-	3	-	mA
	Power down mode	-	1	-	µA
RSDS reference					
	Normal mode	-	400	-	µA
	Power down mode	-	0.1	-	µA
Data rate					
	Data Frequency		50	50	MHz
Driver specs					
V_{od}	Differential o/p voltage	100	200	400	mV
V_{os}	Common mode voltage (VOS)	-	1.2	-	V
t_R/t_F	Rise/Fall time	-	500	-	ps
	Startup Time (RSDS_ref)	-	6	-	µs
	Startup time (RSDSTx)	-	6	-	µs
Termination					

Table continues on the next page...

Table 20. LVDS pads electrical specifications (continued)

	V_{DDE} [1]	3	3.3	-	V
Current consumption					
LVDS Tx					
	Normal mode (V_{DDE} [1])	—	5	—	mA
	Switching currents	—	±1.5 (during output transition)	—	mA
	Power down mode	—	1	—	µA
LVDS Reference					
	Normal mode	—	400	—	µA
	Power down mode	—	0.1	—	µA
Data Rate					
	Data Frequency	—	—	560	Mbps
Driver specs					
V_{od}	Differential o/p voltage [2]	247	—	454	mV
V_{os}	Common mode voltage (V_{OS})	1.125	—	1.375	V
t_r/t_f	Rise/Fall time [3]	—	—	800	ps
	Startup Time (lvds_ref)	—	5	—	µs
	Startup time (lvds_Tx)	—	5	—	µs
Termination					
	Termination Resistance	—	100±1%	—	Ω
	Trans. Line (differential Zo)	95	100	105	Ω

1. V_{DDE} is the V_{DDE_B} supply.
2. The limit applies to the default drive current.
3. Rise/fall time is assumed to be measured with 20%-80% levels.

5.9 Functional reset pad electrical specifications

The device implements a dedicated bidirectional RESET pin.

Table 21. Functional reset pad electrical specifications

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
V_{IH}	Input high level TTL (Schmitt Trigger)	—	2.0	—	V_{DDE_A}+0.4	V
V_{IL}	Input low level TTL (Schmitt Trigger)	—	–0.4	—	0.65	V
V_{HYS}	Input hysteresis TTL (Schmitt Trigger)	—	300	—	—	mV

Table continues on the next page...

Table 32. Flash memory program and erase specifications (continued)

Symbol	Characteristic[1]	Typ[2]	Factory Programming[3, 4]		Field Update			Unit
			Initial Max	Initial Max, Full Temp	Typical End of Life[5]	Lifetime Max[6]		
			20°C ≤T_A ≤30°C	-40°C ≤T_J ≤150°C	-40°C ≤T_J ≤150°C	≤ 1,000 cycles	≤ 250,000 cycles	
t_{qppgn}	Quad-page (1024 bits) program time	268	800	1,200	396	2,000		µs
t_{16kers}	16 KB Block erase time	168	290	320	250	1,000		ms
t_{16kpgn}	16 KB Block program time	34	45	50	40	1,000		ms
t_{32kers}	32 KB Block erase time	217	360	390	310	1,200		ms
t_{32kpgm}	32 KB Block program time	69	100	110	90	1,200		ms
t_{64kers}	64 KB Block erase time	315	490	590	420	1,600		ms
t_{64kpgm}	64 KB Block program time	138	180	210	170	1,600		ms
$t_{256kers}$	256 KB Block erase time	884	1,520	2,030	1,080	4,000	—	ms
$t_{256kpgm}$	256 KB Block program time	552	720	880	650	4,000	—	ms

1. Program times are actual hardware programming times and do not include software overhead. Block program times assume quad-page programming.
2. Typical program and erase times represent the median performance and assume nominal supply values and operation at 25 °C. Typical program and erase times may be used for throughput calculations.
3. Conditions: ≤ 150 cycles, nominal voltage.
4. Plant Programing times provide guidance for timeout limits used in the factory.
5. Typical End of Life program and erase times represent the median performance and assume nominal supply values. Typical End of Life program and erase values may be used for throughput calculations.
6. Conditions: -40°C ≤ T_J ≤ 150°C, full spec voltage.

6.3.1.2 Flash memory Array Integrity and Margin Read specifications

Table 33. Flash memory Array Integrity and Margin Read specifications

Symbol	Characteristic	Min	Typical	Max[1]	Units[2]
$t_{ai16kseq}$	Array Integrity time for sequential sequence on 16KB block.	—	—	512 x Tperiod x Nread	—
$t_{ai32kseq}$	Array Integrity time for sequential sequence on 32KB block.	—	—	1024 x Tperiod x Nread	—
$t_{ai64kseq}$	Array Integrity time for sequential sequence on 64KB block.	—	—	2048 x Tperiod x Nread	—
tai256kseq	Array Integrity time for sequential sequence on 256KB block.	—	—	8192 x Tperiod x Nread	—
$t_{mr16kseq}$	Margin Read time for sequential sequence on 16KB block.	73.81	—	110.7	µs
$t_{mr32kseq}$	Margin Read time for sequential sequence on 32KB block.	128.43	—	192.6	µs

Table continues on the next page...

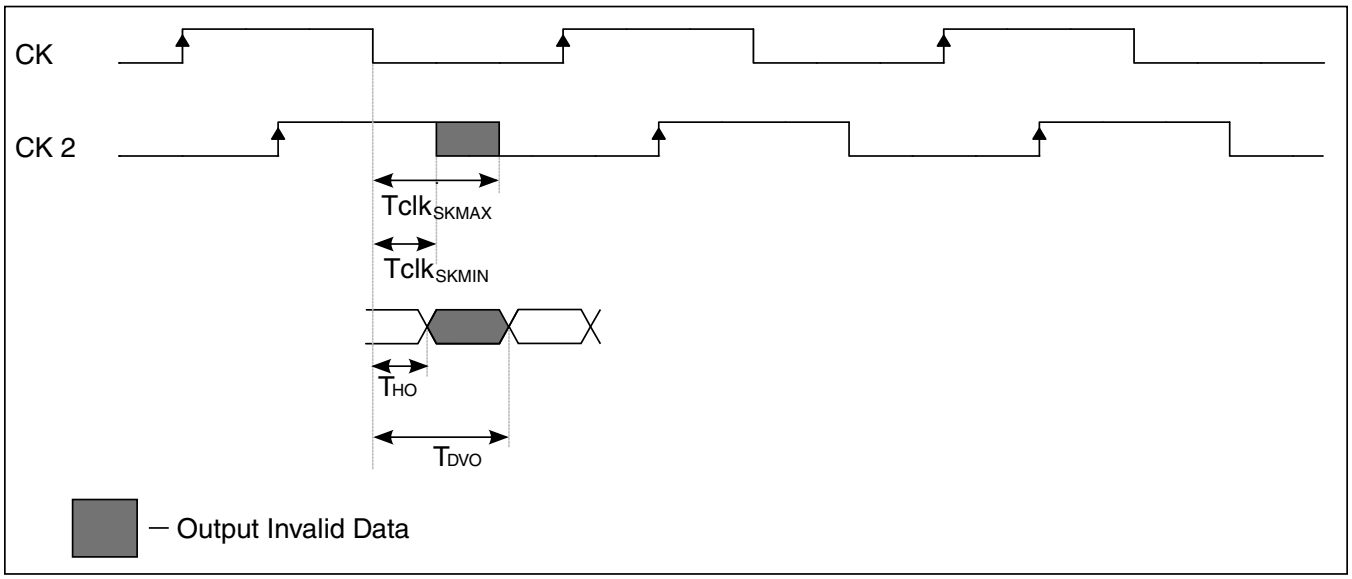

Figure 16. QuadSPI output timing (Hyperflash mode) diagram

Table 44. QuadSPI output timing (Hyperflash mode) specifications

Symbol	Parameter	Value		Unit
		Min	Max	
T_{DVO}	Output Data Valid	-	3	ns
T_{HO}	Output Data Hold	1.3	-	ns
$Tclk_{SKMAX}$	CK to CK2 skew max	-	T/4 + 0.5	ns
$Tclk_{SKMIN}$	CK to CK2 skew min	T/4 - 0.5	-	ns

6.3.3 SDR AC specifications

For details on read timings with and without the external capacitor and capacitance value, refer the "Chip-specific MDDRC information" section of the device Reference Manual.

For SDRAM operating frequencies above 80 MHz the SDR_A12 pin cannot be used for the SDRAM address. At higher operating frequencies this pin requires an external capacitor connected with V_{SS} to adjust the read timing.

Round trip delay (consisting of board trace delay of SDCK and DQ(READ)) should not be more than 450 ps.

NOTE

1. All transitions measured at mid-supply ($V_{DDE\_SDR}/2$).
2. Data signal which are driven from ATE are given a swing of 20%/80% of full signal swing.

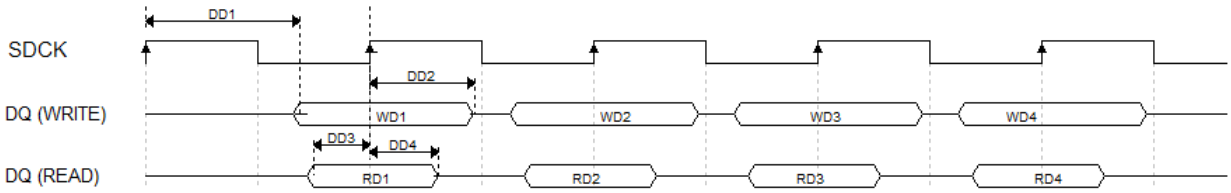

Figure 17. SDR (@ 160 MHz and @ 80 MHz) AC read and write timings

6.3.3.1 SDR DC specifications

The SDR DC specifications are same as pad_fc_hv specs described in this document.

6.3.4 DDR2 SDRAM AC specifications

NOTE

DDR2-800 (-25E speed grade) is the lowest speed grade supported. If self-refresh mechanism needs to be supported, an external pull-down resistance needs to be connected to the DDR CKE pin.

NOTE

Specified values in the table are at recommended operating conditions with V_{DDE_DDR} of 1.8±5.5%

Table 47. DDR2 SDRAM timing specifications[1, 2, 3, 4, 5]

ID	Symbol	Parameter	Min	Typ	Max	Unit
—	F	Frequency of operation (Clock Period)	—	—	320	MHz
—	V_{IX-AC}	MCK AC differential crosspoint voltage	0.5 × V_{DDE_DDR} — 0.175	—	0.5 × V_{DDE_DDR} + 0.175	V
DD1	t_{DDR_CLK}	Clock period	3.125	—	—	ns
DD2	t_{DDR_CLKH}	High pulse width[6]	0.47	—	0.53	tCK
DD3	t_{DDR_CLKL}	Low pulse width	0.47	—	0.53	tCK
DD4	t_{CMS}	Address/Command Output Setup	0.5 × t_{DDR_CLK}–0.75	—	—	ns
DD5	t_{CMH}	Address/Command Output Hold	0.5 × t_{DDR_CLK}–0.75	—	—	ns
DD6	t_{DQSS}	First DQS latching transition to associated clock edge	-0.18 × t_{DDR_CLK}	—	0.18 × t_{DDR_CLK}	ns

Table continues on the next page...

Table 47. DDR2 SDRAM timing specifications[1, 2, 3, 4, 5] (continued)

ID	Symbol	Parameter	Min	Typ	Max	Unit
DD7	t_{OS}	Data and Data Mask Output Setup relative to DQS (DDR Write Mode) [8, 9]	$t_{DDR\_CLK}/4 - 0.4$	—	—	ns
DD8	t_{OH}	Data and Data Mask Output Hold relative to DQS (DDR Write Mode) [7, 10]	$t_{DDR\_CLK}/4 - 0.4$	—	—	ns
DD9	t_{IS}	Input Data Skew relative to DQS[11]		—	0.24	ns
—	—	Parallel termination address lines	—	50	—	Ohms
—	—	Differential clock lines	—	100	—	Ohms
—	—	Trans. Line (differential Zo)	—	50	—	Ohms

1. V_{DDE_DDR} value is 1.8 V for DDR2 mode
2. C_Z at -40 to 125 °C.
3. Measured with clock pin loaded with differential 100 ohm termination resistor.
4. All transitions measured at mid-supply ($V_{DDE\_DDR}/2$).
5. Measured with all outputs except the clock loaded with 50 ohm termination resistor to $V_{DDE\_DDR}/2$.
6. Pulse width high + pulse width low cannot exceed minimum and maximum clock period.
7. The losses for IO and package are 190 ps and are already included in the 400 ps budget taken by the device.
8. This specification relates to the required input setup time of DDR memories. The chip output setup should be larger than the input setup of the DDR memories. If it is not larger, then the input setup on the memory is in violation. DDR_DQ[31:24] is relative to DDR_DQS[3]; DDR_DQ[23:16] is relative to DDR_DQS[2], DDR_DQ[15:8] is relative to DDR_DQS[1] and DDR_DQ[7:0] is relative to DDR_DQS[0].
9. The first data beat is valid before the first rising edge of DQS and after the DQS write preamble. The remaining data beats are valid for each subsequent DQS edge.
10. This specification relates to the required hold time of DDR memories. DDR_DQ[31:24] is relative to DDR_DQS[3]; DDR_DQ[23:16] is relative to DDR_DQS[2], DDR_DQ[15:8] is relative to DDR_DQS[1] and DDR_DQ[7:0] is relative to DDR_DQS[0].
11. Data input skew is derived from each DDR_DQS clock edge. It begins with a DDR_DQS transition and ends when the last data line becomes valid. This input skew must include DDR memory output skew and system level board skew (due to routing or other factors).

Figure 18 shows the DDR2 SDRAM write timing.

NOTE

For numbers shown in the following figures, see Table 48

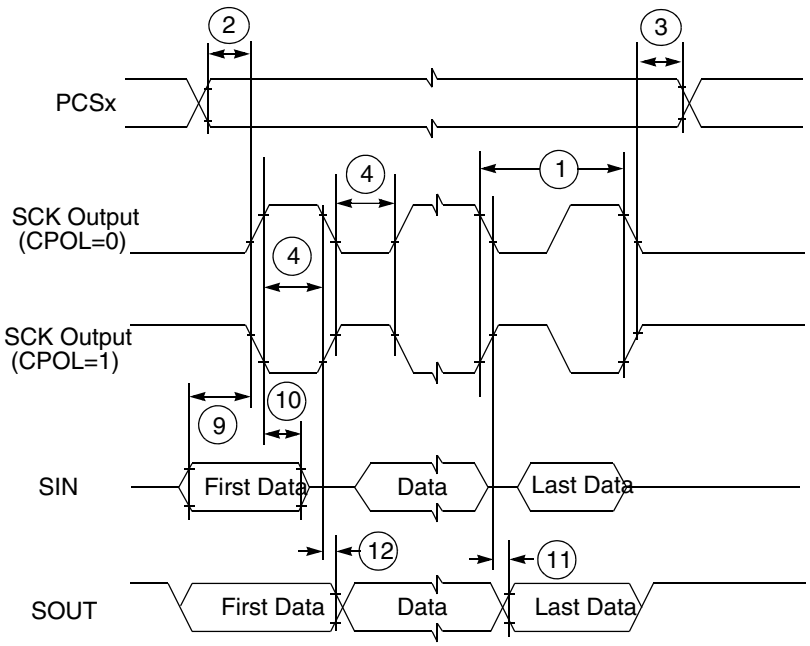

Figure 20. SPI classic SPI timing — master, CPHA = 0

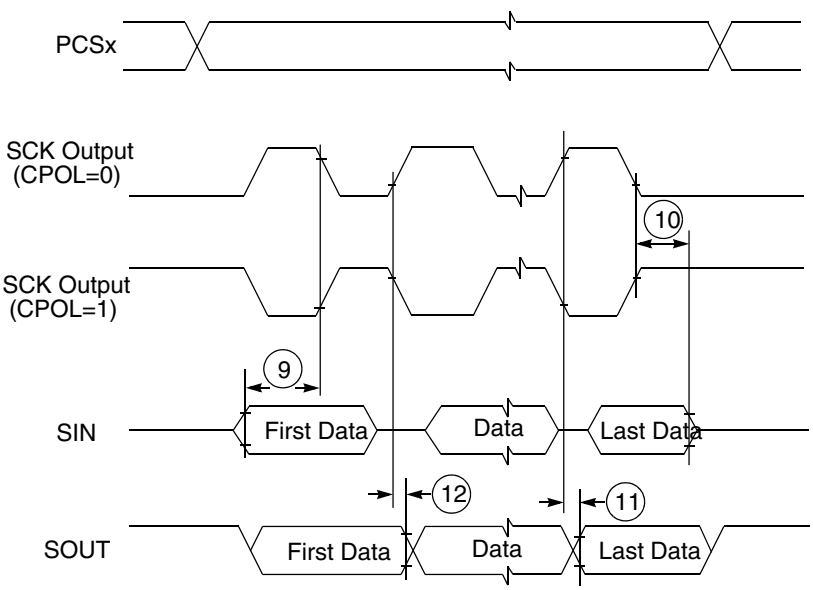

Figure 21. SPI classic SPI timing — master, CPHA = 1

6.4.2 Ethernet AC specifications

The following timing specs are defined at the chip I/O pin and must be translated appropriately to arrive at timing specs/constraints for the physical interface.

6.4.2.1 MII signal switching specifications

The following timing specs meet the requirements for MII style interfaces for a range of transceiver devices.

Table 49. MII signal switching specifications

Symbol	Description	Min.	Max.	Unit
—	RXCLK frequency	—	25	MHz
MII1	RXCLK pulse width high	35%	65%	RXCLK period
MII2	RXCLK pulse width low	35%	65%	RXCLK period
MII3	RXD[3:0], RXDV, RXER to RXCLK setup	5	—	ns
MII4	RXCLK to RXD[3:0], RXDV, RXER hold	5	—	ns
—	TXCLK frequency	—	25	MHz
MII5	TXCLK pulse width high	35%	65%	TXCLK period
MII6	TXCLK pulse width low	35%	65%	TXCLK period
MII7	TXCLK to TXD[3:0], TXEN, TXER invalid	2	—	ns
MII8	TXCLK to TXD[3:0], TXEN, TXER valid	—	25	ns

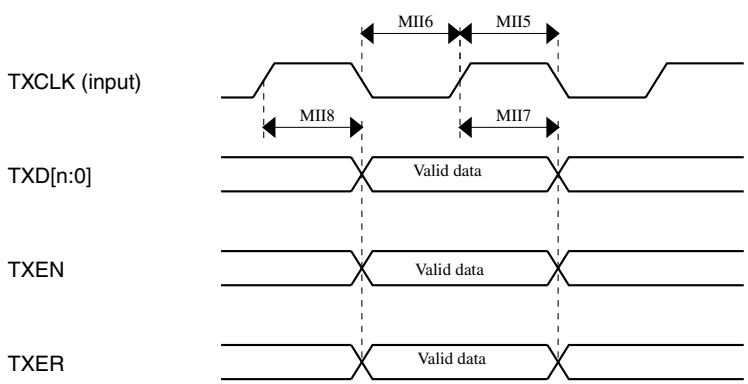

Figure 29. RMII/MII transmit signal timing diagram

6.5.4 TCON electrical specifications

6.5.4.1 TCON RSDS electrical specifications

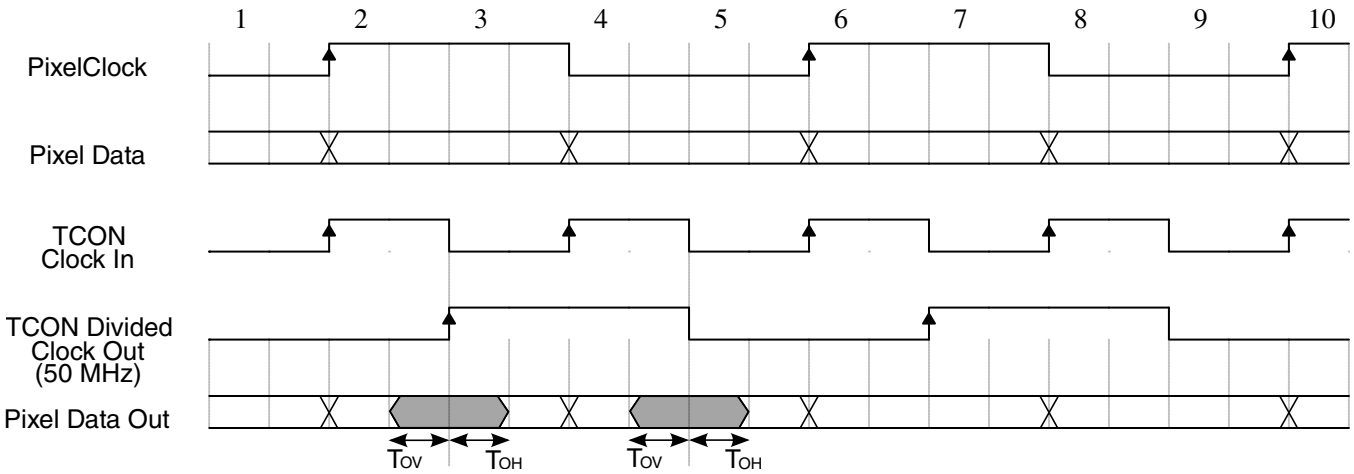

Figure 37. TCON RSDS timing diagram

Table 58. TCON RSDS timing parameters

Symbol	Parameter	Value		Unit
		Min	Max	
T_{OV}	Output data valid time	2	-	ns
T_{OH}	Output data hold time	2	-	ns

6.5.4.2 TCON TTL electrical specifications

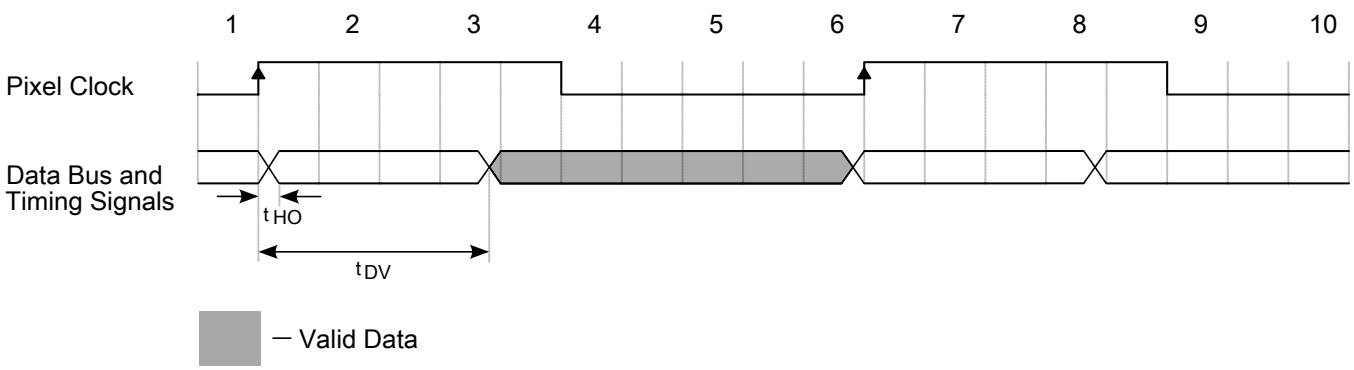

Figure 38. TCON TTL timing diagram

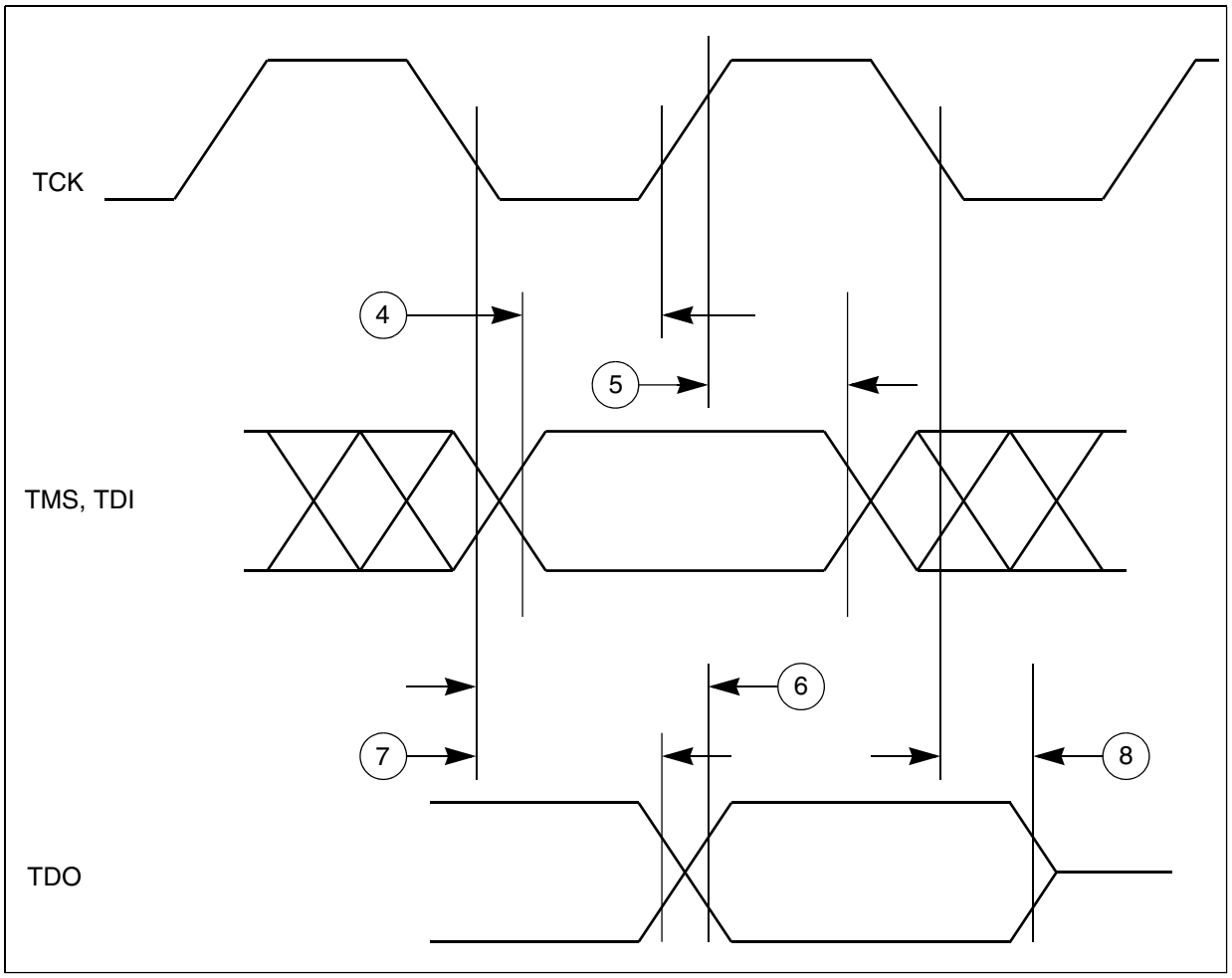

Figure 40. JTAG test access port timing

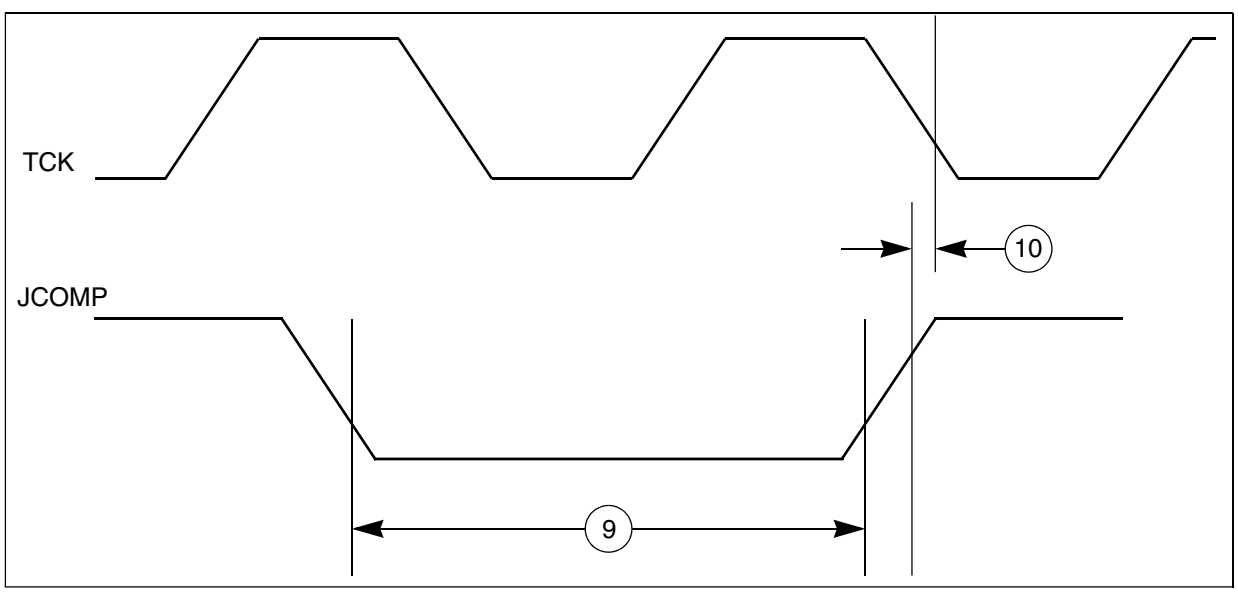

Figure 41. JTAG JCOMP timing

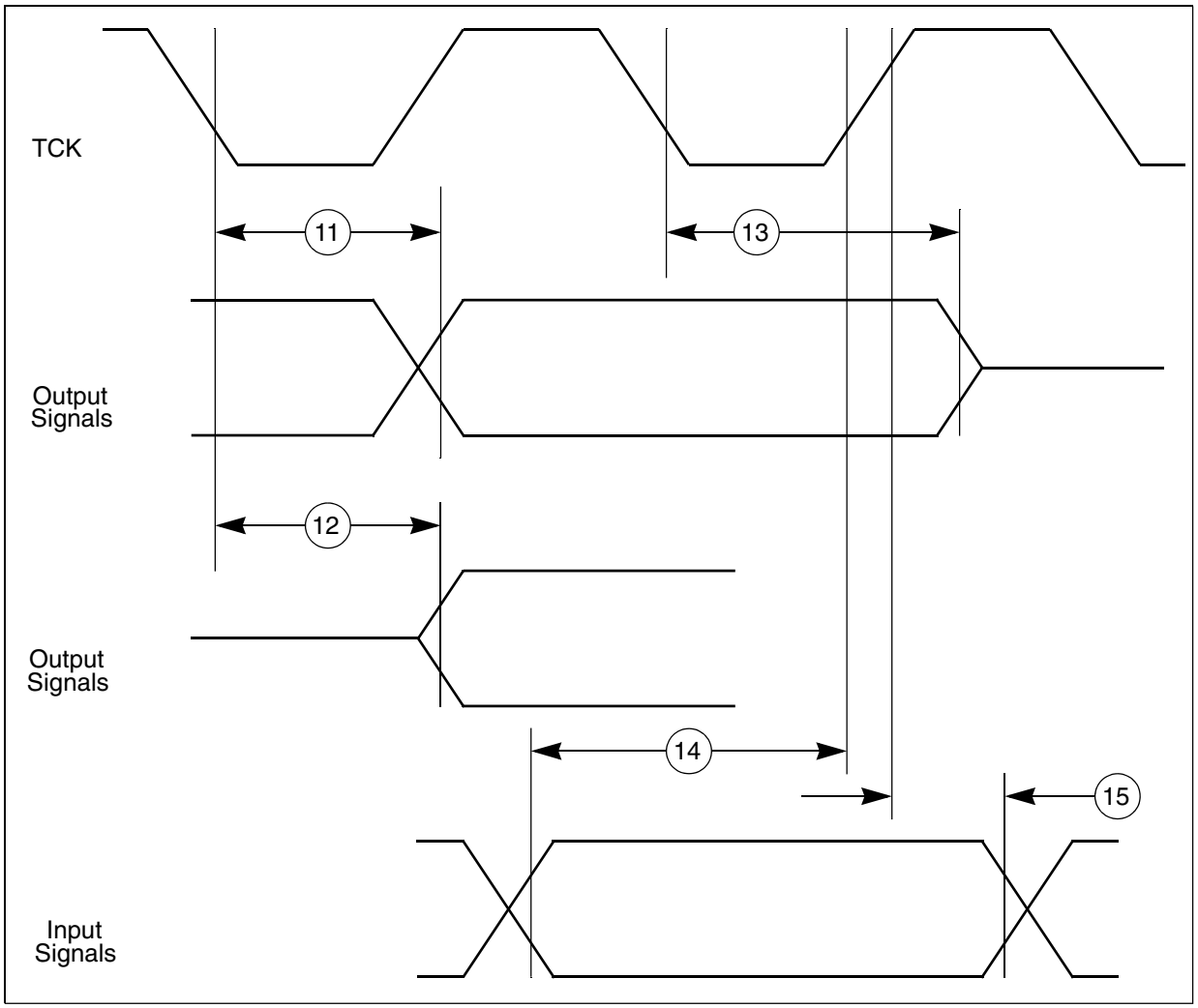

Figure 42. JTAG boundary scan timing

6.7.2 Debug trace timing specifications

Table 62. Debug trace operating behaviors

Symbol	Description	Min.	Max.	Unit
T_{cyc}	Clock period	40		MHz
T_{wl}	Low pulse width	2	—	ns
T_{wh}	High pulse width	2	—	ns
t_{DV}	Data output valid	7.5	—	ns
t_{HO}	Data output hold	0.5	—	ns

These values applies when IRQ pins are configured for rising edge or falling edge events, but not both.

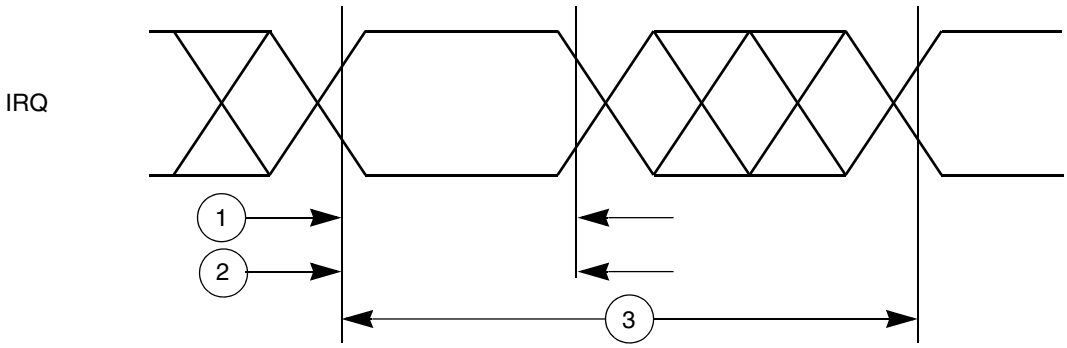

Figure 45. External interrupt timing

7 Thermal attributes

7.1 Thermal attributes

Board type	Symbol	Description	208LQFP	Unit	Notes
Single-layer (1s)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	19.1	°C/W	1,2
Four-layer (2s2p)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	16.4	°C/W	1,2,3
Single-layer (1s)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./ min. air speed)	12.4	°C/W	1,3
Four-layer (2s2p)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./ min. air speed)	12.4	°C/W	1,3
—	$R_{\theta JB}$	Thermal resistance, junction to board	7.4	°C/W	4
—	$R_{\theta JC}$	Thermal resistance, junction to case	5.3	°C/W	5
—	Ψ_{JT}	Thermal characterization parameter, junction to package top	0.2	°C/W	6

Table continues on the next page...