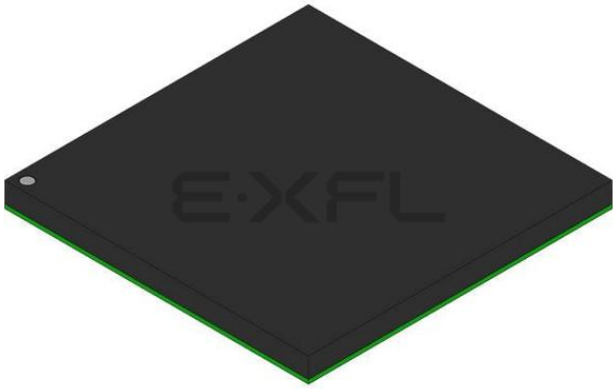

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Details	
Product Status	Active
Core Processor	ARM® Cortex®-A5/M4/M0+
Core Size	32-Bit Tri-Core
Speed	80MHz, 160MHz, 320MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, LINbus, SPI
Peripherals	DMA, LCD, LVD/HVD, POR, PWM, WDT
Number of I/O	-
Program Memory Size	4MB (4M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2.3M x 8
Voltage - Supply (Vcc/Vdd)	3.15V ~ 5.5V
Data Converters	A/D 24x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	516-BGA
Supplier Device Package	516-MAPBGA (27x27)
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- Graphics interfaces
  - Vivante GC355 GPU supporting OpenVG 1.1
  - 2 x 2D-ACE Display Controllers (with inline Head-Up-Display warping)
  - Digital RGB, TCON_0 (RSDS), TCON_1 and OpenLDI/LVDS output options
  - Digital Video Input (VIU4)
  - RLE Decoder for memory-memory decompression
  - 40x4 segment LCD driver, reconfigurable as 38x6 or 36x8
- Cluster peripherals
  - Sound Generator Module (SGM)
  - 6 Stepper Motor Drivers with Stepper Stall Detect
- Communication
  - Ethernet 10/100 + AVB (ENET)
  - MLB50
  - FlexCAN x 3
  - DSPI x 5
  - LINFlexD x 3 (1 x Master/Slave, 2 x Master only)
  - I2C x 2
- eDMA controller with multiple transfer request sources using DMAMUX
- Boot Assist Flash (BAF) supports internal flash programming

1. All monitors that are active at power up will gate the power up recovery and prevent exit from POWERUP phase until the minimum level is crossed. These monitors can in some cases be masked during normal device operation, but when active will always generate a destructive reset.

4.5 Power consumption

The following table shows the power consumption for the device in the various modes of operation.

Table 6. Power consumption

Mode	Configuration	Typ	Max	Unit
Run Mode	CA5 320 MHz, CM4 160 MHz, DDR2 320 MHz, Dual Display (516 BGA)	800	1500	mA
Run Mode	CA5 320 MHz, CM4 160 MHz, SDR 160 MHz, Single Display (208 QFP)	600	1200	mA
IOP Run Mode	CM0+ 16 MHz, PD1/0 domains powered, remainder of device power gated off.	3[1]	35	mA
IOP Stop Mode	CM0+ halted, PD1/0 domains powered, all module enabled and LCD running in IOP domain, remainder of device power gated off.	0.25[2]	20	mA
Stop Mode	Cores halted, Device fully powered.	240	700 [3]	mA
Standby Mode[4, 5]	ARTC/32 KHz + 32 KB SRAM powered	50 (25 °C)	70 (25 °C)	µA
		500 (55 °C)	900 (55 °C)	
		1500 (85 °C)	2500 (85 °C)	
		2000 (105 °C)	4000 (105 °C)	
	ARTC/32 KHz + 8 KB SRAM powered	45 (25 °C)	65 (25 °C)	µA
		500 (55 °C)	900 (55 °C)	
		1500 (85 °C)	2500 (85 °C)	
		2000 (105 °C)	4000 (105 °C)	

1. IOP_Run typical is measured at 25ºC.
2. IOP_Stop typical is measured at 25ºC.
3. There could be 10% variation based on the characterization.
4. Weak pull functionality provided in I/O pads must be used to configure I/Os in a known state (that does not cause contention with external connection on the pin) to avoid floating input to cause crow-bar currents and hence increased leakage during low power modes.
5. During STANDBY/IOP modes, it is recommended to keep V_{DDE_A}, V_{DDEH_ADC}, $V_{DDA}$and V_{DDA_REF} powered to their respective functional levels to obtain best power performance of the device. All other supplies are recommended be kept unpowered in these low power modes.

1. Slew rate control modes
2. Input slope = 2 ns

5.2 DC electrical specifications @ 3.3 V range

Table 9. DC electrical specifications @ 3.3 V range

Symbol	Parameter	Value		Unit
		Min	Max	
Vdde	I/O Supply Voltage	3.15	3.63	V
V_{ih}	CMOS Input Buffer High Voltage (with hysteresis disabled)	0.55 x Vdde	Vdde + 0.3	V
V_{il}	CMOS Input Buffer Low Voltage (with hysteresis disabled)	Vss – 0.3	0.40 x Vdde	V
V_{ih_hys}	CMOS Input Buffer High Voltage (with hysteresis enabled)	0.65 x Vdde	Vdde + 0.3	V
V_{il_hys}	CMOS Input Buffer Low Voltage (with hysteresis enabled)	Vss – 0.3	0.35 x Vdde	V
V_{hys}	CMOS Input Buffer Hysteresis	0.1 x Vdde		V
Pull_Ioh_vil_hys	Weak Pullup Current measured when pad = 0.35 x Vdde	25	80	µA
Pull_Ioh_vih_hys	Weak Pulldown Current measured when pad = 0.65 x Vdde	25	80	µA
Iinact_d	Digital Pad Input Leakage Current (weak pull inactive)	–2.5	2.5	µA
V_{oh}	Output High Voltage[1]	0.8 x Vdde	—	V
V_{ol}	Output Low Voltage[2]	—	0.2 x Vdde	V
V_{ih_ttl}	TTL High Level Input Voltage	1.8		V
V_{il_ttl}	TTL Low Level Input Voltage		0.6	V
V_{hyst_ttl}	TTL Input Hysteresis Voltage	0.25		V
V_{ih_auto}	Automotive High Level Input Voltage	0.75 x Vdde	Vdde + 0.3	V
V_{il_auto}[3]	Automotive Low Level Input Voltage	–0.3	0.35 × Vdde	V
V_{hyst_auto}	Automotive Input Hysteresis Voltage	0.11 x Vdde		V

1. Measured when pad is sourcing 2 mA.
2. Measured when pad is sinking 2 mA.
3. Auto levels are applicable to the ‘input only' channels (CH0-7) of the ADC pins

Table 13. SSTL_18 Class II 1.8 V DDR2 DC specifications (continued)

Symbol	Parameter	Condition	Min	Typ	Max	Unit	Notes	SpecID
$I_{oh(dc)}$	Output min source dc current	$V_{out} = V_{oh}$	–12.86	—	—	mA	JESD8-15 A V_{DDE_DDR} = 1.7V Voh = 1.42V	A5.25
$I_{ol(dc)}$	Output min sink dc current	$V_{out}= V_{ol}$	12.86	—	—	mA	JESD8-15 A V_{DDE_DDR} = 1.7 V Vol = 0.28 V	A5.26

Table 14. Current-draw Characteristics for DDR_VREF

Symbol	Parameter	Min	Max	Unit
DDR_VREF	Current-draw characteristics for DDR_VREF	-	5	mA

5.6 SMC pads IO specifications

5.6.1 SMC 5V pads IO specifications

NOTE

In Table 15, Table 16, "V_{DDE}" is the V_{DDM_SMD} supply

5.6.1.1 SMC 5V pads IO DC specifications

Table 15. SMC 5V IO DC specifications(4.5V<vdde<5.5V)

Symbol	Characteristic	Min	Typ	Max	Unit
V_{il}	Low level input voltage	–0.3		0.35 × vdde	V
V_{ih}	High level input voltage	0.65 × vdde		vdde + 0.3	V
V_{hyst}	Schmitt trigger hysteresis	0.1 × vdde			V
I_{pu}	Internal pull up device current ($V_{in}=V_{il}$)	–130			µA
I_{pu}	Internal pull up device current ($V_{in}=V_{ih}$)			–10	µA
I_{pd}	Internal pull down device current ($V_{in}=V_{il}$)	10			µA
I_{pd}	Internal pull down device current ($V_{in}=V_{ih}$)			130	µA
I_{in}	Input leakage current (ipp_pue=0)	–2.5		2.5	µA
V_{ol}	Low level output voltage (I_{ol}=+20 mA)			0.32	V

Table continues on the next page...

Table 15. SMC 5V IO DC specifications(4.5V<vdde<5.5V) (continued)

Symbol	Characteristic	Min	Typ	Max	Unit
V_{oh}	High level output voltage (I_{oh}=-20 mA)	vdde – 0.32			V
V_{sum}	Vsum (| Vol | + | Voh |) (I_{ol}=+40 mA and I_{oh}=-40 mA)			1.0	V
V_{oh} delta / V_{ol} delta	Delta V_{oh} across one motor segment and Delta V_{ol} across one motor segment	–50		50	mV
R_{dsonh}	Pad drive active high impedance (test load I_{oh} = 30 mA)	4		13	Ω
R_{dsonl}	Pad drive active low impedance (test load I_{ol} = 30 mA)	2.75		9	Ω

5.6.1.2 SMC 5V pads IO AC specifications

Table 16. SMC 5V IO functional pad AC specifications (4.5V<vdde<5.5V)

Name	Symbol	Symbol	Rise/Fall Edge (ns)		Drive Load (pF)	Drive/Slew Rate Select
			Min	Max		ipp_sre_lv
CMOS input				0.5/0.5	0.5	NA

5.6.2 SMC 3.3 V pads IO specifications

NOTE

In Table 17, Table 18, the "V_{DDE}" refers to the V_{DDM_SMD} supply.

5.6.2.1 SMC 3.3 V pads IO DC specifications

Table 17. SMC 3.3 V pads IO DC specifications (3.0V<vdde<3.6V)

Symbol	Characteristic	Min	Typ	Max	Unit
V_{il}	Low level input voltage	-0.3		0.35 × vdde	V
V_{ih}	High level input voltage	0.65 × vdde		vdde + 0.3	V
V_{hyst}	Schmitt trigger hysteresis	0.1 × vdde			V
I_{pu}	Internal pull up device current (V_{in}=V_{il})	-130			µA
I_{pu}	Internal pull up device current (V_{in}=V_{ih})			-10	µA
I_{pd}	Internal pull down device current (V_{in}=V_{il})	10			µA

Table continues on the next page...

Table 21. Functional reset pad electrical specifications (continued)

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
V_{DD_POR}	Minimum supply for strong pull-down activation	—	—	—	1.2	V
I_{OL_R}	Strong pull-down current	Device under power-on reset $V_{DDE\_A}=V_{DD\_POR}$ V_{OL} = 0.35 x V_{DDE_A}	0.2	—	—	mA
W_{FRST}	$\overline{\text{RESET}}$ input filtered pulse	—	—	—	500	ns
W_{NFRST}	$\overline{\text{RESET}}$ input not filtered pulse	—	2000	—	—	ns
$\lvert I_{WPU} \rvert$	Weak pull-up current absolute value	RESET pin $V_{IN} = V_{DD}$	23	—	82	µA

5.10 PORST electrical specifications

Table 22. PORST electrical specifications

Symbol	Parameter	Value			Unit
		Min	Typ	Max	
W_{FPORST}	$\overline{\text{PORST}}$ input filtered pulse	—	—	200	ns
$W_{NFPORST}$	$\overline{\text{PORST}}$ input not filtered pulse	1000	—	—	ns
V_{IH}	Input high level	—	0.65 x V_{DDE_A}	—	V
V_{IL}	Input low level	—	0.35 x V_{DDE_A}	—	V

6 Peripheral operating requirements and behaviors

6.1 Analog modules

6.1.1 ADC electrical specifications

The device provides a 12-bit Successive Approximation Register (SAR) Analog-to-Digital Converter.

Table 24. Comparator and 6-bit DAC electrical specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit
	• CR0[HYSTCTR] = 10 • CR0[HYSTCTR] = 11	—	60	105	mV
t_{DHS}	Propagation Delay, High Speed Mode (Full Swing) [1, 3]	—	—	250	ns
t_{DLS}	Propagation Delay, Low power Mode (Full Swing) [1, 3]	—	5	14	µs
	Analog comparator initialization delay, High speed mode[4]	—	4		µs
	Analog comparator initialization delay, Low speed mode [4]	—	100		µs
I_{DAC6b}	6-bit DAC current adder (when enabled)				
	3.3V Reference Voltage	—	6	9	µA
INL	6-bit DAC integral non-linearity	–1	—	1	LSB[5]
DNL	6-bit DAC differential non-linearity	–0.8	—	0.8	LSB

1. Measured with hysteresis mode of 00
2. Typical hysteresis is measured with input voltage range limited to 0.6 to $V_{DD\_HV\_A}$-0.6V
3. Full swing = VIH, VIL
4. Comparator initialization delay is defined as the time between software writes to change control inputs (Writes to DACEN, VRSEL, PSEL, MSEL, VOSEL) and the comparator output settling to a stable level.
5. 1 LSB = $V_{reference}$/64

6.2 Clocks and PLL interfaces modules

6.2.1 Fast Oscillator (FXOSC) electrical specifications

This device provides a driver for oscillator in pierce configuration with amplitude control. Controlling the amplitude allows a more sinusoidal oscillation, reducing in this way the EMI. Other benefits arises by reducing the power consumption. This Loop Controlled Pierce (LCP mode) requires good practices to reduce the stray capacitance of traces between crystal and MCU.

An operation in Full Swing Pierce (FSP mode), implemented by an inverter is also available in case of parasitic capacitances and cannot be reduced by using crystal with high equivalent series resistance. For this mode, a special care needs to be taken regarding the serial resistance used to avoid the crystal overdrive.

Other two modes called External (EXT Wave) and disable (OFF mode) are provided. For EXT Wave, the drive is disabled and an external source of clock within CMOS level based in analog oscillator supply can be used. When OFF, EXTAL is pulled down by 240 Kohms resistor and the feedback resistor remains active connecting XTAL through EXTAL by 1M resistor.

Table 31. Percentage of sample exceeding specified value of jitter

N	Percentage of samples exceeding specified value of jitter (%)
1	31.73
2	4.55
3	0.27
4	6.30 × 1e-03
5	5.63 × 1e-05
6	2.00 × 1e-07
7	2.82 × 1e-10

6.3 Memory interfaces

6.3.1 Flash memory specifications

NOTE

Flash specs defined in this section at 150°C are also valid for the maximum temperature specifications of the device.

6.3.1.1 Flash memory program and erase specifications

NOTE

All timing, voltage, and current numbers specified in this section are defined for a single embedded flash memory within an SoC, and represent average currents for given supplies and operations.

Table 32 shows the estimated Program/Erase times.

Table 32. Flash memory program and erase specifications

Symbol	Characteristic[1]	Typ[2]	Factory Programming[3, 4]		Field Update			Unit
			Initial Max	Initial Max, Full Temp	Typical End of Life[5]	Lifetime Max[6]		
			20°C ≤T_A ≤30°C	-40°C ≤T_J ≤150°C	-40°C ≤T_J ≤150°C	≤ 1,000 cycles	≤ 250,000 cycles	
t_{dwpgm}	Doubleword (64 bits) program time	43	100	150	55	500		µs
t_{ppgm}	Page (256 bits) program time	73	200	300	108	500		µs

Table continues on the next page...

Table 32. Flash memory program and erase specifications (continued)

Symbol	Characteristic[1]	Typ[2]	Factory Programming[3, 4]		Field Update			Unit
			Initial Max	Initial Max, Full Temp	Typical End of Life[5]	Lifetime Max[6]		
			20°C ≤T_A ≤30°C	-40°C ≤T_J ≤150°C	-40°C ≤T_J ≤150°C	≤ 1,000 cycles	≤ 250,000 cycles	
t_{qppgn}	Quad-page (1024 bits) program time	268	800	1,200	396	2,000		µs
t_{16kers}	16 KB Block erase time	168	290	320	250	1,000		ms
t_{16kpgn}	16 KB Block program time	34	45	50	40	1,000		ms
t_{32kers}	32 KB Block erase time	217	360	390	310	1,200		ms
t_{32kpgm}	32 KB Block program time	69	100	110	90	1,200		ms
t_{64kers}	64 KB Block erase time	315	490	590	420	1,600		ms
t_{64kpgm}	64 KB Block program time	138	180	210	170	1,600		ms
$t_{256kers}$	256 KB Block erase time	884	1,520	2,030	1,080	4,000	—	ms
$t_{256kpgm}$	256 KB Block program time	552	720	880	650	4,000	—	ms

1. Program times are actual hardware programming times and do not include software overhead. Block program times assume quad-page programming.
2. Typical program and erase times represent the median performance and assume nominal supply values and operation at 25 °C. Typical program and erase times may be used for throughput calculations.
3. Conditions: ≤ 150 cycles, nominal voltage.
4. Plant Programing times provide guidance for timeout limits used in the factory.
5. Typical End of Life program and erase times represent the median performance and assume nominal supply values. Typical End of Life program and erase values may be used for throughput calculations.
6. Conditions: -40°C ≤ T_J ≤ 150°C, full spec voltage.

6.3.1.2 Flash memory Array Integrity and Margin Read specifications

Table 33. Flash memory Array Integrity and Margin Read specifications

Symbol	Characteristic	Min	Typical	Max[1]	Units[2]
$t_{ai16kseq}$	Array Integrity time for sequential sequence on 16KB block.	—	—	512 x Tperiod x Nread	—
$t_{ai32kseq}$	Array Integrity time for sequential sequence on 32KB block.	—	—	1024 x Tperiod x Nread	—
$t_{ai64kseq}$	Array Integrity time for sequential sequence on 64KB block.	—	—	2048 x Tperiod x Nread	—
tai256kseq	Array Integrity time for sequential sequence on 256KB block.	—	—	8192 x Tperiod x Nread	—
$t_{mr16kseq}$	Margin Read time for sequential sequence on 16KB block.	73.81	—	110.7	µs
$t_{mr32kseq}$	Margin Read time for sequential sequence on 32KB block.	128.43	—	192.6	µs

Table continues on the next page...

Table 42. QuadSPI output timing (DDR mode) specifications (continued)

Symbol	Parameter	Value		Unit
		Min	Max	
T_{csh}	Chip select output hold time	-1	-	ns

6.3.2.3 HyperFlash mode

NOTE

In HyperFlash mode, the read/write maximum frequency is 90 MHz.

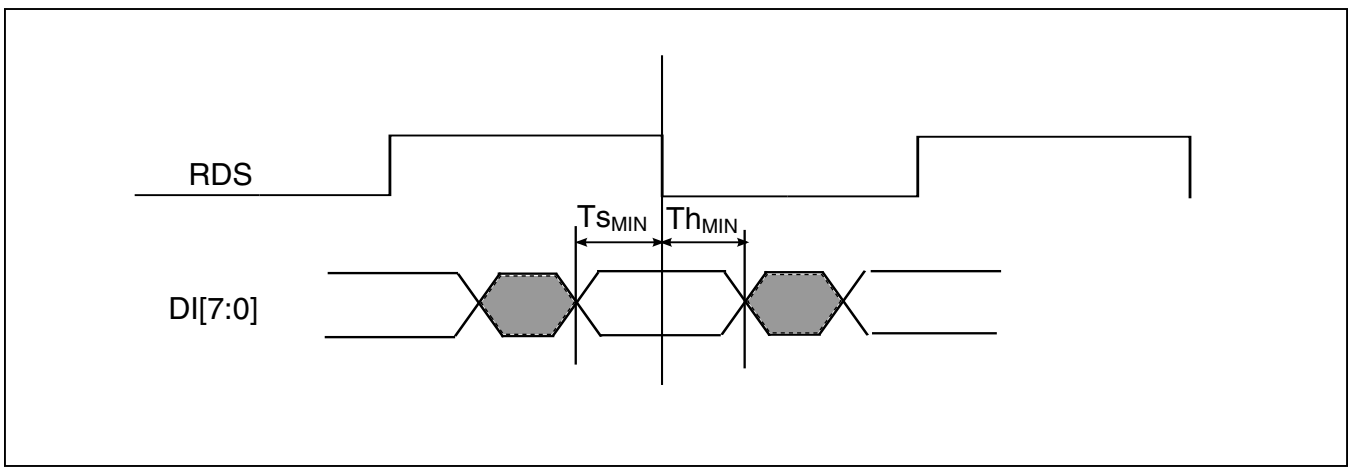

Figure 15. QuadSPI input timing (Hyperflash mode) diagram

Table 43. QuadSPI input timing (Hyperflash mode) specifications

Symbol	Parameter	Value		Unit	Configurations
		Min	Max		
Tis	Setup time for incoming data	2	-	ns	Refer Table 37
Tih	Hold time for incoming data	2	-	ns	

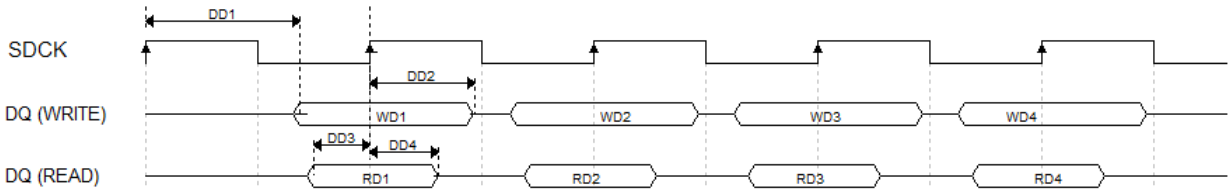

Figure 17. SDR (@ 160 MHz and @ 80 MHz) AC read and write timings

6.3.3.1 SDR DC specifications

The SDR DC specifications are same as pad_fc_hv specs described in this document.

6.3.4 DDR2 SDRAM AC specifications

NOTE

DDR2-800 (-25E speed grade) is the lowest speed grade supported. If self-refresh mechanism needs to be supported, an external pull-down resistance needs to be connected to the DDR CKE pin.

NOTE

Specified values in the table are at recommended operating conditions with V_{DDE_DDR} of 1.8±5.5%

Table 47. DDR2 SDRAM timing specifications[1, 2, 3, 4, 5]

ID	Symbol	Parameter	Min	Typ	Max	Unit
—	F	Frequency of operation (Clock Period)	—	—	320	MHz
—	V_{IX-AC}	MCK AC differential crosspoint voltage	0.5 × V_{DDE_DDR} — 0.175	—	0.5 × V_{DDE_DDR} + 0.175	V
DD1	t_{DDR_CLK}	Clock period	3.125	—	—	ns
DD2	t_{DDR_CLKH}	High pulse width[6]	0.47	—	0.53	tCK
DD3	t_{DDR_CLKL}	Low pulse width	0.47	—	0.53	tCK
DD4	t_{CMS}	Address/Command Output Setup	0.5 × t_{DDR_CLK}–0.75	—	—	ns
DD5	t_{CMH}	Address/Command Output Hold	0.5 × t_{DDR_CLK}–0.75	—	—	ns
DD6	t_{DQSS}	First DQS latching transition to associated clock edge	-0.18 × t_{DDR_CLK}	—	0.18 × t_{DDR_CLK}	ns

Table continues on the next page...

6.5 Display modules

6.5.1 LCD driver electrical specifications

NOTE

When using the LCD segment display module in the 208LQFP package options the V_{DDE_B} and V_{DDE_SDR} supply pins should be shorted together if LCD signal pins are used in both I/O supply domains.

Table 54. LCD driver specifications

Symbol	Parameter	Value[1]			Unit
		Min	Typ	Max	
$Z_{BP/FP}$	LCD output impedance (BP[n-1:0], FP[m-1:0]) for output levels VLCD, VSS	-	-	10	kΩ
$I_{BP/FP}$	LCD output current (BP[n-1:0], FP[m-1:0]) for outputs charge/discharge voltage levels VLCD2/3, VLCD1/2, VLCD1/3) [2,3]	-	2-180	-	µA
Offset	Offset of outputs with capacitive load	-	-	50 [4]	mV

1. VDD = 5.0 V ± 10%, TA = –40 to 105 °C, unless otherwise specified.
2. Outputs measured one at a time, low impedance voltage source connected to the VLCD pin.
3. With PWR = 0-3, BSTEN = 0-1, BSTAO = 0-1.
4. 50 mV offset is only guaranteed across temperature with BSTEN=1 / BSTAO=1 up to 85ºC.

6.5.2 2D-ACE electrical specifications

6.5.2.1 Interface to TFT LCD Panels (2D-ACE)

The following figure depicts the LCD interface timing for a generic active matrix color TFT panel. In this figure signals are shown with positive polarity. The sequence of events for active matrix interface timing is:

- PCLK latches data into the panel on its positive edge (when positive polarity is selected). In active mode, PCLK runs continuously. This signal frequency could be from 5 to 80 MHz depending on the panel type.
- HSYNC causes the panel to start a new line. It always encompasses at least one PCLK pulse.
- VSYNC causes the panel to start a new frame. It always encompasses at least one HSYNC pulse.
- DE acts like an output enable signal to the LCD panel. This output enables the data to be shifted onto the display. When disabled, the data is invalid and the trace is off.

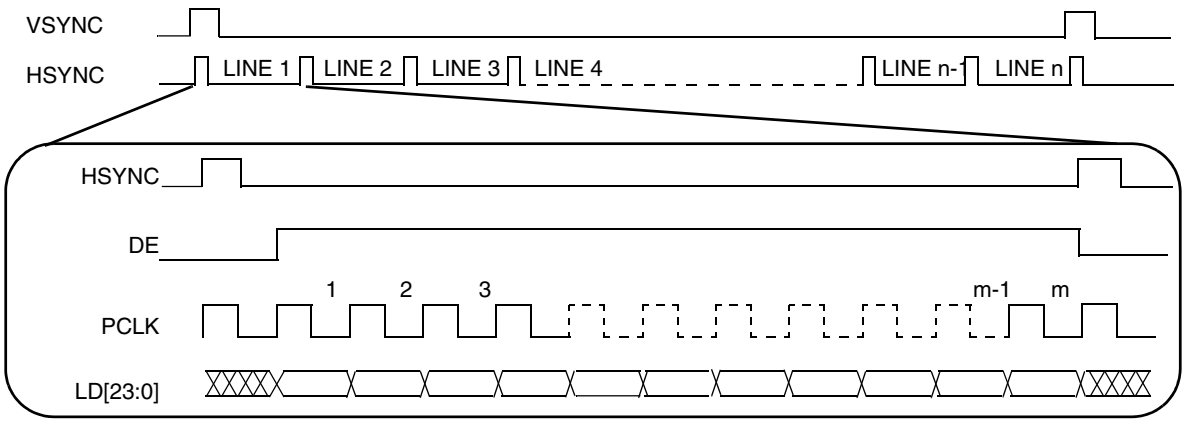

Figure 32. TFT LCD interface timing

6.5.2.2 Interface to TFT LCD Panels—pixel level timings

The following figure depicts depicts the horizontal timing (timing of one line), including both the horizontal sync pulse and data. All parameters shown in the diagram are programmable. This timing diagram corresponds to positive polarity of the PCLK signal (meaning the data and sync signals change on the rising edge) and active-high polarity of the HSYNC, VSYNC and DE signals. The user can select the polarity of the HSYNC and VSYNC signals via the SYN_POL register, whether active-high or active-low. The default is active-high. The DE signal is always active-high.

Pixel clock inversion and a flexible programmable pixel clock delay are also supported. They are programmed via the DCU Clock Confide Register (DCCR) in the system clock module.

The DELTA_X and DELTA_Y parameters are programmed via the DISP_SIZE register. The PW_H, BP_H and FP_H parameters are programmed via the HSYN PARA register. The PW_V, BP_V and FP_V parameters are programmed via the VSYN_PARA register.

6.5.3 Video input unit (VIU4) electrical specifications

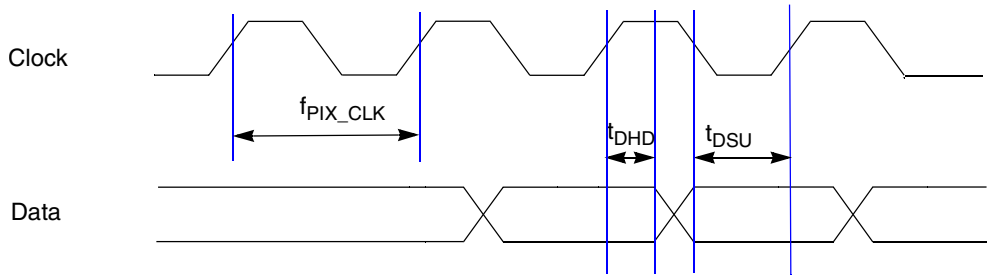

Figure 36. VIU4 timing diagram

Table 57. VIU4 timing parameters

Symbol	Parameter	Min	Typ	Max	Unit
f_{PIX_CK}	VIU4 pixel clock frequency	—	—	53	MHz
t_{DSU}	VIU4 data setup time	4	—	—	ns
t_{DHD}	VIU4 data hold time	1	—	—	ns

6.5.4 TCON electrical specifications

6.5.4.1 TCON RSDS electrical specifications

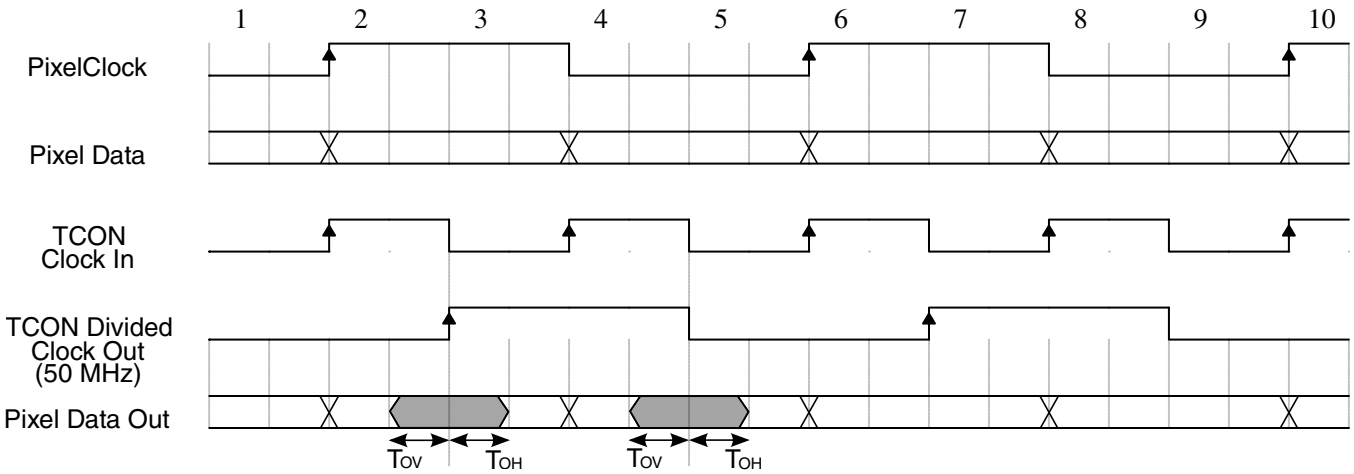

Figure 37. TCON RSDS timing diagram

Table 58. TCON RSDS timing parameters

Symbol	Parameter	Value		Unit
		Min	Max	
T_{OV}	Output data valid time	2	-	ns
T_{OH}	Output data hold time	2	-	ns

6.5.4.2 TCON TTL electrical specifications

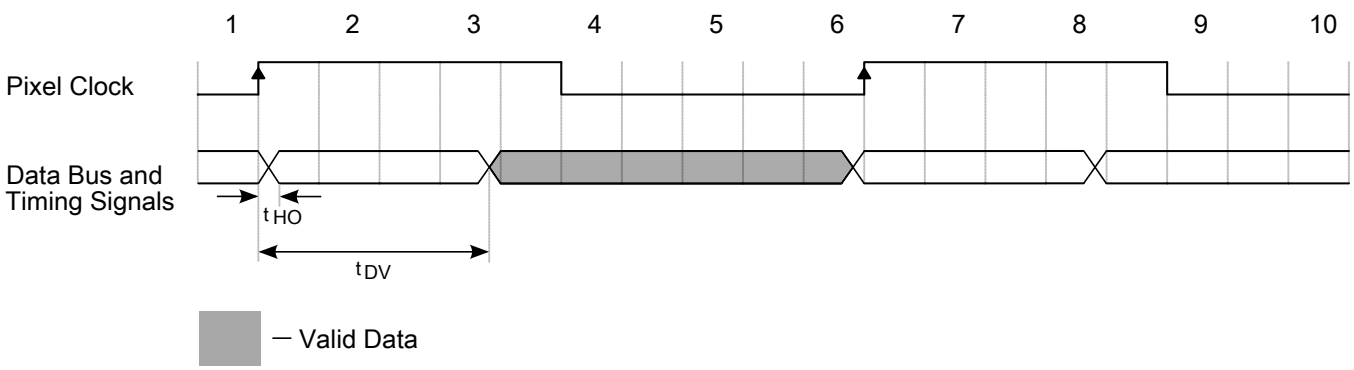

Figure 38. TCON TTL timing diagram

6.7 Debug specifications

6.7.1 JTAG interface timing

Table 61. JTAG pin AC electrical characteristics [1]

#	Symbol	Characteristic	Min	Max	Unit
1	t_{JCYC}	TCK Cycle Time	62.5	—	ns
2	t_{JDC}	TCK Clock Pulse Width	40	60	%
3	$t_{TCKRISE}$	TCK Rise and Fall Times (40% - 70%)	—	3	ns
4	t_{TMSS}, t_{TDIS}	TMS, TDI Data Setup Time	5	—	ns
5	t_{TMSH}, t_{TDIH}	TMS, TDI Data Hold Time	5	—	ns
6	t_{TDOV}	TCK Low to TDO Data Valid	—	20	ns
7	t_{TDOI}	TCK Low to TDO Data Invalid	0	—	ns
8	t_{TDOHZ}	TCK Low to TDO High Impedance	—	15	ns
9	t_{JCMPPW}	JCOMP Assertion Time	100	—	ns
10	t_{JCMPS}	JCOMP Setup Time to TCK Low	40	—	ns
11	t_{BSDV}	TCK Falling Edge to Output Valid	—	600	ns
12	t_{BSDVZ}	TCK Falling Edge to Output Valid out of High Impedance	—	600	ns
13	t_{BSDHZ}	TCK Falling Edge to Output High Impedance	—	600	ns
14	t_{BSDST}	Boundary Scan Input Valid to TCK Rising Edge	15	—	ns
15	t_{BSDHT}	TCK Rising Edge to Boundary Scan Input Invalid	15	—	ns

1. These specifications apply to JTAG boundary scan only.

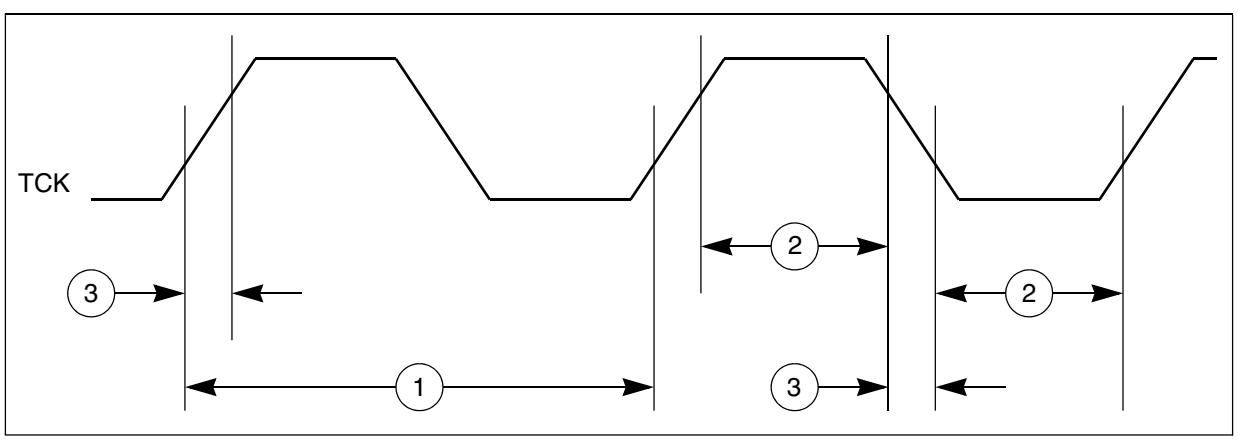

Figure 39. JTAG test clock input timing

Board type	Symbol	Description	208LQFP	Unit	Notes
—	Ψ_{JB}	Thermal characterization parameter, junction to package bottom	0.3	°C/W	7

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance
2. Per SEMI G38-87 and JEDEC JESD51-2 with the single layer board horizontal.
3. Per JEDEC JESD51-6 with the board horizontal.
4. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package. With provided Theta-JB, Max junction temperature must be 125 degreeC.
5. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
6. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2.
7. Thermal characterization parameter indicating the temperature difference between package bottom center and the junction temperature per JEDEC JESD51-12.

Board type	Symbol	Description	516MAPBGA	Unit	Notes
Single-layer (1s)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	23.2	°C/W	1,2
Four-layer (2s2p)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	16.2	°C/W	1,2,3
Single-layer (1s)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./ min. air speed)	15.9	°C/W	1,3
Four-layer (2s2p)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./ min. air speed)	12.2	°C/W	1,3
—	$R_{\theta JB}$	Thermal resistance, junction to board	7.0	°C/W	4
—	$R_{\theta JC}$	Thermal resistance, junction to case	3.7	°C/W	5
—	Ψ_{JT}	Thermal characterization parameter, junction to package top	0.1	°C/W	6
—	Ψ_{JB}	Thermal characterization parameter, junction to package bottom	2.7	°C/W	7

Table 65. Revision History (continued)

Rev. No.	Date	Substantial Changes
		• aded Total unadjusted error with current injection • removed footnote in "Conditions" column • Revised the whole section "Comparator and 6-bit DAC electrical specifications table" • In Fast Oscillator electrical characteristics table, removed FOSC VIH/VIL Min and Max spec and replaced with TYP specs: VIH as 1.84V, VIL as 1.48V . • In Fast internal RC Oscillator electrical specifications table, removed $F_{Untrimmed}$ spec • In Slow internal RC oscillator electrical specifications table, removed F_{oscu} spec. • Revised PLL electrical specifications table • Revised the whole section "Flash Read Wait State and Address Pipeline Control Guidelines" • In LCD driver electrical specifications, added offset, $I_{BP/FP}$, $Z_{BP/FP}$ • In 208LQFP and 516BGA thermal attribute tables, for RθJB updated footnote to add, "With provided Theta-JB, Max junction temperature must be 125 degreeC".
3 (continued)	13 March 2015	• Revised Voltage monitor electrical specifications • Revised Voltage regulator electrical specifications • Revised Power consumption specifications • Revised SSD electrical specifications • Updated SAR-ADC electrical specifications by providing values for both 12-bit and 10-bit modes • Revised QuadSPI, VIU and TCON specifications • Updated Debug trace operating behaviors • Renamed VDD_0P9_DDR to DDR_VREF throughout the document

4	17 Jun 2015	• In "Recommended operating conditions", removed phrase, "V_{DDE_A} (4.5 V to 5.5 V) configuration is only supported in 176 LQFP".
		• In "LVDS pads electrical specifications",
		  • V_{dde} parameter, updated foonote, from "V_{DDE} is the V_{DDE_OLDI} supply" to "V_{DDE} is the V_{DDE_B} supply"
		  • "Differential o/p voltage" parameter, added foonote, "The limit applies to the default drive current".
		  • "Rise/Fall time" parameter, added footnote, "Rise/fall time is assumed to be measured with 20%-80% levels".
		• In "Analog Comparator (CMP) electrical specifications", updated min V_{AIO} from -35 mV to -42 mV and max V_{AIO} from 35 mV to 42 mV.
		• Editorial changes in "Memory Interfaces" section.
		• In "QuadSPI electrical specifications",
		  • updated table title from "QuadSPI delay chain read/write settings" to "QuadSPI read/write settings" and revised the content.
		  • revised notes in the "SDR mode" section.
		  • "QuadSPI input timing (SDR mode)" diagram, renamed SFCK to SCK
		  • "QuadSPI output timing (SDR mode)" diagram, renamed SFCK to SCK
		  • "QuadSPI input timing (SDR mode) specifications" table, added "$F_{SCK"}$ parameter
		  • removed notes in the "DDR mode" section.
		  • added new table, "QuadSPI input timing (DDR mode) specifications with learning".
		  • "QuadSPI output timing (DDR mode) specifications" table, removed "T_{ck} ".
		  • "QuadSPI output timing (Hyperflash mode) specifications" table, renamed "T_{dvMAX}" to "T_{DVO} ".
		• In "SDR AC specifications",
		  • SDR @ 160 MHz AC timing specification table, moved value of t_{SDCK} from Min to Typ
		  • SDR @ 80 MHz AC timing specification table, moved value of t_{SDCK} from Min to Typ
		• In "DDR2 SDRAM AC specifications", added a note, "If self-refresh mechanism needs to be supported, an external pull-down resistance needs to be connected to the DDR CKE pin".
		• Revised "TCON RSDS timing diagram"
		• In "TCON RSDS timing parameters" table, updated T_{DS} to T_{OV} and updated T_H to T_{OH}.

Table continues on the next page...

Table 65. Revision History

Rev. No.	Date	Substantial Changes
		• added note, 'All transitions measured at mid-supply .....with EMC improvement'. • added footnotes for DD1 and DD2 specs of Table 45 and Table 46 that these parameters also apply to command and address buses. • In Table 47, updated DD2 and DD3 values and unit. • In Table 54, in footnote 4, added phrase '..up to 85ºC'. • In Table 55 updated 'Display pixel clock period' (tPCP) value to 12.5 ns. • In Table 60, updated the values for all parameters of SSD_{OFFSET} and added footnote 3.