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Details

Product Status	Obsolete
Core Processor	12V1
Core Size	16-Bit
Speed	25MHz
Connectivity	IrDA, LINbus, SCI, SPI
Peripherals	LVD, POR, PWM, WDT
Number of I/O	16
Program Memory Size	48KB (48K x 8)
Program Memory Type	FLASH
EEPROM Size	512 x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	3.13V ~ 5.5V
Data Converters	A/D 2x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	32-LQFP
Supplier Device Package	32-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/s9s12vr48f2clc

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Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

Device Overview MC9S12VR-Family

- Can be initialized out of reset using option bits located in flash memory
- Clock monitor supervising the correct function of the oscillator

1.4.9 Timer (TIM)

- Up to 4 x 16-bit channels for input capture or output compare
- 16-bit free-running counter with 8-bit precision prescaler

1.4.10 Pulse Width Modulation Module (PWM)

- Up to eight 8-bit channels or reconfigurable four 16-bit channel PWM resolution
 - Programmable period and duty cycle per channel
 - Center-aligned or left-aligned outputs
 - Programmable clock select logic with a wide range of frequencies

1.4.11 LIN physical layer transceiver (LINPHY)

- Compliant with LIN physical layer 2.1
- Standby mode with glitch-filtered wake-up.
- Slew rate selection optimized for the baud rates: 10kBit/s, 20kBit/s and Fast Mode (up to 250kBit/s).
- Selectable pull-up of $30k\Omega$ or $330k\Omega$ (in Shutdown Mode, $330k\Omega$ only)
- Current limitation by LIN Bus pin rising and falling edges
- Over-current protection with transmitter shutdown

1.4.12 Serial Peripheral Interface Module (SPI)

- Configurable 8- or 16-bit data size
- Full-duplex or single-wire bidirectional
- Double-buffered transmit and receive
- Master or slave
- MSB-first or LSB-first shifting
- Serial clock phase and polarity options

1.4.13 Serial Communication Interface Module (SCI)

- Full-duplex or single-wire operation
- Standard mark/space non-return-to-zero (NRZ) format
- Selectable IrDA 1.4 return-to-zero-inverted (RZI) format with programmable pulse widths
- 13-bit baud rate selection
- Programmable character length

1.6.1 Part ID Assignments

The part ID is located in two 8-bit registers PARTIDH and PARTIDL (addresses 0x001A and 0x001B). The read-only value is a unique part ID for each revision of the chip. Table 1-4 shows the assigned part ID number and mask set number.

Device	Mask Set Number	Part ID
MC9S12VR48	1N05E	\$3281
MC9S12VR64	1N05E	\$3281
MC9S12VR48	2N05E ¹	\$3282
MC9S12VR64	2N05E ¹	\$3282

Table 1-4. Assigned Part ID Numbers

¹ The open load detection feature described in **Section 13.4.2 Open Load Detection** is not available on mask set 2N05E

1.7 Signal Description and Device Pinouts

This section describes signals that connect off-chip. It includes a pinout diagram, a table of signal properties, and detailed discussion of signals. It is built from the signal description sections of the individual IP blocks on the device.

1.7.1 Pin Assignment Overview

Table 1-5 provides a summary of which ports are available for 32-pin and 48-pin package option.

Port	32 LQFP	48 LQFP
Port AD	PAD[1:0]	PAD[5:0]
Port E	PE[1:0]	PE[1:0]
Port P	PP1,PP2	PP[5:0]
Port S	PS[3:2]	PS[5:0]
Port T	PT[3:0]	PT[3:0]
Port L	PL[3:0]	PL[3:0]
sum of ports	16	28
I/O power pairs VDDX/VSSX	1/1	2/2

Table 1-5. Port Availability by Package Option

Table 2-16.	PTS	Register	Field	Descriptions

Field	Description
5 PTS	PorT data register port S — General-purpose input/output data, SPI \overline{SS} When not used with the alternative function, the associated pin can be used as general-purpose I/O. In general-purpose output mode the register bit value is driven to the pin. If the associated data direction bit is set to 1, a read returns the value of the port register bit, otherwise the synchronized pin input state is read.
	• The SPI function takes precedence over the general-purpose I/O function if enabled.
4 PTS	PorT data register port S — General-purpose input/output data, SPI SCK When not used with the alternative function, the associated pin can be used as general-purpose I/O. In general-purpose output mode the register bit value is driven to the pin. If the associated data direction bit is set to 1, a read returns the value of the port register bit, otherwise the synchronized pin input state is read.
	• The SPI function takes precedence over the general-purpose I/O function if enabled.
3 PTS	 PorT data register port S — General-purpose input/output data, ECLK, SPI MOSI, routed SCI1, routed PWM, routed ETRIG When not used with the alternative function, the associated pin can be used as general-purpose I/O. In general-purpose output mode the register bit value is driven to the pin. If the associated data direction bit is set to 1, a read returns the value of the port register bit, otherwise the synchronized pin input state is read. The ECLK output function takes precedence over the SPI, routed SCI1 and PWM and the general purpose I/O function if enabled. The SPI function takes precedence over the routed SCI1, routed PWM and the general purpose I/O function if enabled. The routed SCI1 function takes precedence over the PWM and general-purpose I/O function if enabled. The routed PWM function takes precedence over the general-purpose I/O function if enabled.
2 PTS	 PorT data register port S — General-purpose input/output data, SPI MISO, routed SCI1, routed PWM, routed ETRIG When not used with the alternative function, the associated pin can be used as general-purpose I/O. In general-purpose output mode the register bit value is driven to the pin. If the associated data direction bit is set to 1, a read returns the value of the port register bit, otherwise the synchronized pin input state is read. The SPI function takes precedence over the routed SCI1, routed PWM and the general purpose I/O function if enabled. The routed SCI1 function takes precedence over the routed PWM and the general-purpose I/O function if enabled.

2.3.27 Port P Reduced Drive Register (RDRP)



Table 2-27. RDRP Register Field Descriptions

Field	Description
2 RDRP	 Reduced Drive Register port P — Select reduced drive for output pin This bit configures the drive strength of the associated output pin as either full or reduced. If a pin is used as input this bit has no effect. The reduced drive function is independent of which function is being used on a particular pin. 1 Reduced drive selected (approx. 1/10 of the full drive strength) 0 Full drive strength enabled
1-0 RDRP	 Reduced Drive Register port P — Select reduced drive for output pin This bit configures the drive strength of the associated output pin as either full or reduced. If a pin is used as input this bit has no effect. The reduced drive function is independent of which function is being used on a particular pin. 1 Reduced drive selected (approx. 1/5 of the full drive strength) 0 Full drive strength enabled

2.3.28 Port P Pull Device Enable Register (PERP)



¹ Read: Anytime Write: Anytime

Module Interrupt Sources	Local Enable
Port L pin interrupt	PIEL[PIEL3-PIEL0]
Port AD pin interrupt	PIE1AD[PIE1AD5-PIE1AD0]
Port P over-current	PIEP[OCIE]

Table 2-49. PIM Interrupt Sources

2.4.4.1 XIRQ, IRQ Interrupts

The $\overline{\text{XIRQ}}$ pin allows requesting non-maskable interrupts after reset initialization. During reset, the X bit in the condition code register is set and any interrupts are masked until software enables them.

The \overline{IRQ} pin allows requesting asynchronous interrupts. The interrupt input is disabled out of reset. To enable the interrupt the IRQCR[IRQEN] bit must be set and the I bit cleared in the condition code register. The interrupt can be configured for level-sensitive or falling-edge-sensitive triggering. If IRQCR[IRQEN] is cleared while an interrupt is pending, the request will deassert.

Both interrupts are capable to wake-up the device from stop mode. Means for glitch filtering are not provided on these pins.

2.4.4.2 Pin Interrupts and Wakeup

Ports P, L and AD offer pin interrupt capability. The related interrupt enable (PIE) as well as the sensitivity to rising or falling edges (PPS) can be individually configured on per-pin basis. All bits/pins in a port share the same interrupt vector. Interrupts can be used with the pins configured as inputs or outputs.

An interrupt is generated when a bit in the port interrupt flag (PIF) and its corresponding port interrupt enable (PIE) are both set. The pin interrupt feature is also capable to wake up the CPU when it is in stop or wait mode.

A digital filter on each pin prevents short pulses from generating an interrupt. A valid edge on an input is detected if 4 consecutive samples of a passive level are followed by 4 consecutive samples of an active level. Else the sampling logic is restarted.

In run and wait mode the filters are continuously clocked by the bus clock. Pulses with a duration of $t_{PULSE} < n_{P_MASK}/f_{bus}$ are assuredly filtered out while pulses with a duration of $t_{PULSE} > n_{P_PASS}/f_{bus}$ guarantee a pin interrupt.

In stop mode the clock is generated by an RC-oscillator. The minimum pulse length varies over process conditions, temperature and voltage (Figure 2-47). Pulses with a duration of $t_{PULSE} < t_{P_MASK}$ are assuredly filtered out while pulses with a duration of $t_{PULSE} > t_{P_PASS}$ guarantee a wakeup event.

Please refer to the appendix table "Pin Interrupt Characteristics" for pulse length limits.

To maximize current saving the RC oscillator is active only if the following condition is true on any individual pin:

Sample count ≤ 4 (at active or passive level) and interrupt enabled (PIE[x]=1) and interrupt flag not set (PIF[x]=0).

- Enable the external oscillator (OSCE bit)
- Wait for oscillator to start up (UPOSC=1)
- Select the Oscillator Clock (OSCCLK) as Bus Clock (PLLSEL=0).
- The PLLCLK is on and used to qualify the external oscillator clock.

4.1.2.2 Wait Mode

For S12CPMU_UHV Wait Mode is the same as Run Mode.

4.1.2.3 Stop Mode

This mode is entered by executing the CPU STOP instruction.

The voltage regulator is in Reduced Performance Mode (RPM).

NOTE

The voltage regulator output voltage may degrade to a lower value than in Full Performance Mode (FPM), additionally the current sourcing capability is substantially reduced (see also Appendix for VREG electrical parameters). Only clock source ACLK is available and the Power On Reset (POR) circuitry is functional. The Low Voltage Interrupt (LVI) and Low Voltage Reset (LVR) are disabled.

The API is available.

The Phase Locked Loop (PLL) is off.

The Internal Reference Clock (IRC1M) is off.

Core Clock, Bus Clock and BDM Clock are stopped.

Depending on the setting of the PSTP and the OSCE bit, Stop Mode can be differentiated between Full Stop Mode (PSTP = 0 or OSCE=0) and Pseudo Stop Mode (PSTP = 1 and OSCE=1). In addition, the behavior of the COP in each mode will change based on the clocking method selected by COPOSCSEL[1:0].

• Full Stop Mode (PSTP = 0 or OSCE=0)

External oscillator (XOSCLCP) is disabled.

```
— If COPOSCSEL1=0:
```

The COP and RTI counters halt during Full Stop Mode.

After wake-up from Full Stop Mode the Core Clock and Bus Clock are running on PLLCLK (PLLSEL=1). COP and RTI are running on IRCCLK (COPOSCSEL0=0, RTIOSCSEL=0).

— If COPOSCSEL1=1:

The clock for the COP is derived from ACLK (trimmable internal RC-Oscillator clock). During Full Stop Mode the ACLK for the COP can be stopped (COP static) or running (COP active) depending on the setting of bit CSAD. When bit CSAD is set the ACLK clock source for the COP is stopped during Full Stop Mode and COP continues to operate after exit from Full Stop





Figure 4-29. Influence of TCTRIM[4:0] on the Temperature Coefficient

NOTE

The frequency is not necessarily linear with the temperature (in most cases it will not be). The above diagram is meant only to give the direction (positive or negative) of the variation of the TC, relative to the nominal TC.

Setting TCTRIM[4:0] at 0x00000 or 0x10000 does not mean that the temperature coefficient will be zero. These two combinations basically switch off the TC compensation module, which results in the nominal TC of the IRC1M.

6.3.2.7.2 Debug State Control Register 2 (DBGSCR2)

Address: 0x0027



Figure 6-10. Debug State Control Register 2 (DBGSCR2)

Read: If COMRV[1:0] = 01

Write: If COMRV[1:0] = 01 and DBG is not armed.

This register is visible at 0x0027 only with COMRV[1:0] = 01. The state control register 2 selects the targeted next state whilst in State2. The matches refer to the match channels of the comparator match control logic as depicted in Figure 6-1 and described in Section 6.3.2.8.1, "Debug Comparator Control Register (DBGXCTL). Comparators must be enabled by setting the comparator enable bit in the associated DBGXCTL control register.

Table 6-17. DBGSCR2 F	Field Descriptions
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Field	Description
3–0 SC[3:0]	These bits select the targeted next state whilst in State2, based upon the match event.

Table 6-18. State2 — Sequencer Next State Selection

SC[3:0]	Description (Unspecified matches have no effect)
0000	Match0 to State1 Match2 to State3.
0001	Match1 to State3
0010	Match2 to State3
0011	Match1 to State3 Match0 Final State
0100	Match1 to State1 Match2 to State3.
0101	Match2 to Final State
0110	Match2 to State1 Match0 to Final State
0111	Either Match0 or Match1 to Final State
1000	Reserved
1001	Reserved
1010	Reserved
1011	Reserved
1100	Either Match0 or Match1 to Final StateMatch2 to State3
1101	Reserved
1110	Reserved
1111	Either Match0 or Match1 to Final StateMatch2 to State1

The priorities described in Table 6-36 dictate that in the case of simultaneous matches, a match leading to final state has priority followed by the match on the lower channel number (0,1,2)

Table 8-16. ATDSTAT0 Field Descriptions (continued)

Field	Description
3–0 CC[3:0]	Conversion Counter — These 4 read-only bits are the binary value of the conversion counter. The conversion counter points to the result register that will receive the result of the current conversion. E.g. CC3=0, CC2=1, CC1=1, CC0=0 indicates that the result of the current conversion will be in ATD Result Register 6. If in non-FIFO mode (FIFO=0) the conversion counter is initialized to zero at the beginning and end of the conversion sequence. If in FIFO mode (FIFO=1) the register counter is not initialized. The conversion counter wraps around when its maximum value is reached. Aborting a conversion or starting a new conversion clears the conversion counter even if FIFO=1.

8.3.2.8 ATD Compare Enable Register (ATDCMPE)

Writes to this register will abort current conversion sequence.

Read: Anytime

Write: Anytime

Module Base + 0x0008



Figure 8-10. ATD Compare Enable Register (ATDCMPE)

Table 8-17. ATDCMPE Field Descriptions

Field	Description
5–0 CMPE[5:0]	Compare Enable for Conversion Number <i>n</i> (<i>n</i> = 5, 4, 3, 2, 1, 0) of a Sequence (<i>n conversion number, NOT channel number!</i>) — These bits enable automatic compare of conversion results individually for conversions of a sequence. The sense of each comparison is determined by the CMPHT[<i>n</i>] bit in the ATDCMPHT register.
	For each conversion number with CMPE[<i>n</i>]=1 do the following: 1) Write compare value to ATDDR <i>n</i> result register 2) Write compare operator with CMPHT[<i>n</i>] in ATDCPMHT register
	 CCF[<i>n</i>] in ATDSTAT2 register will flag individual success of any comparison. 0 No automatic compare 1 Automatic compare of results for conversion <i>n</i> of a sequence is enabled.

NOTE

Changing the PWM output mode from left aligned to center aligned output (or vice versa) while channels are operating can cause irregularities in the PWM output. It is recommended to program the output mode before enabling the PWM channel.



Figure 9-17. PWM Left Aligned Output Waveform

To calculate the output frequency in left aligned output mode for a particular channel, take the selected clock source frequency for the channel (A, B, SA, or SB) and divide it by the value in the period register for that channel.

- PWMx Frequency = Clock (A, B, SA, or SB) / PWMPERx
- PWMx Duty Cycle (high time as a% of period):
 - Polarity = 0 (PPOLx = 0)
 - Duty Cycle = [(PWMPERx-PWMDTYx)/PWMPERx] * 100%
 - Polarity = 1 (PPOLx = 1)
 - Duty Cycle = [PWMDTYx / PWMPERx] * 100%

As an example of a left aligned output, consider the following case:

Clock Source = E, where E = 10 MHz (100 ns period) PPOLx = 0 PWMPERx = 4 PWMDTYx = 1 PWMx Frequency = 10 MHz/4 = 2.5 MHz PWMx Period = 400 ns PWMx Duty Cycle = 3/4 *100% = 75%

The output waveform generated is shown in Figure 9-18.





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10.3.2.5 SCI Alternative Control Register 2 (SCIACR2)

Module Base + 0x0002



Read: Anytime, if AMAP = 1

Write: Anytime, if AMAP = 1

Table 10-8. SCIACR2 Field Descriptions

Field	Description
2:1 BERRM[1:0]	Bit Error Mode — Those two bits determines the functionality of the bit error detect feature. See Table 10-9.
0 BKDFE	 Break Detect Feature Enable — BKDFE enables the break detect circuitry. 0 Break detect circuit disabled 1 Break detect circuit enabled

Table 10-9. Bit Error Mode Coding

BERRM1	BERRM0	Function
0	0	Bit error detect circuit is disabled
0	1	Receive input sampling occurs during the 9th time tick of a transmitted bit (refer to Figure 10-19)
1	0	Receive input sampling occurs during the 13th time tick of a transmitted bit (refer to Figure 10-19)
1	1	Reserved

10.4.1 Infrared Interface Submodule

This module provides the capability of transmitting narrow pulses to an IR LED and receiving narrow pulses and transforming them to serial bits, which are sent to the SCI. The IrDA physical layer specification defines a half-duplex infrared communication link for exchange data. The full standard includes data rates up to 16 Mbits/s. This design covers only data rates between 2.4 Kbits/s and 115.2 Kbits/s.

The infrared submodule consists of two major blocks: the transmit encoder and the receive decoder. The SCI transmits serial bits of data which are encoded by the infrared submodule to transmit a narrow pulse for every zero bit. No pulse is transmitted for every one bit. When receiving data, the IR pulses should be detected using an IR photo diode and transformed to CMOS levels by the IR receive decoder (external from the MCU). The narrow pulses are then stretched by the infrared submodule to get back to a serial bit stream to be received by the SCI. The polarity of transmitted pulses and expected receive pulses can be inverted so that a direct connection can be made to external IrDA transceiver modules that uses active low pulses.

The infrared submodule receives its clock sources from the SCI. One of these two clocks are selected in the infrared submodule in order to generate either 3/16, 1/16, 1/32 or 1/4 narrow pulses during transmission. The infrared block receives two clock sources from the SCI, R16XCLK and R32XCLK, which are configured to generate the narrow pulse width during transmission. The R16XCLK and R32XCLK are internal clocks with frequencies 16 and 32 times the baud rate respectively. Both R16XCLK and R32XCLK clocks are used for transmitting data. The receive decoder uses only the R16XCLK clock.

10.4.1.1 Infrared Transmit Encoder

The infrared transmit encoder converts serial bits of data from transmit shift register to the TXD pin. A narrow pulse is transmitted for a zero bit and no pulse for a one bit. The narrow pulse is sent in the middle of the bit with a duration of 1/32, 1/16, 3/16 or 1/4 of a bit time. A narrow high pulse is transmitted for a zero bit when TXPOL is cleared, while a narrow low pulse is transmitted for a zero bit when TXPOL is set.

10.4.1.2 Infrared Receive Decoder

The infrared receive block converts data from the RXD pin to the receive shift register. A narrow pulse is expected for each zero received and no pulse is expected for each one received. A narrow high pulse is expected for a zero bit when RXPOL is cleared, while a narrow low pulse is expected for a zero bit when RXPOL is set. This receive decoder meets the edge jitter requirement as defined by the IrDA serial infrared physical layer specification.

10.4.2 LIN Support

This module provides some basic support for the LIN protocol. At first this is a break detect circuitry making it easier for the LIN software to distinguish a break character from an incoming data stream. As a further addition is supports a collision detection at the bit level as well as cancelling pending transmissions.

11.3.2.3 SPI Baud Rate Register (SPIBR)

Module Base +0x0002



Read: Anytime

Write: Anytime; writes to the reserved bits have no effect

Table 11-0. SFIDE FIELD Descriptions

Field	Description
6–4 SPPR[2:0]	SPI Baud Rate Preselection Bits — These bits specify the SPI baud rates as shown in Table 11-7. In master mode, a change of these bits will abort a transmission in progress and force the SPI system into idle state.
2–0 SPR[2:0]	SPI Baud Rate Selection Bits — These bits specify the SPI baud rates as shown in Table 11-7. In master mode, a change of these bits will abort a transmission in progress and force the SPI system into idle state.

The baud rate divisor equation is as follows:

BaudRateDivisor = (SPPR + 1) • 2 ^(SPR + 1)	Ean. 11-1
	/ _	

The baud rate can be calculated with the following equation:

Baud Rate = BusClock / BaudRateDivisor Eqn. 11-2

NOTE

For maximum allowed baud rates, please refer to the SPI Electrical Specification in the Electricals chapter of this data sheet.

Table 11-7. Exami	ple SPI Baud Rate	Selection (25 M	MHz Bus Clock)	(Sheet 1 of 3)

SPPR2	SPPR1	SPPR0	SPR2	SPR1	SPR0	Baud Rate Divisor	Baud Rate
0	0	0	0	0	0	2	12.5 Mbit/s
0	0	0	0	0	1	4	6.25 Mbit/s
0	0	0	0	1	0	8	3.125 Mbit/s
0	0	0	0	1	1	16	1.5625 Mbit/s
0	0	0	1	0	0	32	781.25 kbit/s
0	0	0	1	0	1	64	390.63 kbit/s
0	0	0	1	1	0	128	195.31 kbit/s
0	0	0	1	1	1	256	97.66 kbit/s
0	0	1	0	0	0	4	6.25 Mbit/s

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12.1.3 Block Diagrams



Figure 12-1. TIM16B8CV3 Block Diagram

12.3.2.4 Output Compare 7 Data Register (OC7D)

Module Base + 0x0003

_	7	6	5	4	3	2	1	0
R W	OC7D7	OC7D6	OC7D5	OC7D4	OC7D3	OC7D2	OC7D1	OC7D0
Reset	0	0	0	0	0	0	0	0

Figure 12-9. Output Compare 7 Data Register (OC7D)

¹ This register is available only when channel 7 exists and is reserved if that channel does not exist. Writes to a reserved register have no functional effect. Reads from a reserved register return zeroes.

Read: Anytime

Write: Anytime

Table 12-5. OC7D Field Descriptions

Field	Description
7:0 OC7D[7:0]	Output Compare 7 Data — A channel 7 event, which can be a counter overflow when TTOV[7] is set or a successful output compare on channel 7, can cause bits in the output compare 7 data register to transfer to the timer port data register depending on the output compare 7 mask register.

12.3.2.5 Timer Count Register (TCNT)

Module Base + 0x0004



Figure 12-10. Timer Count Register High (TCNTH)

Module Base + 0x0005



Figure 12-11. Timer Count Register Low (TCNTL)

The 16-bit main timer is an up counter.

A full access for the counter register should take place in one clock cycle. A separate read/write for high byte and low byte will give a different result than accessing them as a word.

Read: Anytime

12.3.2.8 Timer Control Register 1/Timer Control Register 2 (TCTL1/TCTL2)



Read: Anytime

Module Base + 0x0008

Write: Anytime

Table 12-8. TCTL1/TCTL2 Field Descriptions

Note: Bits related to available channels have functional significance. Writing to unavailable bits has no effect. Read from unavailable bits return a zero

Field	Description
7:0 OMx	 Output Mode — These eight pairs of control bits are encoded to specify the output action to be taken as a result of a successful OCx compare. When either OMx or OLx is 1, the pin associated with OCx becomes an output tied to OCx. Note: To enable output action by OMx bits on timer port, the corresponding bit in OC7M should be cleared. For an output line to be driven by an OCx the OCPDx must be cleared.
7:0 OLx	 Output Level — These eight pairs of control bits are encoded to specify the output action to be taken as a result of a successful OCx compare. When either OMx or OLx is 1, the pin associated with OCx becomes an output tied to OCx. Note: To enable output action by OLx bits on timer port, the corresponding bit in OC7M should be cleared. For an output line to be driven by an OCx the OCPDx must be cleared.

Table 12-9. Compare Result Output Action

ОМх	OLx	Action
0	0	No output compare action on the timer output signal
0	1	Toggle OCx output line
1	0	Clear OCx output line to zero
1	1	Set OCx output line to one

12.4.1 Prescaler

The prescaler divides the bus clock by 1, 2, 4, 8, 16, 32, 64 or 128. The prescaler select bits, PR[2:0], select the prescaler divisor. PR[2:0] are in timer system control register 2 (TSCR2).

The prescaler divides the bus clock by a prescalar value. Prescaler select bits PR[2:0] of in timer system control register 2 (TSCR2) are set to define a prescalar value that generates a divide by 1, 2, 4, 8, 16, 32, 64 and 128 when the PRNT bit in TSCR1 is disabled.

By enabling the PRNT bit of the TSCR1 register, the performance of the timer can be enhanced. In this case, it is possible to set additional prescaler settings for the main timer counter in the present timer by using PTPSR[7:0] bits of PTPSR register generating divide by 1, 2, 3, 4,....20, 21, 22, 23,......255, or 256.

12.4.2 Input Capture

Clearing the I/O (input/output) select bit, IOSx, configures channel x as an input capture channel. The input capture function captures the time at which an external event occurs. When an active edge occurs on the pin of an input capture channel, the timer transfers the value in the timer counter into the timer channel registers, TCx.

The minimum pulse width for the input capture input is greater than two bus clocks.

An input capture on channel x sets the CxF flag. The CxI bit enables the CxF flag to generate interrupt requests. Timer module or Pulse Accumulator must stay enabled (TEN bit of TSCR1 or PAEN bit of PACTL register must be set to one) while clearing CxF (writing one to CxF).

12.4.3 Output Compare

Setting the I/O select bit, IOSx, configures channel x when available as an output compare channel. The output compare function can generate a periodic pulse with a programmable polarity, duration, and frequency. When the timer counter reaches the value in the channel registers of an output compare channel, the timer can set, clear, or toggle the channel pin if the corresponding OCPDx bit is set to zero. An output compare on channel x sets the CxF flag. The CxI bit enables the CxF flag to generate interrupt requests. Timer module or Pulse Accumulator must stay enabled (TEN bit of TSCR1 or PAEN bit of PACTL register must be set to one) while clearing CxF (writing one to CxF).

The output mode and level bits, OMx and OLx, select set, clear, toggle on output compare. Clearing both OMx and OLx results in no output compare action on the output compare channel pin.

Setting a force output compare bit, FOCx, causes an output compare on channel x. A forced output compare does not set the channel flag.

The following channel 7 feature is available only when channel 7 exists. A channel 7 event, which can be a counter overflow when TTOV[7] is set or a successful output compare on channel 7, overrides output compares on all other output compare channels. The output compare 7 mask register masks the bits in the output compare 7 data register. The timer counter reset enable bit, TCRE, enables channel 7 output compares to reset the timer counter. A channel 7 output compare can reset the timer counter even if the IOC7 pin is being used as the pulse accumulator input.



Figure 17-9. Flash Error Configuration Register (FERCNFG)

All assigned bits in the FERCNFG register are readable and writable.

Table 17-13. FERCNFG Field Descriptions

Field	Description
1 DFDIE	 Double Bit Fault Detect Interrupt Enable — The DFDIE bit controls interrupt generation when a double bit fault is detected during a Flash block read operation. 0 DFDIF interrupt disabled 1 An interrupt will be requested whenever the DFDIF flag is set (see Section 17.3.2.8)
0 SFDIE	 Single Bit Fault Detect Interrupt Enable — The SFDIE bit controls interrupt generation when a single bit fault is detected during a Flash block read operation. 0 SFDIF interrupt disabled whenever the SFDIF flag is set (see Section 17.3.2.8) 1 An interrupt will be requested whenever the SFDIF flag is set (see Section 17.3.2.8)

17.3.2.7 Flash Status Register (FSTAT)

The FSTAT register reports the operational status of the Flash module.

Offset Module Base + 0x0006

Offset Module Base + 0x0005



Figure 17-10. Flash Status Register (FSTAT)

¹ Reset value can deviate from the value shown if a double bit fault is detected during the reset sequence (see Section 17.6).

CCIF, ACCERR, and FPVIOL bits are readable and writable, MGBUSY and MGSTAT bits are readable but not writable, while remaining bits read 0 and are not writable.

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by the user. The P-Flash protection scheme can be used by applications requiring reprogramming in single chip mode while providing as much protection as possible if reprogramming is not required.

Appendix F IRC Electrical Specifications

Table F-1. IRC electrical characteristics

Num	С	Rating	Symbol	Min	Тур	Max	Unit
1	Ρ	Junction Temperature - 40 to 150 Celsius Internal Reference Frequency, factory trimmed	f _{IRC1M_TRIM}	0.987	1	1.013	MHz