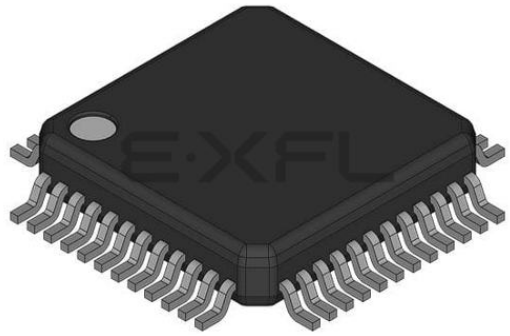

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	12V1
Core Size	16-Bit
Speed	25MHz
Connectivity	IrDA, LINbus, SCI, SPI
Peripherals	LVD, POR, PWM, WDT
Number of I/O	28
Program Memory Size	48KB (48K x 8)
Program Memory Type	FLASH
EEPROM Size	512 x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	3.13V ~ 5.5V
Data Converters	A/D 6x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=s9s12vr48f2clf

- Sun roof modules

1.2 Features

This section describes the key features of the MC9S12VR-Family.

1.2.1 MC9S12VR-Family Member Comparison

Table 1-2 provides a summary of different members of the MC9S12VR-Family and their features. This information is intended to provide an understanding of the range of functionality offered by this microcontroller family.

Table 1-2. MC9S12VR - Family

Feature	MC9S12VR48	MC9S12VR64
CPU	HCS12	
Flash memory (ECC)	48 Kbytes	64 Kbytes
EEPROM (ECC)	512 Bytes	
RAM	2 Kbytes	
LIN physical layer	1	
SPI	1	
SCI	Up to 2	
Timer	4ch x 16-bit	
PWM	8ch x 8-bit or 4ch x 16-bit	
ADC	6 ch x 10-bit available on external pins and four internal channels. see Table 1-13.	
Frequency modulated PLL	Yes	
Internal 1 MHz RC oscillator	Yes	
Autonomous window watchdog	1	
Low-side drivers (protected for inductive loads)	2	
High-side drivers	Up to 2	
High voltage Inputs	4	
General purpose I/Os (5V)	Up to 28	
Direct battery sense pin	Yes	
Supply voltage sense	Yes	
Chip temperature sensor	1 general sensor	

  - Can be initialized out of reset using option bits located in flash memory
- Clock monitor supervising the correct function of the oscillator

1.4.9 Timer (TIM)

- Up to 4 x 16-bit channels for input capture or output compare
- 16-bit free-running counter with 8-bit precision prescaler

1.4.10 Pulse Width Modulation Module (PWM)

- Up to eight 8-bit channels or reconfigurable four 16-bit channel PWM resolution
  - Programmable period and duty cycle per channel
  - Center-aligned or left-aligned outputs
  - Programmable clock select logic with a wide range of frequencies

1.4.11 LIN physical layer transceiver (LINPHY)

- Compliant with LIN physical layer 2.1
- Standby mode with glitch-filtered wake-up.
- Slew rate selection optimized for the baud rates: 10kBit/s, 20kBit/s and Fast Mode (up to 250kBit/s).
- Selectable pull-up of 30kΩ or 330kΩ (in Shutdown Mode, 330kΩ only)
- Current limitation by LIN Bus pin rising and falling edges
- Over-current protection with transmitter shutdown

1.4.12 Serial Peripheral Interface Module (SPI)

- Configurable 8- or 16-bit data size
- Full-duplex or single-wire bidirectional
- Double-buffered transmit and receive
- Master or slave
- MSB-first or LSB-first shifting
- Serial clock phase and polarity options

1.4.13 Serial Communication Interface Module (SCI)

- Full-duplex or single-wire operation
- Standard mark/space non-return-to-zero (NRZ) format
- Selectable IrDA 1.4 return-to-zero-inverted (RZI) format with programmable pulse widths
- 13-bit baud rate selection
- Programmable character length

1.4.17 Low-side drivers (LSDRV)

- 2x low-side drivers targeted for up to approximately 150mA current capability.
- Internal timer or PWM channels can be routed to control the low-side drivers
- Open-load detection
- Over-current protection with shutdown and interrupt
- Active clamp (for driving relays)
- Recirculation detection

1.4.18 High-side drivers (HSDRV)

- 2 High-side drivers targeted for up to approximately 44mA current capability
- Internal timer or PWM channels can be routed to control the high-side drivers
- Open load detection
- Over-current protection with shutdown and interrupt

1.4.19 Background Debug (BDM)

- Background debug module (BDM) with single-wire interface
  - — Non-intrusive memory access commands
  - — Supports in-circuit programming of on-chip nonvolatile memory

1.4.20 Debugger (DBG)

- Trace buffer with depth of 64 entries
- Three comparators (A, B and C)
  - — Access address comparisons with optional data comparisons
  - — Program counter comparisons
  - — Exact address or address range comparisons
- Two types of comparator matches
  - — Tagged This matches just before a specific instruction begins execution
  - — Force This is valid on the first instruction boundary after a match occurs
- Four trace modes
- Four stage state sequencer

1.9 Modes of Operation

The MCU can operate in different modes. These are described in 1.9.1 Chip Configuration Summary.

The MCU can operate in different power modes to facilitate power saving when full system performance is not required. These are described in 1.9.2 Low Power Operation.

Some modules feature a software programmable option to freeze the module status whilst the background debug module is active to facilitate debugging.

1.9.1 Chip Configuration Summary

The different modes and the security state of the MCU affect the debug features (enabled or disabled).

The operating mode out of reset is determined by the state of the MODC signal during reset (see Table 1-8). The MODC bit in the MODE register shows the current operating mode and provides limited mode switching during operation. The state of the MODC signal is latched into this bit on the rising edge of $\overline{\text{RESET}}$.

Table 1-8. Chip Modes

Chip Modes	MODC
Normal single chip	1
Special single chip	0

1.9.1.1 Normal Single-Chip Mode

This mode is intended for normal device operation. The opcode from the on-chip memory is being executed after reset (requires the reset vector to be programmed correctly). The processor program is executed from internal memory.

1.9.1.2 Special Single-Chip Mode

This mode is used for debugging single-chip operation, boot-strapping, or security related operations. The background debug module BDM is active in this mode. The CPU executes a monitor program located in an on-chip ROM. BDM firmware waits for additional serial commands through the BKGD pin.

1.9.2 Low Power Operation

The MC9S12VR-Family has two dynamic-power modes (run and wait) and two static low-power modes stop and pseudo stop). For a detailed description refer to **Section Chapter 4 S12 Clock, Reset and Power Management Unit (S12CPMU_UHV)**.

- Dynamic power mode: Run
  - Run mode is the main full performance operating mode with the entire device clocked. The user can configure the device operating speed through selection of the clock source and the phase locked loop (PLL) frequency. To save power, unused peripherals must not be enabled.

2. Select either a pullup or pulldown device if PER is active.

Table 2-2. Pin Configuration Summary[1]

DDR	PORT PT	PER	PPS[1]	PIE[2]	Function	Pull Device	Interrupt
0	x	0	x	0	Input	Disabled	Disabled
0	x	1	0	0	Input	Pullup	Disabled
0	x	1	1	0	Input	Pulldown	Disabled
0	x	0	0	1	Input	Disabled	Falling edge
0	x	0	1	1	Input	Disabled	Rising edge
0	x	1	0	1	Input	Pullup	Falling edge
0	x	1	1	1	Input	Pulldown	Rising edge
1	0	x	x	0	Output, drive to 0	Disabled	Disabled
1	1	x	x	0	Output, drive to 1	Disabled	Disabled
1	0	x	0	1	Output, drive to 0	Disabled	Falling edge
1	1	x	1	1	Output, drive to 1	Disabled	Rising edge

1 Always “0” on Port E

2 Applicable only on Port P and AD

NOTE

- All register bits in this module are completely synchronous to internal clocks during a register read.
- Figure of port data registers also display the alternative functions if applicable on the related pin as defined in Table 2-1. Names in parentheses denote the availability of the function when using a specific routing option.
- Figures of module routing registers also display the module instance or module channel associated with the related routing bit.

1. Not applicable for Port L. Refer to register descriptions.

Chapter 4
S12 Clock, Reset and Power Management Unit (S12CPMU_UHV)

Revision History

Rev. No. (Item No)	Date (Submitted By)	Sections Affected	Substantial Change(s)
V01.00	22.Dec 10		Initial Version.
V02.00	08. Apr 11	4.1.2.3/4-121 4.1.2.4/4-122 4.1.3/4-123 4.3.1/4-127 4.3.2.6/4-134 4.3.2.18/4-153 4.4.3/4-164 4.4.4/4-165 4.5.2.2/4-170 4.7.2/4-174 Table 4-5 Table 4-14 Table 4-31 Figure 4-1 Figure 4-3 Figure 4-9	Added bit CSAD (COP in Stop Mode ACLK Disable) in register CPMUCLKS. This bit allows halting the COP in Stop Mode (Full or Pseudo) when ACLK is the COP clock source. Description of Stop Modes, Block Diagram, CPMUCLKS register and COP Watchdog feature are updated.
V02.01	21.June 12		Improved signal descriptions of VSUP, VDDA/VSSA, VDDX/VSSX concerning recommended decoupling capacitors.
V02.02	30.July 12		Figure “Startup of clock system after Reset”: Corrected PLL clock frequencies to 12.5Mhz and 25MHz (instead of 16MHz and 32Mhz before)

4.1 Introduction

This specification describes the function of the Clock, Reset and Power Management Unit (S12CPMU_UHV).

- The Pierce oscillator (XOSCLCP) provides a robust, low-noise and low-power external clock source. It is designed for optimal start-up margin with typical crystal oscillators.
- The Voltage regulator (VREGAUTO) operates from the range 6V to 18V. It provides all the required chip internal voltages and voltage monitors.
- The Phase Locked Loop (PLL) provides a highly accurate frequency multiplier with internal filter.
- The Internal Reference Clock (IRC1M) provides a 1MHz internal clock.

4.3.2.2 S12CPMU_UHV Reference Divider Register (CPMUREFDIV)

The CPMUREFDIV register provides a finer granularity for the PLL multiplier steps when using the external oscillator as reference.

0x0035

	7	6	5	4	3	2	1	0
R	REFFRQ[1:0]		0	0	REFDIV[3:0]			
W								
Reset	0	0	0	0	1	1	1	1

Figure 4-5. S12CPMU_UHV Reference Divider Register (CPMUREFDIV)

Read: Anytime

Write: If PROT=0 (CPMUPROT register) and PLLSEL=1 (CPMUCLKS register), then write anytime. Else write has no effect.

NOTE

Write to this register clears the LOCK and UPOSC status bits.

If XOSCLCP is enabled (OSCE=1) $$f_{REF} = \frac{f_{OSC}}{(REFDIV + 1)}$$

If XOSCLCP is disabled (OSCE=0) $$f_{REF} = f_{IRC1M}$$

The REFFRQ[1:0] bits are used to configure the internal PLL filter for optimal stability and lock time. For correct PLL operation the REFFRQ[1:0] bits have to be selected according to the actual REFCLK frequency as shown in Table 4-2.

If IRC1M is selected as REFCLK (OSCE=0) the PLL filter is fixed configured for the 1MHz <= f_{REF} <= 2MHz range. The bits can still be written but will have no effect on the PLL filter configuration.

For OSCE=1, setting the REFFRQ[1:0] bits incorrectly can result in a non functional PLL (no locking and/or insufficient stability).

Table 4-2. Reference Clock Frequency Selection if OSC_LCP is enabled

REFCLK Frequency Ranges (OSCE=1)	REFFRQ[1:0]
1MHz <= f_{REF} <= 2MHz	00
2MHz < f_{REF} <= 6MHz	01
6MHz < f_{REF} <= 12MHz	10
f_{REF} >12MHz	11

Table 4-11. RTI Frequency Divide Rates for RTDEC=1

RTR[3:0]	RTR[6:4] =							
	000 ($1x10^3$)	**001 ($2x10^3$)**	**010 ($5x10^3$)**	**011 ($10x10^3$)**	**100 ($20x10^3$)**	**101 ($50x10^3$)**	**110 ($100x10^3$)**	**111 ($200x10^3$)**
0000 (÷1)	$1x10^3$	$2x10^3$	$5x10^3$	$10x10^3$	$20x10^3$	$50x10^3$	$100x10^3$	$200x10^3$
0001 (÷2)	$2x10^3$	$4x10^3$	$10x10^3$	$20x10^3$	$40x10^3$	$100x10^3$	$200x10^3$	$400x10^3$
0010 (÷3)	$3x10^3$	$6x10^3$	$15x10^3$	$30x10^3$	$60x10^3$	$150x10^3$	$300x10^3$	$600x10^3$
0011 (÷4)	$4x10^3$	$8x10^3$	$20x10^3$	$40x10^3$	$80x10^3$	$200x10^3$	$400x10^3$	$800x10^3$
0100 (÷5)	$5x10^3$	$10x10^3$	$25x10^3$	$50x10^3$	$100x10^3$	$250x10^3$	$500x10^3$	$1x10^6$
0101 (÷6)	$6x10^3$	$12x10^3$	$30x10^3$	$60x10^3$	$120x10^3$	$300x10^3$	$600x10^3$	$1.2x10^6$
0110 (÷7)	$7x10^3$	$14x10^3$	$35x10^3$	$70x10^3$	$140x10^3$	$350x10^3$	$700x10^3$	$1.4x10^6$
0111 (÷8)	$8x10^3$	$16x10^3$	$40x10^3$	$80x10^3$	$160x10^3$	$400x10^3$	$800x10^3$	$1.6x10^6$
1000 (÷9)	$9x10^3$	$18x10^3$	$45x10^3$	$90x10^3$	$180x10^3$	$450x10^3$	$900x10^3$	$1.8x10^6$
1001 (÷10)	$10\ x10^3$	$20x10^3$	$50x10^3$	$100x10^3$	$200x10^3$	$500x10^3$	$1x10^6$	$2x10^6$
1010 (÷11)	$11\ x10^3$	$22x10^3$	$55x10^3$	$110x10^3$	$220x10^3$	$550x10^3$	$1.1x10^6$	$2.2x10^6$
1011 (÷12)	$12x10^3$	$24x10^3$	$60x10^3$	$120x10^3$	$240x10^3$	$600x10^3$	$1.2x10^6$	$2.4x10^6$
1100 (÷13)	$13x10^3$	$26x10^3$	$65x10^3$	$130x10^3$	$260x10^3$	$650x10^3$	$1.3x10^6$	$2.6x10^6$
1101 (÷14)	$14x10^3$	$28x10^3$	$70x10^3$	$140x10^3$	$280x10^3$	$700x10^3$	$1.4x10^6$	$2.8x10^6$
1110 (÷15)	$15x10^3$	$30x10^3$	$75x10^3$	$150x10^3$	$300x10^3$	$750x10^3$	$1.5x10^6$	$3x10^6$
1111 (÷16)	$16x10^3$	$32x10^3$	$80x10^3$	$160x10^3$	$320x10^3$	$800x10^3$	$1.6x10^6$	$3.2x10^6$

6.3.2.8.2 Debug Comparator Address High Register (DBGXAH)

Address: 0x0029

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	Bit 17	Bit 16
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 6-16. Debug Comparator Address High Register (DBGXAH)

The DBGC1_COMRV bits determine which comparator address registers are visible in the 8-byte window from 0x0028 to 0x002F as shown in Section Table 6-24., “Comparator Address Register Visibility

Table 6-24. Comparator Address Register Visibility

COMRV	Visible Comparator
00	DBGAAH, DBGAAM, DBGAAL
01	DBGBAH, DBGBAM, DBGBAL
10	DBGCAH, DBGCAM, DBGCAL
11	None

Read: Anytime. See Table 6-24 for visible register encoding.

Write: If DBG not armed. See Table 6-24 for visible register encoding.

Table 6-25. DBGXAH Field Descriptions

Field	Description
1–0 Bit[17:16]	**Comparator Address High Compare Bits** — The Comparator address high compare bits control whether the selected comparator compares the address bus bits [17:16] to a logic one or logic zero. 0 Compare corresponding address bit to a logic zero 1 Compare corresponding address bit to a logic one

6.3.2.8.3 Debug Comparator Address Mid Register (DBGXAM)

Address: 0x002A

	7	6	5	4	3	2	1	0
R	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
W								
Reset	0	0	0	0	0	0	0	0

Figure 6-17. Debug Comparator Address Mid Register (DBGXAM)

Read: Anytime. See Table 6-24 for visible register encoding.

Write: If DBG not armed. See Table 6-24 for visible register encoding.

data entry may also contain newer data entries in fields 0 and 1. Thus if rollover is indicated by the TBF bit, the line status must be decoded using the INF bits in field3 of that line. If both INF bits are clear then the line contains only entries from before the last rollover.
If INF0=1 then field 0 contains post rollover data but fields 1 and 2 contain pre rollover data.
If INF1=1 then fields 0 and 1 contain post rollover data but field 2 contains pre rollover data.

The pointer is initialized by each aligned write to DBGTBH to point to the oldest data again. This enables an interrupted trace buffer read sequence to be easily restarted from the oldest data entry.

The least significant word of line is read out first. This corresponds to the fields 1 and 0 of Table 6-37. The next word read returns field 2 in the least significant bits [3:0] and “0” for bits [15:4].

Reading the Trace Buffer while the DBG module is armed returns invalid data and no shifting of the RAM pointer occurs.

6.4.5.6 Trace Buffer Reset State

The Trace Buffer contents and DBGCNT bits are not initialized by a system reset. Thus should a system reset occur, the trace session information from immediately before the reset occurred can be read out and the number of valid lines in the trace buffer is indicated by DBGCNT. The internal pointer to the current trace buffer address is initialized by unlocking the trace buffer and points to the oldest valid data even if a reset occurred during the tracing session. To read the trace buffer after a reset, TSOURCE must be set, otherwise the trace buffer reads as all zeroes. Generally debugging occurrences of system resets is best handled using end trigger alignment since the reset may occur before the trace trigger, which in the begin trigger alignment case means no information would be stored in the trace buffer.

The Trace Buffer contents and DBGCNT bits are undefined following a POR.

NOTE

An external pin RESET that occurs simultaneous to a trace buffer entry can, in very seldom cases, lead to either that entry being corrupted or the first entry of the session being corrupted. In such cases the other contents of the trace buffer still contain valid tracing information. The case occurs when the reset assertion coincides with the trace buffer entry clock edge.

6.4.6 Tagging

A tag follows program information as it advances through the instruction queue. When a tagged instruction reaches the head of the queue a tag hit occurs and can initiate a state sequencer transition.

Each comparator control register features a TAG bit, which controls whether the comparator match causes a state sequencer transition immediately or tags the opcode at the matched address. If a comparator is enabled for tagged comparisons, the address stored in the comparator match address registers must be an opcode address.

Using Begin trigger together with tagging, if the tagged instruction is about to be executed then the transition to the next state sequencer state occurs. If the transition is to the Final State, tracing is started. Only upon completion of the tracing session can a breakpoint be generated. Using End alignment, when

Write: Anytime.

Table 12-11. TCTL3/TCTL4 Field Descriptions

Note: Bits related to available channels have functional significance. Writing to unavailable bits has no effect. Read from unavailable bits return a zero.

Field	Description
7:0 EDGnB EDGnA	**Input Capture Edge Control** — These eight pairs of control bits configure the input capture edge detector circuits.

Table 12-12. Edge Detector Circuit Configuration

EDGnB	EDGnA	Configuration
0	0	Capture disabled
0	1	Capture on rising edges only
1	0	Capture on falling edges only
1	1	Capture on any edge (rising or falling)

12.3.2.10 Timer Interrupt Enable Register (TIE)

Module Base + 0x000C

	7	6	5	4	3	2	1	0
R W	C7I	C6I	C5I	C4I	C3I	C2I	C1I	C0I
Reset	0	0	0	0	0	0	0	0

Figure 12-18. Timer Interrupt Enable Register (TIE)

Read: Anytime

Write: Anytime.

Table 12-13. TIE Field Descriptions

Note: Bits related to available channels have functional significance. Writing to unavailable bits has no effect. Read from unavailable bits return a zero

Field	Description
7:0 C7I:C0I	**Input Capture/Output Compare "x" Interrupt Enable —** The bits in TIE correspond bit-for-bit with the bits in the TFLG1 status register. If cleared, the corresponding flag is disabled from causing a hardware interrupt. If set, the corresponding flag is enabled to cause a interrupt.

13.4 Functional Description

13.4.1 General

The HSDRV module provides two high-side drivers able to drive LED or resistive loads. The driver gate can be controlled directly through register bits or alternatively by dedicated timer or PWM channels. See PIM section for routing details.

Both drivers feature open-load and over-current detection described in the following sub-sections.

13.4.2 Open Load Detection

A “High-load resistance Open Load Detection” can be enabled for each driver by setting the corresponding HSEOLx bit (refer to Section 13.3.4, “HSDRV Configuration Register (HSCR)”. This detection will only be executed when the driver is enabled and it is not being driven (HSDRx = 0). To detect an open-load condition a small current I_{HVOLDC} will flow through the load. Then if the driving pin HSx stays at high voltage, which is higher than a threshold set by the internal Schmitt trigger, then an open load will be detected (no load or load >300K under typical power supply) for the corresponding high-side driver and it can be observed that the current in the pin is $I_{HS} < I_{HLROLDC}$.

An open-load condition is flagged with bits HSOL0 and HSOL1 in the HSDRV Status Register (HSSR).

13.4.3 Over-Current Detection

Each high-side driver has an over-current detection while enabled with a current threshold of I_{LIMHSX}.

If over-current is detected the related interrupt flag (HSOCIF1 or HSOCIF0) is set in the HSDRV Interrupt Flag Register (HSIF). As long as the over-current interrupt flag remains set, the related high-side driver gate is turned off to protect the circuit.

NOTE

Although the gate is turned off by the over-current detection, the open-load detection might not be active. Open-load detection is only active if the selected source (e.g. PWM, Timer, HSDRx) for the high-side driver is turned off.

Clearing the related over-current interrupt flag returns back the control of the gate to the selected source in the PIM module.

13.4.4 Interrupts

This section describes the interrupt generated by HSDRV module. The interrupt is only available in CPU run mode. Entering and exiting CPU stop mode has no effect on the interrupt flags.

The HSDRV interrupt vector is named in Table 13-10. Vector addresses and interrupt priorities are defined at MCU level.

14.3.5 Reserved Register

Module Base + 0x0002 Access: User read/write[1]

	7	6	5	4	3	2	1	0
R W	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Reset	x	x	x	x	x	x	x	x
Reset	0	0	0	0	0	0	F	F

After de-assert of System Reset a value is automatically loaded from the Flash Memory

= Unimplemented

Figure 14-4. Reserved Register

[1] Read: Anytime
Write: Only in special mode

NOTE

This reserved register is designed for factory test purposes only, and is not intended for general user access. Writing to this register when in special mode can alter the module's functionality.

Table 14-6. Reserved Register

Field	Description
7-0 Reserved	These reserved bits are used for test purposes. Writing to these bits can alter the module functionality.
1-0 TRLS0OC	**Trimming Bit** Threshold trimming for both LS1 and LS0 over-current comparators. The trimming is coded representing an one-hot coding 0 -> "0001", 1 -> "0010", 2-> "0100" and 3 -> "1000".

15.4.4 Interrupts

The interrupt vector requested by the LIN Physical Layer is listed in Table 15-12. Vector address and interrupt priority is defined at MCU level.

The module internal interrupt sources are combined into one module interrupt source.

Table 15-12. Interrupt Vectors

Module Interrupt Source	Module Internal Interrupt Source	Local Enable
LIN Interrupt (LPI)	LIN Over-Current Interrupt (LPOCI)	LPOCIE = 1; available only in Normal Mode

15.4.4.1 Over-Current Interrupt

The output low side FET (transmitter) is protected against over-current. In case of an over-current condition occurring within a time frame called t_{OCLIM} starting from a transition on TXD, the current through the transmitter is limited (the transmitter is not shut down), the transmitted data is lost and the bit LPOC remains at 0. If an over-current occurs out of this time frame, the transmitter is shut down and the bit LPOC in the LPSR register is set as long as the condition is present. The inhibition of an over-current within the time frame t_{OCLIM} is meant to avoid “false” over-current conditions due to charging/discharging the LIN bus during transition phases.

The bit LPOCIF is set to 1 when the status of LPOC changes and it remains set until it has been cleared by writing a 1. If the bit LPOCIE is set in the LPIE register, an interrupt will be requested.

As long as LPOC is 1, the transmitter is disable.

NOTE

On entering Standby Mode (stop mode at the device level), the LPOCIF bit is not cleared.

15.5 Application Information

15.5.1 Over-current handling

In case of an over-current condition, the transmitter is switched off. The transmitter will stay disabled until the condition is gone. At this moment it is up to the software to activate again the transmitter through the RXONLY bit.

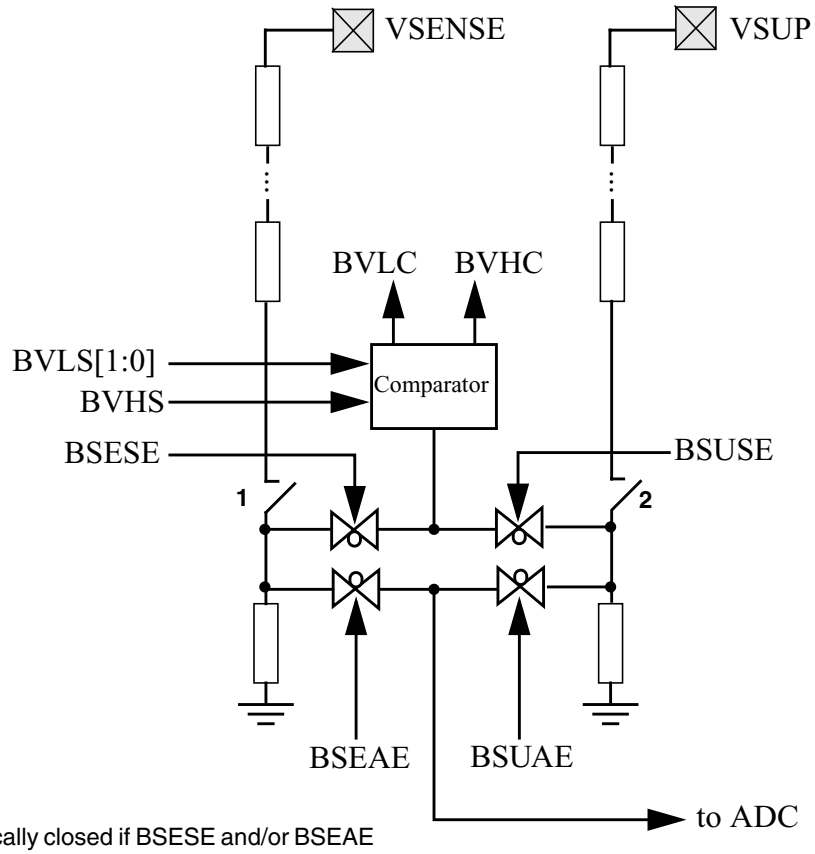
However, if the over-current occurs within a transition phase, the transmitter is internally limiting the current but no over-current event will be reported. Indeed, charging/discharging the bus can cause over-current events at each transition, which should not be reported. The time frame during which an over-current is not reported is equal to t_{OCLIM} starting from a rising or a falling edge of txd.

During stop mode operation the path from the VSUP pin through the resistor chain to ground is opened and the low voltage sense features are disabled.
The content of the configuration register is unchanged.

16.1.3 Block Diagram

Figure 16-1 shows a block diagram of the BATS module. See device guide for connectivity to ADC channel.

Figure 16-1. BATS Block Diagram



1 automatically closed if BSESE and/or BSEAE is active, open during Stop mode
2 automatically closed if BSUSE and/or BSUAE is active, open during Stop mode

16.2 External Signal Description

This section lists the name and description of all external ports.

16.2.1 VSENSE — Supply (Battery) Voltage Sense Pin

This pin can be connected to the supply (Battery) line for voltage measurements. The voltage present at this input is scaled down by an internal voltage divider, and can be routed to the internal ADC or to a

Table A-13. Stop Current Characteristics

Conditions are: V_{SUP}=V_{SUPHS}=12V API see CPMU Configuration for Pseudo Stop Current MeasurementTable A-9.							
Num	**C**	**Rating**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
Stop Current all modules off							
1	P	$T_A = T_J$ = -40°C[1]	I_{SUPS}		29	60	µA
2	P	$T_A = T_J$ = 150°C[1]	I_{SUPS}		140	600	µA
3	C	$T_A = T_J$ = 25°C[1]	I_{SUPS}		33	65	µA
4	C	$T_A = T_J$ = 105°C[1]	I_{SUPS}		55	90	µA
Stop Current API enabled & LINPHY in standby (see 15.4.3.4 Standby Mode with wake-up feature)							
5	C	$T_A = T_J$ = 25°C[1]	I_{SUPS}		50	80	µA

[1] If MCU is in STOP long enough then $T_A = T_J$. Die self heating due to stop current can be ignored.

Table A-14. Pseudo Stop Current Characteristics

Conditions are: V_{SUP}=V_{SUPHS}=12V, API see CPMU Configuration for Pseudo Stop Current MeasurementTable A-9., COP & RTI enabled							
Num	**C**	**Rating**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
1	C	T_A= 25°C	I_{SUPPS}		358	480	µA

Table C-2. ATD Electrical Characteristics

Supply voltage 3.13 V < V_{DDA} < 5.5 V, -40°C < T_J < 150°C							
Num	**C**	**Rating**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
1	C	Max input source resistance[1]	R_S	—	—	1	KΩ
2	D	Total input capacitance Non sampling Total input capacitance Sampling	C_{INN} C_{INS}	— —	— —	10 16	pF
3	D	Input internal Resistance	R_{INA}	-	5	15	kΩ
4	C	Disruptive analog input current	I_{NA}	-2.5	—	2.5	mA
5	C	Coupling ratio positive current injection	K_p	—	—	1E-4	A/A
6	C	Coupling ratio negative current injection	K_n	—	—	5E-3	A/A

[1] 1 Refer to C.2.2 for further information concerning source resistance

C.3 ATD Accuracy

Table C-3. and **Table C-4.** specifies the ATD conversion performance excluding any errors due to current injection, input capacitance and source resistance.

C.3.1 ATD Accuracy Definitions

For the following definitions see also Figure C-1.
Differential non-linearity (DNL) is defined as the difference between two adjacent switching steps.

$$DNL(i) = \frac{V_i - V_{i-1}}{1LSB} - 1$$

The integral non-linearity (INL) is defined as the sum of all DNLs:

$$INL(n) = \sum_{i=1}^{n} DNL(i) = \frac{V_n - V_0}{1LSB} - n$$

1 % deviation from target frequency

2 f_{REF} = 1MHz (IRC), f_{BUS} = 25MHz equivalent f_{PLL}=50MHz, CPMUSYNR=0x58, CPMUREFDIV=0x00,CPMUPOSTDIV=0x00

3 f_{REF} = 4MHz (XOSCLCP), f_{BUS} = 24MHz equivalent f_{PLL}=48MHz, CPMUSYNR=0x05,CPMUREFDIV=0x40,CPMUPOSTDIV=0x00

Appendix H
LSDRV Electrical Specifications

This section provides electrical parametric and ratings for the LSDRV.

H.1 Static Characteristics

Table H-1. Static Characteristics - LSDRV

Characteristics noted under conditions 6V ≤ VSUP ≤ 18 V, -40˚C ≤ T_J ≤ 150˚C[1] unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25˚C[2] under nominal conditions unless otherwise noted.							
Num	**C**	**Ratings**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
1	P	VSUP range for LSDRV compliant electrical characteristics	V_{SUP}	6	12	18	V
2	C	VSUP range within which the device is working without LSDRV compliant electrical characteristics	V_{SUP}		3.5 to 6 and 18 to 27		V
3	P	Output Drain-to-Source On Resistance T_J = 25˚C, $I_{PLS0/1}$ = 150 mA T_J = 150˚C, $I_{PLS0/1}$ = 150 mA	$R_{DS(ON)}$	 – –	 2.3 –	 – 4.5	Ω
4	P	Output Over-Current Threshold The threashold is valid for each LS-driver output. **Note:** **The low-side driver is NOT intended to switch capacitive loads. A significant capacitive load on PLS0/1 would induce a current when the low-side driver gate is turned on. This current will be sensed by the over-current circuitry and eventually lead to an immediate over-current shut down.**	I_{LIMLSX}	160	270	350	mA
5	D	Nominal Current for continuous operation. This value is valid for each LS-driver output.	I_{NOMLSX}	–	–	150	mA
5	D	Settling time after the low-side driver is enabled (write LSEx Bits)	$t_{LS\_settling}$	1	–		µs
7	P	High-Load Resistance Open-Load Detection Current (if low-side driver is enabled and gate turned off)	$I_{HLROLDC}$	28	40	52	µA
8	C	Leakage Current -40˚C < T_J < 80˚C Open Load Detection disabled.	I_{LEAK_L}	–	–	1	µA µA
9	P	Leakage Current -40˚C < T_J< 150˚C Open Load Detection disabled.	I_{LEAK_H}	–	–	10	µA µA