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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Discontinued at Digi-Key
Core Processor	C166
Core Size	16-Bit
Speed	25MHz
Connectivity	EBI/EMI, I²C, SLDM, SPI, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	93
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	10K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 12x10b
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	128-LQFP
Supplier Device Package	PG-TQFP-128-2
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/sab-c161ji-lf-ca

- Idle, Sleep, and Power Down Modes with Flexible Power Management
- Programmable Watchdog Timer and Oscillator Watchdog
- Up to 93 General Purpose I/O Lines,
  partly with Selectable Input Thresholds and Hysteresis
- Supported by a Large Range of Development Tools like C-Compilers,
  Macro-Assembler Packages, Emulators, Evaluation Boards, HLL-Debuggers,
  Simulators, Logic Analyzer Disassemblers, Programming Boards
- On-Chip Bootstrap Loader
- 128-Pin TQFP Package

This document describes several derivatives of the C161 group. **Table 1** enumerates these derivatives and summarizes the differences. As this document refers to all of these derivatives, some descriptions may not apply to a specific product.

Table 1 C161CS/JC/JI Derivative Synopsis

Derivative	On-Chip Program Memory	Serial Bus Interface(s)	Maximum CPU Frequency
SAK-C161CS-32RF SAB-C161CS-32RF	256 KByte ROM	CAN1, CAN2	25 MHz
SAK-C161CS-LF SAB-C161CS-LF	---	CAN1, CAN2	25 MHz
SAK-C161JC-32RF SAB-C161JC-32RF	256 KByte ROM	CAN1, SDLM	25 MHz
SAK-C161JC-LF SAB-C161JC-LF	---	CAN1, SDLM	25 MHz
SAK-C161JI-32RF SAB-C161JI-32RF	256 KByte ROM	SDLM	25 MHz
SAK-C161JI-LF SAB-C161JI-LF	---	SDLM	25 MHz

For simplicity all versions are referred to by the term **C161CS/JC/JI** throughout this document.

Table 2 Pin Definitions and Functions (cont'd)

Symbol	Pin No.	Input Outp.	Function	
P3		IO	Port 3 is a 15-bit bidirectional I/O port. It is bit-wise programmable for input or output via direction bits. For a pin configured as input, the output driver is put into high-impedance state. Port 3 outputs can be configured as push/pull or open drain drivers. The input threshold of Port 3 is selectable (TTL or special). The following Port 3 pins also serve for alternate functions:	
P3.0	53	I	T0IN	CAPCOM1 Timer T0 Count Input,
		O	TxD1	ASC1 Clock/Data Output (Async./Sync)
P3.1	54	O	T6OUT	GPT2 Timer T6 Toggle Latch Output,
		I/O	RxD1	ASC1 Data Input (Async.) or Inp./Output (Sync.)
P3.2	55	I	CAPIN	GPT2 Register CAPREL Capture Input
P3.3	56	O	T3OUT	GPT1 Timer T3 Toggle Latch Output
P3.4	57	I	T3EUD	GPT1 Timer T3 External Up/Down Control Input
P3.5	58	I	T4IN	GPT1 Timer T4 Count/Gate/Reload/Capture Inp
P3.6	59	I	T3IN	GPT1 Timer T3 Count/Gate Input
P3.7	60	I	T2IN	GPT1 Timer T2 Count/Gate/Reload/Capture Inp
P3.8	61	I/O	MRST	SSC Master-Receive/Slave-Transmit Inp./Outp.
P3.9	62	I/O	MTSR	SSC Master-Transmit/Slave-Receive Outp./Inp.
P3.10	63	O	TxD0	ASC0 Clock/Data Output (Async./Sync.)
P3.11	64	I/O	RxD0	ASC0 Data Input (Async.) or Inp./Outp. (Sync.)
P3.12	65	O	$\overline{\text{BHE}}$	External Memory High Byte Enable Signal,
		O	$\overline{\text{WRH}}$	External Memory High Byte Write Strobe
P3.13	66	I/O	SCLK	SSC Master Clock Output / Slave Clock Input.
P3.15	67	O	CLKOUT	System Clock Output (= CPU Clock)
		O	FOUT	Programmable Frequency Output

Table 2 Pin Definitions and Functions (cont'd)

Symbol	Pin No.	Input Outp.	Function
$\overline{\text{READY}}$	82	I	Ready Input. When the Ready function is enabled, a high level at this pin during an external memory access will force the insertion of memory cycle time waitstates until the pin returns to a low level. An internal pullup device will hold this pin high when nothing is driving it.
ALE	83	O	Address Latch Enable Output. Can be used for latching the address into external memory or an address latch in the multiplexed bus modes.
$\overline{\text{EA}}$	84	I	External Access Enable pin. A low level at this pin during and after Reset forces the C161CS/JC/JI to begin instruction execution out of external memory. A high level forces execution out of the internal program memory. "ROMless" versions must have this pin tied to '0'.
PORT0 P0L.0-7 P0H.0-7	 85-92 95-102	IO	PORT0 consists of the two 8-bit bidirectional I/O ports P0L and P0H. It is bit-wise programmable for input or output via direction bits. For a pin configured as input, the output driver is put into high-impedance state. In case of an external bus configuration, PORT0 serves as the address (A) and address/data (AD) bus in multiplexed bus modes and as the data (D) bus in demultiplexed bus modes. **Demultiplexed bus modes:** Data Path Width: 8-bit 16-bit P0L.0 – P0L.7: D0 – D7 D0 - D7 P0H.0 – P0H.7: I/O D8 - D15 **Multiplexed bus modes:** Data Path Width: 8-bit 16-bit P0L.0 – P0L.7: AD0 – AD7 AD0 - AD7 P0H.0 – P0H.7: A8 - A15 AD8 - AD15 *Note: At the end of an external reset (EA = '0') PORT0 also inputs the configuration values.*

Functional Description

The architecture of the C161CS/JC/JI combines advantages of both RISC and CISC processors and of advanced peripheral subsystems in a very well-balanced way. In addition the on-chip memory blocks allow the design of compact systems with maximum performance.
The following block diagram gives an overview of the different on-chip components and of the advanced, high bandwidth internal bus structure of the C161CS/JC/JI.

Note: All time specifications refer to a CPU clock of 25 MHz (see definition in the AC Characteristics section).

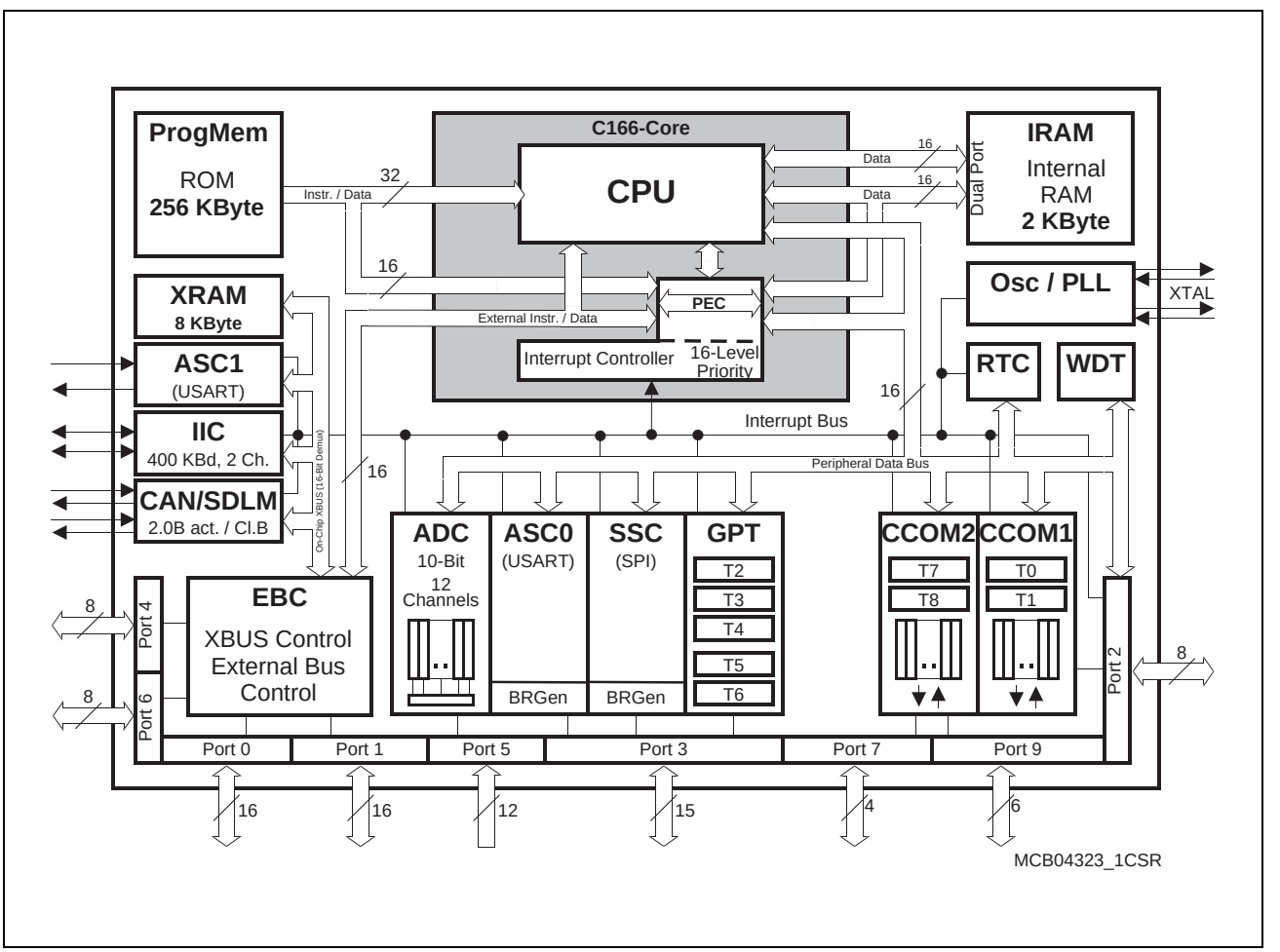

Figure 3 Block Diagram

The program memory, the internal RAM (IRAM) and the set of generic peripherals are connected to the CPU via separate buses. A fourth bus, the XBUS, connects external resources as well as additional on-chip resoures, the X-Peripherals (see **Figure 3**).

The XBUS resources (XRAM, CAN, SDLM, IIC, ASC1) of the C161CS/JC/JI can be enabled during initialization by setting the general X-Peripheral enable bit XPEN (SYSCON.2).
If the X-Peripherals remain disabled they consume neither address space nor port pins.

after the capture procedure. This allows the C161CS/JC/JI to measure absolute time differences or to perform pulse multiplication without software overhead.

The capture trigger (timer T5 to CAPREL) may also be generated upon transitions of GPT1 timer T3's inputs T3IN and/or T3EUD. This is especially advantageous when T3 operates in Incremental Interface Mode.

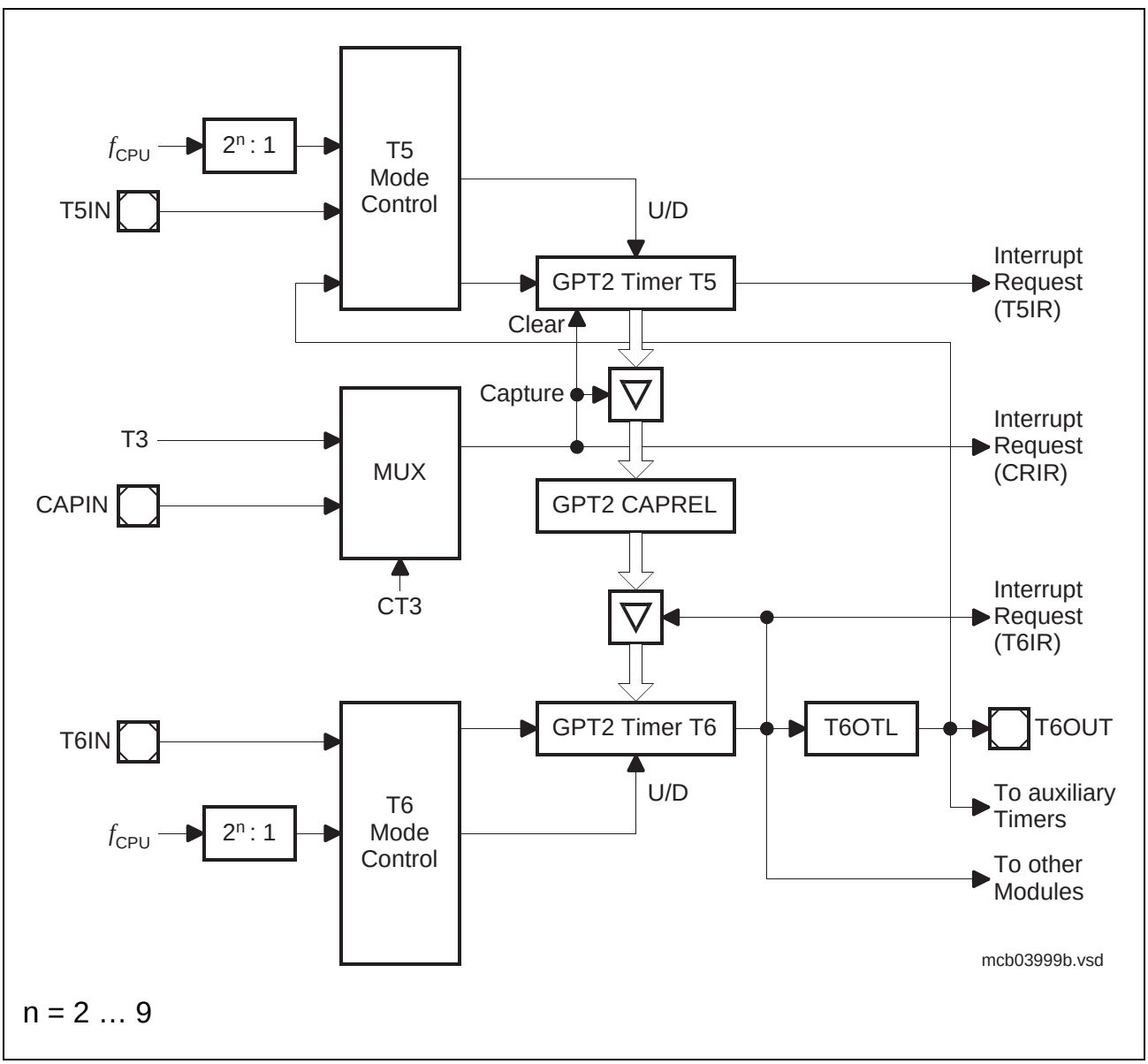

Figure 7 Block Diagram of GPT2

Real Time Clock

The Real Time Clock (RTC) module of the C161CS/JC/JI consists of a chain of 3 divider blocks, a fixed 8:1 divider, the reloadable 16-bit timer T14, and the 32-bit RTC timer (accessible via registers RTCH and RTCL). The RTC module is directly clocked via a separate clock driver with the on-chip main oscillator frequency divided by 32 ($f_{RTC} = f_{OSCm} / 32$) or with the on-chip auxiliary oscillator frequency ($f_{RTC} = f_{OSCa}$). It is therefore independent from the selected clock generation mode of the C161CS/JC/JI. All timers count up.

The RTC module can be used for different purposes:

- System clock to determine the current time and date
- Cyclic time based interrupt
- 48-bit timer for long term measurements

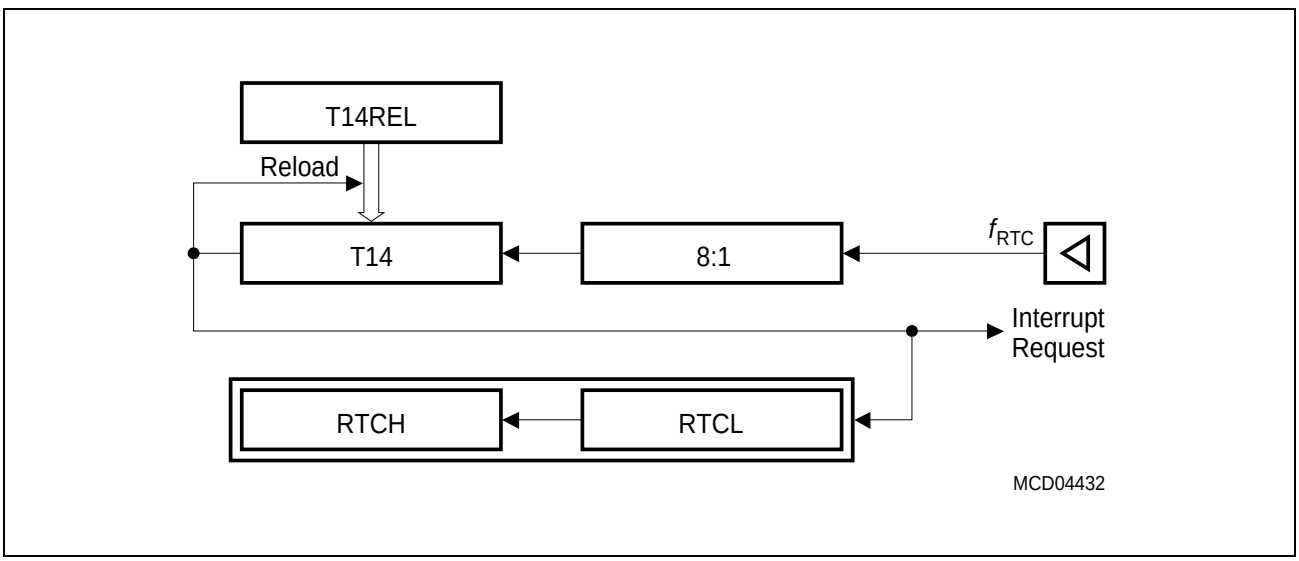

Figure 8 RTC Block Diagram

Note: The registers associated with the RTC are not affected by a reset in order to maintain the correct system time even when intermediate resets are executed.

Serial Channels

Serial communication with other microcontrollers, processors, terminals or external peripheral components is provided by three serial interfaces with different functionality, two Asynchronous/Synchronous Serial Channels (**ASC0**/**ASC1**) and a High-Speed Synchronous Serial Channel (**SSC**).

The ASC0 is upward compatible with the serial ports of the Infineon 8-bit microcontroller families and supports full-duplex asynchronous communication at up to 781 kBaud and half-duplex synchronous communication at up to 3.1 MBaud (@ 25 MHz CPU clock).
A dedicated baud rate generator allows to set up all standard baud rates without oscillator tuning. For transmission, reception and error handling 4 separate interrupt vectors are provided. In asynchronous mode, 8- or 9-bit data frames are transmitted or received, preceded by a start bit and terminated by one or two stop bits. For multiprocessor communication, a mechanism to distinguish address from data bytes has been included (8-bit data plus wake up bit mode).
In synchronous mode, the ASC0 transmits or receives bytes (8 bits) synchronously to a shift clock which is generated by the ASC0. The ASC0 always shifts the LSB first. A loop back option is available for testing purposes.
A number of optional hardware error detection capabilities has been included to increase the reliability of data transfers. A parity bit can automatically be generated on transmission or be checked on reception. Framing error detection allows to recognize data frames with missing stop bits. An overrun error will be generated, if the last character received has not been read out of the receive buffer register at the time the reception of a new character is complete.

The ASC1 is function compatible with the ASC0, except that its registers are not bit-addressable (XBUS peripheral) and it provides only three interrupt vectors.

The SSC supports full-duplex synchronous communication at up to 6.25 MBaud (@ 25 MHz CPU clock). It may be configured so it interfaces with serially linked peripheral components. A dedicated baud rate generator allows to set up all standard baud rates without oscillator tuning. For transmission, reception and error handling three separate interrupt vectors are provided.
The SSC transmits or receives characters of 2 … 16 bits length synchronously to a shift clock which can be generated by the SSC (master mode) or by an external master (slave mode). The SSC can start shifting with the LSB or with the MSB and allows the selection of shifting and latching clock edges as well as the clock polarity.
A number of optional hardware error detection capabilities has been included to increase the reliability of data transfers. Transmit and receive error supervise the correct handling of the data buffer. Phase and baudrate error detect incorrect serial data.

Table 7 C161CS/JC/JI Registers, Ordered by Name (cont'd)

Name	Physical Address	8-Bit Addr.	Description	Reset Value
RXD18	$EB58_H$ **X**	---	SDLM Receive Data Register 18 (bus)	0000_H
S0BG	$FEB4_H$	$5A_H$	Serial Channel 0 Baud Rate Generator Reload Register	0000_H
S0CON **b**	$FFB0_H$	$D8_H$	Serial Channel 0 Control Register	0000_H
S0EIC **b**	$FF70_H$	$B8_H$	Serial Channel 0 Error Interrupt Ctrl. Reg.	0000_H
S0RBUF	$FEB2_H$	59_H	Serial Channel 0 Receive Buffer Register (read only)	$XXXX_H$
S0RIC **b**	$FF6E_H$	$B7_H$	Serial Channel 0 Receive Interrupt Control Register	0000_H
S0TBIC **b**	$F19C_H$ **E**	CE_H	Serial Channel 0 Transmit Buffer Interrupt Control Register	0000_H
S0TBUF	$FEB0_H$	58_H	Serial Channel 0 Transmit Buffer Register	0000_H
S0TIC **b**	$FF6C_H$	$B6_H$	Serial Channel 0 Transmit Interrupt Control Register	0000_H
S1BG	$EDA4_H$ **X**	---	Serial Channel 1 Baud Rate Generator Reload Register	0000_H
S1CON	$EDA6_H$ **X**	---	Serial Channel 1 Control Register	0000_H
S1RBUF	$EDA2_H$ **X**	---	Serial Channel 1 Receive Buffer Register (read only)	$XXXX_H$
S1TBUF	$EDA0_H$ **X**	---	Serial Channel 1 Transmit Buffer Register	0000_H
SOFPTR	$EB60_H$ **X**	---	SDLM Start-of-Frame Pointer Register	0000_H
SP	$FE12_H$	09_H	CPU System Stack Pointer Register	$FC00_H$
SSCBR	$F0B4_H$ **E**	$5A_H$	SSC Baudrate Register	0000_H
SSCCON **b**	$FFB2_H$	$D9_H$	SSC Control Register	0000_H
SSCEIC **b**	$FF76_H$	BB_H	SSC Error Interrupt Control Register	0000_H
SSCRB	$F0B2_H$ **E**	59_H	SSC Receive Buffer (read only)	$XXXX_H$
SSCRIC **b**	$FF74_H$	BA_H	SSC Receive Interrupt Control Register	0000_H
SSCTB	$F0B0_H$ **E**	58_H	SSC Transmit Buffer (write only)	0000_H
SSCTIC **b**	$FF72_H$	$B9_H$	SSC Transmit Interrupt Control Register	0000_H
STKOV	$FE14_H$	$0A_H$	CPU Stack Overflow Pointer Register	$FA00_H$
STKUN	$FE16_H$	$0B_H$	CPU Stack Underflow Pointer Register	$FC00_H$

Table 7 C161CS/JC/JI Registers, Ordered by Name (cont'd)

Name	Physical Address	8-Bit Addr.	Description	Reset Value
T8	$F052_H$ **E**	29_H	CAPCOM Timer 8 Register	0000_H
T8IC b	$F17C_H$ **E**	BE_H	CAPCOM Timer 8 Interrupt Ctrl. Reg.	0000_H
T8REL	$F056_H$ **E**	$2B_H$	CAPCOM Timer 8 Reload Register	0000_H
TFR b	$FFAC_H$	$D6_H$	Trap Flag Register	0000_H
TRANSSTAT	$EB1E_H$ **X**	---	SDLM Transmission Status Register	0000_H
TXCNT	$EB3C_H$ **X**	---	SDLM Bus Transmit Byte Counter Reg.	0000_H
TXCPU	$EB3E_H$ **X**	---	SDLM CPU Transmit Byte Counter Reg.	0000_H
TXD0	$EB30_H$ **X**	---	SDLM Transmit Data Register 0	0000_H
TXD10	$EB3A_H$ **X**	---	SDLM Transmit Data Register 10	0000_H
TXD2	$EB32_H$ **X**	---	SDLM Transmit Data Register 2	0000_H
TXD4	$EB34_H$ **X**	---	SDLM Transmit Data Register 4	0000_H
TXD6	$EB36_H$ **X**	---	SDLM Transmit Data Register 6	0000_H
TXD8	$EB38_H$ **X**	---	SDLM Transmit Data Register 8	0000_H
TxDELAY	$EB16_H$ **X**	---	SDLM Transceiver Delay Register	0014_H
WDT	$FEAE_H$	57_H	Watchdog Timer Register (read only)	0000_H
WDTCON b	$FFAE_H$	$D7_H$	Watchdog Timer Control Register	[2] $00XX_H$
XP0IC b	$F186_H$ **E**	$C3_H$	IIC Data Interrupt Control Register	0000_H
XP1IC b	$F18E_H$ **E**	$C7_H$	IIC Protocol Interrupt Control Register	0000_H
XP2IC b	$F196_H$ **E**	CB_H	CAN1 Interrupt Control Register	0000_H
XP3IC b	$F19E_H$ **E**	CF_H	PLL/RTC Interrupt Control Register	0000_H
XP4IC b	$F182_H$ **E**	$C1_H$	ASC1 Transmit Interrupt Ctrl. Reg.	0000_H
XP5IC b	$F18A_H$ **E**	$C5_H$	ASC1 Receive Interrupt Control Register	0000_H
XP6IC b	$F192_H$ **E**	$C9_H$	ASC1 Error Interrupt Control Register	0000_H
XP7IC b	$F19A_H$ **E**	CD_H	CAN2/SDLM Interrupt Control Register	0000_H
ZEROS b	$FF1C_H$	$8E_H$	Constant Value 0's Register (read only)	0000_H

1) The system configuration is selected during reset.

2) The reset value depends on the indicated reset source.

Absolute Maximum Ratings

Table 8 Absolute Maximum Rating Parameters

Parameter	Symbol	Limit Values		Unit	Notes
		min.	max.		
Storage temperature	T_{ST}	-65	150	°C	–
Junction temperature	T_J	-40	150	°C	under bias
Voltage on V_{DD} pins with respect to ground (V_{SS})	V_{DD}	-0.5	6.5	V	–
Voltage on any pin with respect to ground (V_{SS})	V_{IN}	-0.5	V_{DD} + 0.5	V	–
Input current on any pin during overload condition	–	-10	10	mA	–
Absolute sum of all input currents during overload condition	–	–	|100|	mA	–
Power dissipation	P_{DISS}	–	1.5	W	–

Note: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
During absolute maximum rating overload conditions ($V_{IN} > V_{DD}$ or $V_{IN} < V_{SS}$) the voltage on V_{DD} pins with respect to ground (V_{SS}) must not exceed the values defined by the absolute maximum ratings.

Operating Conditions

The following operating conditions must not be exceeded in order to ensure correct operation of the C161CS/JC/JI. All parameters specified in the following sections refer to these operating conditions, unless otherwise noticed.

Table 9 Operating Condition Parameters

Parameter	Symbol	Limit Values		Unit	Notes
		min.	max.		
Digital supply voltage	V_{DD}	4.5	5.5	V	Active mode, f_{CPUmax} = 25 MHz
		2.5[1)]	5.5	V	PowerDown mode
Digital ground voltage	V_{SS}	0		V	Reference voltage
Overload current	I_{OV}	–	±5	mA	Per pin[2)3)4)]
Absolute sum of overload currents	$\Sigma\|I_{OV}\|$	–	50	mA	[3)]
External Load Capacitance	C_L	–	100	pF	Pin drivers in **fast edge** mode[5)]
Ambient temperature	T_A	0	70	°C	SAB-C161CS/JC/JI …
		-40	85	°C	SAF-C161CS/JC/JI …
		-40	125	°C	SAK-C161CS/JC/JI …

1) Output voltages and output currents will be reduced when V_{DD} leaves the range defined for active mode.

2) Overload conditions occur if the standard operatings conditions are exceeded, i.e. the voltage on any pin exceeds the specified range (i.e. $V_{OV} > V_{DD}$ + 0.5 V or $V_{OV} < V_{SS}$ - 0.5 V). The absolute sum of input overload currents on all pins may not exceed **50 mA**. The supply voltage must remain within the specified limits. Proper operation is not guaranteed if overload conditions occur on functional pins line XTAL1, $\overline{RD}$, $\overline{WR}$, etc.

3) Not 100% tested, guaranteed by design and characterization.

4) Due to the different port structure of Port 9 (required by the IIC bus specification) the pins of Port 9 can only tolerate positive overload current, i.e. $V_{OV} > V_{SS}$ - 0.5 V.

5) The timing is valid for pin drivers in high current or dynamic current mode. The reduced static output current in dynamic current mode must be respected when designing the system.

6) These parameters describe the $\overline{\text{RSTIN}}$ pullup, which equals a resistance of ca. 50 to 250 kΩ.

7) The maximum current may be drawn while the respective signal line remains inactive.

8) The minimum current must be drawn in order to drive the respective signal line active.

9) This specification is valid during Reset and during Hold-mode or Adapt-mode. During Hold-mode Port 6 pins are only affected, if they are used (configured) for $\overline{\text{CS}}$ output and the open drain function is not enabled. The $\overline{\text{READY}}$-pullup is always active, except for Powerdown mode.

10) This specification is valid during Reset and during Adapt-mode.

11) Not 100% tested, guaranteed by design and characterization.

Power Consumption C161CS/JC/JI

(Operating Conditions apply)

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Power supply current (active) with all peripherals active	I_{DD}	–	15 + 2.5 × f_{CPU}	mA	$\overline{\text{RSTIN}}$ = V_{IL} f_{CPU} in [MHz][1]
Idle mode supply current with all peripherals active	I_{IDX}	–	5 + 1.5 × f_{CPU}	mA	$\overline{\text{RSTIN}}$ = V_{IH1} f_{CPU} in [MHz][1]
Idle mode supply curr., Main osc, with all peripherals deactivated, PLL off, SDD factor = 32	I_{IDOM}[2]	–	500 + 50 × f_{OSC}	µA	$\overline{\text{RSTIN}}$ = V_{IH1} f_{OSC} in [MHz][1]
Idle mode supply curr., Aux. osc, with all peripherals deactivated, PLL off, SDD factor = 32	I_{IDOA}[2]	–	100	µA	V_{DD} = V_{DDmax} f_{OSC} = 32 kHz[3]
Sleep and Power-down mode supply current with RTC running on main oscillator	I_{PDRM}[2]	–	200 + 25 × f_{OSC}	µA	V_{DD} = V_{DDmax} f_{OSC} in [MHz][3]
Sleep and Power-down mode supply current with RTC disabled	I_{PDO}	–	50	µA	V_{DD} = V_{DDmax}[3]

1) The supply current is a function of the operating frequency. This dependency is illustrated in **Figure 10**. These parameters are tested at V_{DDmax} and maximum CPU clock with all outputs disconnected and all inputs at V_{IL} or V_{IH}.

2) This parameter is determined mainly by the current consumed by the oscillator (see **Figure 9**). This current, however, is influenced by the external oscillator circuitry (crystal, capacitors). The values given refer to a typical circuitry and may change in case of a not optimized external oscillator circuitry.

3) This parameter is tested including leakage currents. All inputs (including pins configured as inputs) at 0 V to 0.1 V or at V_{DD} - 0.1 V to V_{DD}, all outputs (including pins configured as outputs) disconnected.

The timings listed in the AC Characteristics that refer to TCLs therefore must be calculated using the minimum TCL that is possible under the respective circumstances.

The actual minimum value for TCL depends on the jitter of the PLL. As the PLL is constantly adjusting its output frequency so it corresponds to the applied input frequency (crystal or oscillator) the relative deviation for periods of more than one TCL is lower than for one single TCL (see formula and **Figure 12**).
For a period of $N \times$ TCL the minimum value is computed using the corresponding deviation D_N:

$$(N \times TCL)_{min} = N \times TCL_{NOM} - D_N \quad D_N\,[ns] = \pm(13.3 + N \times 6.3) / f_{CPU}\,[MHz],$$

where N = number of consecutive TCLs and $1 \le N \le 40$.

So for a period of 3 TCLs @ 25 MHz (i.e. $N = 3$): $D_3 = (13.3 + 3 \times 6.3) / 25 = 1.288$ ns, and $(3TCL)_{min} = 3TCL_{NOM} - 1.288$ ns = 58.7 ns (@ f_{CPU} = 25 MHz).

This is especially important for bus cycles using waitstates and e.g. for the operation of timers, serial interfaces, etc. For all slower operations and longer periods (e.g. pulse train generation or measurement, lower baudrates, etc.) the deviation caused by the PLL jitter is neglectible.

*Note: For all periods longer than 40 TCL the N = 40 value can be used (see **Figure 12**).*

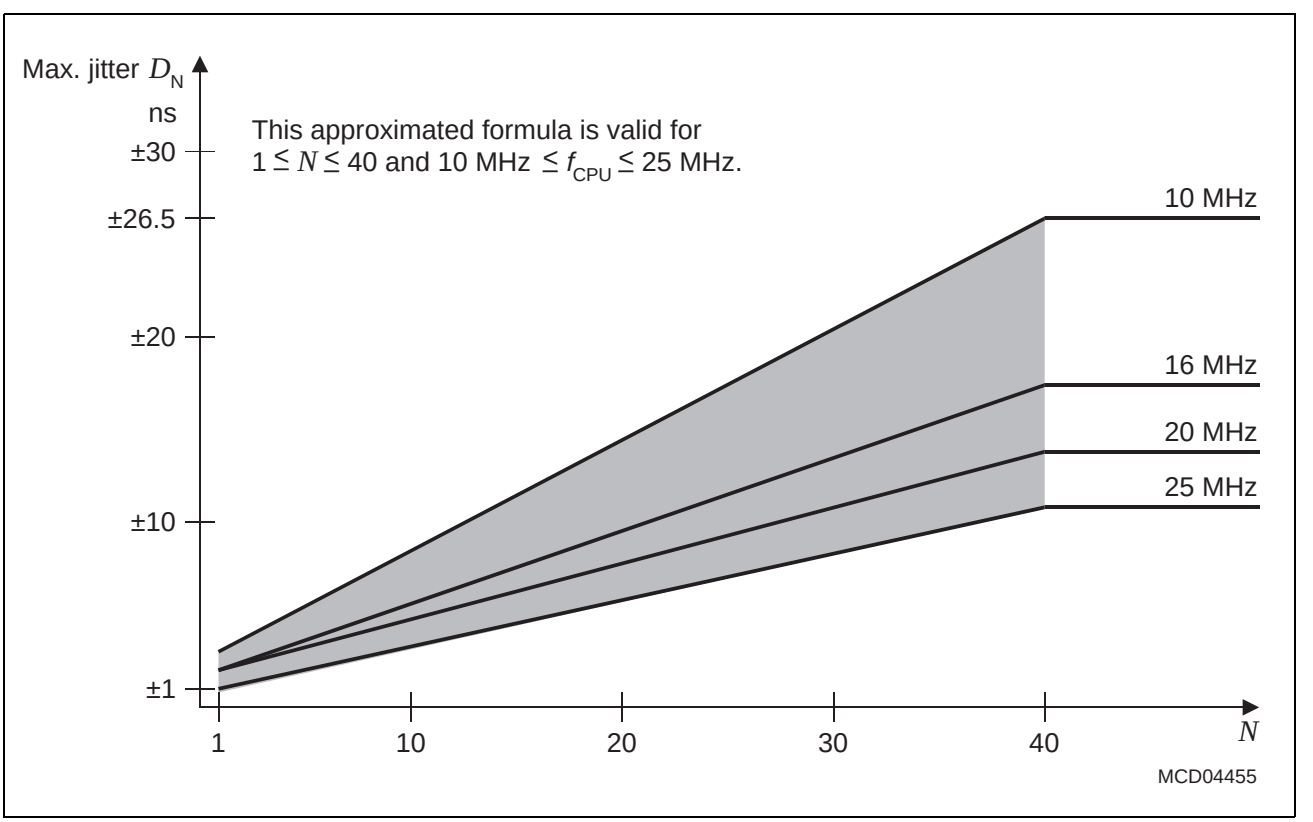

Figure 12 Approximated Maximum Accumulated PLL Jitter

AC Characteristics

External Clock Drive XTAL1 (Main Oscillator)

(Operating Conditions apply)

Table 11 External Clock Drive Characteristics

Parameter	Symbol		Direct Drive 1:1		Prescaler 2:1		PLL 1:N		Unit
			min.	max.	min.	max.	min.	max.	
Oscillator period	t_{OSCM}	SR	40	–	20	–	60[1]	500[1]	ns
High time[2]	t_1	SR	20[3]	–	6	–	10	–	ns
Low time[2]	t_2	SR	20[3]	–	6	–	10	–	ns
Rise time[2]	t_3	SR	–	10	–	6	–	10	ns
Fall time[2]	t_4	SR	–	10	–	6	–	10	ns

1) The minimum and maximum oscillator periods for PLL operation depend on the selected CPU clock generation mode. Please see respective table above.

2) The clock input signal must reach the defined levels V_{IL2} and V_{IH2}.

3) The minimum high and low time refers to a duty cycle of 50%. The maximum operating frequency (f_{CPU}) in direct drive mode depends on the duty cycle of the clock input signal.

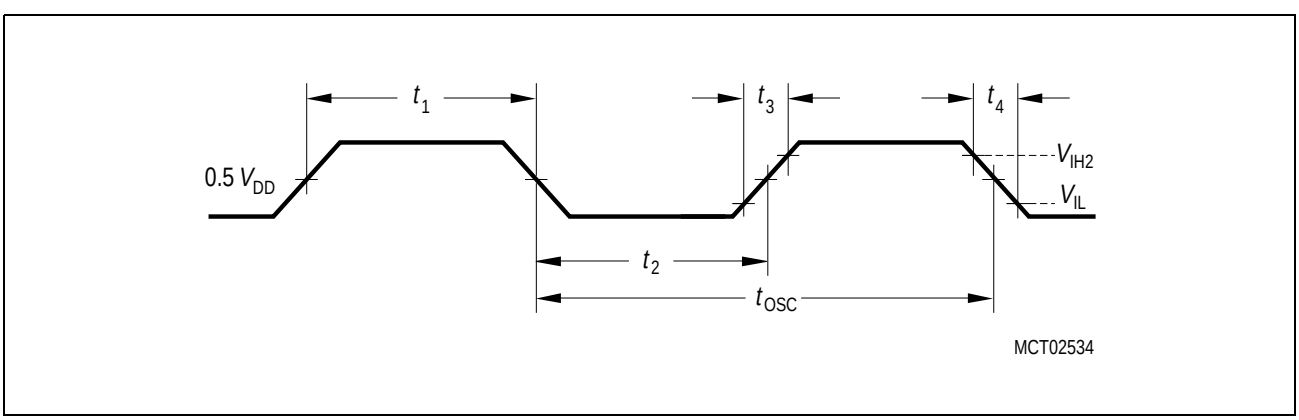

Figure 13 External Clock Drive XTAL1

Note: If the on-chip oscillator is used together with a crystal, the oscillator frequency is limited to a range of 4 MHz to 16 MHz.
It is strongly recommended to measure the oscillation allowance (or margin) in the final target system (layout) to determine the optimum parameters for the oscillator operation. Please refer to the limits specified by the crystal supplier.
When driven by an external clock signal it will accept the specified frequency range. Operation at lower input frequencies is possible but is guaranteed by design only (not 100% tested).

AC Characteristics

External Clock Drive XTAL3 (Auxiliary Oscillator)

(Operating Conditions apply)

Table 12 AC Characteristics

Parameter	Symbol		Optimum Input Clock = 32 kHz		Variable Input Clock 1 / t_{OSCA} = 10 to 50 kHz		Unit
			min.	max.	min.	max.	
Oscillator period	t_{OSCA}	SR	31	31	20	100	µs
High time	t_1	SR	6[1)]	–	$0.2 \times t_{OSCA}$[1)]	–	µs
Low time	t_2	SR	6[1)]	–	$0.2 \times t_{OSCA}$[1)]	–	µs
Rise time	t_3	SR	–	12	–	$0.4 \times t_{OSCA}$	µs
Fall time	t_4	SR	–	12	–	$0.4 \times t_{OSCA}$	µs

1) The clock input signal must reach the defined levels V_{IL} and V_{IH2}.

Note: The auxiliary oscillator is optimized for oscillation with a crystal at a frequency of 32 kHz. When driven by an external clock signal it will accept the specified frequency range.
Operation at lower input frequencies is possible but is guaranteed by design only (not 100% tested).

A/D Converter Characteristics

(Operating Conditions apply)

Table 13 A/D Converter Characteristics

Parameter	Symbol		Limit Values		Unit	Test Condition
			min.	max.		
Analog reference supply	V_{AREF}	SR	4.0	V_{DD} + 0.1	V	1)
Analog reference ground	V_{AGND}	SR	V_{SS} - 0.1	V_{SS} + 0.2	V	
Analog input voltage range	V_{AIN}	SR	V_{AGND}	V_{AREF}	V	2)
Basic clock frequency	f_{BC}		0.5	6.25	MHz	3)
Conversion time	t_C	CC	–	40 t_{BC} + t_S + 2t_{CPU}	–	4) $t_{CPU} = 1 / f_{CPU}$
Calibration time after reset	t_{CAL}	CC	–	3328 t_{BC}	–	5)
Total unadjusted error	TUE	CC	–	±2	LSB	1)
Internal resistance of reference voltage source	R_{AREF}	SR	–	t_{BC} / 60 - 0.25	kΩ	t_{BC} in [ns]6)7)
Internal resistance of analog source	R_{ASRC}	SR	–	t_S / 450 - 0.25	kΩ	t_S in [ns]7)8)
ADC input capacitance	C_{AIN}	CC	–	33	pF	7)

1) TUE is tested at V_{AREF} = 5.0 V, V_{AGND} = 0 V, V_{DD} = 4.9 V. It is guaranteed by design for all other voltages within the defined voltage range.
If the analog reference supply voltage exceeds the power supply voltage by up to 0.2 V (i.e. V_{AREF} = V_{DD} = +0.2 V) the maximum TUE is increased to ±3 LSB. This range is not 100% tested.
The specified TUE is guaranteed only if the absolute sum of input overload currents on Port 5 pins (see I_{OV} specification) does not exceed 10 mA.
During the reset calibration sequence the maximum TUE may be ±4 LSB.

2) V_{AIN} may exceed V_{AGND} or V_{AREF} up to the absolute maximum ratings. However, the conversion result in these cases will be $X000_H$ or $X3FF_H$, respectively.

3) The limit values for f_{BC} must not be exceeded when selecting the CPU frequency and the ADCTC setting.

4) This parameter includes the sample time t_S, the time for determining the digital result and the time to load the result register with the conversion result.
Values for the basic clock t_{BC} depend on programming and can be taken from **Table 14**.
This parameter depends on the ADC control logic. It is not a real maximum value, but rather a fixum.

5) During the reset calibration conversions can be executed (with the current accuracy). The time required for these conversions is added to the total reset calibration time.

6) During the conversion the ADC's capacitance must be repeatedly charged or discharged. The internal resistance of the reference voltage source must allow the capacitance to reach its respective voltage level within each conversion step. The maximum internal resistance results from the programmed conversion timing.

7) Not 100% tested, guaranteed by design and characterization.

8) During the sample time the input capacitance C_{AIN} can be charged/discharged by the external source. The internal resistance of the analog source must allow the capacitance to reach its final voltage level within t_S. After the end of the sample time t_S, changes of the analog input voltage have no effect on the conversion result.
Values for the sample time t_S depend on programming and can be taken from **Table 14**.

Sample time and conversion time of the C161CS/JC/JI's A/D Converter are programmable. **Table 14** should be used to calculate the above timings.
The limit values for f_{BC} must not be exceeded when selecting ADCTC.

Table 14 A/D Converter Computation Table

ADCON.15|14 (ADCTC)	A/D Converter Basic Clock f_{BC}	ADCON.13|12 (ADSTC)	Sample time t_S
00	f_{CPU} / 4	00	$t_{BC} \times 8$
01	f_{CPU} / 2	01	$t_{BC} \times 16$
10	f_{CPU} / 16	10	$t_{BC} \times 32$
11	f_{CPU} / 8	11	$t_{BC} \times 64$

Converter Timing Example:

Assumptions:	f_{CPU}	= 25 MHz (i.e. t_{CPU} = 40 ns), ADCTC = '00', ADSTC = '00'.
Basic clock	f_{BC}	= f_{CPU} / 4 = 6.25 MHz, i.e. t_{BC} = 160 ns.
Sample time	t_S	= $t_{BC} \times 8$ = 1280 ns.
Conversion time	t_C	= t_S + 40 t_{BC} + 2 t_{CPU} = (1280 + 6400 + 80) ns = 7.8 µs.

Memory Cycle Variables

The timing tables below use three variables which are derived from the BUSCONx registers and represent the special characteristics of the programmed memory cycle. The following table describes, how these variables are to be computed.

Table 15 Memory Cycle Variables

Description	Symbol	Values
ALE Extension	t_A	TCL × <ALECTL>
Memory Cycle Time Waitstates	t_C	2TCL × (15 - <MCTC>)
Memory Tristate Time	t_F	2TCL × (1 - <MTTC>)

Note: Please respect the maximum operating frequency of the respective derivative.

AC Characteristics

Multiplexed Bus

(Operating Conditions apply)

ALE cycle time = 6 TCL + 2t_A + t_C + t_F (120 ns at 25 MHz CPU clock without waitstates)

Parameter	Symbol		Max. CPU Clock = 25 MHz		Variable CPU Clock 1 / 2TCL = 1 to 25 MHz		Unit
			min.	max.	min.	max.	
ALE high time	t_5	CC	10 + t_A	–	TCL - 10 + t_A	–	ns
Address setup to ALE	t_6	CC	4 + t_A	–	TCL - 16 + t_A	–	ns
Address hold after ALE	t_7	CC	10 + t_A	–	TCL - 10 + t_A	–	ns
ALE falling edge to $\overline{RD}$, $\overline{WR}$ (with RW-delay)	t_8	CC	10 + t_A	–	TCL - 10 + t_A	–	ns
ALE falling edge to $\overline{RD}$, $\overline{WR}$ (no RW-delay)	t_9	CC	-10 + t_A	–	-10 + t_A	–	ns
Address float after $\overline{RD}$, $\overline{WR}$ (with RW-delay)	t_{10}	CC	–	6	–	6	ns
Address float after $\overline{RD}$, $\overline{WR}$ (no RW-delay)	t_{11}	CC	–	26	–	TCL + 6	ns
$\overline{RD}$, $\overline{WR}$ low time (with RW-delay)	t_{12}	CC	30 + t_C	–	2TCL - 10 + t_C	–	ns

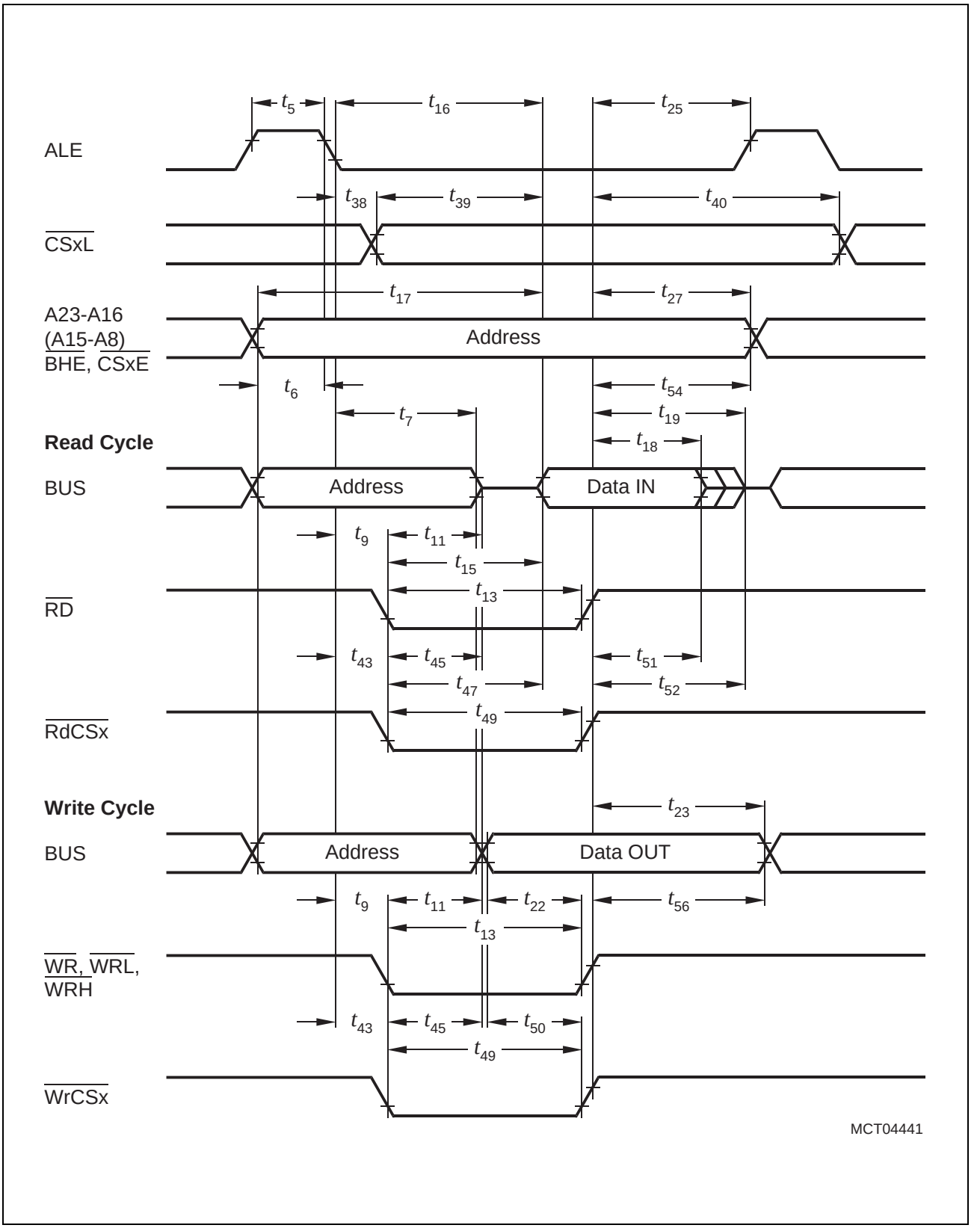

**Figure 18 External Memory Cycle:
Multiplexed Bus, No Read/Write Delay, Normal ALE**

Demultiplexed Bus (cont'd)
(Operating Conditions apply)
ALE cycle time = 4 TCL + 2t_A + t_C + t_F (80 ns at 25 MHz CPU clock without waitstates)

Parameter	Symbol		Max. CPU Clock = 25 MHz		Variable CPU Clock 1 / 2TCL = 1 to 25 MHz		Unit
			min.	max.	min.	max.	
Data float after $\overline{\text{RdCS}}$ (no RW-delay)[1]	t_{68}	SR	–	0 + t_F	–	TCL - 20 + 2t_A + t_F[1]	ns
Address hold after $\overline{\text{RdCS}}$, $\overline{\text{WrCS}}$	t_{55}	CC	-6 + t_F	–	-6 + t_F	–	ns
Data hold after $\overline{\text{WrCS}}$	t_{57}	CC	6 + t_F	–	TCL - 14 + t_F	–	ns

1) RW-delay and t_A refer to the next following bus cycle (including an access to an on-chip X-Peripheral).

2) Read data are latched with the same clock edge that triggers the address change and the rising $\overline{\text{RD}}$ edge. Therefore address changes before the end of $\overline{\text{RD}}$ have no impact on read cycles.

3) These parameters refer to the latched chip select signals ($\overline{\text{CSxL}}$). The early chip select signals ($\overline{\text{CSxE}}$) are specified together with the address and signal $\overline{\text{BHE}}$ (see figures below).