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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Discontinued at Digi-Key
Core Processor	C166
Core Size	16-Bit
Speed	25MHz
Connectivity	EBI/EMI, I²C, SLDM, SPI, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	93
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	10K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 12x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	128-LQFP
Supplier Device Package	PG-TQFP-128-2
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/saf-c161ji-lf-ca

Data Sheet, V3.0, Jan. 2001

C161CS-32R/-L
C161JC-32R/-L
C161JI-32R/-L

16-Bit Single-Chip Microcontroller

Microcontrollers

Infineon technologies

Never stop thinking.

Table 2 Pin Definitions and Functions (cont'd)

Symbol	Pin No.	Input Outp.	Function		
P5		I	Port 5 is a 12-bit input-only port with Schmitt-Trigger char. The pins of Port 5 also serve as analog input channels for the A/D converter, or they serve as timer inputs:		
P5.0	27	I	AN0		
P5.1	28	I	AN1		
P5.2	29	I	AN2		
P5.3	30	I	AN3		
P5.4	31	I	AN4		
P5.5	32	I	AN5		
P5.6	33	I	AN6		
P5.7	34	I	AN7		
P5.12	37	I	AN12,	T6IN	GPT2 Timer T6 Count Inp.
P5.13	38	I	AN13,	T5IN	GPT2 Timer T5 Count Inp.
P5.14	39	I	AN14,	T4EUD	GPT1 Timer T4 Ext. Up/Down Ctrl. Inp.
P5.15	40	I	AN15,	T2EUD	GPT1 Timer T5 Ext. Up/Down Ctrl. Inp.

Note: When one or both of the on-chip CAN Modules or the SDLM are used with the interface lines assigned to Port 4, the interface lines override the segment address lines and the segment address output on Port 4 is therefore limited to 6/4 bits i.e. address lines A21/A19 … A16. $\overline{CS}$ lines can be used to increase the total amount of addressable external memory.

Central Processing Unit (CPU)

The main core of the CPU consists of a 4-stage instruction pipeline, a 16-bit arithmetic and logic unit (ALU) and dedicated SFRs. Additional hardware has been spent for a separate multiply and divide unit, a bit-mask generator and a barrel shifter.

Based on these hardware provisions, most of the C161CS/JC/JI's instructions can be executed in just one machine cycle which requires 80 ns at 25 MHz CPU clock. For example, shift and rotate instructions are always processed during one machine cycle independent of the number of bits to be shifted. All multiple-cycle instructions have been optimized so that they can be executed very fast as well: branches in 2 cycles, a 16 × 16 bit multiplication in 5 cycles and a 32-/16-bit division in 10 cycles. Another pipeline optimization, the so-called 'Jump Cache', allows reducing the execution time of repeatedly performed jumps in a loop from 2 cycles to 1 cycle.

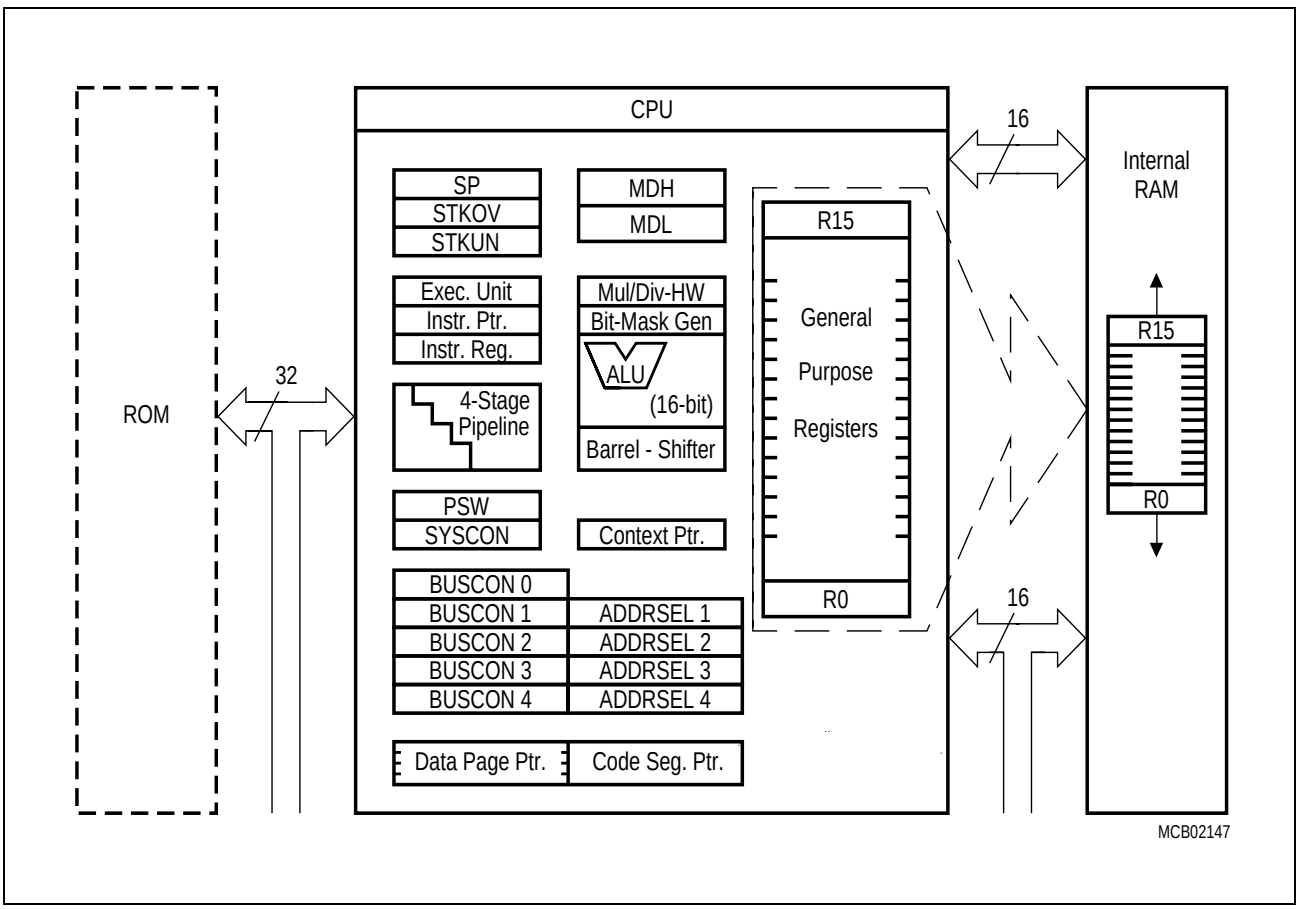

Figure 4 CPU Block Diagram

Interrupt System

With an interrupt response time within a range from just 5 to 12 CPU clocks (in case of internal program execution), the C161CS/JC/JI is capable of reacting very fast to the occurrence of non-deterministic events.

The architecture of the C161CS/JC/JI supports several mechanisms for fast and flexible response to service requests that can be generated from various sources internal or external to the microcontroller. Any of these interrupt requests can be programmed to being serviced by the Interrupt Controller or by the Peripheral Event Controller (PEC).

In contrast to a standard interrupt service where the current program execution is suspended and a branch to the interrupt vector table is performed, just one cycle is ‘stolen’ from the current CPU activity to perform a PEC service. A PEC service implies a single byte or word data transfer between any two memory locations with an additional increment of either the PEC source or the destination pointer. An individual PEC transfer counter is implicity decremented for each PEC service except when performing in the continuous transfer mode. When this counter reaches zero, a standard interrupt is performed to the corresponding source related vector location. PEC services are very well suited, for example, for supporting the transmission or reception of blocks of data. The C161CS/JC/JI has 8 PEC channels each of which offers such fast interrupt-driven data transfer capabilities.

A separate control register which contains an interrupt request flag, an interrupt enable flag and an interrupt priority bitfield exists for each of the possible interrupt sources. Via its related register, each source can be programmed to one of sixteen interrupt priority levels. Once having been accepted by the CPU, an interrupt service can only be interrupted by a higher prioritized service request. For the standard interrupt processing, each of the possible interrupt sources has a dedicated vector location.

Fast external interrupt inputs are provided to service external interrupts with high precision requirements. These fast interrupt inputs feature programmable edge detection (rising edge, falling edge or both edges).

Software interrupts are supported by means of the ‘TRAP’ instruction in combination with an individual trap (interrupt) number.

Table 3 shows all of the possible C161CS/JC/JI interrupt sources and the corresponding hardware-related interrupt flags, vectors, vector locations and trap (interrupt) numbers.

Note: Interrupt nodes which are not used by associated peripherals, may be used to generate software controlled interrupt requests by setting the respective interrupt request bit (xIR).

Capture/Compare (CAPCOM) Units

The CAPCOM units support generation and control of timing sequences on up to 32 channels with a maximum resolution of 16 TCL. The CAPCOM units are typically used to handle high speed I/O tasks such as pulse and waveform generation, pulse width modulation (PMW), Digital to Analog (D/A) conversion, software timing, or time recording relative to external events.

Four 16-bit timers (T0/T1, T7/T8) with reload registers provide two independent time bases for the capture/compare register array.

The input clock for the timers is programmable to several prescaled values of the internal system clock, or may be derived from an overflow/underflow of timer T6 in module GPT2. This provides a wide range of variation for the timer period and resolution and allows precise adjustments to the application specific requirements. In addition, external count inputs for CAPCOM timers T0 and T7 allow event scheduling for the capture/compare registers relative to external events.

Both of the two capture/compare register arrays contain 16 dual purpose capture/compare registers, each of which may be individually allocated to either CAPCOM timer T0 or T1 (T7 or T8, respectively), and programmed for capture or compare function. Eight registers of each module have one port pin associated with it which serves as an input pin for triggering the capture function, or as an output pin to indicate the occurrence of a compare event.

When a capture/compare register has been selected for capture mode, the current contents of the allocated timer will be latched (‘captured’) into the capture/compare register in response to an external event at the port pin which is associated with this register. In addition, a specific interrupt request for this capture/compare register is generated. Either a positive, a negative, or both a positive and a negative external signal transition at the pin can be selected as the triggering event.

The contents of all registers which have been selected for one of the five compare modes are continuously compared with the contents of the allocated timers.

Table 5 Compare Modes (CAPCOM)

Compare Modes	Function
Mode 0	Interrupt-only compare mode; several compare interrupts per timer period are possible
Mode 1	Pin toggles on each compare match; several compare events per timer period are possible
Mode 2	Interrupt-only compare mode; only one compare interrupt per timer period is generated
Mode 3	Pin set ‘1’ on match; pin reset ‘0’ on compare time overflow; only one compare event per timer period is generated

When a match occurs between the timer value and the value in a capture/compare register, specific actions will be taken based on the selected compare mode.

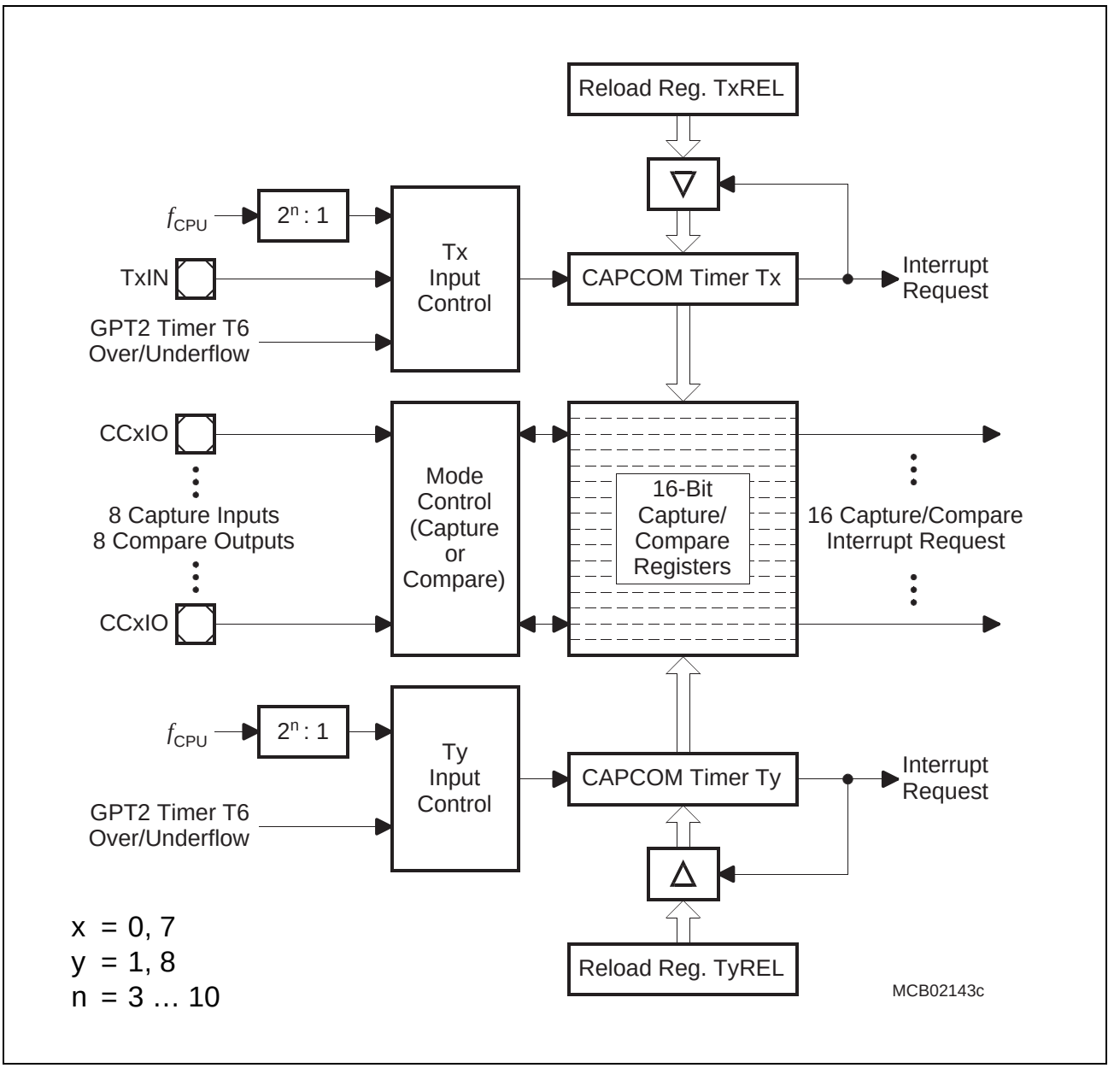

Figure 5 CAPCOM Unit Block Diagram

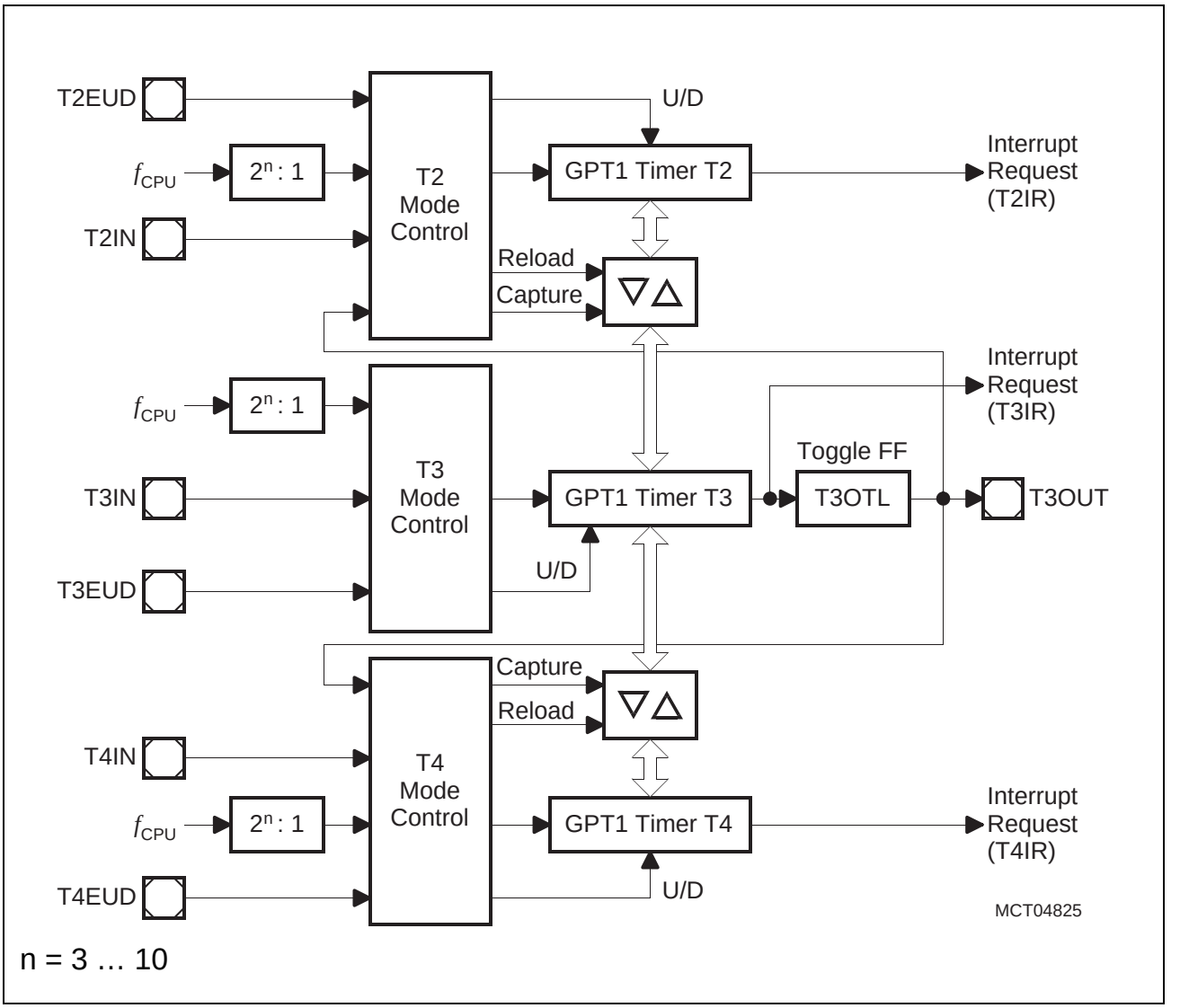

Figure 6 Block Diagram of GPT1

With its maximum resolution of 8 TCL, the **GPT2 module** provides precise event control and time measurement. It includes two timers (T5, T6) and a capture/reload register (CAPREL). Both timers can be clocked with an input clock which is derived from the CPU clock via a programmable prescaler or with external signals. The count direction (up/down) for each timer is programmable by software or may additionally be altered dynamically by an external signal on a port pin (TxEUD). Concatenation of the timers is supported via the output toggle latch (T6OTL) of timer T6, which changes its state on each timer overflow/underflow.

The state of this latch may be used to clock timer T5, and/or it may be output on pin T6OUT. The overflows/underflows of timer T6 can additionally be used to clock the CAPCOM timers T0 or T1, and to cause a reload from the CAPREL register. The CAPREL register may capture the contents of timer T5 based on an external signal transition on the corresponding port pin (CAPIN), and timer T5 may optionally be cleared

after the capture procedure. This allows the C161CS/JC/JI to measure absolute time differences or to perform pulse multiplication without software overhead.

The capture trigger (timer T5 to CAPREL) may also be generated upon transitions of GPT1 timer T3's inputs T3IN and/or T3EUD. This is especially advantageous when T3 operates in Incremental Interface Mode.

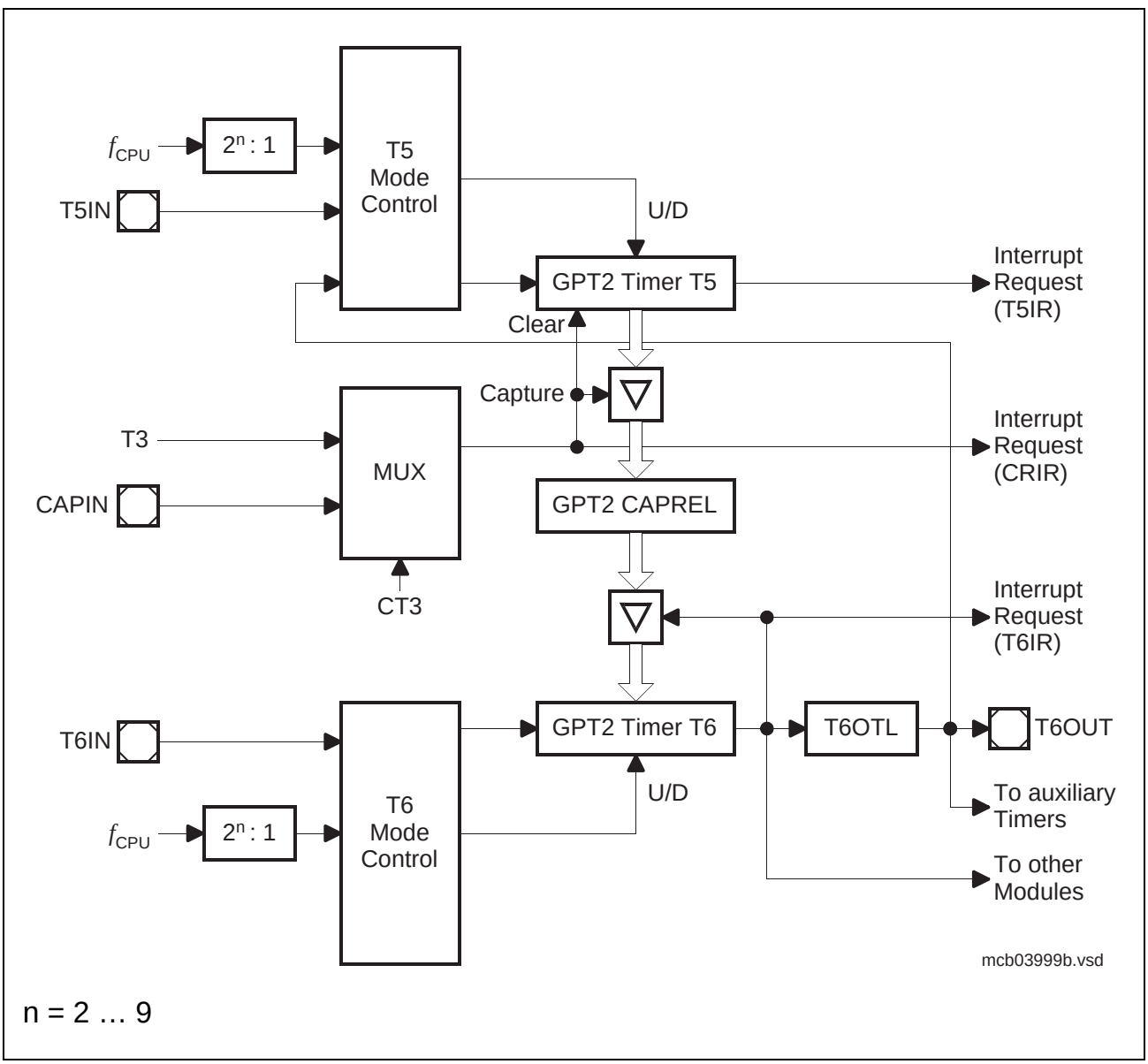

Figure 7 Block Diagram of GPT2

Serial Data Link Module (SDLM)

The Serial Data Link Module (SDLM) provides serial communication via a J1850 type multiplexed serial bus via an external J1850 bus transceiver. The module conforms to the SAE Class B J1850 specification for variable pulse width modulation (VPW). The SDLM is integrated as an on-chip peripheral and is connected to the CPU via the XBUS.

General SDLM Features:

- Compliant to the SAE Class B J1850 specification (VPW)
- Class 2 protocol fully supported
- Variable Pulse Width (VPW) operation at 10.4 kBaud
- High Speed 4X operation at 41.6 kBaud
- Programmable Normalization Bit
- Programmable Delay for transceiver interface
- Digital Noise Filter
- Power Down mode with automatic wakeup support upon bus activity
- Single Byte Header and Consolidated Header supported
- CRC generation and checking
- Receive and transmit Block Mode

Data Link Operation Features:

- 11 Byte Transmit Buffer
- Double buffered 11 Byte receive buffer (optional overwrite enable)
- Support for In Frame Response (IFR) types 1, 2 and 3
- Transmit and Receiver Message Buffers configurable for either FIFO or Byte mode
- Advanced Interrupt Handling with 8 separately enabled sources:
  Error, format or bus shorted
  CRC error
  Lost Arbitration
  Break received
  In-Frame-Response request
  Header received
  Complete message received
  Transmit successful
- Automatic IFR transmission (Types 1 and 2) for 3-Byte consolidated headers
- User configurable clock divider
- Bus status flags (IDLE, EOF, EOD, SOF, Tx and Rx in progress)

Note: When the SDLM is used with the interface lines assigned to Port 4, the interface lines override the segment address lines and the segment address output on Port 4 is therefore limited to 6/4 bits i.e. address lines A21/A19 … A16. $\overline{CS}$ lines can be used to increase the total amount of addressable external memory.

Instruction Set Summary

Table 6 lists the instructions of the C161CS/JC/JI in a condensed way.
The various addressing modes that can be used with a specific instruction, the operation of the instructions, parameters for conditional execution of instructions, and the opcodes for each instruction can be found in the **“C166 Family Instruction Set Manual”**.

This document also provides a detailled description of each instruction.

Table 6 Instruction Set Summary

Mnemonic	Description	Bytes
ADD(B)	Add word (byte) operands	2 / 4
ADDC(B)	Add word (byte) operands with Carry	2 / 4
SUB(B)	Subtract word (byte) operands	2 / 4
SUBC(B)	Subtract word (byte) operands with Carry	2 / 4
MUL(U)	(Un)Signed multiply direct GPR by direct GPR (16-16-bit)	2
DIV(U)	(Un)Signed divide register MDL by direct GPR (16-/16-bit)	2
DIVL(U)	(Un)Signed long divide reg. MD by direct GPR (32-/16-bit)	2
CPL(B)	Complement direct word (byte) GPR	2
NEG(B)	Negate direct word (byte) GPR	2
AND(B)	Bitwise AND, (word/byte operands)	2 / 4
OR(B)	Bitwise OR, (word/byte operands)	2 / 4
XOR(B)	Bitwise XOR, (word/byte operands)	2 / 4
BCLR	Clear direct bit	2
BSET	Set direct bit	2
BMOV(N)	Move (negated) direct bit to direct bit	4
BAND, BOR, BXOR	AND/OR/XOR direct bit with direct bit	4
BCMP	Compare direct bit to direct bit	4
BFLDH/L	Bitwise modify masked high/low byte of bit-addressable direct word memory with immediate data	4
CMP(B)	Compare word (byte) operands	2 / 4
CMPD1/2	Compare word data to GPR and decrement GPR by 1/2	2 / 4
CMPI1/2	Compare word data to GPR and increment GPR by 1/2	2 / 4
PRIOR	Determine number of shift cycles to normalize direct word GPR and store result in direct word GPR	2
SHL / SHR	Shift left/right direct word GPR	2
ROL / ROR	Rotate left/right direct word GPR	2
ASHR	Arithmetic (sign bit) shift right direct word GPR	2

Table 7 C161CS/JC/JI Registers, Ordered by Name (cont'd)

Name	Physical Address	8-Bit Addr.	Description	Reset Value
IDPROG	$F078_H$ **E**	$3C_H$	Identifier	$XXXX_H$
IFR	$EB18_H$ **X**	---	SDLM In-Frame Response Register	0000_H
INTCON	$EB2C_H$ **X**	---	SDLM Interrupt Control Register	0000_H
IPCR	$EB04_H$ **X**	---	SDLM Interface Port Connect Register	0007_H
ISNC	$F1DE_H$ **E**	EF_H	Interrupt Subnode Control Register	0000_H
MDC b	$FF0E_H$	87_H	CPU Multiply Divide Control Register	0000_H
MDH	$FE0C_H$	06_H	CPU Multiply Divide Reg. – High Word	0000_H
MDL	$FE0E_H$	07_H	CPU Multiply Divide Reg. – Low Word	0000_H
ODP2 b	$F1C2_H$ **E**	$E1_H$	Port 2 Open Drain Control Register	0000_H
ODP3 b	$F1C6_H$ **E**	$E3_H$	Port 3 Open Drain Control Register	0000_H
ODP4 b	$F1CA_H$ **E**	$E5_H$	Port 4 Open Drain Control Register	00_H
ODP6 b	$F1CE_H$ **E**	$E7_H$	Port 6 Open Drain Control Register	00_H
ODP7 b	$F1D2_H$ **E**	$E9_H$	Port 7 Open Drain Control Register	00_H
ONES b	$FF1E_H$	$8F_H$	Constant Value 1's Register (read only)	$FFFF_H$
P0H b	$FF02_H$	81_H	Port 0 High Reg. (Upper half of PORT0)	00_H
P0L b	$FF00_H$	80_H	Port 0 Low Reg. (Lower half of PORT0)	00_H
P1H b	$FF06_H$	83_H	Port 1 High Reg. (Upper half of PORT1)	00_H
P1L b	$FF04_H$	82_H	Port 1 Low Reg. (Lower half of PORT1)	00_H
P2 b	$FFC0_H$	$E0_H$	Port 2 Register	0000_H
P3 b	$FFC4_H$	$E2_H$	Port 3 Register	0000_H
P4 b	$FFC8_H$	$E4_H$	Port 4 Register (7 bits)	00_H
P5 b	$FFA2_H$	$D1_H$	Port 5 Register (read only)	$XXXX_H$
P6 b	$FFCC_H$	$E6_H$	Port 6 Register (8 bits)	00_H
P7 b	$FFD0_H$	$E8_H$	Port 7 Register (8 bits)	00_H
P9 b	$FFD8_H$	EC_H	Port 9 Register (8 bits)	00_H
PECC0	$FEC0_H$	60_H	PEC Channel 0 Control Register	0000_H
PECC1	$FEC2_H$	61_H	PEC Channel 1 Control Register	0000_H
PECC2	$FEC4_H$	62_H	PEC Channel 2 Control Register	0000_H
PECC3	$FEC6_H$	63_H	PEC Channel 3 Control Register	0000_H
PECC4	$FEC8_H$	64_H	PEC Channel 4 Control Register	0000_H
PECC5	$FECA_H$	65_H	PEC Channel 5 Control Register	0000_H
PECC6	$FECC_H$	66_H	PEC Channel 6 Control Register	0000_H

Table 7 C161CS/JC/JI Registers, Ordered by Name (cont'd)

Name	Physical Address	8-Bit Addr.	Description	Reset Value
SYSCON b	$FF12_H$	89_H	CPU System Configuration Register	[1]$0XX0_H$
SYSCON1 b	$F1DC_H$ **E**	EE_H	CPU System Configuration Register 1	0000_H
SYSCON2 b	$F1D0_H$ **E**	$E8_H$	CPU System Configuration Register 2	0000_H
SYSCON3 b	$F1D4_H$ **E**	EA_H	CPU System Configuration Register 3	$0X00_H$
T0	$FE50_H$	28_H	CAPCOM Timer 0 Register	0000_H
T01CON b	$FF50_H$	$A8_H$	CAPCOM Timer 0 and Timer 1 Ctrl. Reg.	0000_H
T0IC b	$FF9C_H$	CE_H	CAPCOM Timer 0 Interrupt Ctrl. Reg.	0000_H
T0REL	$FE54_H$	$2A_H$	CAPCOM Timer 0 Reload Register	0000_H
T1	$FE52_H$	29_H	CAPCOM Timer 1 Register	0000_H
T14	$F0D2_H$ **E**	69_H	RTC Timer 14 Register	no
T14REL	$F0D0_H$ **E**	68_H	RTC Timer 14 Reload Register	no
T1IC b	$FF9E_H$	CF_H	CAPCOM Timer 1 Interrupt Ctrl. Reg.	0000_H
T1REL	$FE56_H$	$2B_H$	CAPCOM Timer 1 Reload Register	0000_H
T2	$FE40_H$	20_H	GPT1 Timer 2 Register	0000_H
T2CON b	$FF40_H$	$A0_H$	GPT1 Timer 2 Control Register	0000_H
T2IC b	$FF60_H$	$B0_H$	GPT1 Timer 2 Interrupt Control Register	0000_H
T3	$FE42_H$	21_H	GPT1 Timer 3 Register	0000_H
T3CON b	$FF42_H$	$A1_H$	GPT1 Timer 3 Control Register	0000_H
T3IC b	$FF62_H$	$B1_H$	GPT1 Timer 3 Interrupt Control Register	0000_H
T4	$FE44_H$	22_H	GPT1 Timer 4 Register	0000_H
T4CON b	$FF44_H$	$A2_H$	GPT1 Timer 4 Control Register	0000_H
T4IC b	$FF64_H$	$B2_H$	GPT1 Timer 4 Interrupt Control Register	0000_H
T5	$FE46_H$	23_H	GPT2 Timer 5 Register	0000_H
T5CON b	$FF46_H$	$A3_H$	GPT2 Timer 5 Control Register	0000_H
T5IC b	$FF66_H$	$B3_H$	GPT2 Timer 5 Interrupt Control Register	0000_H
T6	$FE48_H$	24_H	GPT2 Timer 6 Register	0000_H
T6CON b	$FF48_H$	$A4_H$	GPT2 Timer 6 Control Register	0000_H
T6IC b	$FF68_H$	$B4_H$	GPT2 Timer 6 Interrupt Control Register	0000_H
T7	$F050_H$ **E**	28_H	CAPCOM Timer 7 Register	0000_H
T78CON b	$FF20_H$	90_H	CAPCOM Timer 7 and 8 Ctrl. Reg.	0000_H
T7IC b	$F17A_H$ **E**	BD_H	CAPCOM Timer 7 Interrupt Ctrl. Reg.	0000_H
T7REL	$F054_H$ **E**	$2A_H$	CAPCOM Timer 7 Reload Register	0000_H

Parameter Interpretation

The parameters listed in the following partly represent the characteristics of the C161CS/JC/JI and partly its demands on the system. To aid in interpreting the parameters right, when evaluating them for a design, they are marked in column “Symbol”:

CC (**C**ontroller **C**haracteristics):
The logic of the C161CS/JC/JI will provide signals with the respective timing characteristics.

SR (**S**ystem **R**equirement):
The external system must provide signals with the respective timing characteristics to the C161CS/JC/JI.

DC Characteristics

(Operating Conditions apply)[1)]

Parameter	Symbol		Limit Values		Unit	Test Condition
			min.	max.		
Input low voltage (TTL, all except XTAL1, XTAL3, Port 9)	V_{IL}	SR	-0.5	0.2 V_{DD} - 0.1	V	–
Input low voltage XTAL1, XTAL3, Port 9	V_{IL2}	SR	-0.5	0.3 V_{DD}	V	–
Input low voltage (Special Threshold)	V_{ILS}	SR	-0.5	2.0	V	–
Input high voltage (TTL, all except $\overline{\text{RSTIN}}$, XTAL1, XTAL3, Port 9)	V_{IH}	SR	0.2 V_{DD} + 0.9	V_{DD} + 0.5	V	–
Input high voltage $\overline{\text{RSTIN}}$ (when operated as input)	V_{IH1}	SR	0.6 V_{DD}	V_{DD} + 0.5	V	–
Input high voltage XTAL1, XTAL3, Port 9	V_{IH2}	SR	0.7 V_{DD}	V_{DD} + 0.5	V	–
Input high voltage (Special Threshold)	V_{IHS}	SR	0.8 V_{DD} - 0.2	V_{DD} + 0.5	V	–
Input Hysteresis (Special Threshold)	HYS		400	–	mV	Series resistance = 0 Ω
Output low voltage (PORT0, PORT1, Port 4, ALE, $\overline{\text{RD}}$, $\overline{\text{WR}}$, $\overline{\text{BHE}}$, CLKOUT, $\overline{\text{RSTOUT}}$, $\overline{\text{RSTIN}}$[2)])	V_{OL}	CC	–	0.45	V	I_{OL} = 2.4 mA[3)] I_{OL} = 0.5 mA[4)]
Output low voltage (Port 9)	V_{OL9}	CC	–	0.4	V	I_{OL} = 3.0 mA

P0.15-13 (P0H.7-5). Register RP0H can be loaded from the upper half of register RSTCON under software control.

Table 10 associates the combinations of these three bits with the respective clock generation mode.

Table 10 C161CS/JC/JI Clock Generation Modes

CLKCFG (P0H.7-5)	CPU Frequency $f_{CPU} = f_{OSC} \times F$	External Clock Input Range[1)]	Notes
1 1 1	$f_{OSC} \times 4$	2.5 to 6.25 MHz	Default configuration
1 1 0	$f_{OSC} \times 3$	3.33 to 8.33 MHz	–
1 0 1	$f_{OSC} \times 2$	5 to 12.5 MHz	–
1 0 0	$f_{OSC} \times 5$	2 to 5 MHz	–
0 1 1	$f_{OSC} \times 1$	1 to 25 MHz	Direct drive[2)]
0 1 0	$f_{OSC} \times 1.5$	6.66 to 16.6 MHz	–
0 0 1	$f_{OSC} / 2$	2 to 50 MHz	CPU clock via prescaler
0 0 0	$f_{OSC} \times 2.5$	4 to 10 MHz	–

1) The external clock input range refers to a CPU clock range of 10 … 25 MHz.

2) The maximum frequency depends on the duty cycle of the external clock signal.

Prescaler Operation

When prescaler operation is configured (CLKCFG = 001_B) the CPU clock is derived from the internal oscillator (input clock signal) by a 2:1 prescaler.
The frequency of f_{CPU} is half the frequency of f_{OSC} and the high and low time of f_{CPU} (i.e. the duration of an individual TCL) is defined by the period of the input clock f_{OSC}.

The timings listed in the AC Characteristics that refer to TCLs therefore can be calculated using the period of f_{OSC} for any TCL.

Phase Locked Loop

When PLL operation is configured (via CLKCFG) the on-chip phase locked loop is enabled and provides the CPU clock (see table above). The PLL multiplies the input frequency by the factor **F** which is selected via the combination of pins P0.15-13 (i.e. $f_{CPU} = f_{OSC} \times$ **F**). With every **F**'th transition of f_{OSC} the PLL circuit synchronizes the CPU clock to the input clock. This synchronization is done smoothly, i.e. the CPU clock frequency does not change abruptly.

Due to this adaptation to the input clock the frequency of f_{CPU} is constantly adjusted so it is locked to f_{OSC}. The slight variation causes a jitter of f_{CPU} which also effects the duration of individual TCLs.

A/D Converter Characteristics

(Operating Conditions apply)

Table 13 A/D Converter Characteristics

Parameter	Symbol		Limit Values		Unit	Test Condition
			min.	max.		
Analog reference supply	V_{AREF}	SR	4.0	V_{DD} + 0.1	V	1)
Analog reference ground	V_{AGND}	SR	V_{SS} - 0.1	V_{SS} + 0.2	V	
Analog input voltage range	V_{AIN}	SR	V_{AGND}	V_{AREF}	V	2)
Basic clock frequency	f_{BC}		0.5	6.25	MHz	3)
Conversion time	t_C	CC	–	40 t_{BC} + t_S + 2t_{CPU}	–	4) $t_{CPU} = 1 / f_{CPU}$
Calibration time after reset	t_{CAL}	CC	–	3328 t_{BC}	–	5)
Total unadjusted error	TUE	CC	–	±2	LSB	1)
Internal resistance of reference voltage source	R_{AREF}	SR	–	t_{BC} / 60 - 0.25	kΩ	t_{BC} in [ns]6)7)
Internal resistance of analog source	R_{ASRC}	SR	–	t_S / 450 - 0.25	kΩ	t_S in [ns]7)8)
ADC input capacitance	C_{AIN}	CC	–	33	pF	7)

1) TUE is tested at V_{AREF} = 5.0 V, V_{AGND} = 0 V, V_{DD} = 4.9 V. It is guaranteed by design for all other voltages within the defined voltage range.
If the analog reference supply voltage exceeds the power supply voltage by up to 0.2 V (i.e. V_{AREF} = V_{DD} = +0.2 V) the maximum TUE is increased to ±3 LSB. This range is not 100% tested.
The specified TUE is guaranteed only if the absolute sum of input overload currents on Port 5 pins (see I_{OV} specification) does not exceed 10 mA.
During the reset calibration sequence the maximum TUE may be ±4 LSB.

2) V_{AIN} may exceed V_{AGND} or V_{AREF} up to the absolute maximum ratings. However, the conversion result in these cases will be $X000_H$ or $X3FF_H$, respectively.

3) The limit values for f_{BC} must not be exceeded when selecting the CPU frequency and the ADCTC setting.

4) This parameter includes the sample time t_S, the time for determining the digital result and the time to load the result register with the conversion result.
Values for the basic clock t_{BC} depend on programming and can be taken from **Table 14**.
This parameter depends on the ADC control logic. It is not a real maximum value, but rather a fixum.

5) During the reset calibration conversions can be executed (with the current accuracy). The time required for these conversions is added to the total reset calibration time.

6) During the conversion the ADC's capacitance must be repeatedly charged or discharged. The internal resistance of the reference voltage source must allow the capacitance to reach its respective voltage level within each conversion step. The maximum internal resistance results from the programmed conversion timing.

7) Not 100% tested, guaranteed by design and characterization.

Multiplexed Bus (cont'd)
(Operating Conditions apply)
ALE cycle time = 6 TCL + $2t_A$ + t_C + t_F (120 ns at 25 MHz CPU clock without waitstates)

Parameter	Symbol		Max. CPU Clock = 25 MHz		Variable CPU Clock 1 / 2TCL = 1 to 25 MHz		Unit
			min.	max.	min.	max.	
$\overline{RD}$, $\overline{WR}$ low time (no RW-delay)	t_{13}	CC	50 + t_C	–	3TCL - 10 + t_C	–	ns
$\overline{RD}$ to valid data in (with RW-delay)	t_{14}	SR	–	20 + t_C	–	2TCL - 20 + t_C	ns
$\overline{RD}$ to valid data in (no RW-delay)	t_{15}	SR	–	40 + t_C	–	3TCL - 20 + t_C	ns
ALE low to valid data in	t_{16}	SR	–	40 + t_A + t_C	–	3TCL - 20 + t_A + t_C	ns
Address to valid data in	t_{17}	SR	–	50 + $2t_A$ + t_C	–	4TCL - 30 + $2t_A$ + t_C	ns
Data hold after $\overline{RD}$ rising edge	t_{18}	SR	0	–	0	–	ns
Data float after $\overline{RD}$	t_{19}	SR	–	26 + t_F	–	2TCL - 14 + t_F	ns
Data valid to $\overline{WR}$	t_{22}	CC	20 + t_C	–	2TCL - 20 + t_C	–	ns
Data hold after $\overline{WR}$	t_{23}	CC	26 + t_F	–	2TCL - 14 + t_F	–	ns
ALE rising edge after $\overline{RD}$, $\overline{WR}$	t_{25}	CC	26 + t_F	–	2TCL - 14 + t_F	–	ns
Address hold after $\overline{RD}$, $\overline{WR}$	t_{27}	CC	26 + t_F	–	2TCL - 14 + t_F	–	ns
ALE falling edge to $\overline{CS}$[1)]	t_{38}	CC	-4 - t_A	10 - t_A	-4 - t_A	10 - t_A	ns
$\overline{CS}$ low to Valid Data In[1)]	t_{39}	SR	–	40 + t_C + $2t_A$	–	3TCL - 20 + t_C + $2t_A$	ns
$\overline{CS}$ hold after $\overline{RD}$, $\overline{WR}$[1)]	t_{40}	CC	46 + t_F	–	3TCL - 14 + t_F	–	ns
ALE fall. edge to $\overline{RdCS}$, $\overline{WrCS}$ (with RW delay)	t_{42}	CC	16 + t_A	–	TCL - 4 + t_A	–	ns

Demultiplexed Bus (cont'd)
(Operating Conditions apply)
ALE cycle time = 4 TCL + $2t_A$ + t_C + t_F (80 ns at 25 MHz CPU clock without waitstates)

Parameter	Symbol		Max. CPU Clock = 25 MHz		Variable CPU Clock 1 / 2TCL = 1 to 25 MHz		Unit
			min.	max.	min.	max.	
Data valid to $\overline{WR}$	t_{22}	CC	20 + t_C	–	2TCL - 20 + t_C	–	ns
Data hold after $\overline{WR}$	t_{24}	CC	10 + t_F	–	TCL - 10 + t_F	–	ns
ALE rising edge after $\overline{RD}$, $\overline{WR}$	t_{26}	CC	-10 + t_F	–	-10 + t_F	–	ns
Address hold after $\overline{WR}$[2]	t_{28}	CC	0 + t_F	–	0 + t_F	–	ns
ALE falling edge to $\overline{CS}$[3]	t_{38}	CC	-4 - t_A	10 - t_A	-4 - t_A	10 - t_A	ns
$\overline{CS}$ low to Valid Data In[3]	t_{39}	SR	–	40 + t_C + $2t_A$	–	3TCL - 20 + t_C + $2t_A$	ns
$\overline{CS}$ hold after $\overline{RD}$, $\overline{WR}$[3]	t_{41}	CC	6 + t_F	–	TCL - 14 + t_F	–	ns
ALE falling edge to $\overline{RdCS}$, $\overline{WrCS}$ (with RW-delay)	t_{42}	CC	16 + t_A	–	TCL - 4 + t_A	–	ns
ALE falling edge to $\overline{RdCS}$, $\overline{WrCS}$ (no RW-delay)	t_{43}	CC	-4 + t_A	–	-4 + t_A	–	ns
$\overline{RdCS}$ to Valid Data In (with RW-delay)	t_{46}	SR	–	16 + t_C	–	2TCL - 24 + t_C	ns
$\overline{RdCS}$ to Valid Data In (no RW-delay)	t_{47}	SR	–	36 + t_C	–	3TCL - 24 + t_C	ns
$\overline{RdCS}$, $\overline{WrCS}$ Low Time (with RW-delay)	t_{48}	CC	30 + t_C	–	2TCL - 10 + t_C	–	ns
$\overline{RdCS}$, $\overline{WrCS}$ Low Time (no RW-delay)	t_{49}	CC	50 + t_C	–	3TCL - 10 + t_C	–	ns
Data valid to $\overline{WrCS}$	t_{50}	CC	26 + t_C	–	2TCL - 14 + t_C	–	ns
Data hold after $\overline{RdCS}$	t_{51}	SR	0	–	0	–	ns
Data float after $\overline{RdCS}$ (with RW-delay)[1]	t_{53}	SR	–	20 + t_F	–	2TCL - 20 + $2t_A$ + t_F[1]	ns

Demultiplexed Bus (cont'd)
(Operating Conditions apply)
ALE cycle time = 4 TCL + 2t_A + t_C + t_F (80 ns at 25 MHz CPU clock without waitstates)

Parameter	Symbol		Max. CPU Clock = 25 MHz		Variable CPU Clock 1 / 2TCL = 1 to 25 MHz		Unit
			min.	max.	min.	max.	
Data float after $\overline{\text{RdCS}}$ (no RW-delay)[1]	t_{68}	SR	–	0 + t_F	–	TCL - 20 + 2t_A + t_F[1]	ns
Address hold after $\overline{\text{RdCS}}$, $\overline{\text{WrCS}}$	t_{55}	CC	-6 + t_F	–	-6 + t_F	–	ns
Data hold after $\overline{\text{WrCS}}$	t_{57}	CC	6 + t_F	–	TCL - 14 + t_F	–	ns

1) RW-delay and t_A refer to the next following bus cycle (including an access to an on-chip X-Peripheral).

2) Read data are latched with the same clock edge that triggers the address change and the rising $\overline{\text{RD}}$ edge. Therefore address changes before the end of $\overline{\text{RD}}$ have no impact on read cycles.

3) These parameters refer to the latched chip select signals ($\overline{\text{CSxL}}$). The early chip select signals ($\overline{\text{CSxE}}$) are specified together with the address and signal $\overline{\text{BHE}}$ (see figures below).

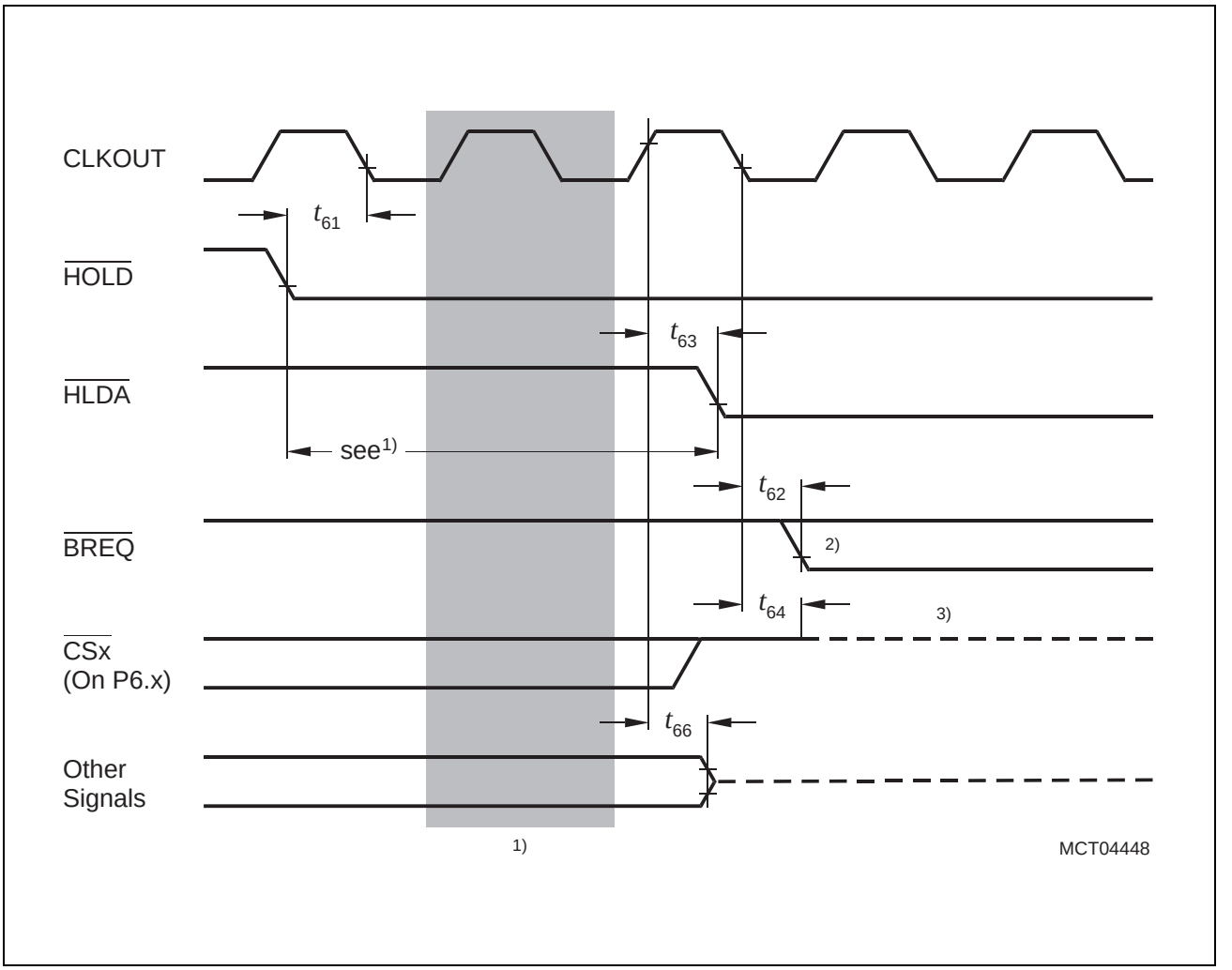

Figure 25 External Bus Arbitration, Releasing the Bus

Notes
1) The C161CS/JC/JI will complete the currently running bus cycle before granting bus access.
2) This is the first possibility for $\overline{\text{BREQ}}$ to get active.
3) The $\overline{\text{CS}}$ outputs will be resistive high (pullup) after t_{64}.

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