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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

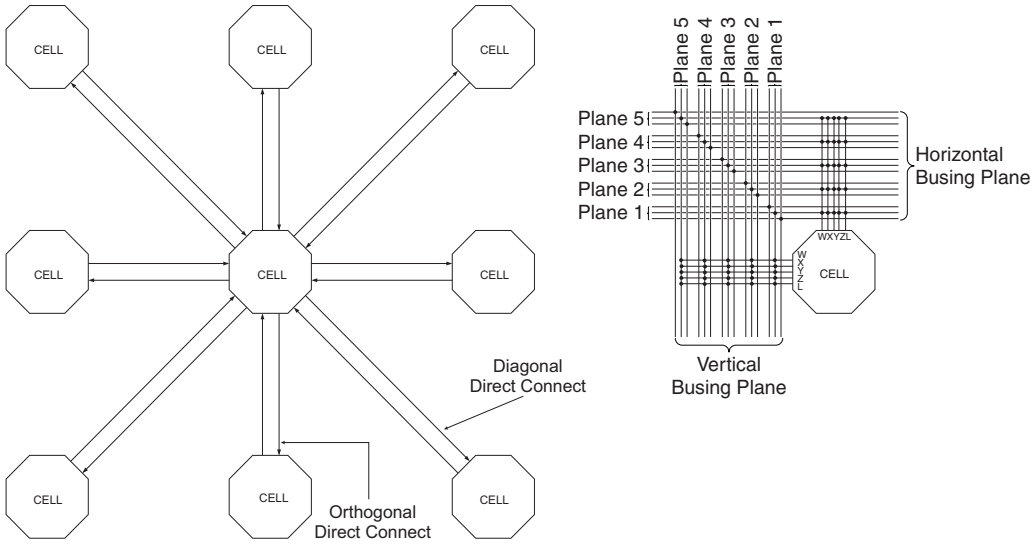
The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	1024
Total RAM Bits	8192
Number of I/O	193
Number of Gates	30000
Voltage - Supply	4.5V ~ 5.5V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 85°C (TC)
Package / Case	240-BFQFP
Supplier Device Package	240-PQFP (32x32)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/at40k20-2eqj

4. Cell Connections

Figure 4-1(a) depicts direct connections between a cell and its eight nearest neighbors. Figure 4-1(b) shows the connections between a cell and five horizontal local buses (one per busing plane) and five vertical local buses (one per busing plane).

Figure 4-1. Cell Connections



(a) Cell-to-cell Connections

(b) Cell-to-bus Connections

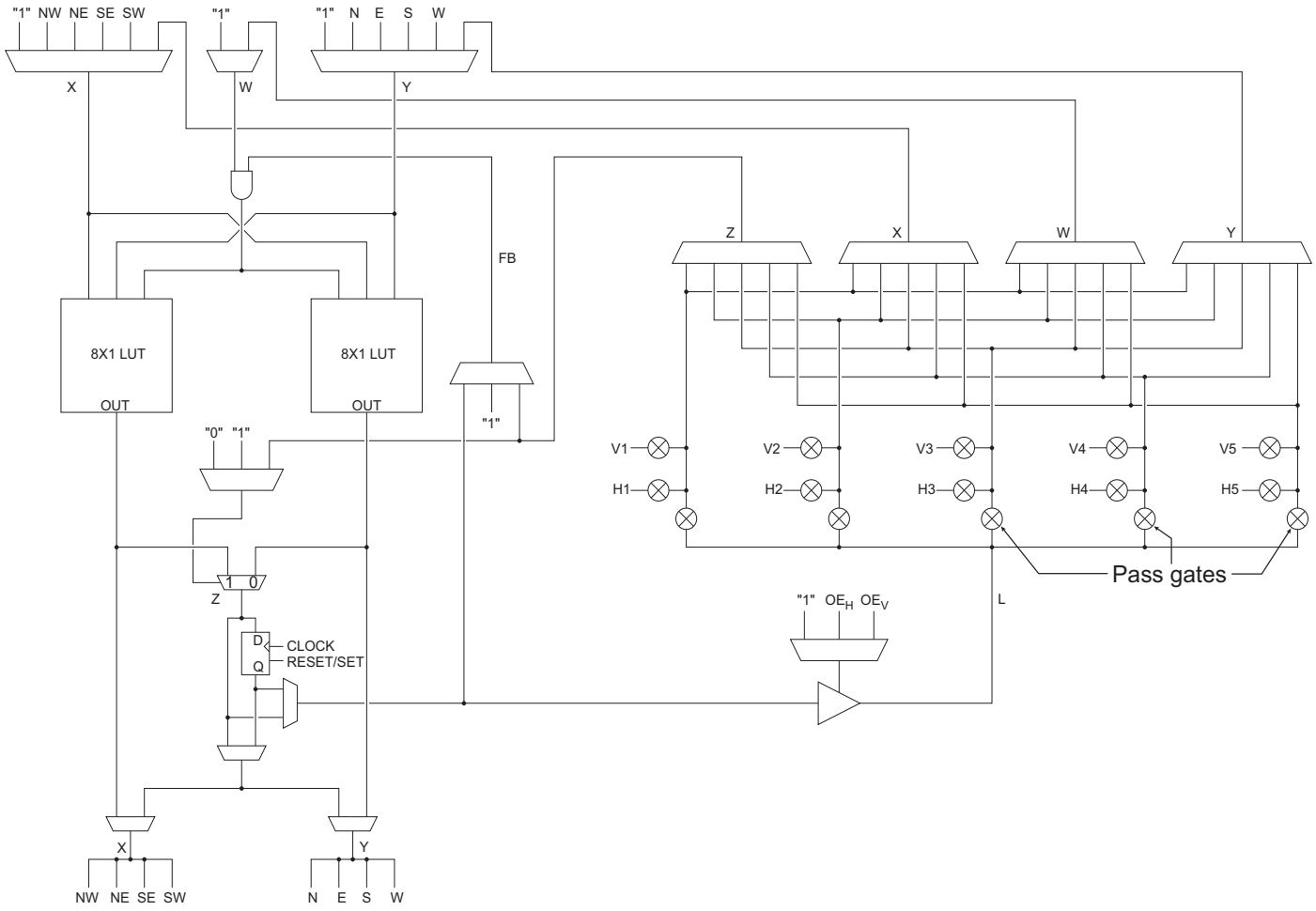
5. The Cell

Figure 5-1 depicts the AT40K cell. Configuration bits for separate muxes and pass gates are independent. All permutations of programmable muxes and pass gates are legal. V_n (V_1 – V_5) is connected to the vertical local bus in plane n. H_n (H_1 – H_5) is connected to the horizontal local bus in plane *n*. A local/local turn in plane n is achieved by turning on the two pass gates connected to V_n and H_n. Pass gates are opened to let signals into the cell from a local bus or to drive a signal out onto a local bus. Signals coming into the logic cell on one local bus plane can be switched onto another plane by opening two of the pass gates. This allows bus signals to switch planes to achieve greater route ability. Up to five simultaneous local/local turns are possible.

The AT40K FPGA core cell is a highly configurable logic block based around two 3-input LUTs (8 x 1 ROM), which can be combined to produce one 4-input LUT. This means that any core cell can implement two functions of three inputs or one function of four inputs. There is a Set/Reset D flip-flop in every cell, the output of which may be tri-stated and fed back internally within the core cell. There is also a 2-to-1 multiplexer in every cell, and an upstream AND gate in the “front end” of the cell. This AND gate is an important feature in the implementation of efficient array multipliers.

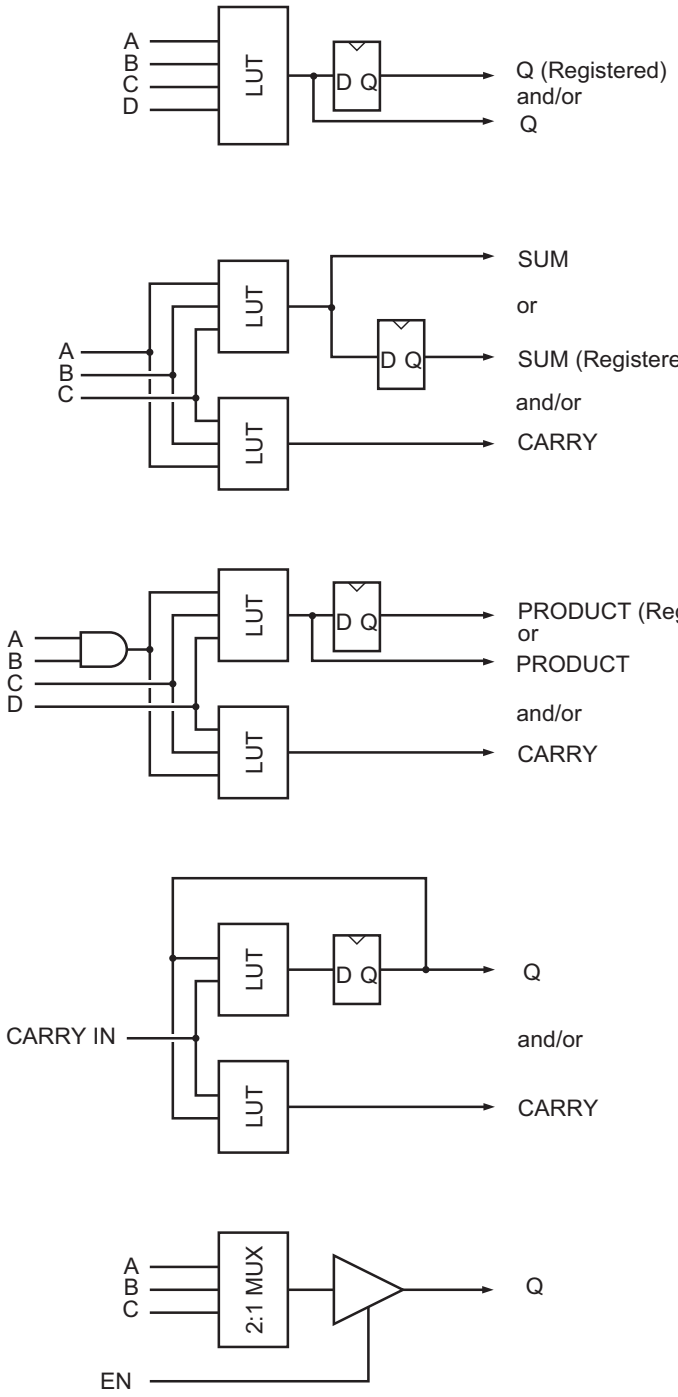
With this functionality in each core cell, the core cell can be configured in several modes. The core cell flexibility makes the AT40K architecture well suited to most digital design application areas, see Figure 5-2.

Figure 5-1. The Cell



X = Diagonal Direct Connect or Bus
Y = Orthogonal Direct Connect or Bus
W = Bus Connection
Z = Bus Connection
FB = Internal Feedback

Figure 5-2. Some Single Cell Modes



Synthesis Mode. This mode is particularly important for the use of VHDL/Verilog design. VHDL/Verilog Synthesis tools generally will produce as their output large amounts of random logic functions. Having a 4-input LUT structure gives efficient random logic optimization without the delays associated with larger LUT structures. The output of any cell may be registered, tri-stated and/or fed back into a core cell.

Arithmetic Mode is frequently used in many designs. As can be seen in the figure, the AT40K core cell can implement a 1-bit full adder (2-input adder with both Carry In and Carry Out) in one core cell. Note that the sum output in this diagram is registered. This output could then be tri-stated and/or fed back into the cell.

DSP/Multiplier Mode. This mode is used to efficiently implement array multipliers. An array multiplier is an array of bitwise multipliers, each implemented as a full adder with an upstream AND gate. Using this AND gate and the diagonal interconnects between cells, the array multiplier structure fits very well into the AT40K architecture.

Counter Mode. Counters are fundamental to almost all digital designs. They are the basis of state machines, timing chains and clock dividers. A counter is essentially an increment by one function (i.e., an adder), with the input being an output (or a decode of an output) from the previous stage. A 1-bit counter can be implemented in one core cell. Again, the output can be registered, tri-stated and/or fed back.

Tri-state/Mux Mode. This mode is used in many telecommunications applications, where data needs to be routed through more than one possible path. The output of the core cell is very often tri-statable for many inputs to many outputs data switching.

7. Clocking Scheme

There are eight Global Clock buses (GCK1 – GCK8) on the AT40K FPGA. Each of the eight dedicated Global Clock buses is connected to one of the dual-use Global Clock pins. Any clocks used in the design should use global clocks where possible: this can be done by using Assign Pin Locks to lock the clocks to the Global Clock locations. In addition to the eight Global Clocks, there are four Fast Clocks (FCK1 – FCK4), two per edge column of the array for PCI specification.

Each column of an array has a “Column Clock mux” and a “Sector Clock mux”. The Column Clock mux is at the top of every column of an array and the Sector Clock mux is at every four cells. The Column Clock mux is selected from one of the eight Global Clock buses. The clock provided to each sector column of four cells is inverted, non-inverted or tied off to “0”, using the Sector Clock mux to minimize the power consumption in a sector that has no clocks. The clock can either come from the Column Clock or from the Plane 4 express bus, see Figure 7-1. The extreme-left Column Clock mux has two additional inputs, FCK1 and FCK2, to provide fast clocking to left-side I/Os. The extreme-right Column Clock mux has two additional inputs as well, FCK3 and FCK4, to provide fast clocking to right-side I/Os.

The register in each cell is triggered on a rising clock edge by default. Before configuration on power-up, constant “0” is provided to each register’s clock pins. After configuration on power-up, the registers either set or reset, depending on the user’s choice.

The clocking scheme is designed to allow efficient use of multiple clocks with low clock skew, both within a column and across the core cell array.

Figure 8-1. Set/Reset (for One Column of Cells)

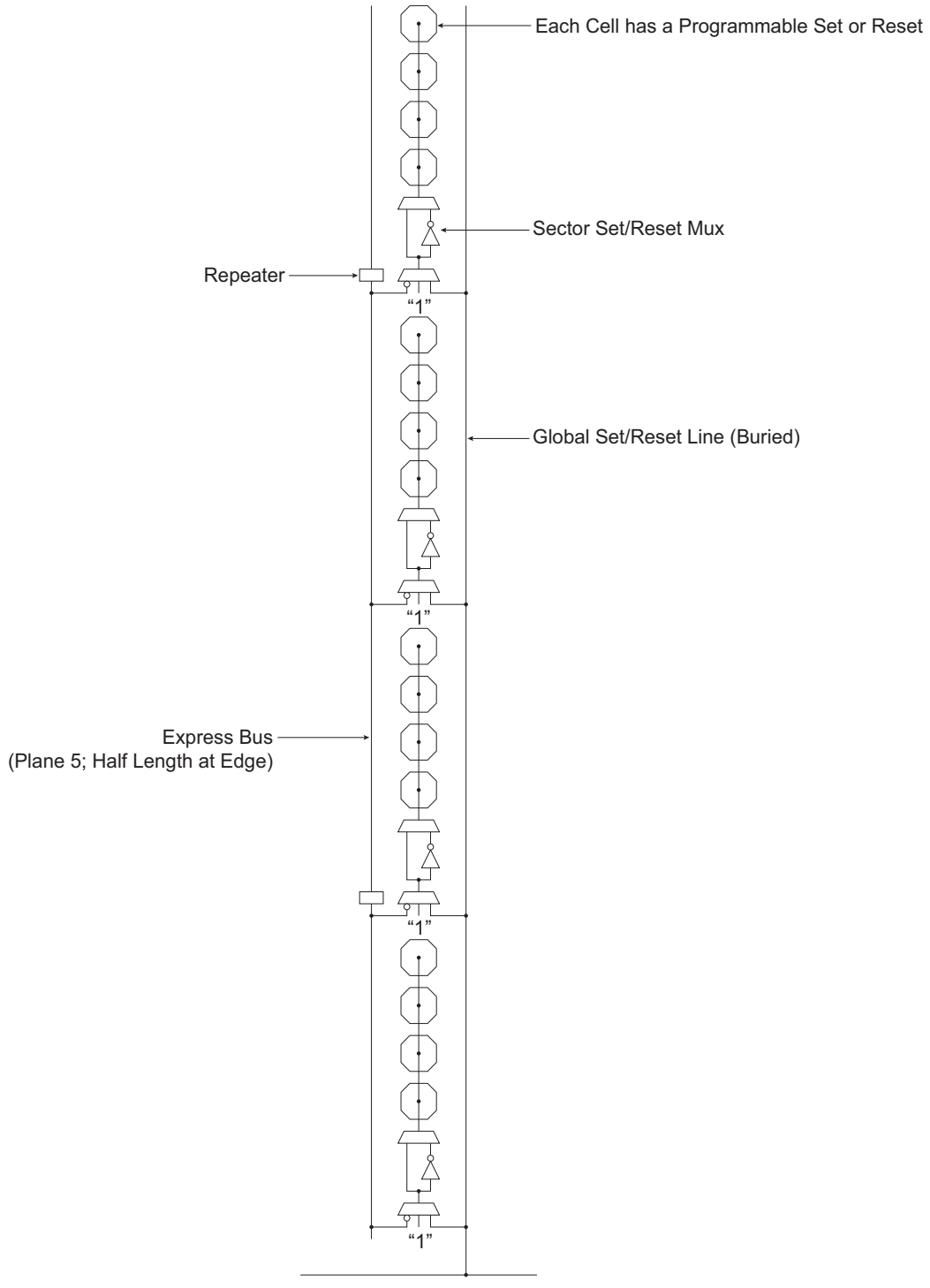
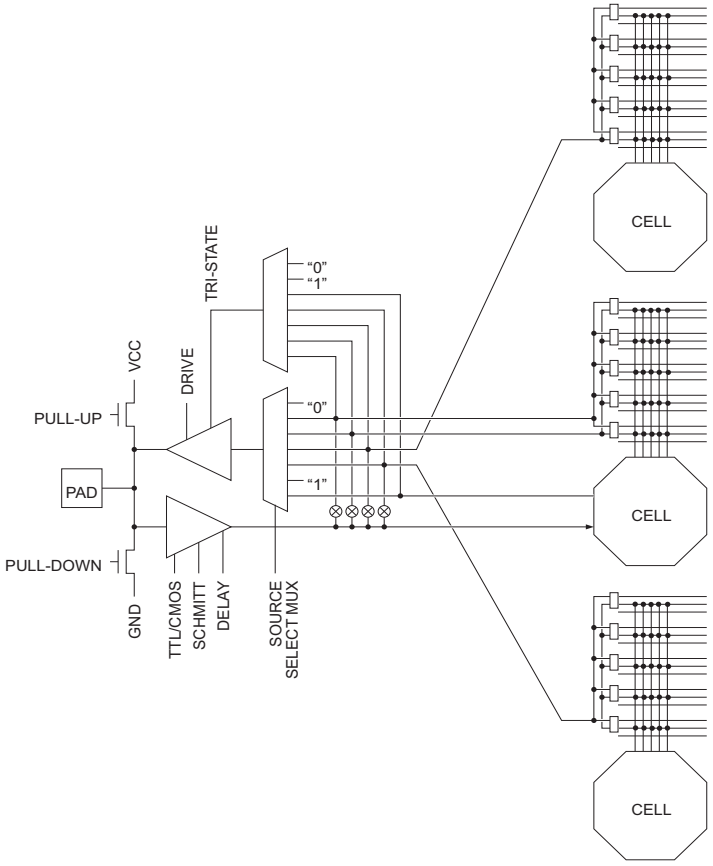
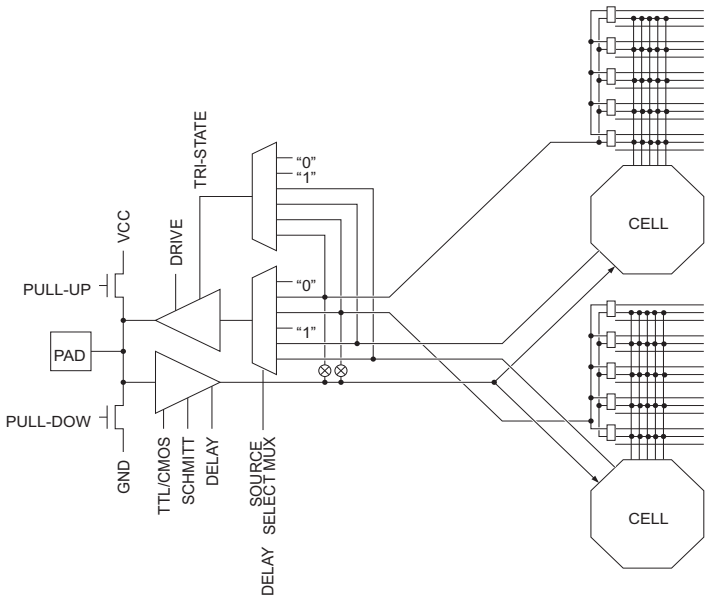


Figure 9-1. West I/O (Mirrored for East I/O) AT40K

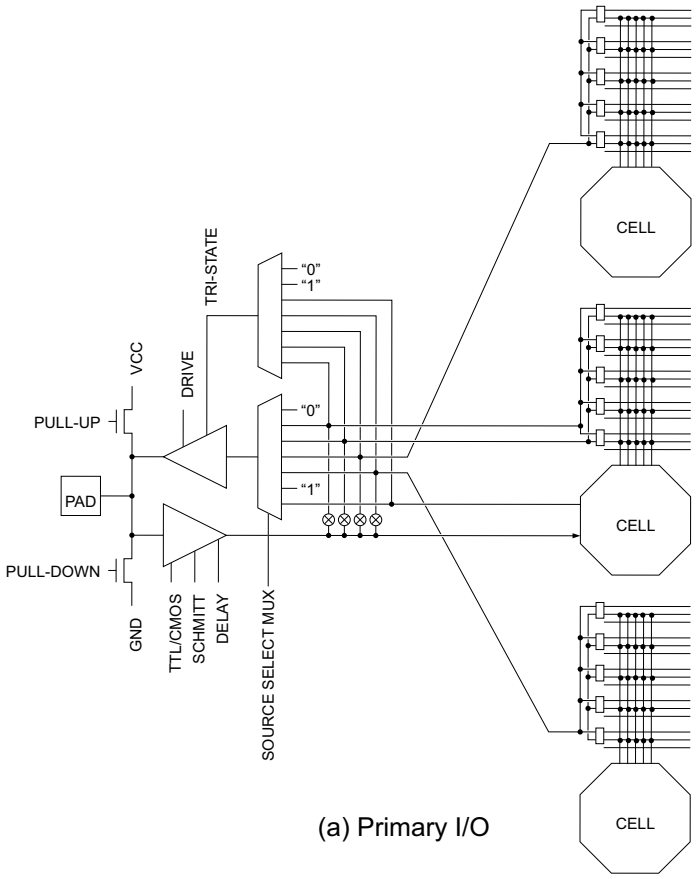


(a) Primary I/O

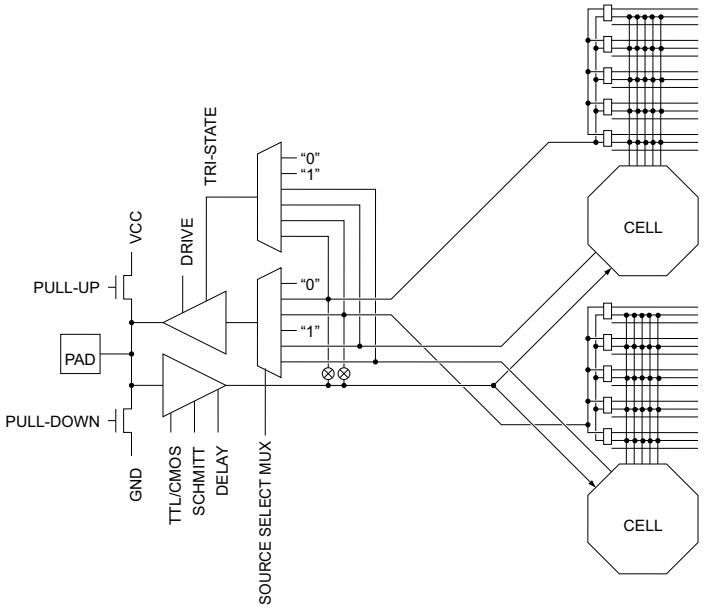


(b) Secondary I/O

Figure 9-2. South I/O (Mirrored for North I/O) AT40K



(a) Primary I/O



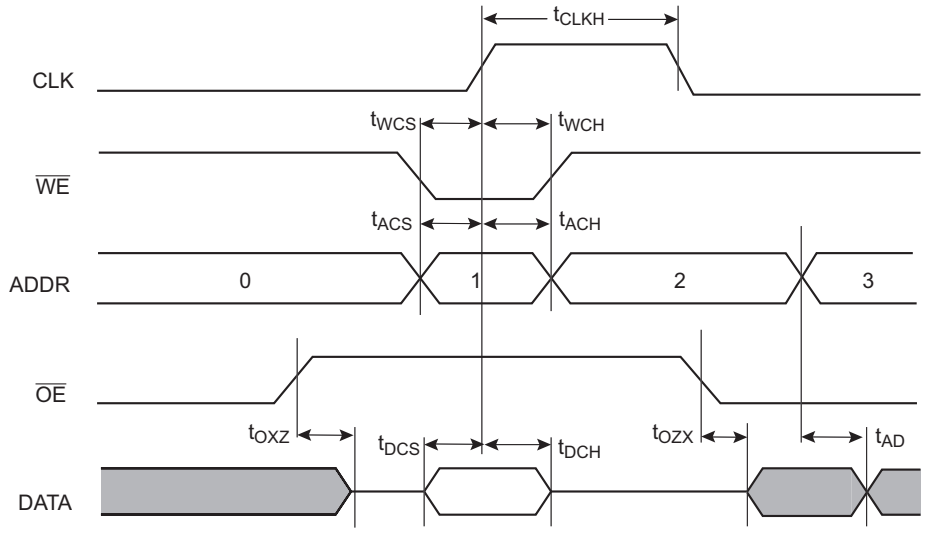
(a) Secondary I/O

10.3 DC Characteristics — 5V Operation Commercial/Industrial/Military AT40K

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{IH}	High-level Input Voltage	CMOS	70% V_{CC}			V
		TTL	2.0			V
V_{IL}	Low-level Input Voltage	CMOS	-0.3		30% V_{CC}	V
		TTL	-0.3		0.8	V
V_{OH}	High-level Output Voltage	I_{OH} = 6mA V_{CC} = V_{CC} Minimum	Ind. = 3.15 4.0 Con = 3.325			V
		I_{OH} = 14mA V_{CC} = V_{CC} Minimum	Ind. = 3.15 4.0 Con = 3.325			V
		I_{OH} = 20mA Commercial = 4.75V Industrial/Military = 4.5V	Ind. = 3.15 4.0 Con = 3.325			V
V_{OL}	Low-level Output Voltage	I_{OL} = -6mA Commercial = 4.75V Industrial/Military = 4.5V			0.4	V
		I_{OL} = -14mA Commercial = 4.75V Industrial/Military = 4.5V			0.4	V
		I_{OL} = -20mA Commercial = 4.75V Industrial/Military = 4.5V			0.4	V
I_{IH}	High-level Input Current	V_{IN} = V_{CC} Maximum			10.0	µA
		With pull-down, V_{IN} = V_{CC}	125.0	250.0	500.0	µA
I_{IL}	Low-level Input Current	V_{IN} = V_{SS}	-10.0			µA
		With pull-up, V_{IN} = V_{SS}	CON = -1mA to -250µA	-250.0	CON = -1mA to -250µA	µA
I_{OZH}	High-level Tri-state Output Leakage Current	Without pull-down, V_{IN} = V_{CC}			10.0	µA
		With pull-down, V_{IN} = V_{CC}	125.0	250.0	500.0	µA
I_{OZL}	Low-level Tri-state Output Leakage Current	Without pull-up, V_{IN} = V_{SS} Maximum	-10.0			µA
		With pull-up, V_{IN} = V_{SS} Maximum	-500.0	-250.0	-125.0	µA
I_{CC}	Standby Current Consumption	Standby, unprogrammed		0.6	1.0	mA
C_{IN}	Input Capacitance	All pins			10.0	pF

12. FreeRAM Synchronous Timing Characteristics

12.1 Single-port Write/Read



12.2 Dual-port Write with Read

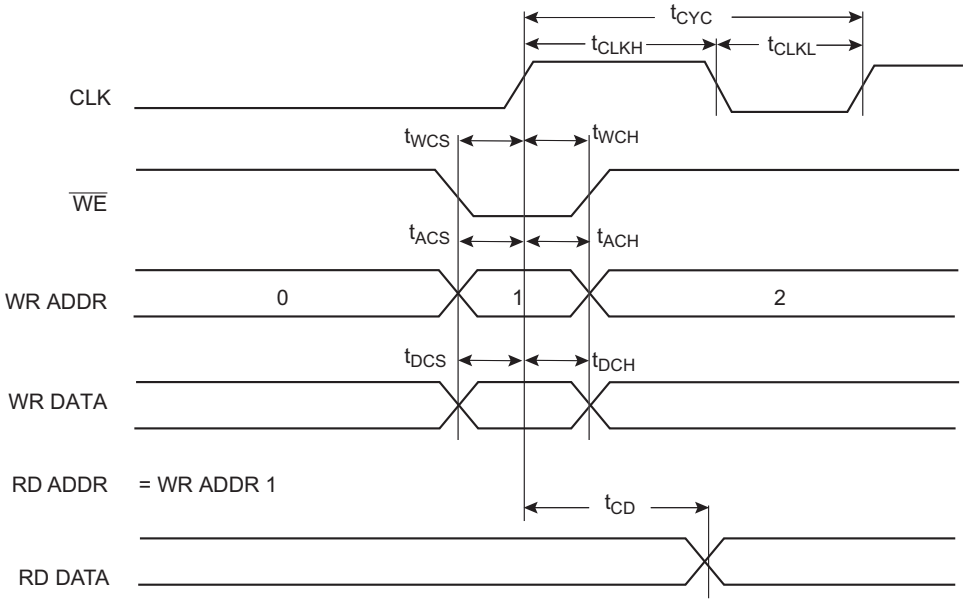


Table 12-1. Left Side (Top to Bottom)

AT40K05	AT40K10	AT40K20	AT40K40	Left Side (Top to Bottom)								
128 I/O	192 I/O	256 I/O	384 I/O	84 PLCC	100 PQFP	100 TQFP	144 LQFP	160 PQFP	208 PQFP	240 PQFP	304 PQFP[2]	352 SBGA[2]
GND	GND	GND	GND	12	4	1	1	1	2	1	304	GND[1]
I/O1, GCK1 (A16)	I/O1, GCK1 (A16)	I/O1, GCK1 (A16)	I/O1, GCK1 (A16)	13	5	2	2	2	4	2	303	D23
I/O2 (A17)	I/O2 (A17)	I/O2 (A17)	I/O2 (A17)	14	6	3	3	3	5	3	302	C25
I/O3	I/O3	I/O3	I/O3				4	4	6	4	301	D24
I/O4	I/O4	I/O4	I/O4				5	5	7	5	300	E23
I/O5 (A18)	I/O5 (A18)	I/O5 (A18)	I/O5 (A18)	15	7	4	6	6	8	6	299	C26
I/O6 (A19)	I/O6 (A19)	I/O6 (A19)	I/O6 (A19)	16	8	5	7	7	9	7	298	E24
			GND									
			I/O7									
			I/O8									
			I/O9									D25
			I/O10									F23
		I/O7	I/O11								297	F24
		I/O8	I/O12								296	E25
		VCC	VCC									VCC[1]
		GND	GND									GND[1]
			I/O13									
			I/O14									
I/O7	I/O7	I/O9	I/O15					8	10	8	295	D26
I/O8	I/O8	I/O10	I/O16					9	11	9	294	G24
	I/O9	I/O11	I/O17						12	10	293	F25
	I/O10	I/O12	I/O18						13	11	292	F26
			GND									
			I/O19									
			I/O20									
	I/O11	I/O13	I/O21							12	291	H23
	I/O12	I/O14	I/O22							13	290	H24
		I/O15	I/O23								289	G25
		I/O16	I/O24								288	G26

Notes:
1. Pads labeled GND or V_{CC} are internally bonded to Ground or V_{CC} planes within the package. They have no direct connection to any specific package pin.
2. This package has an inverted die.
3. On-chip tri-state.

Table 12-1. Left Side (Top to Bottom) (Continued)

AT40K05	AT40K10	AT40K20	AT40K40	Left Side (Top to Bottom)								
128 I/O	192 I/O	256 I/O	384 I/O	84 PLCC	100 PQFP	100 TQFP	144 LQFP	160 PQFP	208 PQFP	240 PQFP	304 PQFP[2]	352 SBGA[2]
I/O24, FCK2	I/O36, FCK2	I/O48, FCK2	I/O72, FCK2				26	28	36	44	249	U23
GND	GND	GND	GND				27	29	37	45	248	GND[1]
		I/O49	I/O73								247	Y26
		I/O50	I/O74								246	W25
	I/O37	I/O51	I/O75							46	245	W24
	I/O38	I/O52	I/O76							47	244	V23
			I/O77									
			I/O78									
			GND									
			I/O79									
			I/O80									
	I/O39	I/O53	I/O81						38	48	243	AA26
	I/O40	I/O54	I/O82						39	49	242	Y25
I/O25	I/O41	I/O55	I/O83					30	40	50	241	Y24
I/O26	I/O42	I/O56	I/O84					31	41	51	240	AA25
		GND	GND									GND[1]
		VCC	VCC									VCC[1]
		I/O57	I/O85								239	AB25
		I/O58	I/O86								238	AA24
			I/O87									
			I/O88									
I/O27	I/O43	I/O59	I/O89	27	21	18	28	32	42	52	237	Y23
I/O28	I/O44	I/O60	I/O90		22	19	29	33	43	53	236	AC26
			GND									
			I/O91									AD26
			I/O92									AC25
I/O29	I/O45	I/O61	I/O93				30	34	44	54	235	AA23
I/O30	I/O46	I/O62	I/O94				31	35	45	55	234	AB24
I/O31 ($\overline{OTS}$)[3]	I/O47 ($\overline{OTS}$)[3]	I/O63 ($\overline{OTS}$)[3]	I/O95 ($\overline{OTS}$)[3]	28	23	20	32	36	46	56	233	AD25
I/O32, GCK2	I/O48, GCK2	I/O64, GCK2	I/O96, GCK2	29	24	21	33	37	47	57	232	AC24

Notes:
1. Pads labeled GND or V_{CC} are internally bonded to Ground or V_{CC} planes within the package. They have no direct connection to any specific package pin.
2. This package has an inverted die.
3. On-chip tri-state.

Table 12-1. Left Side (Top to Bottom) (Continued)

AT40K05	AT40K10	AT40K20	AT40K40	Left Side (Top to Bottom)								
128 I/O	192 I/O	256 I/O	384 I/O	84 PLCC	100 PQFP	100 TQFP	144 LQFP	160 PQFP	208 PQFP	240 PQFP	304 PQFP[2]	352 SBGA[2]
M1	M1	M1	M1	30	25	22	34	38	48	58	231	AB23
GND	GND	GND	GND	31	26	23	35	39	49	59	230	GND[1]
M0	M0	M0	M0	32	27	24	36	40	50	60	229	AD24

Notes: 1. Pads labeled GND or V_{CC} are internally bonded to Ground or V_{CC} planes within the package. They have no direct connection to any specific package pin.
2. This package has an inverted die.
3. On-chip tri-state.

Table 12-2. Bottom Side (Left to Right)

AT40K05	AT40K10	AT40K20	AT40K40	Bottom Side (Left to Right)								
128 I/O	192 I/O	256 I/O	384 I/O	84 PLCC	100 PQFP	100 TQFP	144 LQFP	160 PQFP	208 PQFP	240 PQFP	304 PQFP[1]	352 SBGA[2]
VCC	VCC	VCC	VCC	33	28	25	37	41	55	61	228	VCC[1]
M2	M2	M2	M2	34	29	26	38	42	56	62	227	AC23
I/O33, GCK3	I/O49, GCK3	I/O65, GCK3	I/O97, GCK3	35	30	27	39	43	57	63	226	AE24
I/O34 (HDC)	I/O50 (HDC)	I/O66 (HDC)	I/O98 (HDC)	36	31	28	40	44	58	64	225	AD23
I/O35	I/O51	I/O67	I/O99				41	45	59	65	224	AC22
I/O36	I/O52	I/O68	I/O100				42	46	60	66	223	AF24
I/O37	I/O53	I/O69	I/O101		32	29	43	47	61	67	222	AD22
I/O38 (LDC)	I/O54 (LDC)	I/O70 (LDC)	I/O102 (LDC)	37	33	30	44	48	62	68	221	AE23
			GND									
			I/O103									
			I/O104									
			I/O105									AC21
			I/O106									AD21
		I/O71	I/O107								220	AE22
		I/O72	I/O108								219	AF23
		VCC	VCC									VCC[1]
		GND	GND									GND[1]
I/O39	I/O55	I/O73	I/O109					49	63	69	218	AD20
I/O40	I/O56	I/O74	I/O110					50	64	70	217	AE21
	I/O57	I/O75	I/O111						65	71	216	AF21

Notes: 1. Pads labeled GND or VCC are internally bonded to Ground or VCC planes within the package. They have no direct connection to any specific package pin.
2. This package has an inverted die.

Table 12-2. Bottom Side (Left to Right) (Continued)

AT40K05	AT40K10	AT40K20	AT40K40	Bottom Side (Left to Right)								
128 I/O	192 I/O	256 I/O	384 I/O	84 PLCC	100 PQFP	100 TQFP	144 LQFP	160 PQFP	208 PQFP	240 PQFP	304 PQFP[1]	352 SBGA[2]
			GND									
			I/O139									
			I/O140									
			I/O141									
			I/O142									
I/O47 (D15)	I/O71 (D15)	I/O95 (D15)	I/O143 (D15)	40	38	35	52	58	76	88	193	AE14
I/O48 (INIT)	I/O72 (INIT)	I/O96 (INIT)	I/O144 (INIT)	41	39	36	53	59	77	89	192	AF14
VCC	VCC	VCC	VCC	42	40	37	54	60	78	90	191	VCC[1]
GND	GND	GND	GND	43	41	38	55	61	79	91	190	GND[1]
I/O49 (D14)	I/O73 (D14)	I/O97 (D14)	I/O145 (D14)	44	42	39	56	62	80	92	189	AE13
I/O50 (D13)	I/O74 (D13)	I/O98 (D13)	I/O146 (D13)	45	43	40	57	63	81	93	188	AC13
			I/O147									
			I/O148									
			I/O149									
			I/O150									
			GND									
I/O51	I/O75	I/O99	I/O151		44	41	58	64	82	94	187	AD13
I/O52	I/O76	I/O100	I/O152		45	42	59	65	83	95	186	AF12
	I/O77	I/O101	I/O153						84	96	185	AE12
	I/O78	I/O102	I/O154						85	97	184	AD12
		I/O103	I/O155								183	AC12
		I/O104	I/O156								182	AF11
			VCC									VCC[1]
		GND	GND							98		GND[1]
		I/O105	I/O157								181	AE11
		I/O106	I/O158								180	AD11
			I/O159									AE10
			I/O160									AC11
			I/O161									
			I/O162									

Notes: 1. Pads labeled GND or VCC are internally bonded to Ground or VCC planes within the package. They have no direct connection to any specific package pin.

2. This package has an inverted die.

Table 12-3. Right Side (Bottom to Top) (Continued)

AT40K05	AT40K10	AT40K20	AT40K40	Right Side (Bottom to Top)								
128 I/O	192 I/O	256 I/O	384 I/O	84 PLCC	100 PQFP	100 TQFP	144 LQFP	160 PQFP	208 PQFP	240 PQFP	304 PQFP(2)	352 SBGA(2)
		VCC	VCC									VCC(1)
		GND	GND									GND(1)
I/O69 (D6)	I/O103 (D6)	I/O137 (D6)	I/O205 (D6)	58	58	55	79	87	113	129	142	Y3
I/O70	I/O104	I/O138	I/O206		59	56	80	88	114	130	141	AA2
I/O71	I/O105	I/O139	I/O207					89	115	131	140	AA1
I/O72	I/O106	I/O140	I/O208					90	116	132	139	W4
			I/O209									
			I/O210									
			GND									
			I/O211									
			I/O212									
	I/O107	I/O141	I/O213						117	133	138	W3
	I/O108	I/O142	I/O214						118	134	137	Y2
		I/O143	I/O215								136	Y1
		I/O144	I/O216								135	V4
GND	GND	GND	GND				81	91	119	135	134	GND(1)
	I/O109	I/O145	I/O217							136	133	V3
	I/O110	I/O146	I/O218							137	132	W2
I/O73, FCK3	I/O111, FCK3	I/O147, FCK3	I/O219, FCK3				82	92	120	138	131	U4
I/O74	I/O112	I/O148	I/O220				83	93	121	139	130	U3
	VCC	VCC	VCC							140	129	VCC(1)
I/O75 (D5)	I/O113 (D5)	I/O149 (D5)	I/O221 (D5)	59	60	57	84	94	122	141	127	V2
I/O76 (CS0)	I/O114 (CS0)	I/O150 (CS0)	I/O222 (CS0)	60	61	58	85	95	123	142	126	V1
			GND									
			I/O223									T4
			I/O224									T3
			I/O225									
			I/O226									
		I/O151	I/O227								125	U2
		I/O152	I/O228								124	T2
		GND	GND							143		GND(1)

Notes: 1. Pads labeled GND or VCC are internally bonded to Ground or VCC planes within the package. They have no direct connection to any specific package pin.

2. This package has an inverted die.

Table 12-3. Right Side (Bottom to Top) (Continued)

AT40K05	AT40K10	AT40K20	AT40K40	Right Side (Bottom to Top)								
128 I/O	192 I/O	256 I/O	384 I/O	84 PLCC	100 PQFP	100 TQFP	144 LQFP	160 PQFP	208 PQFP	240 PQFP	304 PQFP(2)	352 SBGA(2)
		I/O170	I/O254								104	L3
			I/O255									K2
			I/O256									L4
			I/O257									
			I/O258									
			GND									
I/O85 (D2)	I/O127 (D2)	I/O171 (D2)	I/O259 (D2)	67	71	68	96	106	138	159	103	J1
I/O86	I/O128	I/O172	I/O260	68	72	69	97	107	139	160	102	K3
	VCC	VCC	VCC							161	101	VCC(1)
I/O87	I/O129	I/O173	I/O261				98	108	140	162	99	J2
I/O88, FCK4	I/O130, FCK4	I/O174, FCK4	I/O262, FCK4				99	109	141	163	98	J3
	I/O131	I/O175	I/O263							164	97	K4
	I/O132	I/O176	I/O264							165	96	G1
GND	GND	GND	GND				100	110	142	166	95	GND(1)
		I/O177	I/O265								94	H2
		I/O178	I/O266								93	H3
	I/O133	I/O179	I/O267							167	92	J4
	I/O134	I/O180	I/O268							168	91	F1
			I/O269									
			I/O270									
			GND									
	I/O135	I/O181	I/O271						143	169	90	G2
	I/O136	I/O182	I/O272						144	170	89	G3
I/O89	I/O137	I/O183	I/O273					111	145	171	88	F2
I/O90	I/O138	I/O184	I/O274					112	146	172	87	E2
			I/O275									
			I/O276									
		GND	GND									GND(1)
		VCC	VCC									VCC(1)
I/O91 (D1)	I/O139 (D1)	I/O185 (D1)	I/O277 (D1)	69	73	70	101	113	147	173	86	F3
I/O92	I/O140	I/O186	I/O278	70	74	71	102	114	148	174	85	G4

Notes: 1. Pads labeled GND or VCC are internally bonded to Ground or VCC planes within the package. They have no direct connection to any specific package pin.

2. This package has an inverted die.

Table 12-4. Top Side (Right to Left) (Continued)

AT40K05	AT40K10	AT40K20	AT40K40	Top Side (Right to Left)								
128 I/O	192 I/O	256 I/O	384 I/O	84 PLCC	100 PQFP	100 TQFP	144 LQFP	160 PQFP	208 PQFP	240 PQFP	304 PQFP(2)	352 SBGA(2)
I/O121	I/O183	I/O245	I/O369					152	197	230	14	C20
I/O122	I/O184	I/O246	I/O370					153	198	231	13	B21
I/O123 (A12)	I/O185 (A12)	I/O247 (A12)	I/O371 (A12)	7	99	96	138	154	199	232	12	B22
I/O124 (A13)	I/O186 (A13)	I/O248 (A13)	I/O372 (A13)	8	100	97	139	155	200	233	10	C21
		GND	GND									GND(1)
		VCC	VCC									VCC(1)
		I/O249	I/O373								9	D20
		I/O250	I/O374								8	A23
			I/O375									A24
			I/O376									B23
			I/O377									
			I/O378									
			GND									
	I/O187	I/O251	I/O379							234	7	D21
	I/O188	I/O252	I/O380							235	6	C22
I/O125	I/O189	I/O253	I/O381				140	156	201	236	5	B24
I/O126	I/O190	I/O254	I/O382				141	157	202	237	4	C23
I/O127 (A14)	I/O191 (A14)	I/O255 (A14)	I/O383 (A14)	9	1	98	142	158	203	238	3	D22
I/O128, GCK8 (A15)	I/O192, GCK8 (A15)	I/O256, GCK8 (A15)	I/O384, GCK8 (A15)	10	2	99	143	159	204	239	2	C24
VCC	VCC	VCC	VCC	11	3	100	144	160	205	240	1	VCC(1)

Notes:
1. Pads labeled GND or VCC are internally bonded to Ground or VCC planes within the package. They have no direct connection to any specific package pin.
2. This package has an inverted die.
3. Shared with TSTCLK. No Connect.

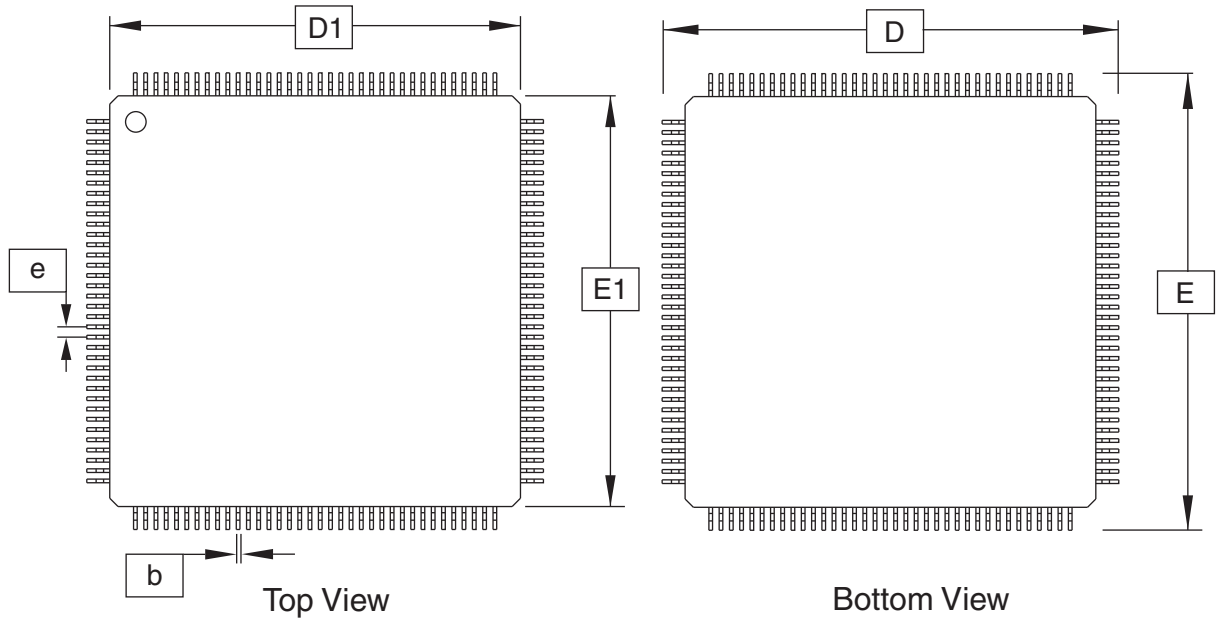
14. AT40K Series Ordering Information

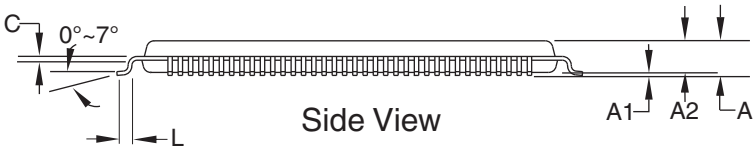
Atmel Ordering Code	Package	Usable Gates	Operating Voltage	Speed Grade (ns)	Operation Range
AT40K05-2BQJ[1]	144AA	5,000 – 10,000	5.0V	2	Industrial (-40°C to 85°C)
AT40K10-W[2]	Wafer	10,000 – 20,000	5.0V	2	Industrial (-40°C to 85°C)
AT40K10-2DQU[3]	208Q1	10,000 – 20,000			
AT40K20-2BQJ[1]	144AA	20,000 – 30,000	5.0V	2	Industrial (-40°C to 85°C)
AT40K20-2EQJ[1]	240Q1	20,000 – 30,000			

Notes:
1. Devices are Pb-free but are *not* RoHS-compliant.
2. For Die Sales of AT40K10, please contact Atmel Sales.
3. Please contact Atmel Sales for availability.

15. Packaging Information

15.1 144AA — 144-lead LQFP





COMMON DIMENSIONS
(Unit of Measure = mm)

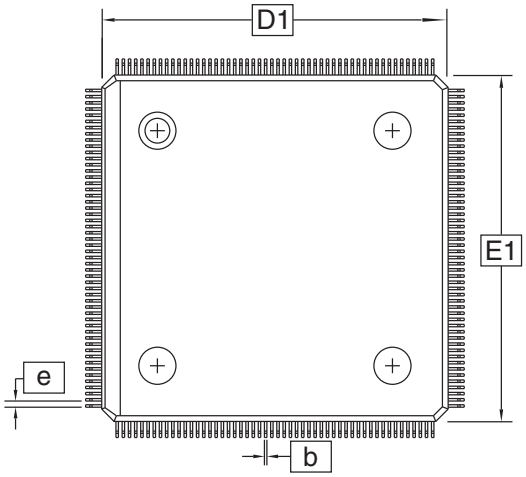
SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	1.60	
A1	0.05	–	0.15	
A2	1.35	1.40	1.45	
D		22.00 BSC		
D1		20.00 BSC		Note 2
E		22.00 BSC		
E1		20.00 BSC		Note 2
b	0.17	0.22	0.27	
C	0.09	–	0.20	
L	0.45	0.60	0.75	
e		0.50 TYP		

Notes: 1. This package conforms to JEDEC reference MS-026, Variation BFB.
2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25 mm per side. Dimensions D1 and E1 are maximum plastic body size dimensions including mold mismatch.
3. Lead coplanarity is 0.10 mm maximum.

10/19/2011

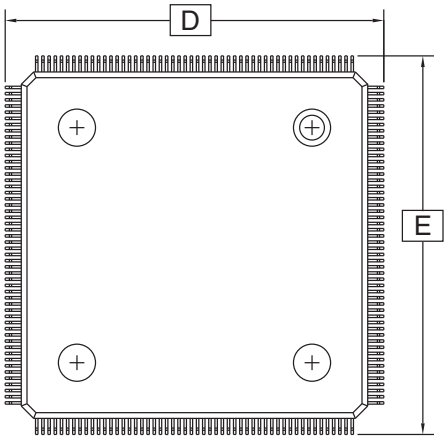
Atmel	TITLE	GPC	DRAWING NO.	REV.
Package Drawing Contact: packagedrawings@atmel.com	**144AA**, 144-lead, 20 x 20 x 1.4mm Body, 0.50mm lead pitch, 2.0mm footprint, Low-profile Plastic Quad Flat Package (LQFP)	AEI	144AA	D

15.2 208Q1 — 208-lead PQFP



Top View

Side View



Bottom View

COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A1	0.25	–	0.50	
A2	3.20	3.40	3.60	
D		30.60 BSC		
D1		28.00 BSC		2, 3
E		30.60 BSC		
E1		28.00 BSC		2, 3
e		0.50 BSC		
b	0.17	–	0.27	4
L1		1.30 REF		

Notes: 1. This drawing is for general information only; refer to JEDEC Drawing MS-129, Variation FA-1, for proper dimensions, tolerances, datums, etc.
2. The top package body size may be smaller than the bottom package size by as much as 0.15 mm.
3. Dimensions D1 and E1 do not include mold protrusions. Allowable protrusion is 0.25 mm per side. D1 and E1 are maximum plastic body size dimensions including mold mismatch.
4. Dimension b does not include Dambar protrusion. Allowable Dambar protrusion shall not cause the lead width to exceed the maximum b dimension by more than 0.08 mm. Dambar cannot be located on the lower radius or the foot. Minimum space between protrusion and an adjacent lead is 0.07 mm.

03/10/05

Atmel Package Drawing Contact: packagedrawings@atmel.com	TITLE **208Q1**, 208-lead (28 x 28 mm Body, 2.6 Form Opt.), Plastic Quad Flat Pack (PQFP)	DRAWING NO. 208Q1	REV. C

16. Revision History

Doc. No.	Date	Comments
0896E	06/2013	Added 208Q1 package option. Reinserted the Left Side (Top to Bottom) table. Updated footers and disclaimer page.
0896D	01/2013	Revised datasheet with lead-free package offering. Removed low voltage (AT40KLV) offering. Removed discontinued lead based package offering. Added AT40K010-W (for die sale program). Updated PDFQ – 240Q1 package drawing. Replaced LQFP – 144L1 with LQFP – 144AA package drawing.
0896C	04/2002	