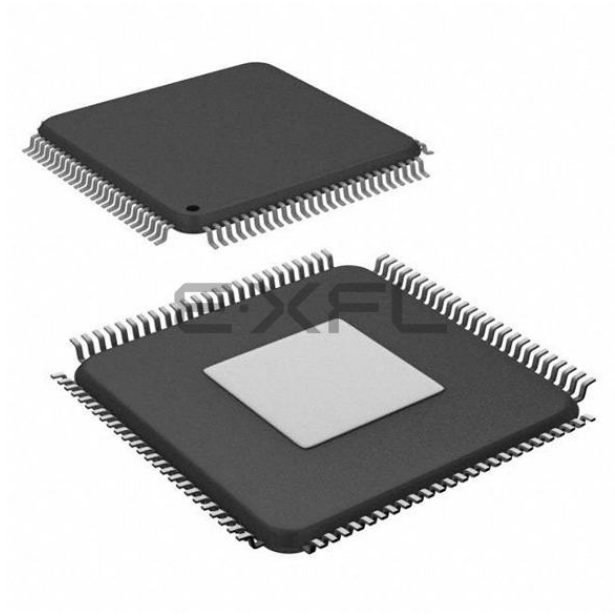
# Infineon Technologies - SAK-XC2364A-72F80L AA Datasheet



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## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | C166SV2 |
| Core Size | 16/32-Bit |
| Speed | 80MHz |
| Connectivity | CANbus, EBI/EMI, I²C, LINbus, SPI, SSC, UART/USART, USI |
| Peripherals | I²S, POR, PWM, WDT |
| Number of I/O | 75 |
| Program Memory Size | 576KB (576K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 50K x 8 |
| Voltage - Supply (Vcc/Vdd) | 3V ~ 5.5V |
| Data Converters | A/D 16x10b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 125°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 100-LQFP Exposed Pad |
| Supplier Device Package | PG-LQFP-100-8 |
| Purchase URL | https://www.e-xfl.com/product-detail/infineon-technologies/sak-xc2364a-72f80l-aa |

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  - Two Synchronizable A/D Converters with a total of up to 16 channels, 10-bit resolution, conversion time below 1 µs, optional data preprocessing (data reduction, range check), broken wire detection
  - Up to 6 serial interface channels to be used as UART, LIN, high-speed synchronous channel (SPI), IIC bus interface (10-bit addressing, 400 kbit/s), IIS interface
  - On-chip MultiCAN interface (Rev. 2.0B active) with up to 64 message objects (Full CAN/Basic CAN) on up to 3 CAN nodes and gateway functionality
  - On-chip system timer and on-chip real time clock
- Up to 12 Mbytes external address space for code and data
  - Programmable external bus characteristics for different address ranges
  - Multiplexed or demultiplexed external address/data buses
  - Selectable address bus width
  - 16-bit or 8-bit data bus width
  - Four programmable chip-select signals
- Single power supply from 3.0 V to 5.5 V
- Programmable watchdog timer and oscillator watchdog
- Up to 76 general purpose I/O lines
- On-chip bootstrap loaders
- Supported by a full range of development tools including C compilers, macro-assembler packages, emulators, evaluation boards, HLL debuggers, simulators, logic analyzer disassemblers, programming boards
- On-chip debug support via Device Access Port (DAP) or JTAG interface
- 100-pin Green LQFP package, 0.5 mm (19.7 mil) pitch

### Ordering Information

The ordering code for an Infineon microcontroller provides an exact reference to a specific product. This ordering code identifies:

- the function set of the corresponding product type
- the temperature range:
  - SAF-…: -40°C to 85°C
  - SAH-…: -40°C to 110°C
  - SAK-…: -40°C to 125°C
- the package and the type of delivery.

For ordering codes for the XC236xA please contact your sales representative or local distributor.

This document describes several derivatives of the XC236xA group:

**Basic Device Types** are readily available and
**Special Device Types** are only available on request.

As this document refers to all of these derivatives, some descriptions may not apply to a specific product, in particular to the special device types.

For simplicity the term **XC236xA** is used for all derivatives throughout this document.

## 1.1 Basic Device Types

Basic device types are available and can be ordered through Infineon's direct and/or distribution channels.

**Table 1 Synopsis of XC236xA Basic Device Types**

| Derivative[1] | Flash Memory[2] | PSRAM DSRAM[3] | Capt./Comp. Modules | ADC[4] Chan. | Interfaces[4] |
|---|---|---|---|---|---|
| XC2365A-104FxxL | 832 Kbytes | 32 Kbytes<br>16 Kbytes | CC2<br>CCU60/1 | 11 + 5 | 3 CAN Nodes,<br>6 Serial Chan. |
| XC2364A-104FxxL | 832 Kbytes | 32 Kbytes<br>16 Kbytes | CC2<br>CCU60/1 | 11 + 5 | 2 CAN Nodes,<br>4 Serial Chan. |
| XC2364A-72FxxL | 576 Kbytes | 32/16 Kbytes<br>16 Kbytes | CC2<br>CCU60/1 | 11 + 5 | 2 CAN Nodes,<br>4 Serial Chan. |

1) xx is a placeholder for the available speed grade (in MHz).

2) Specific information about the on-chip Flash memory in **Table 3**.

3) All derivatives additionally provide 8 Kbytes SBRAM and 2 Kbytes DPRAM.

4) Specific information about the available channels in **Table 5**.
Analog input channels are listed for each Analog/Digital Converter module separately (ADC0 + ADC1).

## 1.2 Special Device Types

Special device types are only available for high-volume applications on request.

**Table 2 Synopsis of XC236xA Special Device Types**

| Derivative[1] | Flash Memory[2] | PSRAM DSRAM[3] | Capt./Comp. Modules | ADC[4] Chan. | Interfaces[4] |
|---|---|---|---|---|---|
| XC2365A-72FxxL | 576 Kbytes | 32/16 Kbytes 16 Kbytes | CC2 CCU60/1 | 11 + 5 | 3 CAN Nodes, 6 Serial Chan. |
| XC2365A-56FxxL | 448 Kbytes | 32/16 Kbytes 16 Kbytes | CC2 CCU60/1 | 11 + 5 | 3 CAN Nodes, 6 Serial Chan. |
| XC2364A-56FxxL | 448 Kbytes | 32/16 Kbytes 16 Kbytes | CC2 CCU60/1 | 11 + 5 | 2 CAN Nodes, 4 Serial Chan. |
| XC2363A-72FxxL | 576 Kbytes | 32/16 Kbytes 16 Kbytes | CC2 CCU60/1 | 4 + 4 | 2 CAN Nodes, 2 Serial Chan. |
| XC2363A-56FxxL | 448 Kbytes | 32/16 Kbytes 16 Kbytes | CC2 CCU60/1 | 4 + 4 | 2 CAN Nodes, 2 Serial Chan. |
| XC2361A-72FxxL | 576 Kbytes | 32 Kbytes 16 Kbytes | CC2 CCU60/1 | 11 + 5 | 2 CAN Nodes, 6 Serial Chan. |
| XC2361A-56FxxL | 448 Kbytes | 16 Kbytes 16 Kbytes | CC2 CCU60/1 | 11 + 5 | 2 CAN Nodes, 6 Serial Chan. |

1) xx is a placeholder for the available speed grade (in MHz).

2) Specific information about the on-chip Flash memory in **Table 3**.

3) All derivatives additionally provide 8 Kbytes SBRAM and 2 Kbytes DPRAM.

4) Specific information about the available channels in **Table 5**.
Analog input channels are listed for each Analog/Digital Converter module separately (ADC0 + ADC1).

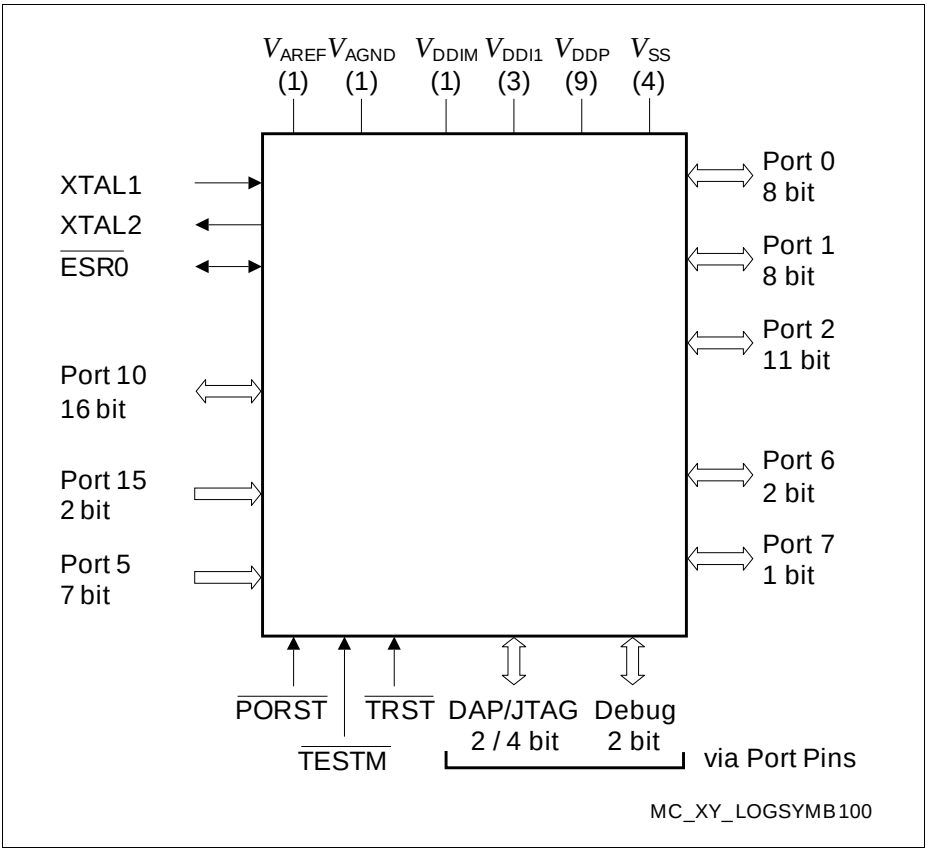


**Figure 3 XC236xA Logic Symbol**

**Table 6 Pin Definitions and Functions** (cont'd)

| Pin | Symbol | Ctrl. | Type | Function |
|---|---|---|---|---|
| 46 | P2.5 | O0 / I | St/B | **Bit 5 of Port 2, General Purpose Input/Output** |
| | U0C0_SCLKOUT | O1 | St/B | **USIC0 Channel 0 Shift Clock Output** |
| | TxDC0 | O2 | St/B | **CAN Node 0 Transmit Data Output** |
| | CC2_CC18 | O3 / I | St/B | **CAPCOM2 CC18IO Capture Inp./ Compare Out.** |
| | A18 | OH | St/B | **External Bus Interface Address Line 18** |
| | U0C0_DX1D | I | St/B | **USIC0 Channel 0 Shift Clock Input** |
| | ESR1_10 | I | St/B | **ESR1 Trigger Input 10** |
| 47 | P4.2 | O0 / I | St/B | **Bit 2 of Port 4, General Purpose Input/Output** |
| | TxDC2 | O2 | St/B | **CAN Node 2 Transmit Data Output** |
| | CC2_CC26 | O3 / I | St/B | **CAPCOM2 CC26IO Capture Inp./ Compare Out.** |
| | $\overline{CS2}$ | OH | St/B | **External Bus Interface Chip Select 2 Output** |
| | T2INA | I | St/B | **GPT12E Timer T2 Count/Gate Input** |
| 48 | P2.6 | O0 / I | St/B | **Bit 6 of Port 2, General Purpose Input/Output** |
| | U0C0_SELO0 | O1 | St/B | **USIC0 Channel 0 Select/Control 0 Output** |
| | U0C1_SELO1 | O2 | St/B | **USIC0 Channel 1 Select/Control 1 Output** |
| | CC2_CC19 | O3 / I | St/B | **CAPCOM2 CC19IO Capture Inp./ Compare Out.** |
| | A19 | OH | St/B | **External Bus Interface Address Line 19** |
| | U0C0_DX2D | I | St/B | **USIC0 Channel 0 Shift Control Input** |
| | RxDC0D | I | St/B | **CAN Node 0 Receive Data Input** |
| | ESR2_6 | I | St/B | **ESR2 Trigger Input 6** |
| 49 | P4.3 | O0 / I | St/B | **Bit 3 of Port 4, General Purpose Input/Output** |
| | U0C1_DOUT | O1 | St/B | **USIC0 Channel 1 Shift Data Output** |
| | CC2_CC27 | O3 / I | St/B | **CAPCOM2 CC27IO Capture Inp./ Compare Out.** |
| | $\overline{CS3}$ | OH | St/B | **External Bus Interface Chip Select 3 Output** |
| | RxDC2A | I | St/B | **CAN Node 2 Receive Data Input** |
| | T2EUDA | I | St/B | **GPT12E Timer T2 External Up/Down Control Input** |

**Table 6 Pin Definitions and Functions** (cont'd)

| Pin | Symbol | Ctrl. | Type | Function |
|---|---|---|---|---|
| 62 | P10.2 | O0 / I | St/B | **Bit 2 of Port 10, General Purpose Input/Output** |
| | U0C0_SCLKOUT | O1 | St/B | **USIC0 Channel 0 Shift Clock Output** |
| | CCU60_CC62 | O2 | St/B | **CCU60 Channel 2 Output** |
| | AD2 | OH / IH | St/B | **External Bus Interface Address/Data Line 2** |
| | CCU60_CC62INA | I | St/B | **CCU60 Channel 2 Input** |
| | U0C0_DX1B | I | St/B | **USIC0 Channel 0 Shift Clock Input** |
| 63 | P0.4 | O0 / I | St/B | **Bit 4 of Port 0, General Purpose Input/Output** |
| | U1C1_SELO0 | O1 | St/B | **USIC1 Channel 1 Select/Control 0 Output** |
| | U1C0_SELO1 | O2 | St/B | **USIC1 Channel 0 Select/Control 1 Output** |
| | CCU61_COUT61 | O3 | St/B | **CCU61 Channel 1 Output** |
| | A4 | OH | St/B | **External Bus Interface Address Line 4** |
| | U1C1_DX2A | I | St/B | **USIC1 Channel 1 Shift Control Input** |
| | RxDC1B | I | St/B | **CAN Node 1 Receive Data Input** |
| | ESR2_8 | I | St/B | **ESR2 Trigger Input 8** |
| 65 | P2.13 | O0 / I | St/B | **Bit 13 of Port 2, General Purpose Input/Output** |
| | U2C1_SELO2 | O1 | St/B | **USIC2 Channel 1 Select/Control 2 Output** |
| | RxDC2D | I | St/B | **CAN Node 2 Receive Data Input** |
| 66 | P2.10 | O0 / I | St/B | **Bit 10 of Port 2, General Purpose Input/Output** |
| | U0C1_DOUT | O1 | St/B | **USIC0 Channel 1 Shift Data Output** |
| | U0C0_SELO3 | O2 | St/B | **USIC0 Channel 0 Select/Control 3 Output** |
| | CC2_CC23 | O3 / I | St/B | **CAPCOM2 CC23IO Capture Inp./ Compare Out.** |
| | A23 | OH | St/B | **External Bus Interface Address Line 23** |
| | U0C1_DX0E | I | St/B | **USIC0 Channel 1 Shift Data Input** |
| | CAPINA | I | St/B | **GPT12E Register CAPREL Capture Input** |

**Table 6 Pin Definitions and Functions** (cont'd)

| Pin | Symbol | Ctrl. | Type | Function |
|---|---|---|---|---|
| 67 | P10.3 | O0 / I | St/B | **Bit 3 of Port 10, General Purpose Input/Output** |
| | CCU60_COUT60 | O2 | St/B | **CCU60 Channel 0 Output** |
| | AD3 | OH / IH | St/B | **External Bus Interface Address/Data Line 3** |
| | U0C0_DX2A | I | St/B | **USIC0 Channel 0 Shift Control Input** |
| | U0C1_DX2A | I | St/B | **USIC0 Channel 1 Shift Control Input** |
| 68 | P0.5 | O0 / I | St/B | **Bit 5 of Port 0, General Purpose Input/Output** |
| | U1C1_SCLKOUT | O1 | St/B | **USIC1 Channel 1 Shift Clock Output** |
| | U1C0_SELO2 | O2 | St/B | **USIC1 Channel 0 Select/Control 2 Output** |
| | CCU61_COUT62 | O3 | St/B | **CCU61 Channel 2 Output** |
| | A5 | OH | St/B | **External Bus Interface Address Line 5** |
| | U1C1_DX1A | I | St/B | **USIC1 Channel 1 Shift Clock Input** |
| | U1C0_DX1C | I | St/B | **USIC1 Channel 0 Shift Clock Input** |
| 69 | P10.4 | O0 / I | St/B | **Bit 4 of Port 10, General Purpose Input/Output** |
| | U0C0_SELO3 | O1 | St/B | **USIC0 Channel 0 Select/Control 3 Output** |
| | CCU60_COUT61 | O2 | St/B | **CCU60 Channel 1 Output** |
| | AD4 | OH / IH | St/B | **External Bus Interface Address/Data Line 4** |
| | U0C0_DX2B | I | St/B | **USIC0 Channel 0 Shift Control Input** |
| | U0C1_DX2B | I | St/B | **USIC0 Channel 1 Shift Control Input** |
| | ESR1_9 | I | St/B | **ESR1 Trigger Input 9** |

**Table 6 Pin Definitions and Functions** (cont'd)

| Pin | Symbol | Ctrl. | Type | Function |
|---|---|---|---|---|
| 98 | $\overline{\text{ESR1}}$ | O0 / I | St/B | **External Service Request 1**<br>After power-up, an internal weak pull-up device holds this pin high when nothing is driving it. |
| | RxDC0E | I | St/B | **CAN Node 0 Receive Data Input** |
| | U1C0_DX0F | I | St/B | **USIC1 Channel 0 Shift Data Input** |
| | U1C0_DX2C | I | St/B | **USIC1 Channel 0 Shift Control Input** |
| | U1C1_DX0C | I | St/B | **USIC1 Channel 1 Shift Data Input** |
| | U1C1_DX2B | I | St/B | **USIC1 Channel 1 Shift Control Input** |
| | U2C1_DX2C | I | St/B | **USIC2 Channel 1 Shift Control Input** |
| 99 | $\overline{\text{ESR0}}$ | O0 / I | St/B | **External Service Request 0**<br>After power-up, $\overline{\text{ESR0}}$ operates as open-drain bidirectional reset with a weak pull-up. |
| | U1C0_DX0E | I | St/B | **USIC1 Channel 0 Shift Data Input** |
| | U1C0_DX2B | I | St/B | **USIC1 Channel 0 Shift Control Input** |
| 10 | $V_{DDIM}$ | - | PS/M | **Digital Core Supply Voltage for Domain M**<br>Decouple with a ceramic capacitor, see Data Sheet for details. |
| 38, 64, 88 | $V_{DDI1}$ | - | PS/1 | **Digital Core Supply Voltage for Domain 1**<br>Decouple with a ceramic capacitor, see Data Sheet for details.<br>All $V_{DDI1}$ pins must be connected to each other. |
| 14 | $V_{DDPA}$ | - | PS/A | **Digital Pad Supply Voltage for Domain A**<br>Connect decoupling capacitors to adjacent $V_{DDP}/V_{SS}$ pin pairs as close as possible to the pins.<br>*Note: The A/D_Converters and ports P5, P6 and P15 are fed from supply voltage $V_{DDPA}$.* |

# 3 Functional Description

The architecture of the XC236xA combines advantages of RISC, CISC, and DSP processors with an advanced peripheral subsystem in a well-balanced design. On-chip memory blocks allow the design of compact systems-on-silicon with maximum performance suited for computing, control, and communication.

The on-chip memory blocks (program code memory and SRAM, dual-port RAM, data SRAM) and the generic peripherals are connected to the CPU by separate high-speed buses. Another bus, the LXBus, connects additional on-chip resources and external resources (see **Figure 6**). This bus structure enhances overall system performance by enabling the concurrent operation of several subsystems of the XC236xA.

The block diagram gives an overview of the on-chip components and the advanced internal bus structure of the XC236xA.

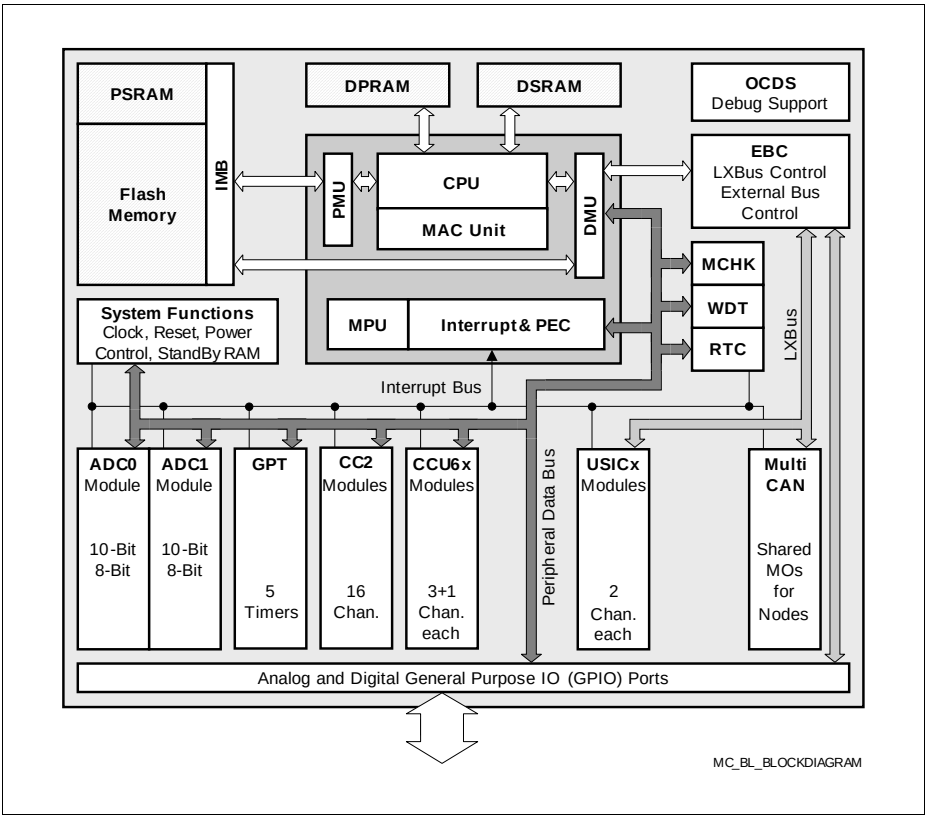


**Figure 6 Block Diagram**

## 3.8 Capture/Compare Unit (CAPCOM2)

The CAPCOM2 unit supports generation and control of timing sequences on up to 16 channels with a maximum resolution of one system clock cycle (eight cycles in staggered mode). The CAPCOM2 unit is typically used to handle high-speed I/O tasks such as pulse and waveform generation, pulse width modulation (PWM), digital to analog (D/A) conversion, software timing, or time recording with respect to external events.

Two 16-bit timers (T7/T8) with reload registers provide two independent time bases for the capture/compare register array.

The input clock for the timers is programmable to several prescaled values of the internal system clock, or may be derived from an overflow/underflow of timer T6 in module GPT2. This provides a wide range or variation for the timer period and resolution and allows precise adjustments to the application-specific requirements. In addition, an external count input allows event scheduling for the capture/compare registers relative to external events.

The capture/compare register array contains 16 dual purpose capture/compare registers, each of which may be individually allocated to either CAPCOM timer and programmed for capture or compare function.
All registers have each one port pin associated with it which serves as an input pin for triggering the capture function, or as an output pin to indicate the occurrence of a compare event.

When a capture/compare register has been selected for capture mode, the current contents of the allocated timer will be latched (‘captured’) into the capture/compare register in response to an external event at the port pin which is associated with this register. In addition, a specific interrupt request for this capture/compare register is generated. Either a positive, a negative, or both a positive and a negative external signal transition at the pin can be selected as the triggering event.

The contents of all registers which have been selected for one of the five compare modes are continuously compared with the contents of the allocated timers.

When a match occurs between the timer value and the value in a capture/compare register, specific actions will be taken based on the selected compare mode.

**Table 9 Compare Modes**

| Compare Modes | Function |
|---|---|
| Mode 0 | Interrupt-only compare mode;<br>Several compare interrupts per timer period are possible |
| Mode 1 | Pin toggles on each compare match;<br>Several compare events per timer period are possible |

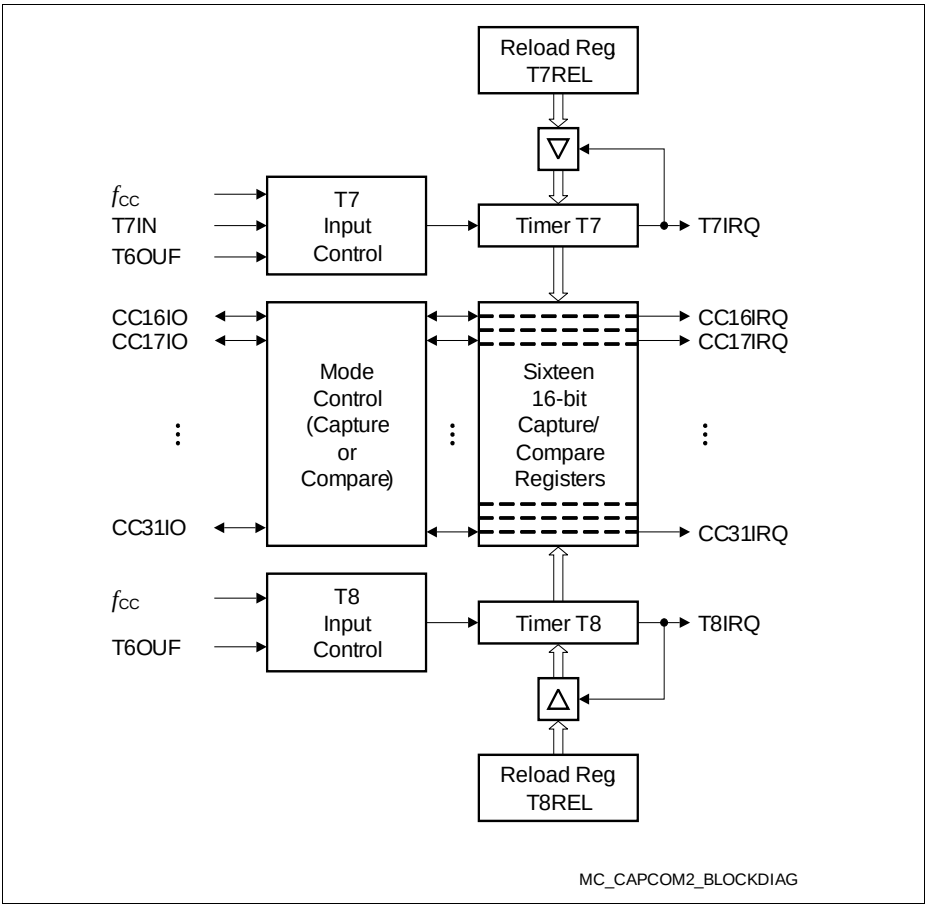


**Figure 8 CAPCOM2 Unit Block Diagram**

## 3.12 A/D Converters

For analog signal measurement, up to two 10-bit A/D converters (ADC0, ADC1) with 11 + 5 multiplexed input channels and a sample and hold circuit have been integrated on-chip. 4 inputs can be converted by both A/D converters. Conversions use the successive approximation method. The sample time (to charge the capacitors) and the conversion time are programmable so that they can be adjusted to the external circuit. The A/D converters can also operate in 8-bit conversion mode, further reducing the conversion time.

Several independent conversion result registers, selectable interrupt requests, and highly flexible conversion sequences provide a high degree of programmability to meet the application requirements. Both modules can be synchronized to allow parallel sampling of two input channels.

For applications that require more analog input channels, external analog multiplexers can be controlled automatically. For applications that require fewer analog input channels, the remaining channel inputs can be used as digital input port pins.

The A/D converters of the XC236xA support two types of request sources which can be triggered by several internal and external events.

- Parallel requests are activated at the same time and then executed in a predefined sequence.
- Queued requests are executed in a user-defined sequence.

In addition, the conversion of a specific channel can be inserted into a running sequence without disturbing that sequence. All requests are arbitrated according to the priority level assigned to them.

Data reduction features reduce the number of required CPU access operations allowing the precise evaluation of analog inputs (high conversion rate) even at a low CPU speed. Result data can be reduced by limit checking or accumulation of results.

The Peripheral Event Controller (PEC) can be used to control the A/D converters or to automatically store conversion results to a table in memory for later evaluation, without requiring the overhead of entering and exiting interrupt routines for each data transfer. Each A/D converter contains eight result registers which can be concatenated to build a result FIFO. Wait-for-read mode can be enabled for each result register to prevent the loss of conversion data.

In order to decouple analog inputs from digital noise and to avoid input trigger noise, those pins used for analog input can be disconnected from the digital input stages. This can be selected for each pin separately with the Port x Digital Input Disable registers.

The Auto-Power-Down feature of the A/D converters minimizes the power consumption when no conversion is in progress.

Broken wire detection for each channel and a multiplexer test mode provide information to verify the proper operation of the analog signal sources (e.g. a sensor system).

**Table 11 Instruction Set Summary** (cont'd)

| Mnemonic | Description | Bytes |
|---|---|---|
| NOP | Null operation | 2 |
| CoMUL/CoMAC | Multiply (and accumulate) | 4 |
| CoADD/CoSUB | Add/Subtract | 4 |
| Co(A)SHR | (Arithmetic) Shift right | 4 |
| CoSHL | Shift left | 4 |
| CoLOAD/STORE | Load accumulator/Store MAC register | 4 |
| CoCMP | Compare | 4 |
| CoMAX/MIN | Maximum/Minimum | 4 |
| CoABS/CoRND | Absolute value/Round accumulator | 4 |
| CoMOV | Data move | 4 |
| CoNEG/NOP | Negate accumulator/Null operation | 4 |

1) The Enter Power Down Mode instruction is not used in the XC236xA, due to the enhanced power control scheme. PWRDN will be correctly decoded, but will trigger no action.

# 4 Electrical Parameters

The operating range for the XC236xA is defined by its electrical parameters. For proper operation the specified limits must be respected when integrating the device in its target environment.

## 4.1 General Parameters

These parameters are valid for all subsequent descriptions, unless otherwise noted.

### 4.1.1 Absolut Maximum Rating Conditions

Stresses above the values listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for an extended time may affect device reliability.
During absolute maximum rating overload conditions ($V_{IN} > V_{DDP}$ or $V_{IN} < V_{SS}$) the voltage on $V_{DDP}$ pins with respect to ground ($V_{SS}$) must not exceed the values defined by the absolute maximum ratings.

**Table 12 Absolute Maximum Rating Parameters**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Output current on a pin when high value is driven | $I_{OH}$ SR | -30 | – | – | mA | |
| Output current on a pin when low value is driven | $I_{OL}$ SR | – | – | 30 | mA | |
| Overload current | $I_{OV}$ SR | -10 | – | 10 | mA | 1) |
| Absolute sum of overload currents | $\Sigma\lvert I_{OV}\rvert$ SR | – | – | 100 | mA | 1) |
| Junction Temperature | $T_J$ SR | -40 | – | 150 | °C | |
| Storage Temperature | $T_{ST}$ SR | -65 | – | 150 | °C | |
| Digital supply voltage for IO pads and voltage regulators | $V_{DDPA}$, $V_{DDPB}$ SR | -0.5 | – | 6.0 | V | |
| Voltage on any pin with respect to ground (Vss) | $V_{IN}$ SR | -0.5 | – | $V_{DDP}$ + 0.5 | V | $V_{IN} \le V_{DDP(max)}$ |

1) Overload condition occurs if the input voltage $V_{IN}$ is out of the absolute maximum rating range. In this case the current must be limited to the listed values by design measures.

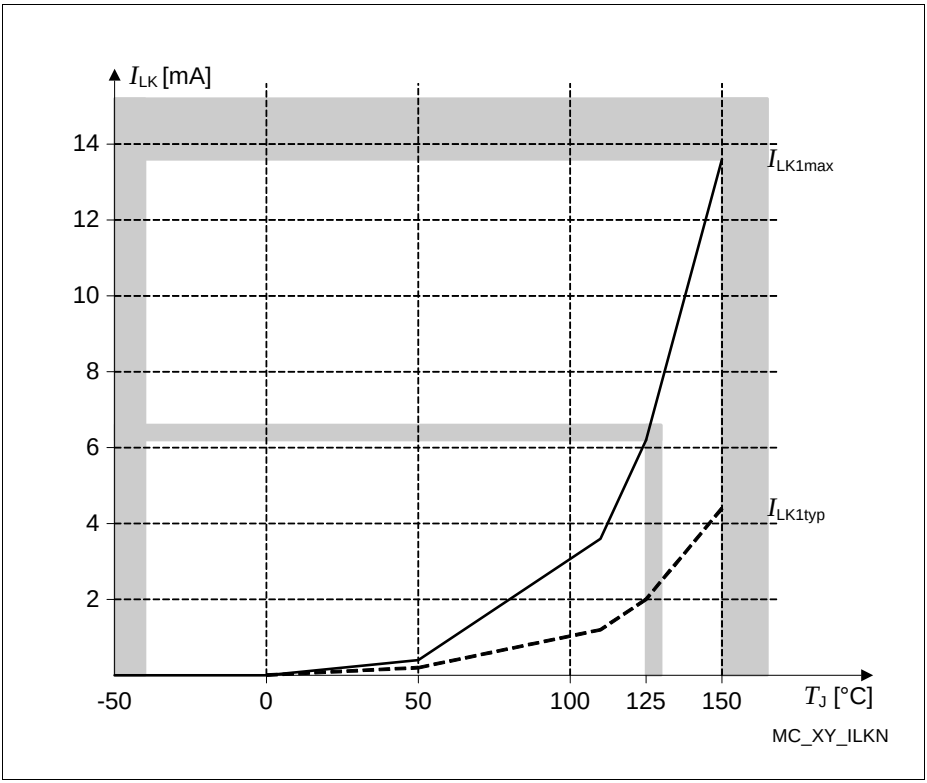


**Figure 17 Leakage Supply Current as a Function of Temperature**

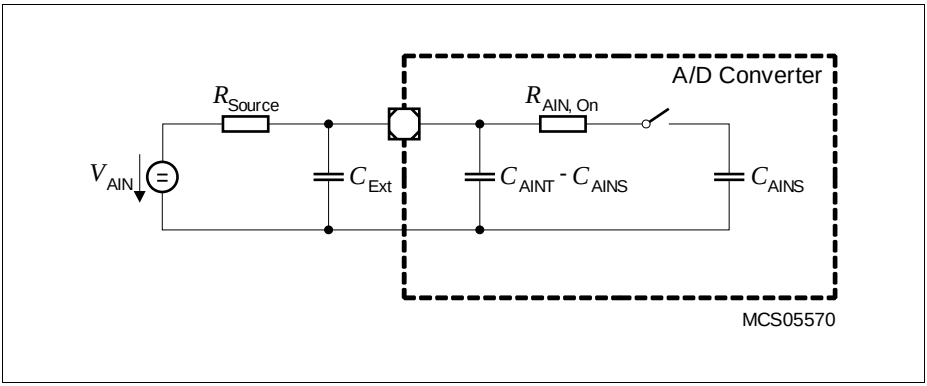


**Figure 18 Equivalent Circuitry for Analog Inputs**

Sample time and conversion time of the XC236xA's A/D converters are programmable. The timing above can be calculated using **Table 19**.
The limit values for $f_{ADCI}$ must not be exceeded when selecting the prescaler value.

**Table 19 A/D Converter Computation Table**

| GLOBCTR.5-0 (DIVA) | A/D Converter Analog Clock $f_{ADCI}$ | | INPCRx.7-0 (STC) | Sample Time[1] $t_S$ |
|---|---|---|---|---|
| $000000_B$ | $f_{SYS}$ | | $00_H$ | $t_{ADCI} \times 2$ |
| $000001_B$ | $f_{SYS}$ / 2 | | $01_H$ | $t_{ADCI} \times 3$ |
| $000010_B$ | $f_{SYS}$ / 3 | | $02_H$ | $t_{ADCI} \times 4$ |
| : | $f_{SYS}$ / (DIVA+1) | | : | $t_{ADCI} \times$ (STC+2) |
| $111110_B$ | $f_{SYS}$ / 63 | | $FE_H$ | $t_{ADCI} \times 256$ |
| $111111_B$ | $f_{SYS}$ / 64 | | $FF_H$ | $t_{ADCI} \times 257$ |

1) The selected sample time is doubled if broken wire detection is active (due to the presampling phase).

**Converter Timing Example A:**

Assumptions: $f_{SYS}$ = 80 MHz (i.e. $t_{SYS}$ = 12.5 ns), DIVA = $03_H$, STC = $00_H$
Analog clock $f_{ADCI}$ = $f_{SYS}$ / 4 = 20 MHz, i.e. $t_{ADCI}$ = 50 ns
Sample time $t_S$ = $t_{ADCI} \times 2$ = 100 ns

**Conversion 10-bit:**

$t_{C10} = 13 \times t_{ADCI} + 2 \times t_{SYS} = 13 \times 50\text{ ns} + 2 \times 12.5\text{ ns} = 0.675\ \mu s$

**Conversion 8-bit:**

$t_{C8} = 11 \times t_{ADCI} + 2 \times t_{SYS} = 11 \times 50\text{ ns} + 2 \times 12.5\text{ ns} = 0.575\ \mu s$

**Converter Timing Example B:**

Assumptions: $f_{SYS}$ = 40 MHz (i.e. $t_{SYS}$ = 25 ns), DIVA = $02_H$, STC = $03_H$
Analog clock $f_{ADCI}$ = $f_{SYS}$ / 3 = 13.3 MHz, i.e. $t_{ADCI}$ = 75 ns
Sample time $t_S$ = $t_{ADCI} \times 5$ = 375 ns

**Conversion 10-bit:**

$t_{C10} = 16 \times t_{ADCI} + 2 \times t_{SYS} = 16 \times 75\text{ ns} + 2 \times 25\text{ ns} = 1.25\ \mu s$

**Conversion 8-bit:**

$t_{C8} = 14 \times t_{ADCI} + 2 \times t_{SYS} = 14 \times 75\text{ ns} + 2 \times 25\text{ ns} = 1.10\ \mu s$

## 4.4 System Parameters

The following parameters specify several aspects which are important when integrating the XC236xA into an application system.

*Note: These parameters are not subject to production test but verified by design and/or characterization.*

*Note: Operating Conditions apply.*

**Table 20 Various System Parameters**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Short-term deviation of internal clock source frequency[1] | $\Delta f_{INT}$ CC | -1 | – | 1 | % | $\Delta T_J \leq 10$ °C |
| Internal clock source frequency | $f_{INT}$ CC | 4.8 | 5.0 | 5.2 | MHz | |
| Wakeup clock source frequency[2] | $f_{WU}$ CC | 400 | – | 700 | kHz | FREQSEL= 00 |
| | | 210 | – | 390 | kHz | FREQSEL= 01 |
| | | 140 | – | 260 | kHz | FREQSEL= 10 |
| | | 110 | – | 200 | kHz | FREQSEL= 11 |
| Startup time from power-on with code execution from Flash | $t_{SPO}$ CC | 1.8 | 2.2 | 2.7 | ms | $f_{WU}$ = 500 kHz |
| Startup time from stopover mode with code execution from PSRAM | $t_{SSO}$ CC | 11 / $f_{WU}$[3] | – | 12 / $f_{WU}$[3] | µs | |
| Core voltage (PVC) supervision level | $V_{PVC}$ CC | $V_{LV}$ - 0.03 | $V_{LV}$ | $V_{LV}$ + 0.07[4] | V | [5] |
| Supply watchdog (SWD) supervision level | $V_{SWD}$ CC | $V_{LV}$ - 0.10[6] | $V_{LV}$ | $V_{LV}$ + 0.15 | V | Lower voltage range[5] |
| | | $V_{LV}$ - 0.15 | $V_{LV}$ | $V_{LV}$ + 0.15 | V | Upper voltage range[5] |

1) The short-term frequency deviation refers to a timeframe of a few hours and is measured relative to the current frequency at the beginning of the respective timeframe. This parameter is useful to determine a time span for re-triggering a LIN synchronization.

2) This parameter is tested for the fastest and the slowest selection. The medium selections are not subject to production test - verified by design/characterization

**Table 30 EBC External Bus Timing for Upper Voltage Range**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Output valid delay for $\overline{RD}$, $\overline{WR}$(L/$\overline{H}$) | $t_{10}$ CC | – | 7 | 13 | ns | |
| Output valid delay for $\overline{BHE}$, ALE | $t_{11}$ CC | – | 7 | 14 | ns | |
| Address output valid delay for A23 ... A0 | $t_{12}$ CC | – | 8 | 14 | ns | |
| Address output valid delay for AD15 ... AD0 (MUX mode) | $t_{13}$ CC | – | 8 | 15 | ns | |
| Output valid delay for $\overline{CS}$ | $t_{14}$ CC | – | 7 | 13 | ns | |
| Data output valid delay for AD15 ... AD0 (write data, MUX mode) | $t_{15}$ CC | – | 8 | 15 | ns | |
| Data output valid delay for D15 ... D0 (write data, DEMUX mode) | $t_{16}$ CC | – | 8 | 15 | ns | |
| Output hold time for $\overline{RD}$, $\overline{WR}$(L/$\overline{H}$) | $t_{20}$ CC | -2 | 6 | 8 | ns | |
| Output hold time for $\overline{BHE}$, ALE | $t_{21}$ CC | -2 | 6 | 10 | ns | |
| Address output hold time for AD15 ... AD0 | $t_{23}$ CC | -3 | 6 | 8 | ns | |
| Output hold time for $\overline{CS}$ | $t_{24}$ CC | -3 | 6 | 11 | ns | |
| Data output hold time for D15 ... D0 and AD15 ... AD0 | $t_{25}$ CC | -3 | 6 | 8 | ns | |
| Input setup time for READY, D15 ... D0, AD15 ... AD0 | $t_{30}$ SR | 25 | 15 | – | ns | |
| Input hold time READY, D15 ... D0, AD15 ... AD0[1)] | $t_{31}$ SR | 0 | -7 | – | ns | |

1) Read data are latched with the same internal clock edge that triggers the address change and the rising edge of RD. Address changes before the end of RD have no impact on (demultiplexed) read cycles. Read data can change after the rising edge of RD.