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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	-
Number of Logic Elements/Cells	1568
Total RAM Bits	25600
Number of I/O	171
Number of Gates	48000
Voltage - Supply	3V ~ 3.6V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 70°C (TA)
Package / Case	208-BFQFP
Supplier Device Package	208-PQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/or3t306s208-db

Table of Contents

System-Level Features

System-level features reduce glue logic requirements and make a system on a chip possible. These features in the *ORCA* Series 3 include:

- Full PCI local bus compliance.
- Dual-use microprocessor interface (MPI) can be used for configuration, readback, device control, and device status, as well as for a general-purpose interface to the FPGA. Glueless interface to *i960** and *PowerPC*† processors with user-configurable address space provided.
- Parallel readback of configuration data capability with the built-in microprocessor interface.
- Programmable clock manager (PCM) adjusts clock phase and duty cycle for input clock rates from 5 MHz to 120 MHz. The PCM may be combined with FPGA logic to create complex functions, such as digital phase-locked loops (DPLL), frequency counters, and frequency synthesizers or clock doublers. Two PCMs are provided per device.
- True, internal, 3-state, bidirectional buses with simple control provided by the SLIC.
- 32 x 4 RAM per PFU, configurable as single- or dual-port at >176 MHz. Create large, fast RAM/ROM blocks (128 x 8 in only eight PFUs) using the SLIC decoders as bank drivers.

* *i960* is a registered trademark of Intel Corporation.
† *PowerPC* is a registered trademark of International Business Machines Corporation.

Table 2. *ORCA* Series 3 System Performance

Parameter	# PFUs	Speed				Unit
		-4	-5	-6	-7	
16-bit Loadable Up/Down Counter	2	78	102	131	168	MHz
16-bit Accumulator	2	78	102	131	168	MHz
8 x 8 Parallel Multiplier:						
Multiplier Mode, Unpipelined[1]	11.5	19	25	30	38	MHz
ROM Mode, Unpipelined[2]	8	51	66	80	102	MHz
Multiplier Mode, Pipelined[3]	15	76	104	127	166	MHz
32 x 16 RAM (synchronous):						
Single-port, 3-state Bus[4]	4	97	127	151	192	MHz
Dual-port[5]	4	127	166	203	253	MHz
128 x 8 RAM (synchronous):						
Single-port, 3-state Bus[4]	8	88	116	139	176	MHz
Dual-port[5]	8	88	116	139	176	MHz
8-bit Address Decode (internal):						
Using Softwired LUTs	0.25	4.87	3.66	2.58	2.03	ns
Using SLICs[6]	0	2.35	1.82	1.23	0.99	ns
32-bit Address Decode (internal):						
Using Softwired LUTs	2	16.06	12.07	9.01	7.03	ns
Using SLICs[7]	0	6.91	5.41	4.21	3.37	ns
36-bit Parity Check (internal)	2	16.06	12.07	9.01	7.03	ns

1. Implemented using 8 x 1 multiplier mode (unpipelined), register-to-register, two 8-bit inputs, one 16-bit output.
2. Implemented using two 32 x 12 ROMs and one 12-bit adder, one 8-bit input, one fixed operand, one 16-bit output.
3. Implemented using 8 x 1 multiplier mode (fully pipelined), two 8-bit inputs, one 16-bit output (7 of 15 PFUs contain only pipelining registers).
4. Implemented using 32 x 4 RAM mode with read data on 3-state buffer to bidirectional read/write bus.
5. Implemented using 32 x 4 dual-port RAM mode.
6. Implemented in one partially occupied SLIC with decoded output set up to CE in same PLC.
7. Implemented in five partially occupied SLICs.

Programmable Logic Cells (continued)

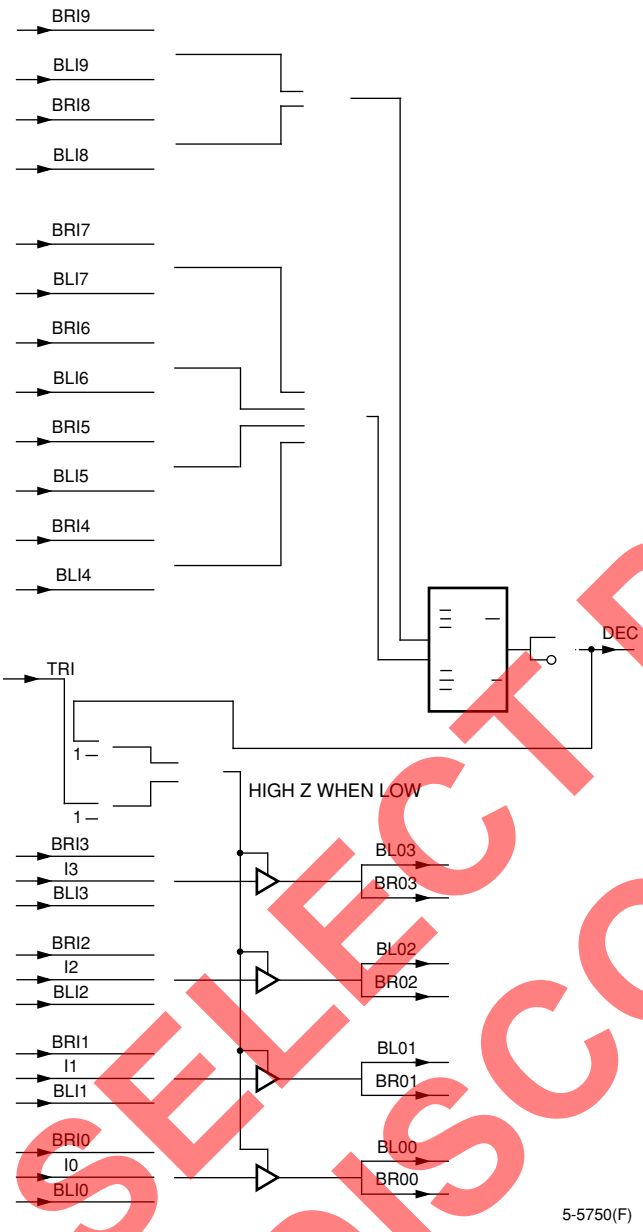


Figure 15. Buffer-Decoder-Decoder Mode

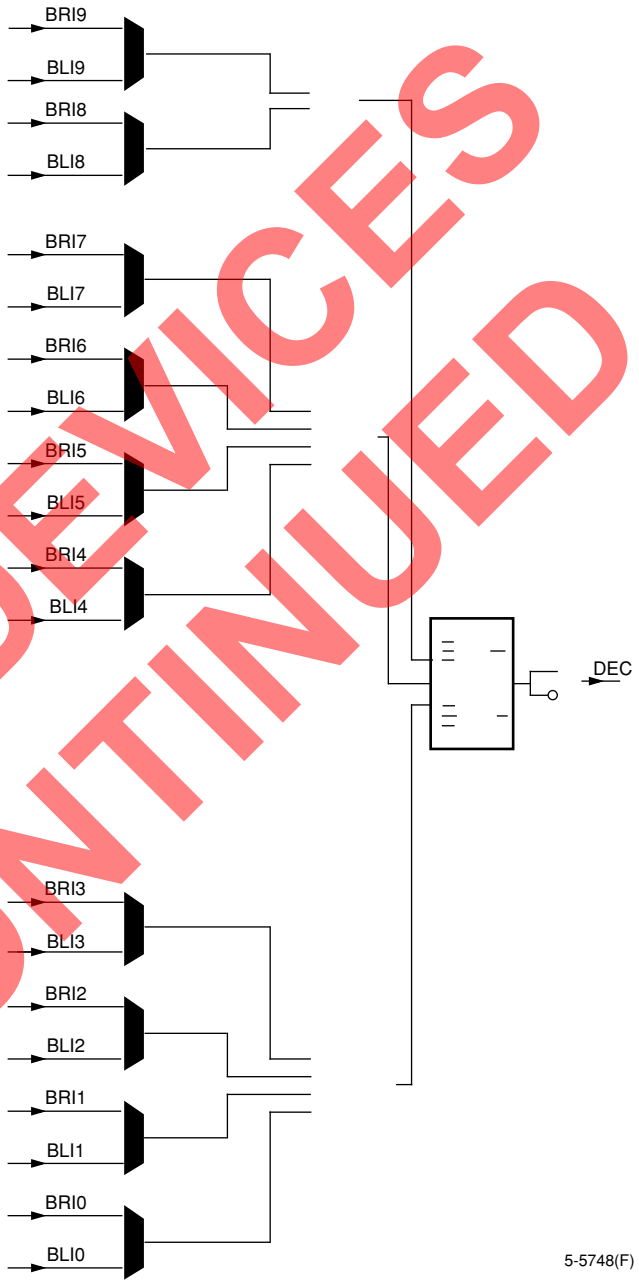


Figure 16. Decoder Mode

Programmable Logic Cells (continued)

Figure 21. PLC Architecture

Programmable Input/Output Cells

(continued)

Table 9. PIO Options

Input	Option
Input Level	TTL, OR3Cxx only CMOS, OR3Cxx or OR3Txxx 3.3 V PCI Compliant, OR3Txxx 5 V PCI Compliant, OR3Txxx
Input Speed	Fast, Delayed
Float Value	Pull-up, Pull-down, None
Register Mode	Latch, FF, Fast Zero Hold FF, None (direct input)
Clock Sense	Inverted, Noninverted
Input Selection	Input 1, Input 2, Clock Input
Output	**Option**
Output Drive Current	12 mA/6 mA or 6 mA/3 mA
Output Function	Normal, Fast Open Drain
Output Speed	Fast, Slewlim, Sinklim
Output Source	FF Direct-out, General Routing
Output Sense	Active-high, Active-low
3-State Sense	Active-high, Active-low (3-state)
FF Clocking	ExpressCLK, System Clock
Clock Sense	Inverted, Noninverted
Logic Options	See Table 10.
I/O Controls	**Option**
Clock Enable	Active-high, Active-low, Always Enabled
Set/Reset Level	Active-high, Active-low, No Local Reset
Set/Reset Type	Synchronous, Asynchronous
Set/Reset Priority	CE over LSR, LSR over CE
GSR Control	Enable GSR, Disable GSR

5 V Tolerant I/O

The I/O on the OR3Txxx Series devices allow interconnection to both 3.3 V and 5 V devices (selectable on a per-pin basis).

The OR3Txxx devices will drive the pin to the 3.3 V levels when the output buffer is enabled. If the other device being driven by the OR3Txxx device has TTL-compatible inputs, then the device will not dissipate much input buffer power. This is because the OR3Txxx output is being driven to a higher level than the TTL level required. If the other device has a CMOS-compatible input, the amount of input buffer power will also be small. Both of these power values are dependent upon the input buffer characteristics of the other device when driven at the OR3Txxx output buffer voltage levels.

The OR3Txxx device has internal programmable pull-ups on the I/O buffers. These pull-up voltages are always referenced to V_{DD} and are always sufficient to pull the input buffer of the OR3Txxx device to a high state. The pin on the OR3Txxx device will be at a level 1.0 V below V_{DD} (minimum of 2.0 V with a minimum V_{DD} of 3.0 V). This voltage is sufficient to pull the external pin up to a 3.3 V CMOS high input level (1.8 V, min) or a TTL high input level (2.0 V, min) in a 5 V tolerant system. Therefore, in a 5 V tolerant system using 5 V CMOS parts, care must be taken to evaluate the use of these pull-ups to pull the pin of the OR3Txxx device to a typical 5 V CMOS high input level (2.2 V, min).

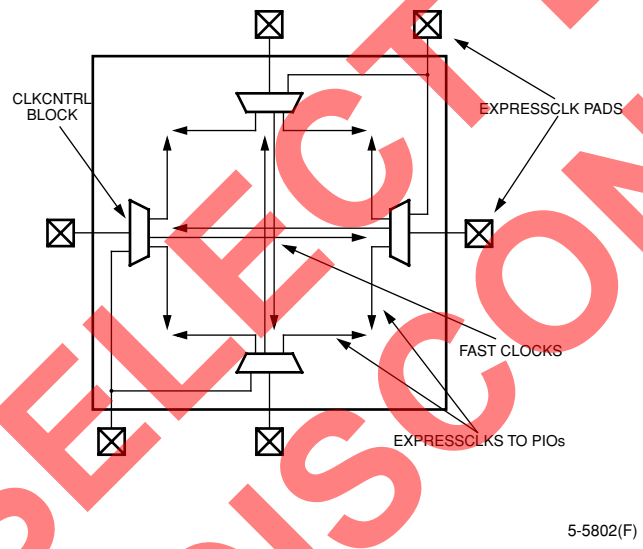
PCI Compliant I/O

The I/O on the OR3Txxx Series devices allows compliance with PCI Local Bus (Rev. 2.2) 5 V and 3.3 V signaling environments. The signaling environment used for each input buffer can be selected on a per-pin basis. The selection provides the appropriate I/O clamping diodes for PCI compliance. Choosing an IBT input buffer will provide PCI compliance in OR3Txxx devices. OR3Cxx devices have PCI Local Bus compliant I/Os for 5 V signaling.

Clock Distribution Network (continued)

ExpressCLK Inputs

There are four dedicated ExpressCLK pads on each Series 3 device: one in the middle of each side. Two other user I/O pads can also be used as corner ExpressCLK inputs, one on the lower-left corner, and one on the upper-right corner. The corner ExpressCLK pads feed the ExpressCLK to the two sides of the array that are adjacent to that corner, always driving the same signal in both directions. The ExpressCLK route from the middle pad and from the corner pad associated with that side are multiplexed and can be glitchlessly stopped/started under user control using the StopCLK feature of the CLKCNTRL function block (described under Special Function Blocks) on that side. The ExpressCLK output of the programmable clock manager (PCM) is programmably connected to the corner ExpressCLK routes. PCM blocks are found in the same corners as the corner ExpressCLK signals and are described in the Special Function Blocks section. The ExpressCLK structure is shown in Figure 34 (PCM blocks are not shown).



Note: All multiplexers are set during configuration.

Figure 34. ExpressCLK and Fast Clock Distribution

Selecting Clock Input Pins

Any user I/O pin on an *ORCA* FPGA can be used as a fast, low-skew system clock input. Since the four dedicated ExpressCLK inputs can only be used to distribute global signals into the FPGA, these pins should be selected first as clock pins. Within the interquad region of the device, these clocks sourced by the ExpressCLK inputs are called fast clocks. Choosing the next clock pin is completely arbitrary, but using a pin that is near the center of an edge of the device will provide the lowest skew system clock network. The pin-to-pin timing numbers in the Timing Characteristics section assume that the clock pin is in one of the PICs at the center of any side of the device next to an ExpressCLK pad. For actual timing characteristics for a given clock pin, use the timing analyzer results from ispLEVER.

To select subsequent clock pins, certain rules should be followed. As discussed in the Programmable Input/Output Cells section, PICs are grouped into adjacent pairs. Each of these pairs contains eight I/Os, but only one of the eight I/Os in a PIC pair can be routed directly onto a system clock spine. Therefore, to achieve top performance, the next clock input chosen should not be one of the pins from a PIC pair previously used for a clock input. If it is necessary to have a second input in the same PIC pair route onto global system clock routing, the input can be routed to a free clock spine using the PIC switching segment (pSW) connections to the clock spine network at some small sacrifice in speed. Alternatively, if global distribution of the secondary clock is not required, the signal can be routed on long lines (xL) and input to the PFU clock input without using a clock spine.

Another rule for choosing clock pins has to do with the alternating nature of clock spine connections to the xL and pxL routing segments. Starting at the left side of the device, the first vertical clock spine from the top connects to hxL[0] (horizontal xL[0]), and the first vertical clock spine from the bottom connects to hxL[5] in all PLC rows. The next vertical clock spine from the top connects to hxL[1], and the next one from the bottom connects to hxL[6]. This progression continues across the device, and after a spine connects to hxL[9], the next spine connects to hxL[0] again. Similar connections are made from horizontal clock spines to vxL (vertical xL) lines from the top to the bottom of the device. Because the *ORCA* Series 3 clock routing only requires the use of an xL line in every other row or column, even two inputs chosen 20 PLCs apart on the same xL line will not conflict, but it is always better to avoid these choices, if possible. The fast clock spines in the interquad routing region also connect to xL[8] and xL[9] for each set of xL lines, so it is better to avoid user I/Os that connect to xL[8] or xL[9] when a fast clock is used that might share one of these connections. Another reason to use the fast clock spines is that since they use only the xL[9:8] lines, they will not conflict with internal data buses which typically use xL[7:0]. For more details on clock selection, refer to application notes on clock distribution in *ORCA* Series 3 devices.

Special Function Blocks (continued)

The external test (EXTEST) instruction allows the interconnections between ICs in a system to be tested for opens and stuck-at faults. If an EXTEST instruction is performed for the system shown in Figure 36, the connections between U1 and U2 (shown by nets a, b, and c) can be tested by driving a value onto the given nets from one device and then determining whether the same value is seen at the other device. This is determined by shifting 2 bits of data for each pin (one for the output value and one for the 3-state value) through the BSR until each one aligns to the appropriate pin. Then, based upon the value of the 3-state signal, either the I/O pad is driven to the value given in the BSR, or the BSR is updated with the input value from the I/O pad, which allows it to be shifted out TDO.

The SAMPLE/PRELOAD instruction is useful for system debugging and fault diagnosis by allowing the data at the FPGA's I/Os to be observed during normal operation or written during test operation. The data for all of the I/Os is captured simultaneously into the BSR, allowing them to be shifted-out TDO to the test host. Since each I/O buffer in the PICs is bidirectional, two pieces of data are captured for each I/O pad: the value at the I/O pad and the value of the 3-state control signal. For preload operation, data is written from the BSR to all of the I/Os simultaneously.

There are five *ORCA*-defined instructions. The PLC scan rings 1 and 2 (PSR1, PSR2) allow user-defined internal scan paths using the PLC latches/FFs. The RAM_Write Enable (RAM_W) instruction allows the user to serially configure the FPGA through TDI. The RAM_Read Enable (RAM_R) allows the user to read back RAM contents on TDO after configuration. The IDCODE instruction allows the user to capture a 32-bit identification code that is unique to each device and serially output it at TDO. The IDCODE format is shown in Table 14.

Table 14. Boundary-Scan ID Code

Device	Version (4 bits)	Part* (10 bits)	Family (6 bits)	Manufacturer (11 bits)	LSB (1 bit)
OR3T20	0000	0011000000	110000	00000011101	1
OR3T30	0000	0111000000	110000	00000011101	1
OR3T55	0000	0100100000	110000	00000011101	1
OR3C/T80	0000	0110100000	110000	00000011101	1
OR3T125	0000	0011100000	110000	00000011101	1

* PLC array size of FPGA, reverse bit order.

Note: Table assumes version 0.

Microprocessor Interface (MPI) (continued)

Device ID Registers

The MPI device ID is broken into four registers holding 1 byte each. The device ID that is available through the MPI is the same as the boundary-scan ID code, except that the device ID in the MPI has a reverse bit order. There is no means to overwrite any of the device ID as can be done with the boundary-scan ID, but the MPI scratchpad register can be used as a personalization register. The format for the entire device ID is shown below followed by family and device values and the partitioning of the device ID into the four device ID registers.

Table 23. Device ID Code

Version	Part*	Family	Manufacturer	MSB
4 bits	10 bits	6 bits	11 bits	1 bit
Example: (First version of OR3C80)			0000 0110100000 110000 00000011101 1	

* PLC array size of FPGA.

Table 24 shows the family and device values for all parts covered by this data sheet.

Table 24. Series 3 Family and Device ID Values

Part Name	Family ID (Hex)	Device ID (Hex)
OR3T20	03	0C
OR3T30	03	0E
OR3T55	03	12
OR3C/T80	03	16
OR3T125	03	1C

Table 25 describes the device IDs for all parts covered by this data sheet as they are partitioned into the four registers found in the MPI.

Table 25. *ORCA* Series 3 Device ID Descriptions

Device ID Register 1	
Bit 0	Logic 1. This bit is always a one.
Bits [7:1]	0011101, the 7 least significant bits of the manufacturer ID.
Device ID Register 2	
Bits [3:0]	0000, the 4 most significant bits of the manufacturer ID.
Bits [7:4]	The 4 least significant bits of the 10-bit part number.
Device ID Register 3	
Bits [5:0]	The 6 most significant bits of the 10-bit part number.
Bits [7:6]	The 2 least significant bits of the device family code.
Device ID Register 4	
Bits [3:0]	The 4 most significant bits of the device family code.
Bits [7:4]	The 4-bit device version code.

Programmable Clock Manager (PCM) (continued)

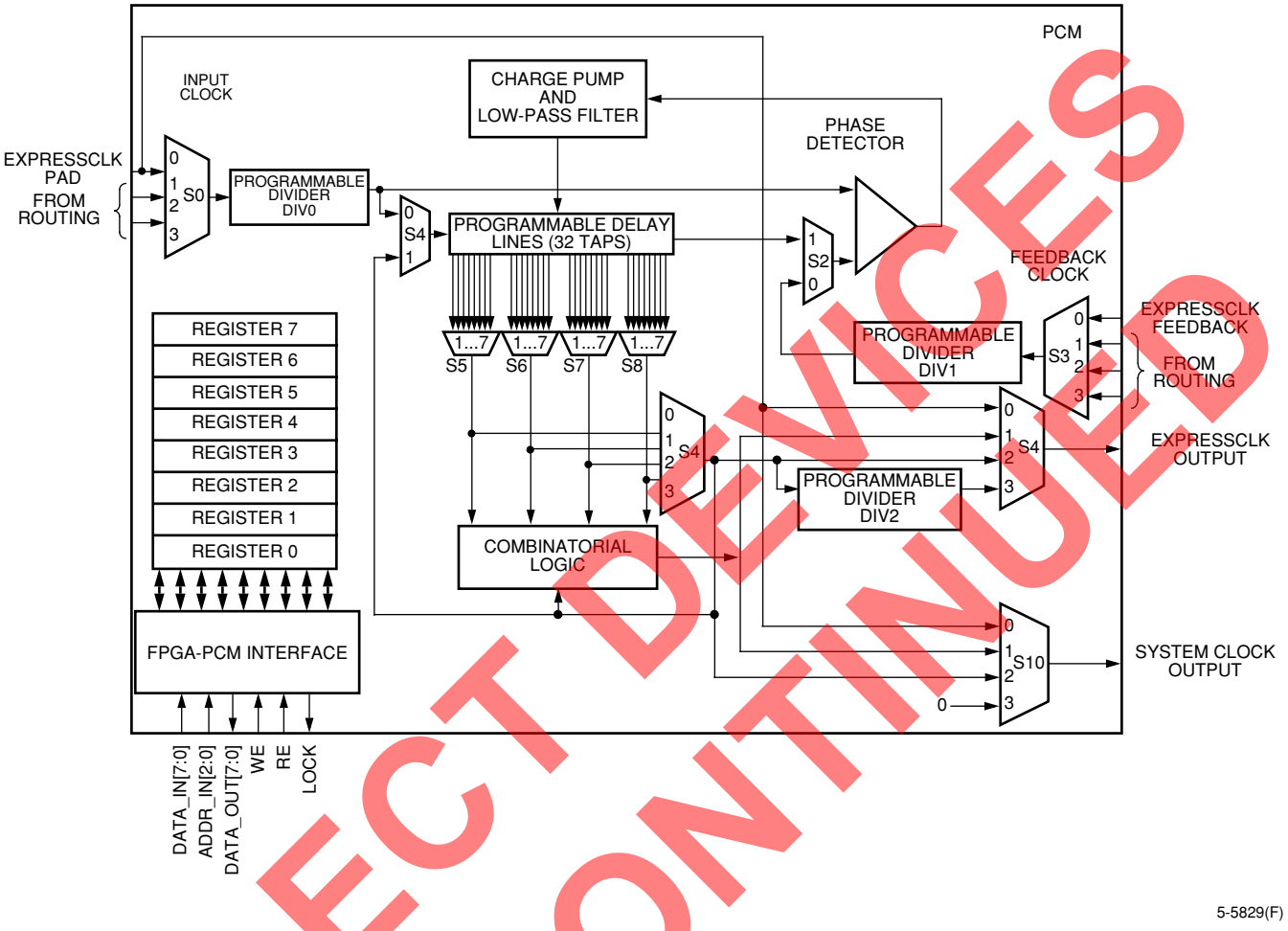


Figure 46. PCM Functional Block Diagram

Programmable Clock Manager (PCM)

(continued)

Table 29. PCM Oscillator Frequency Range 3Txxx

Register 4 76543210	Min (MHz)	System Clock Output Frequency (MHz) NOM	Max (MHz)	T Acquisition (µs)
00XXX010	17.00	58.50	100.00	36.00
00XXX011	16.10	52.50	89.00	37.00
00XXX100	15.17	49.00	82.80	38.00
00XXX101	14.25	45.00	76.50	39.00
00XXX110	13.33	41.50	70.30	40.00
00XXX111	12.40	38.00	64.00	41.00
01XXX000	12.20	36.75	61.30	43.75
01XXX001	12.10	35.00	58.00	46.50
01XXX010	11.90	33.00	54.30	49.25
01XXX011	11.70	31.30	51.00	52.00
01XXX100	11.10	30.00	49.40	54.75
01XXX101	10.50	29.15	47.80	57.50
01XXX110	10.00	28.10	46.20	60.25
01XXX111	9.40	27.00	44.60	63.00
10000XXX	9.20	26.25	43.30	65.40
10001XXX	9.00	25.65	42.30	67.80
10010XXX	8.80	25.00	41.30	70.10
10011XXX	8.60	24.45	40.30	72.50
10100XXX	8.40	23.70	39.00	74.90
10101XXX	8.10	22.90	37.70	77.30
10110XXX	7.90	22.20	36.50	79.60
10111XXX	7.70	21.50	35.20	82.00
11000XXX	7.60	20.80	34.00	84.30
11001XXX	7.45	20.10	32.80	86.50
11010XXX	7.30	19.45	31.60	88.80
11011XXX	7.20	18.85	30.50	91.00
11100XXX	6.60	18.30	30.00	93.30
11101XXX	6.00	17.70	29.40	95.50
11110XXX	5.50	17.10	28.60	97.80
11111XXX	5.00	16.50	28.00	100.00

Note: Use of settings in the first three rows is not recommended. X means don't care.

Table 30. PCM Oscillator Frequency Range 3Cxx

Register 4 76543210	Min (MHz)	System Clock Output Frequency (MHz) NOM	Max (MHz)	T Acquisition (µs)
00XXX010	10.50	73.00	135.00	36.00
00XXX011	10.00	68.00	126.00	37.00
00XXX100	9.50	63.00	117.00	38.00
00XXX101	9.10	58.50	108.00	39.00
00XXX110	8.60	53.80	99.00	40.00
00XXX111	8.10	49.00	90.00	41.00
01XXX000	7.80	47.70	87.50	43.80
01XXX001	7.60	46.30	85.00	46.50
01XXX010	7.30	45.00	82.50	49.30
01XXX011	7.10	43.60	80.00	52.00
01XXX100	6.80	42.10	77.50	55.00
01XXX101	6.50	40.75	75.00	57.50
01XXX110	6.30	39.40	72.50	60.30
01XXX111	6.00	38.00	70.00	63.00
10000XXX	5.90	37.40	68.80	65.40
10001XXX	5.90	36.70	67.50	67.80
10010XXX	5.80	36.00	66.30	70.10
10011XXX	5.80	35.40	65.00	72.50
10100XXX	5.70	35.00	63.80	74.90
10101XXX	5.60	34.10	62.50	77.30
10110XXX	5.60	33.50	61.30	79.60
10111XXX	5.50	32.80	60.00	82.00
11000XXX	5.40	32.10	58.80	84.30
11001XXX	5.40	31.50	57.50	86.50
11010XXX	5.30	30.70	56.30	88.80
11011XXX	5.30	30.10	55.00	91.00
11100XXX	5.20	29.50	53.80	93.30
11101XXX	5.10	28.80	52.50	95.50
11110XXX	5.10	28.20	51.30	97.80
11111XXX	5.00	27.50	50.00	100.00

Note: Use of settings in the first three rows is not recommended. X means don't care.

FPGA States of Operation (continued)

Start-Up

After configuration, the FPGA enters the start-up phase. This phase is the transition between the configuration and operational states and begins when the number of CCLKs received after $\overline{\text{INIT}}$ goes high is equal to the value of the length count field in the configuration frame and when the end of configuration frame has been written. The system design issue in the start-up phase is to ensure the user I/Os become active without inadvertently activating devices in the system or causing bus contention. A second system design concern is the timing of the release of global set/reset of the PLC latches/FFs.

There are configuration options that control the relative timing of three events: DONE going high, release of the set/reset of internal FFs, and user I/Os becoming active. Figure 51 shows the start-up timing for *ORCA* FPGAs. The system designer determines the relative timing of the I/Os becoming active, DONE going high, and the release of the set/reset of internal FFs. In the *ORCA* Series FPGA, the three events can occur in any arbitrary sequence. This means that they can occur before or after each other, or they can occur simultaneously.

There are four main start-up modes: CCLK_NOSYNC, CCLK_SYNC, UCLK_NOSYNC, and UCLK_SYNC. The only difference between the modes starting with CCLK and those starting with UCLK is that for the UCLK modes, a user clock must be supplied to the start-up logic. The timing of start-up events is then based upon this user clock, rather than CCLK. The difference between the SYNC and NOSYNC modes is that for SYNC mode, the timing of two of the start-up events, release of the set/reset of internal FFs, and the I/Os becoming active is triggered by the rise of the external DONE pin followed by a variable number of rising clock edges (either CCLK or UCLK). For the NOSYNC mode, the timing of these two events is based only on either CCLK or UCLK.

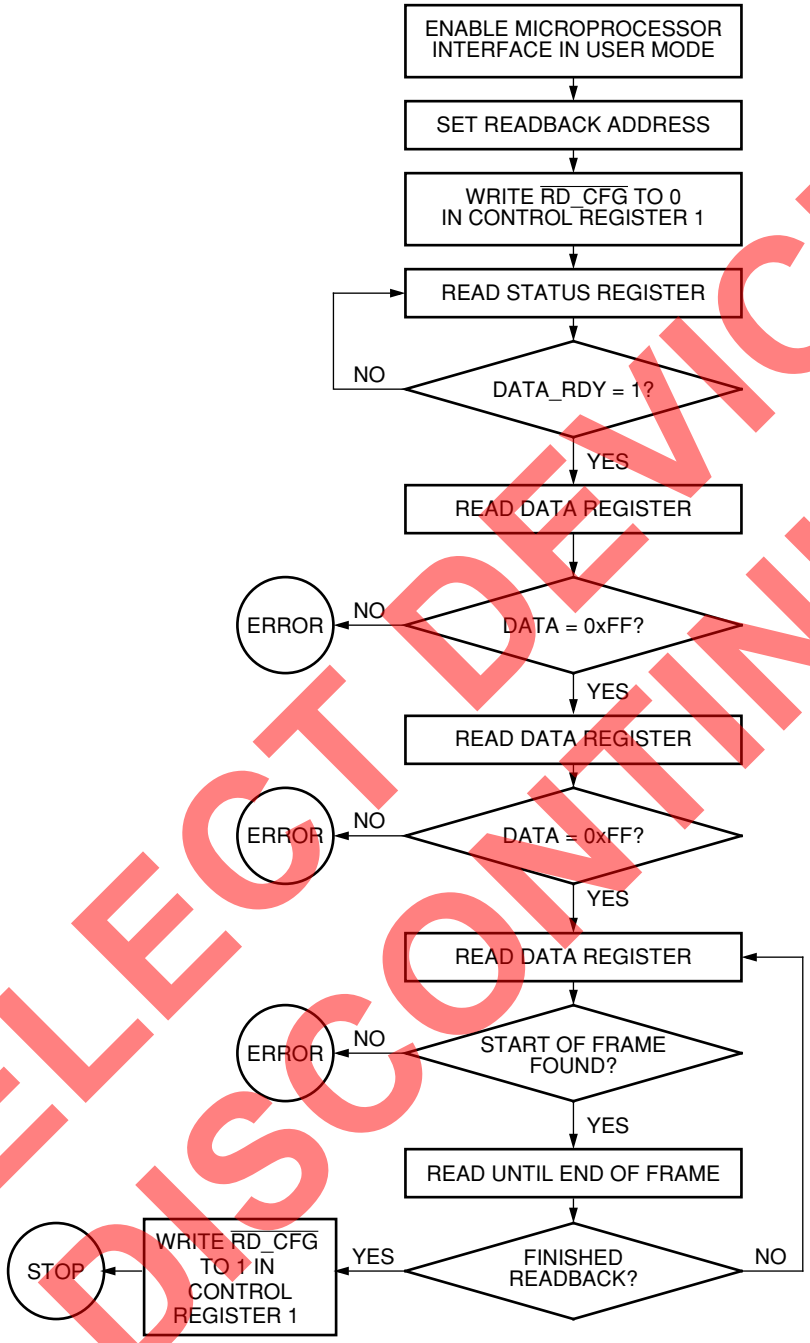
DONE is an open-drain bidirectional pin that may include an optional (enabled by default) pull-up resistor to accommodate wired ANDing. The open-drain DONE signals from multiple FPGAs can be tied together (ANDed) with a pull-up (internal or external) and used as an active-high ready signal, an active-low PROM enable, or a reset to other portions of the system. When used in SYNC mode, these ANDed DONE pins can be used to synchronize the other two start-up events, since they can all be synchronized to the same external signal. This signal will not rise until all FPGAs release their DONE pins, allowing the signal to be pulled high.

The default for *ORCA* is the CCLK_SYNC synchronized start-up mode where DONE is released on the first CCLK rising edge, C1 (see Figure 51). Since this is a synchronized start-up mode, the open-drain DONE signal can be held low externally to stop the occurrence of the other two start-up events. Once the DONE pin has been released and pulled up to a high level, the other two start-up events can be programmed individually to either happen immediately or after up to four rising edges of CCLK (Di, Di + 1, Di + 2, Di + 3, Di + 4). The default is for both events to happen immediately after DONE is released and pulled high.

A commonly used design technique is to release DONE one or more clock cycles before allowing the I/O to become active. This allows other configuration devices, such as PROMs, to be disconnected using the DONE signal so that there is no bus contention when the I/Os become active. In addition to controlling the FPGA during start-up, other start-up techniques that avoid contention include using isolation devices between the FPGA and other circuits in the system, reassigning I/O locations, and maintaining I/Os as 3-stated outputs until contentions are resolved.

Each of these start-up options can be selected during bit stream generation in ispLEVER, using Advanced Options. For more information, please see the ispLEVER documentation.

FPGA Configuration Modes (continued)



5-5764(F)

Figure 60. Readback Through MPI

Timing Characteristics (continued)

PLC Timing

Table 46. PFU Output MUX and Direct Routing Timing Characteristics

OR3Cxx Commercial: VDD = 5.0 V ± 5%, 0 °C < TA < 70 °C; Industrial: VDD = 5.0 V ± 10%, –40 °C < TA < +85 °C.
OR3Txxx Commercial: VDD = 3.0 V to 3.6 V, 0 °C < TA < 70 °C; Industrial: VDD = 3.0 V to 3.6 V, –40 °C < TA < +85 °C.

Parameter (TJ = 85 °C, VDD = min)	Symbol	Speed								Unit
		-4		-5		-6		-7		
		Min	Max	Min	Max	Min	Max	Min	Max	
PFU Output MUX (Fan-out = 1)										
Output MUX Delay (F[7:0]/Q[7:0] to O[9:0])	OMUX_DEL	—	0.50	—	0.39	—	0.35	—	0.28	ns
Carry-out MUX Delay (COUT to O9)	COO9_DEL	—	0.34	—	0.26	—	0.24	—	0.18	ns
Registered Carry-out MUX Delay (REGCOUT to O8)	RCOO8_DEL	—	0.34	—	0.26	—	0.24	—	0.18	ns
Direct Routing										
PFU Feedback (xSW)*	FDBK_DEL	—	1.74	—	1.41	—	1.48	—	1.14	ns
PFU to Orthogonal PFU Delay (xSW to xSW)	ODIR_DEL	—	2.21	—	1.77	—	1.75	—	1.39	ns
PFU to Diagonal PFU Delay (xBID to xSW)	DDIR_DEL	—	2.69	—	2.19	—	2.53	—	1.98	ns

* This is general feedback using switching segments. See the combinatorial PFU timing table for softwired look-up table feedback timing.

SLIC Timing

Table 47. Supplemental Logic and Interconnect Cell (SLIC) Timing Characteristics

OR3Cxx Commercial: VDD = 5.0 V ± 5%, 0 °C < TA < 70 °C; Industrial: VDD = 5.0 V ± 10%, –40 °C < TA < +85 °C.
OR3Txxx Commercial: VDD = 3.0 V to 3.6 V, 0 °C < TA < 70 °C; Industrial: VDD = 3.0 V to 3.6 V, –40 °C < TA < +85 °C.

Parameter (TJ = 85 °C, VDD = min)	Symbol	Speed								Unit
		-4		-5		-6		-7		
		Min	Max	Min	Max	Min	Max	Min	Max	
3-Statable BIDIs										
BIDI Delay (BRx to BLx, BLx to BRx)	BUF_DEL	—	0.84	—	0.70	—	0.94	—	0.77	ns
BIDI Delay (Ox to BRx, Ox to BLx)	OBUF_DEL	—	0.72	—	0.61	—	0.87	—	0.70	ns
BIDI 3-state Enable/Disable Delay (TRI to BL, BR)	TRI_DEL	—	2.55	—	1.90	—	1.31	—	1.01	ns
BIDI 3-state Enable/Disable Delay (BL, BR via DEC, TRI to BL, BR)	DECTRI_DEL	—	3.59	—	2.65	—	1.91	—	1.48	ns
Decoder										
Decoder Delay (BR[9:8], BL[9:8] to DEC)	DEC98_DEL	—	2.39	—	1.85	—	1.27	—	1.02	ns
Decoder Delay (BR[7:0], BL[7:0] to DEC)	DEC_DEL	—	2.35	—	1.82	—	1.23	—	0.99	ns

Timing Characteristics (continued)

Table 48. Programmable I/O (PIO) Timing Characteristics (continued)

OR3Cxx Commercial: VDD = 5.0 V ± 5%, 0 °C < TA < 70 °C; Industrial: VDD = 5.0 V ± 10%, –40 °C < TA < +85 °C.
OR3Txxx Commercial: VDD = 3.0 V to 3.6 V, 0 °C < TA < 70 °C; Industrial: VDD = 3.0 V to 3.6 V, –40 °C < TA < +85 °C.

Parameter	Symbol	Speed								Unit
		-4		-5		-6		-7		
		Min	Max	Min	Max	Min	Max	Min	Max	
PIO Logic Block Delays										
Out to Pad (OUT[2:1] via logic to pad):										
Fast	OUTLF_DEL	—	5.09	—	4.21	—	2.63	—	2.17	ns
Slewlim	OUTLSL_DEL	—	7.86	—	6.49	—	3.49	—	2.91	ns
Sinklim	OUTLSI_DEL	—	9.41	—	7.98	—	8.08	—	7.32	ns
Outreg to Pad (OUTREG via logic to pad):										
Fast	OUTRF_DEL	—	6.71	—	5.44	—	3.56	—	2.78	ns
Slewlim	OUTRSL_DEL	—	9.47	—	7.71	—	4.42	—	3.52	ns
Sinklim	OUTRSI_DEL	—	11.03	—	9.20	—	8.98	—	7.94	ns
Clock to Pad (ECLK, CLK via logic to pad):										
Fast	OUTCF_DEL	—	6.97	—	5.68	—	3.71	—	2.91	ns
Slewlim	OUTCSL_DEL	—	9.74	—	7.96	—	4.57	—	3.64	ns
Sinklim	OUTCSI_DEL	—	11.29	—	9.45	—	9.13	—	8.07	ns
3-State FF Delays										
3-state Enable/Disable Delay (TS direct to pad):										
Fast	TSF_DEL	—	4.93	—	4.09	—	2.33	—	1.88	ns
Slewlim	TSSL_DEL	—	7.70	—	6.37	—	3.00	—	2.41	ns
Sinklim	TSSI_DEL	—	9.25	—	7.86	—	7.95	—	7.23	ns
Local Set/Reset (async) to Pad (LSR to pad):										
Fast	TSLSRF_DEL	—	8.25	—	6.65	—	4.24	—	3.39	ns
Slewlim	TSLSRSL_DEL	—	11.01	—	8.92	—	4.92	—	3.92	ns
Sinklim	TSLSRSI_DEL	—	12.57	—	10.41	—	9.87	—	8.74	ns
Global Set/Reset to Pad (GSRN to pad):										
Fast	TSGSRF_DEL	—	7.52	—	6.09	—	3.88	—	3.11	ns
Slewlim	TSGSRSL_DEL	—	10.28	—	8.36	—	4.55	—	3.64	ns
Sinklim	TSGSRSI_DEL	—	11.84	—	9.85	—	9.51	—	8.45	ns
3-State FF Setup Timing:										
TS to ExpressCLK (TS to ECLK)	TSE_SET	0.00	—	0.00	—	0.00	—	0.00	—	ns
TS to Clock (TS to CLK)	TS_SET	0.00	—	0.00	—	0.00	—	0.00	—	ns
Local Set/Reset (sync) to Clock (LSR to CLK)	TSLSR_SET	0.28	—	0.21	—	0.17	—	0.18	—	ns
3-State FF Hold Timing:										
TS from ExpressCLK (TS from ECLK)	TSE_HLD	0.85	—	0.68	—	0.44	—	0.34	—	ns
TS from Clock (TS from CLK)	TS_HLD	0.85	—	0.68	—	0.44	—	0.34	—	ns
Local Set/Reset (sync) from Clock (LSR from CLK)	TSLSR_HLD	0.00	—	0.00	—	0.00	—	0.00	—	ns
Clock to Pad Delay (ECLK, SCLK to pad):										
Fast	TSREGF_DEL	—	5.94	—	4.82	—	2.84	—	2.23	ns
Slewlim	TSREGSL_DEL	—	8.70	—	7.10	—	3.52	—	2.76	ns
Sinklim	TSREGSI_DEL	—	10.26	—	8.59	—	8.47	—	7.58	ns

Note: The delays for all input buffers assume an input rise/fall time of <1 V/ns.

Timing Characteristics (continued)

Table 49. Microprocessor Interface (MPI) Timing Characteristics (continued)

OR3Cxx Commercial: V_{DD} = 5.0 V ± 5%, 0 °C < T_A < 70 °C; Industrial: V_{DD} = 5.0 V ± 10%, –40 °C < T_A < +85 °C.
OR3Txxx Commercial: V_{DD} = 3.0 V to 3.6 V, 0 °C < T_A < 70 °C; Industrial: V_{DD} = 3.0 V to 3.6 V, –40 °C < T_A < +85 °C.

Parameter	Symbol	Speed								Unit
		–4		–5		–6		–7		
		Min	Max	Min	Max	Min	Max	Min	Max	
User Logic Delay[5]	User Logic Delay	—	—	—	—	—	—	—	—	ns
User Start Delay (MPI_CLK falling to USTART)[6]	USTART_DEL	—	3.6	—	3.4	—	3.3	—	2.8	ns
User Start Clear Delay (MPI_CLK to USTART)	USTARTCLR_DEL	—	7.5	—	7.3	—	7.1	—	6.0	ns
User End Delay (USTART low to UEND low)[7]	UEND_DEL	—	—	—	—	—	—	—	—	ns
Synchronous User Timing:										
User End Setup (UEND to MPI_CLK)	UEND_SET	0.00	—	0.00	—	0.00	—	0.00	—	ns
User End Hold (UEND to MPI_CLK)	UEND_HLD	1.0	—	0.95	—	0.88	—	0.75	—	ns
Data Setup for Read (D[7:0] to MPI_CLK)[9]	RDS_SET	—	—	—	—	—	—	—	—	ns
Data Hold for Read (D[7:0] from MPI_CLK)[9]	RDS_HLD	—	—	—	—	—	—	—	—	ns
Asynchronous User Timing:										
User End to Read Data Delay (UEND to D[7:0])[10]	RDA_DEL	—	—	—	—	—	—	—	—	ns
Data Hold from User Start (low)[9]	RDA_HLD	—	—	—	—	—	—	—	—	ns
Interrupt Request Pulse Width[8]	TUIRQ_PW	—	—	—	—	—	—	—	—	ns

1. For user system flexibility, $\overline{CS0}$ and CS1 may be set up to any one of the three rising clock edges, beginning with the rising clock edge when $\overline{MPI\_STRB}$ is low. If both chip selects are valid and the setup time is met, the MPI will latch the chip select state, and $\overline{CS0}$ and CS1 may go inactive before the end of the read/write cycle.
2. 0.5 MPI_CLK.
3. Write data and W/$\overline{R}$ have to be valid starting from the clock cycle after both $\overline{ADS}$ and $\overline{CS0}$ and CS1 are recognized.
4. Write data and W/$\overline{R}$ have to be held until the microprocessor receives a valid $\overline{RDYRCV}$.
5. User Logic Delay has no predefined value. The user must generate a UEND signal to complete the cycle.
6. USTART_DEL is based on the falling clock edge.
7. There is no specific time associated with this delay. The user must assert UEND low to complete this cycle.
8. The user must assert interrupt request low until a service routine is executed.
9. This should be at least one MPI_CLK cycle.
10. User should set up read data so that RDS_SET and RDS_HLD can be met for the microprocessor timing.

Notes:
Read and write descriptions are referenced to the host microprocessor; e.g., a read is a read by the host (*PowerPC*, *i960*) from the FPGA. *PowerPC* and *i960* timings to/from the clock are relative to the clock at the FPGA microprocessor interface clock pin (MPI_CLK).

Timing Characteristics (continued)

Table 51. Boundary-Scan Timing Characteristics

OR3Cxx Commercial: V_{DD} = 5.0 V ± 5%, 0 °C < T_A < 70 °C; Industrial: V_{DD} = 5.0 V ± 10%, –40 °C < T_A < +85 °C.
OR3Txxx Commercial: V_{DD} = 3.0 V to 3.6 V, 0 °C < T_A < 70 °C; Industrial: V_{DD} = 3.0 V to 3.6 V, –40 °C < T_A < +85 °C.

Parameter	Symbol	Min	Max	Unit
TDI/TMS to TCK Setup Time	T_S	25.0	—	ns
TDI/TMS Hold Time from TCK	T_H	0.0	—	ns
TCK Low Time	T_{CL}	50.0	—	ns
TCK High Time	T_{CH}	50.0	—	ns
TCK to TDO Delay	T_D	—	20.0	ns
TCK Frequency	T_{TCK}	—	10.0	MHz

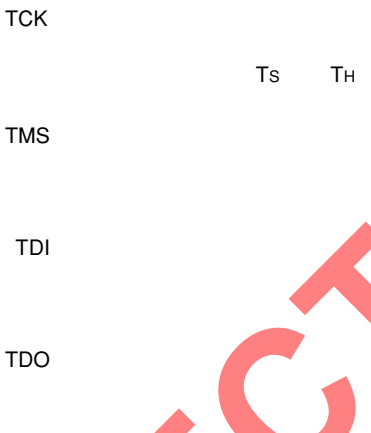


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Figure 75. Boundary-Scan Timing Diagram

Timing Characteristics (continued)

Table 60. General Configuration Mode Timing Characteristics (continued)

OR3Cxx Commercial: V_{DD} = 5.0 V ± 5%, 0 °C < T_A < 70 °C; Industrial: V_{DD} = 5.0 V ± 10%, –40 °C < T_A < +85 °C.
OR3Txxx Commercial: V_{DD} = 3.0 V to 3.6 V, 0 °C < T_A < 70 °C; Industrial: V_{DD} = 3.0 V to 3.6 V, –40 °C < T_A < +85 °C.

Parameter	Symbol	Min	Max	Unit
Slave Parallel Mode				
Power-on Reset Delay	T_{PO}	3.90	13.10	ms
CCLK Period:	T_{CCLK}			
OR3Cxx		40.00	—	ns
OR3Txxx		15.00	—	ns
Configuration Latency (normal mode):	T_{CL}			
OR3T20		0.36	—	ms
OR3T30		0.47	—	ms
OR3T55		0.72	—	ms
OR3C80		2.81	—	ms
OR3T80		1.05	—	ms
OR3T125		1.64	—	ms
Partial Reconfiguration (explicit mode):	T_{PR}			
OR3T20		0.48	—	µs/frame
OR3T30		0.54	—	µs/frame
OR3T55		0.65	—	µs/frame
OR3C80		2.04	—	µs/frame
OR3T80		0.77	—	µs/frame
OR3T125		0.93	—	µs/frame
$\overline{\text{INIT}}$ Timing				
$\overline{\text{INIT}}$ High to CCLK Delay:	T_{INIT_CCLK}			
Slave Parallel		1.00	—	µs
Slave Serial		1.00	—	µs
Master Serial:				
(M3 = 1)		1.00	3.40	µs
(M3 = 0)		0.50	2.00	µs
Master Parallel:				
(M3 = 1)		4.80	16.20	µs
(M3 = 0)		1.00	3.60	µs
Initialization Latency ($\overline{\text{PRGM}}$ high to $\overline{\text{INIT}}$ high):	T_{IL}			
OR3T20		0.21	0.68	ms
OR3T30		0.24	0.79	ms
OR3T55		0.30	1.00	ms
OR3C/T80		0.36	1.20	ms
OR3T125		0.45	1.50	ms
$\overline{\text{INIT}}$ High to $\overline{\text{WR}}$, Asynchronous Peripheral	T_{INIT_WR}	2.00	—	µs

Note: T_{PO} is triggered when V_{DD} reaches between 3.0 V to 4.0 V for the OR3Cxx and between 2.7 V and 3.0 V for the OR3Txxx.

Timing Characteristics (continued)

Table 63. Asynchronous Peripheral Configuration Mode Timing Characteristics

OR3Cxx Commercial: VDD = 5.0 V ± 5%, 0 °C < TA < 70 °C; Industrial: VDD = 5.0 V ± 10%, –40 °C < TA < +85 °C.
OR3Txxx Commercial: VDD = 3.0 V to 3.6 V, 0 °C < TA < 70 °C; Industrial: VDD = 3.0 V to 3.6 V, –40 °C < TA < +85 °C.

Parameter	Symbol	Min	Max	Unit
$\overline{WR}$, $\overline{CS0}$, and CS1 Pulse Width	TWR	50.00	—	ns
D[7:0] Setup Time: 3Cxx 3Txxx	TS	 20.00 10.50	 — —	 ns ns
D[7:0] Hold Time	TH	0.00	—	ns
RDY Delay	TRDY	—	40.00	ns
RDY Low	TB	1.00	8.00	CCLK Periods
Earliest $\overline{WR}$ After RDY Goes High*	TWR2	0.00	—	ns
$\overline{RD}$ to D7 Enable/Disable	TDEN	—	40.00	ns
CCLK to DOUT	TD	—	5.00	ns

* This parameter is valid whether the end of not RDY is determined from the RDY pin or from the D7 pin.

Notes:
Serial data is transmitted out on DOUT on the falling edge of CCLK after the byte is input on D[7:0].
D[6:0] timing is the same as the write data portion of the D7 waveform because D[6:0] are not enabled by $\overline{RD}$.

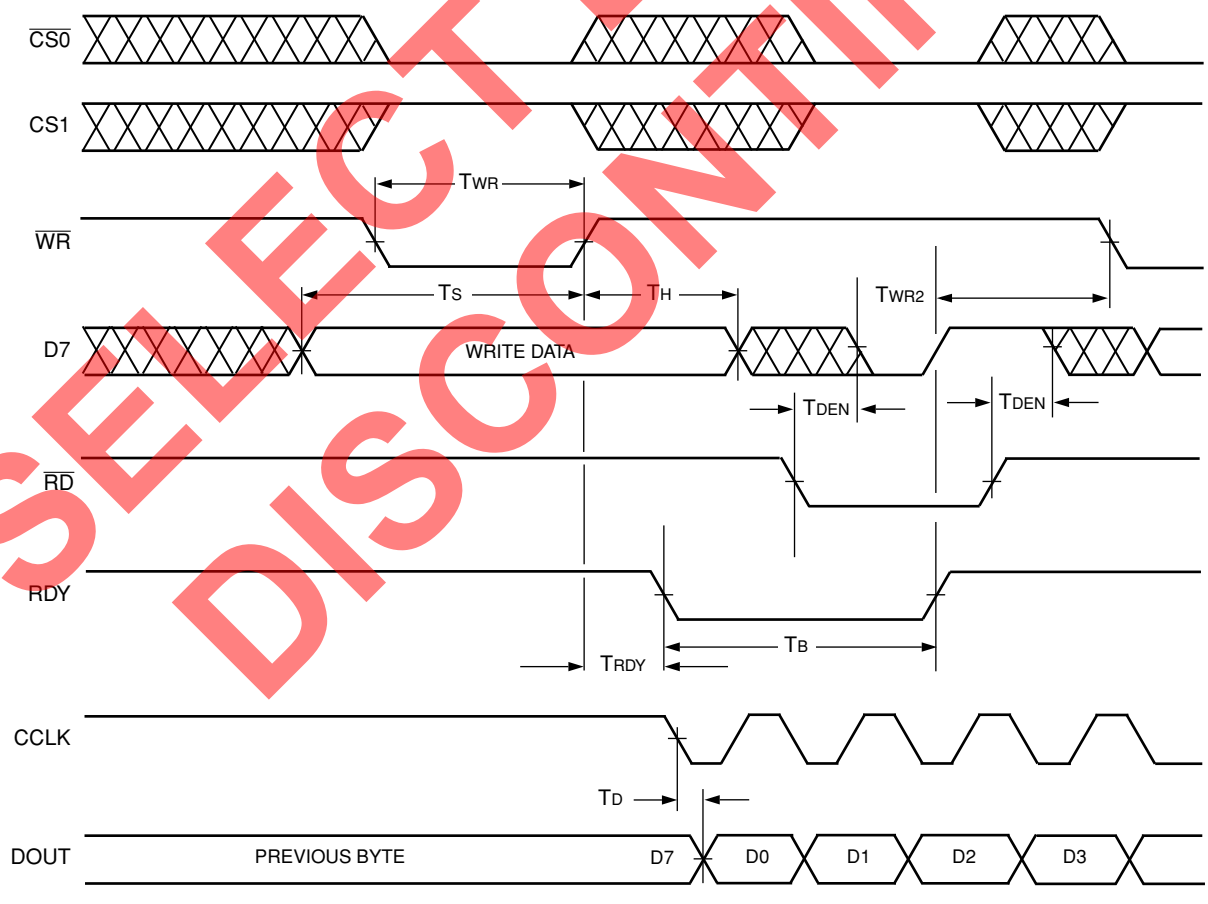
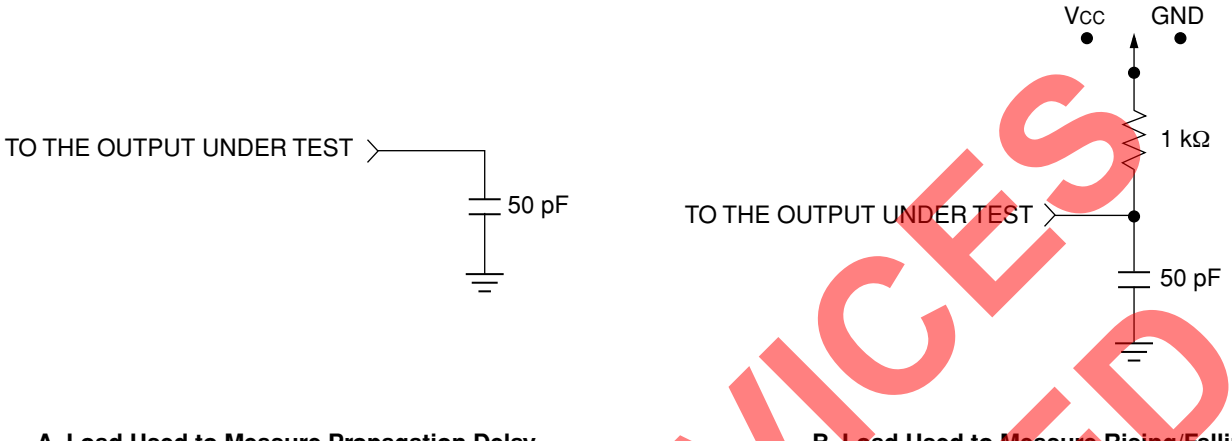


Figure 85. Asynchronous Peripheral Configuration Mode Timing Diagram

Input/Output Buffer Measurement Conditions



A. Load Used to Measure Propagation Delay

B. Load Used to Measure Rising/Falling Edges

Note: Switch to VDD for TPLZ/TPZL; switch to GND for TPHZ/TPZH.

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Figure 89. ac Test Loads

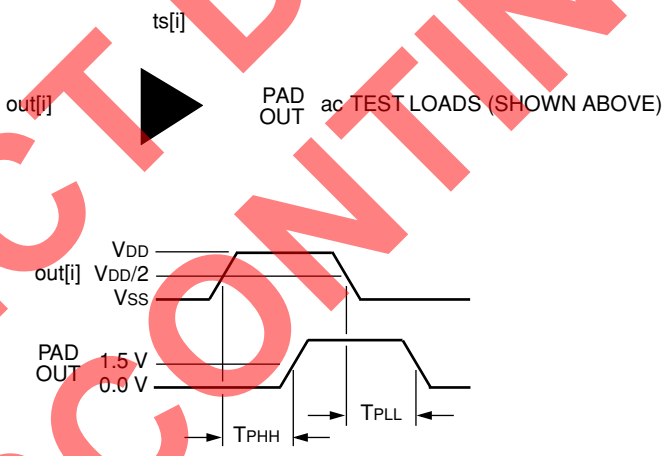

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Figure 90. Output Buffer Delays

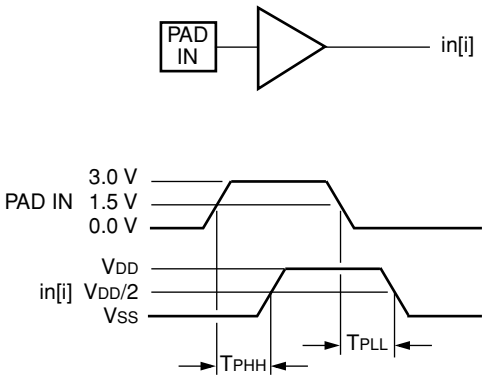

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Figure 91. Input Buffer Delays

Pin	OR3T30 Pad	OR3T55 Pad	OR3C/T80 Pad	OR3T125 Pad	Function
171	PR3B	PR4B	PR5B	PR6A	I/O
172	PR3C	PR4D	PR5D	PR5A	I/O
173	PR3D	PR3A	PR4A	PR4A	I/O
174	VSS	VSS	VSS	VSS	VSS
175	PR2A	PR2A	PR3A	PR3A	I/O-WR
176	PR2D	PR2C	PR2A	PR2A	I/O
177	PR1A	PR1A	PR1A	PR1A	I/O
178	PR1D	PR1D	PR1D	PR1D	I/O
179	VSS	VSS	VSS	VSS	VSS
180	PRD_CFGN	PRD_CFGN	PRD_CFGN	PRD_CFGN	RD_CFG
181	VSS	VSS	VSS	VSS	VSS
182	VDD	VDD	VDD	VDD	VDD
183	VSS	VSS	VSS	VSS	VSS
184	PT14D	PT18D	PT22D	PT28D	I/O-SECKUR
185	PT14C	PT18B	PT22A	PT28A	I/O
186	PT14A	PT18A	PT21D	PT27D	I/O
187	PT13D	PT17D	PT21A	PT27A	I/O-RDY/RCLK/MPI_ALE
188	—	VSS	VSS	VSS	VSS
189	PT13B	PT16D	PT19D	PT25D	I/O
190	PT13A	PT16C	PT19C	PT25C	I/O
191	PT12D	PT16A	PT19A	PT25A	I/O
192	PT12C	PT15D	PT18D	PT24D	I/O-D7
193	PT12A	PT14D	PT17D	PT23D	I/O
194	PT11D	PT14A	PT17A	PT22D	I/O
195	PT11C	PT13D	PT16D	PT21D	I/O
196	PT11B	PT13B	PT16B	PT20D	I/O-D6
197	VDD	VDD	VDD	VDD	VDD
198	PT10D	PT12D	PT15D	PT19D	I/O
199	PT10C	PT12C	PT15B	PT19A	I/O
200	PT10B	PT12B	PT15A	PT18D	I/O
201	PT10A	PT12A	PT14C	PT18A	I/O-D5
202	PT9D	PT11D	PT14B	PT17D	I/O
203	PT9C	PT11C	PT13D	PT17A	I/O
204	PT9B	PT11B	PT13C	PT16D	I/O
205	PT9A	PT11A	PT13A	PT16A	I/O-D4
206	VSS	VSS	VSS	VSS	VSS
207	PECKT	PECKT	PECKT	PECKT	I-ECKT
208	PT8C	PT10C	PT12C	PT15C	I/O
209	PT8B	PT10B	PT12B	PT15B	I/O
210	PT8A	PT10A	PT12A	PT15A	I/O-D3
211	VSS	VSS	VSS	VSS	VSS
212	PT7D	PT9D	PT11D	PT14D	I/O