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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	-
Number of Logic Elements/Cells	1568
Total RAM Bits	25600
Number of I/O	171
Number of Gates	48000
Voltage - Supply	3V ~ 3.6V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 70°C (TA)
Package / Case	208-BFQFP
Supplier Device Package	208-PQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/or3t307s208-db

Description

FPGA Overview

The *ORCA* Series 3 FPGAs are a new generation of SRAM-based FPGAs built on the successful OR2C/TxxA FPGA Series, with enhancements and innovations geared toward today's high-speed designs and tomorrow's systems on a single chip. Designed from the start to be synthesis friendly and to reduce place and route times while maintaining the complete routability of the *ORCA* 2C/2T devices, Series 3 more than doubles the logic available in each logic block and incorporates system-level features that can further reduce logic requirements and increase system speed. *ORCA* Series 3 devices contain many new patented enhancements and are offered in a variety of packages, speed grades, and temperature ranges.

The *ORCA* Series 3 FPGAs consist of three basic elements: programmable logic cells (PLCs), programmable input/output cells (PICs), and system-level features. An array of PLCs is surrounded by PICs. Each PLC contains a programmable function unit (PFU), a supplemental logic and interconnect cell (SLIC), local routing resources, and configuration RAM. Most of the FPGA logic is performed in the PFU, but decoders, *PAL*-like functions, and 3-state buffering can be performed in the SLIC. The PICs provide device inputs and outputs and can be used to register signals and to perform input demultiplexing, output multiplexing, and other functions on two output signals. Some of the system-level functions include the new microprocessor interface (MPI) and the programmable clock manager (PCM).

PLC Logic

Each PFU within a PLC contains eight 4-input (16-bit) look-up tables (LUTs), eight latches/flip-flops (FFs), and one additional flip-flop that may be used independently or with arithmetic functions.

The PFU is organized in a twin-quad fashion: two sets of four LUTs and FFs that can be controlled independently. LUTs may also be combined for use in arithmetic functions using fast-carry chain logic in either 4-bit or 8-bit modes. The carry-out of either mode may be registered in the ninth FF for pipelining. Each PFU may also be configured as a synchronous 32 x 4 single- or dual-port RAM or ROM. The FFs (or latches) may obtain input from LUT outputs or directly from invertible PFU inputs, or they can be tied high or tied low. The FFs also have programmable clock polarity, clock enables, and local set/reset.

The SLIC is connected to PLC routing resources and to the outputs of the PFU. It contains 3-state, bidirectional buffers and logic to perform up to a 10-bit AND function for decoding, or an AND-OR with optional INVERT (AOI) to perform *PAL*-like functions. The 3-state drivers in the SLIC and their direct connections to the PFU outputs make fast, true 3-state buses possible within the FPGA, reducing required routing and allowing for real-world system performance.

Architecture (continued)

5-4489(F)

Figure 1. OR3T55 Array

Programmable Logic Cells (continued)

Half-Logic Mode

Series 3 FPGAs are based upon a twin-quad architecture in the PFUs. The byte-wide nature (eight LUTs, eight latches/FFs) may just as easily be viewed as two nibbles (two sets of four LUTs, four latches/FFs). The two nibbles of the PFU are organized so that any nibble-wide feature (excluding some softwired LUT topologies) can be swapped with any other nibble-wide feature in another PFU. This provides for very flexible use of logic and for extremely flexible routing. The half-logic mode of the PFU takes advantage of the twin-quad architecture and allows half of a PFU, K[7:4] and associated latches/FFs, to be used in logic mode while the other half of the PFU, K[3:0] and associated latches/FFs, is used in ripple mode. In half-logic mode, the ninth FF may be used as a general-purpose FF or as a register in the ripple mode carry chain.

Ripple Mode

The PFU LUTs can be combined to do byte-wide ripple functions with high-speed carry logic. Each LUT has a dedicated carry-out net to route the carry to/from any adjacent LUT. Using the internal carry circuits, fast arithmetic, counter, and comparison functions can be implemented in one PFU. Similarly, each PFU has carry-in (CIN, FCIN) and carry-out (COUT, FCOUT) ports for fast-carry routing between adjacent PFUs.

The ripple mode is generally used in operations on two data buses. A single PFU can support an 8-bit ripple function. Data buses of 4 bits and less can use the nibble-wide ripple chain that is available in half-logic mode. This nibble-wide ripple chain is also useful for longer ripple chains where the length modulo 8 is four or less. For example, a 12-bit adder (12 modulo 8 = 4) can be implemented in one PFU in ripple mode (8 bits) and one PFU in half-logic mode (4 bits), freeing half of a PFU for general logic mode functions.

Each LUT has two operands and a ripple (generally carry) input, and provides a result and ripple (generally carry) output. A single bit is rippled from the previous LUT and is used as input into the current LUT. For LUT K0, the ripple input is from the PFU CIN or FCIN port. The CIN/FCIN data can come from either the fast-carry routing (FCIN) or the PFU input (CIN), or it can be tied to logic 1 or logic 0.

In the following discussions, the notations LUT K7/K3 and F[7:0]/F[3:0] are used to denote the LUT that provides the carry-out and the data outputs for full PFU ripple operation (K7, F[7:0]) and half-logic ripple operation (K3, F[3:0]), respectively. The ripple mode diagram in Figure 6 shows full PFU ripple operation, with half-logic ripple connections shown as dashed lines.

The result output and ripple output are calculated by using generate/propagate circuitry. In ripple mode, the two operands are input into Kz[1] and Kz[0] of each LUT. The result bits, one per LUT, are F[7:0]/F[3:0] (see Figure 6). The ripple output from LUT K7/K3 can be routed on dedicated carry circuitry into any of four adjacent PLCs, and it can be placed on the PFU COUT/FCOUT outputs. This allows the PLCs to be cascaded in the ripple mode so that nibble-wide ripple functions can be expanded easily to any length.

Result outputs and the carry-out may optionally be registered within the PFU. The capability to register the ripple results, including the carry output, provides for improved counter performance and simplified pipelining in arithmetic functions.

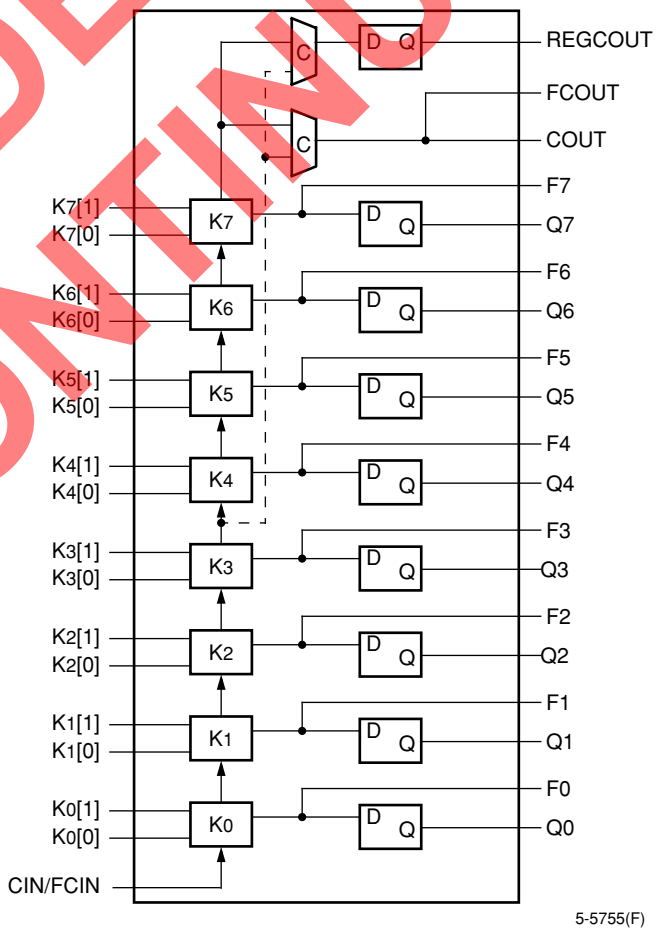


Figure 6. Ripple Mode

Programmable Logic Cells (continued)

Data is written to the write data, write address, and write enable registers on the active edge of the clock, but data is not written into the RAM until the next clock edge one-half cycle later. The read port is actually asynchronous, providing the user with read data very quickly after setting the read address, but timing is also provided so that the read port may be treated as fully synchronous for write then read applications. If the read and write address lines are tied together (maintaining MSB to MSB, etc.), then the dual-port RAM operates as a synchronous single-port RAM. If the write enable is disabled, and an initial memory contents is provided at configuration time, the memory acts as a ROM (the write data and write address ports and write port enables are not used).

Wider memories can be created by operating two or more memory mode PFUs in parallel, all with the same address and control signals, but each with a different nibble of data. To increase memory word depth above 32, two or more PLCs can be used. Figure 10 shows a 128 x 8 dual-port RAM that is implemented in eight PLCs. This figure demonstrates data path width expansion by placing two memories in parallel to achieve an 8-bit data path. Depth expansion is applied to achieve 128 words deep using the 32-word deep PFU memories. In addition to the PFU in each PLC, the SLIC (described in the next section) in each PLC is used for read address decodes and 3-state drivers. The 128 x 8 RAM shown could be made to operate as a single-port RAM by tying (bit-for-bit) the read and write addresses.

To achieve depth expansion, one or two of the write address bits (generally the MSBs) are routed to the write port enables as in Figure 10. For 2 bits, the bits select which 32-word bank of RAM of the four available from a decode of two WPE inputs is to be written. Similarly, 2 bits of the read address are decoded in the SLIC and are used to control the 3-state buffers through which the read data passes. The write data bus is common, with separate nibbles for width expansion, across all PLCs, and the read data bus is common (again, with separate nibbles) to all PLCs at the output of the 3-state buffers.

Figure 10 also shows a new optional capability to provide a read enable for RAMs/ROMs in Series 3 using the SLIC cell. The read enable will 3-state the read data bus when inactive, allowing the write data and read data buses to be tied together if desired.

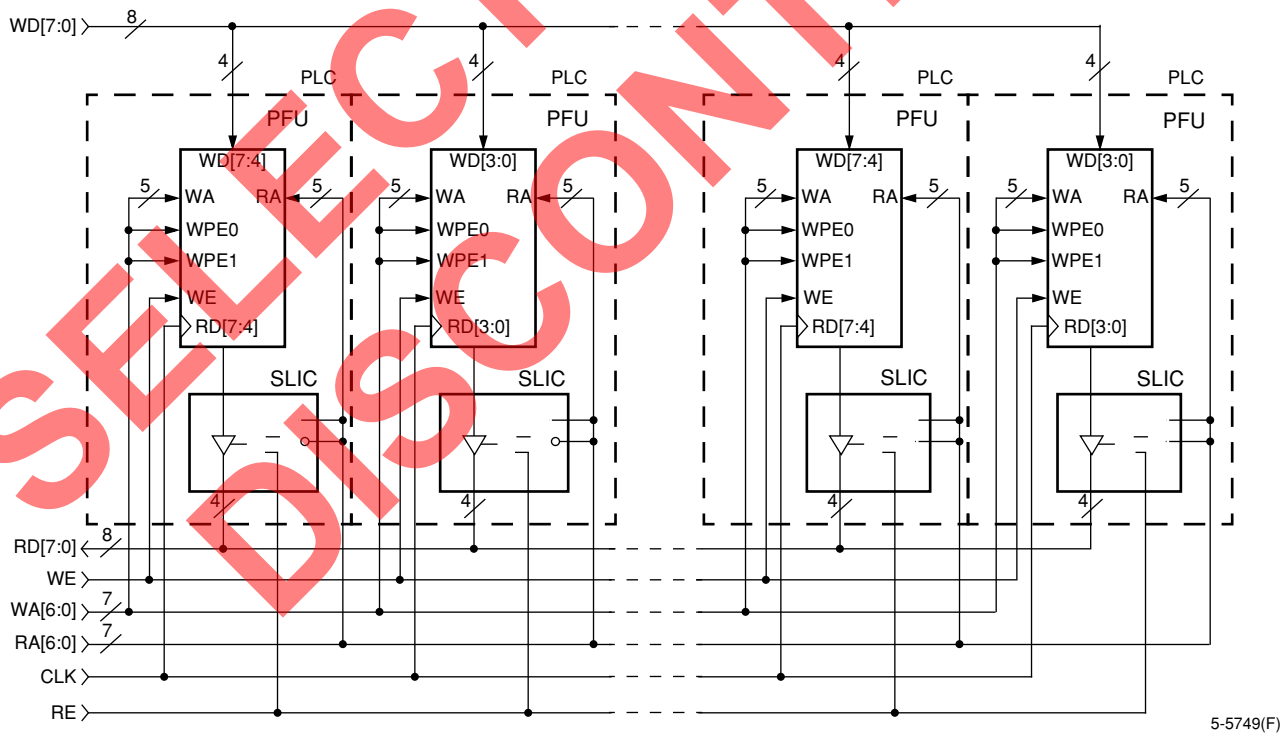


Figure 10. Memory Mode Expansion Example—128 x 8 RAM

Programmable Logic Cells (continued)

The GSRN signal is only asynchronous, and it sets/resets all latches/FFs in the FPGA based upon the set/reset configuration bit for each latch/FF. The set/reset value determines whether GSRN and LSR are set or reset inputs. The set/reset value is independent for each latch/FF. A new option is available to disable the GSRN function per PFU after initial device configuration.

The latch/FF can be configured to have a data front-end select. Two data inputs are possible in the front-end select mode, with the SEL signal used to select which data input is used. The data input into each latch/FF is from the output of its associated LUT, F[7:0], or direct from DIN[7:0], bypassing the LUT. In the front-end data select mode, both signals are available to the latches/FFs.

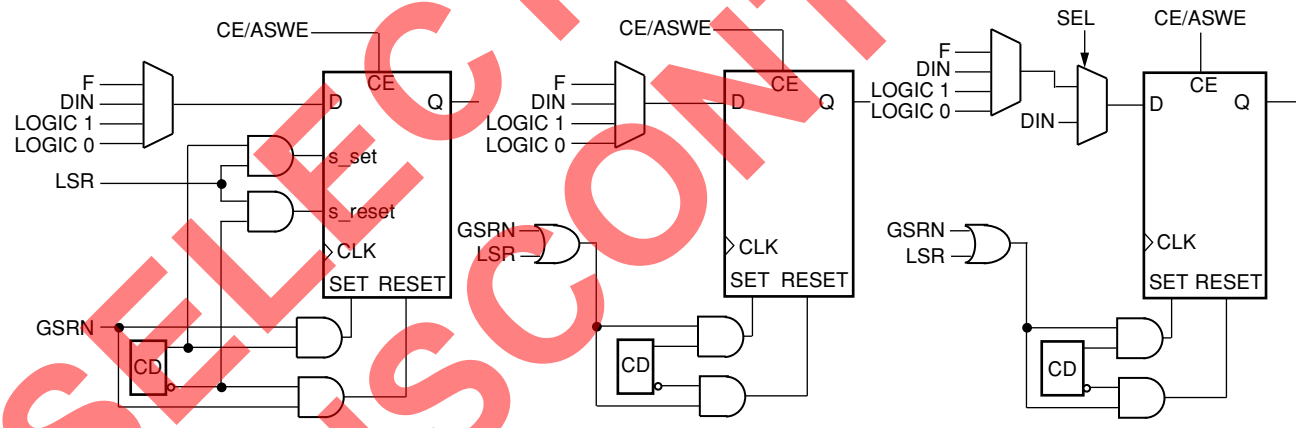
If either or both of these inputs is unused or is unavailable, the latch/FF data input can be tied to a logic 0 or logic 1 instead (the default is logic 0).

The latches/FFs can be configured in three basic modes:

1. Local synchronous set/reset: the input into the PFU's LSR port is used to synchronously set or reset each latch/FF.
2. Local asynchronous set/reset: the input into LSR asynchronously sets or resets each latch/FF.
3. Latch/FF with front-end select, LSR either synchronous or asynchronous: the data select signal selects the input into the latches/FFs between the LUT output and direct data in.

For all three modes, each latch/FF can be independently programmed as either set or reset. Figure 17 provides the logic functionality of the front-end select, global set/reset, and local set/reset operations.

The ninth PFU FF, which is generally associated with registering the carry-out signal in ripple mode functions, can be used as a general-purpose FF. It is only an FF and is not capable of being configured as a latch. Because the ninth FF is not associated with an LUT, there is no front-end data select. The data input to the ninth FF is limited to the CIN input, logic 1, logic 0, or the carry-out in ripple and half-logic modes.



Key: C = configuration data.

Figure 17. Latch/FF Set/Reset Configurations

Programmable Logic Cells (continued)

PLC Architectural Description

Figure 21 is an architectural drawing of the PLC (as seen in ispLEVER) that reflects the PFU, the routing segments, and the CIPs. A discussion of each of the letters in the drawing follows.

A. These are switching routing segments (xSW) that give the router flexibility. In general switching theory, the more levels of indirection there are in the routing, the more routable the network is. The xSW segments can also connect to the xSW lines in adjacent PLCs.

B. These CIPs connect the x1 routing. These are located in the middle of the PLC to allow the block to connect to either the left end of the horizontal x1 segment from the right or the right end of the horizontal x1 segment from the left, or both. By symmetry, the same principle is used in the vertical direction.

C. This set of CIPs is used to connect the x1 and x5 nets to the xSW segments or to other x1 and x5 nets. The CIPs on the major diagonal allow data to be transmitted on a bit-by-bit basis from x1 nets to the xSW segments and between the x1 and x5 nets.

D. This structure is the supplemental logic and interconnect cell, or SLIC. It contains 3-statable bidirectional buffers and logic for building decoders and AND-OR-INVERT type structures.

E. These are the primary and secondary elements of the flexible input structure or FINS. FINS is a switch matrix that provides high connectivity while retaining routing capability. FINS also includes feedback paths for softwired LUT implementation.

F. This is the PFU output switch matrix. It is a complex switch network which, like the FINS at the input, provides high connectivity and maintains routability.

G. This set of CIPs allows an xBID segment to transfer a signal to/from xSW segments on each side. The BIDIs can access the PFU through the xSW segments. These CIPs allow data to be routed through the BIDIs for amplification or 3-state control and continue to another PLC. They also provide an alternative routing resource to improve routability.

H. These CIPs are used to transfer data from/to the xBID segments to/from the x1 and xL routing segments. These CIPs have been optimized to allow the BIDI buffers to drive the loads usually seen when using each type of routing segment.

I. Clock input to PFU.

J. These are the ten switched output routing segments from the PFU. They connect to the PLC switching segments and are input to the SLIC.

K. These lines deliver the auxiliary signals clock enable (CE), local set/reset (LSR), front-end select (SEL), add/subtract/write enable (ASWE), as well as the carry signals (CIN and FCIN) to the latches/FFs.

L. This is the local clock buffer. Any of the horizontal and vertical xL lines can drive the clock input of the PLC latches/FFs. The clock routing segments (vCLK and hCLK) and multiplexers/drivers are used to connect to the xL routing segments for low-skew, low-delay global signals.

M. These routing segments are used to route the fast-carry signal to/from the neighboring four PLCs. The carry-out (COUT) and registered carry-out (REGCOUT) can also be routed out of the PFU.

N. This is the E2 control routing segment. It runs from the SLIC DEC output to the FINS and also provides connectivity to all xBID segments.

O. The xH routing segments run one-half the length (width) of the array before being broken by a CIP.

P. These CIPs connect the xH segments to the xSW segments.

Q. The xBID segments are used to connect the SLIC to the xSW segments, x1 segments, x5 segments, and xL lines, as well as providing for diagonal PLC to PLC connections.

R. These CIPs provide connections from the xBID segments to the E1/E2 routing segments that feed PFU control inputs CE, LSR, CIN, ASWE, SEL, and the clock input. Alternatively, these CIPs connect the BIDI lines to the decoder (DEC) output of the SLIC, for routing the DEC signal.

S. These are clock spines (vCLK and hCLK) with the multiplexers and drivers to connect to the xL routing segments.

T. These CIPs connect xBID segments to switching segments in diagonally and orthogonally adjacent PFUs.

U. These CIPs connect xSW segments to the PFU output segments.

V. These CIPS connect xSW segments in orthogonally adjacent PFUs.

W. This is the SLIC 3-state control routing segment from the FINS to the SLIC 3-state control.

X. This is the E1 control routing segment. It provides a PFU input path from all xBID segments.

Y. These CIPs are used to select which xBID segments are connected to the E1/E2 signal as described in (R).

Programmable Input/Output Cells

(continued)

Table 9. PIO Options

Input	Option
Input Level	TTL, OR3Cxx only CMOS, OR3Cxx or OR3Txxx 3.3 V PCI Compliant, OR3Txxx 5 V PCI Compliant, OR3Txxx
Input Speed	Fast, Delayed
Float Value	Pull-up, Pull-down, None
Register Mode	Latch, FF, Fast Zero Hold FF, None (direct input)
Clock Sense	Inverted, Noninverted
Input Selection	Input 1, Input 2, Clock Input
Output	**Option**
Output Drive Current	12 mA/6 mA or 6 mA/3 mA
Output Function	Normal, Fast Open Drain
Output Speed	Fast, Slewlim, Sinklim
Output Source	FF Direct-out, General Routing
Output Sense	Active-high, Active-low
3-State Sense	Active-high, Active-low (3-state)
FF Clocking	ExpressCLK, System Clock
Clock Sense	Inverted, Noninverted
Logic Options	See Table 10.
I/O Controls	**Option**
Clock Enable	Active-high, Active-low, Always Enabled
Set/Reset Level	Active-high, Active-low, No Local Reset
Set/Reset Type	Synchronous, Asynchronous
Set/Reset Priority	CE over LSR, LSR over CE
GSR Control	Enable GSR, Disable GSR

5 V Tolerant I/O

The I/O on the OR3Txxx Series devices allow interconnection to both 3.3 V and 5 V devices (selectable on a per-pin basis).

The OR3Txxx devices will drive the pin to the 3.3 V levels when the output buffer is enabled. If the other device being driven by the OR3Txxx device has TTL-compatible inputs, then the device will not dissipate much input buffer power. This is because the OR3Txxx output is being driven to a higher level than the TTL level required. If the other device has a CMOS-compatible input, the amount of input buffer power will also be small. Both of these power values are dependent upon the input buffer characteristics of the other device when driven at the OR3Txxx output buffer voltage levels.

The OR3Txxx device has internal programmable pull-ups on the I/O buffers. These pull-up voltages are always referenced to V_{DD} and are always sufficient to pull the input buffer of the OR3Txxx device to a high state. The pin on the OR3Txxx device will be at a level 1.0 V below V_{DD} (minimum of 2.0 V with a minimum V_{DD} of 3.0 V). This voltage is sufficient to pull the external pin up to a 3.3 V CMOS high input level (1.8 V, min) or a TTL high input level (2.0 V, min) in a 5 V tolerant system. Therefore, in a 5 V tolerant system using 5 V CMOS parts, care must be taken to evaluate the use of these pull-ups to pull the pin of the OR3Txxx device to a typical 5 V CMOS high input level (2.2 V, min).

PCI Compliant I/O

The I/O on the OR3Txxx Series devices allows compliance with PCI Local Bus (Rev. 2.2) 5 V and 3.3 V signaling environments. The signaling environment used for each input buffer can be selected on a per-pin basis. The selection provides the appropriate I/O clamping diodes for PCI compliance. Choosing an IBT input buffer will provide PCI compliance in OR3Txxx devices. OR3Cxx devices have PCI Local Bus compliant I/Os for 5 V signaling.

Programmable Input/Output Cells

(continued)

Inputs

As outlined earlier in Table 9, there are six major options on the PIO inputs that can be selected in the ispLEVER tools. For OR3Cxx devices, the inputs and bidirectional buffers can be configured as either TTL or CMOS compatible. OR3Txxx devices support CMOS levels only for input or bidirectional buffers, have 5 V tolerant I/Os as previously explained, but can optionally be selected on a pin-by-pin basis to be PCI bus 3.3 V signaling compliant (PCI bus 5 V signaling compliance occurs in 5 V tolerant operation). The default buffer upon powerup for the unused sites is 5 V tolerant/5 V PCI compliant. Consult the *ORCA* macro library, Series 3 I/O cells, for the appropriate buffers. Inputs may have a pull-up or pull-down resistor selected on an input for signal stabilization and power management. Input signals in a PIO can be passed to PIC routing on any of three paths, two general signal paths into PIC routing, and/or a fast route into the clock routing system.

There is also a programmable delay available on the input. When enabled, this delay affects the IN1 and IN2 signals of each PIO, but not the clock input. The delay allows any signal to have a guaranteed zero hold time when input. This feature is discussed subsequently.

Inputs should have transition times of less than 500 ns and should not be left floating. If any pin is not used, it is 3-stated with an internal pull-up resistor enabled automatically after configuration.

Warning: During configuration, all OR3Txxx inputs have internal pull-ups enabled. If these inputs are driven to 5 V, they will draw substantial current (≅ 5 mA). This is due to the fact that the inputs are pulled up to 3 V.

Floating inputs increase power consumption, produce oscillations, and increase system noise. The OR3Cxx inputs have a typical hysteresis of approximately 280 mV (200 mV for the OR3Txxx) to reduce sensitivity to input noise. The PIC contains input circuitry which provides protection against latch-up and electrostatic discharge.

The other features of the PIO inputs relate to the new latch/FF structure in the input path. As shown in Figure 23, the input is optionally passed to a register or latch/register pair. These structures can operate in the modes listed in Table 9. In latch mode, the input signal is fed to a latch that is clocked by a system clock signal. The clock may be inverted or noninverted from its sense in the PIC routing. There is also a local set/reset signal to the latch from the PIC routing. The senses of these signals are also programmable as well as the capability to enable or disable the global set/reset signal and select the set/reset priority. The same control signals may also be used to control the input latch/FF when it is configured as a FF instead of a latch, with the addition of another control signal used as a clock enable.

Clock Distribution Network (continued)

Clock Distribution in the PLC Array

System Clock (SCLK)

The clock distribution network, or clock spine network, within the PLC array is designed to minimize clock skew while maximizing clock flexibility. Clock flexibility is expressed in two ways: the ease with which a single clock is routed to the entire array, and the capability to provide multiple clocks to the PLC array.

There is one horizontal and one vertical clock spine passing through each PLC. The horizontal clock spine is sourced from the PIC in the same row on either the left- or right-hand side of the array, with the source side (left or right) alternating for each row. The vertical clock spines are similarly sourced from the PICs alternating from the top or bottom of a column. Each clock spine is capable of driving one of the ten xL routing segments that run orthogonal to it within each PLC. Full connectivity to all PFUs is maintained due to the connectivity from the xL lines to the PFU clock signals described in the previous section; however, only an xL line in every other row (column) needs to be driven to allow the given clock signal to be distributed to every PFU. Figure 32 is a high-level diagram of the Series 3 system clock spine network with sample xL line connections for a 4 x 4 array of PLCs.

The clock spine structure previously described provides for complete distribution of a clock from any I/O pin to the entire PLC array by means of a single clock spine and long lines (xL). This distribution system also provides a means to have many different clocks routed to many different and dispersed locations in the PLC array. Each spine can carry a different clock signal, so for the OR3T55 (which has an 18 x 18 array of PLCs, implying nine clock spines per side), 36 input clock signals can be supported using the system clock network.

Fast Clock

Fast clocks are high-speed, low-skew clock spines that originate from the CLKCNTRL special function blocks (described later). There are four fast clock spines—one originating on the middle of each edge of the array. The spines run in the interquad region of the PLC array from their source side of the device to the last row or column on the opposite side of the device. The fast clocks connect to two long lines, xL[8] and xL[9], that run orthogonal to the spine direction in each PLC. These long lines can then be connected to the PFU clock input in the same manner as the general system clocks, and, like the system clock connections, xL lines are only needed in every other row (column) to distribute a clock to every PFU. The limited number of long-line connections and the low skew of the CLKCNTRL source combine to make the fast clocks a very robust, low-skew clock source.

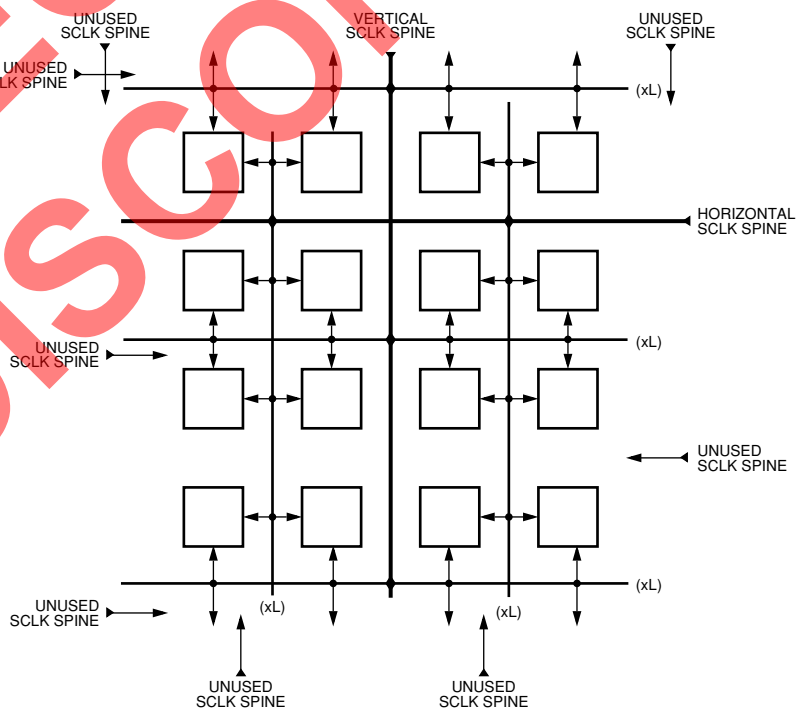


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Figure 32. *ORCA* Series 3 System Clock Distribution Overview

Programmable Clock Manager (PCM)

(continued)

PCM/FPGA Internal Interface

Writing and reading the PCM registers is done through a simple asynchronous interface that connects with the FPGA routing resources. Reads from the PCM by the FPGA logic are accomplished by setting up the 3-bit address, A[2:0], and then applying an active-high read enable (RE) pulse. The read data will be available as long as RE is held high. The address may be changed while RE is high, to read other addresses. When RE goes low, the data output bus is 3-stated.

Writes to the PCM by the FPGA logic are performed by applying the write data to the data input bus of the PCM, applying the 3-bit address to write to, and asserting the write enable (WE) signal high. Data will be written by the high-going transition of the WE pulse.

The read enable (RE) and write enable (WE) signals may not be active at the same time. For detailed timing information and specifications, see the Timing Characteristics section of this data sheet.

The LOCK signal output from the PCM to the FPGA routing indicates a stable output clock signal from the PCM. The LOCK signal is high when the PCM output clock parameters fall within the programmed values and the PCM specifications for jitter. Due to phase corrections that occur internal to the PCM, the LOCK signal might occasionally pulse low when the output clock is out of specification for only one or two clock cycles (high jitter due to temperature, voltage fluctuation, etc.) To accommodate these pulses, it is suggested that the user integrate the LOCK signal over a period suitable to their application to achieve the desired usage of the LOCK signal.

The LOCK signal will also pulse high and low during the acquisition time as the output clock stabilizes. True LOCK is only achieved when the LOCK signal is a solid high. Again, it is suggested that the user integrate the LOCK signal over a time period suitable to the subject application.

PCM Operation

Several features are available for the control of the PCM's overall operation. The PCM may be programmably enabled/disabled via bit 0 of register 7. When disabled, the analog power supply of the PCM is turned off, conserving power and eliminating the possibility of inducing noise into the system power buses. Individual bits (register 7, bits [2:1]) are provided to reset the DLL and PLL functions of the PCM. These resets affect only the logic generating the DLL or PLL function; they do not reset the divider values (DIV0, DIV1, DIV2) or registers [7:0]. The global set/reset (GSRN) is also programmably controlled via register 7, bit 7. If register 7, bit 7 is set to 1, GSRN will have no effect on the PCM logic, allowing the clock to operate during a global set/reset. This function allows the FPGA to be reset without affecting a clock that is sent off-chip and used elsewhere in the system. Bit 6 of register 7 affects the functionality of the PCM during configuration. If set to 1, this bit enables the PCM to operate during configuration, after the PCM has been configured. The PCM functionality is programmed via the bit stream. If register 7, bit 6 is 0, the PCM cannot function and its power supply is disabled until after the configuration DONE signal goes high.

When the PCM is powered up via register 7, bit 0, there is a wake-up time associated with its operation. Following the wake-up time, the PCM will begin to fully function, and, following an acquisition time during which the output clock may be unstable, the PCM will be in steady-state operation. There is also a shutdown time associated with powering off the PCM. The output clock will be unstable during this period. Waveforms and timing parameters can be found in the Timing Characteristics section of this data sheet.

FPGA States of Operation (continued)

Start-Up

After configuration, the FPGA enters the start-up phase. This phase is the transition between the configuration and operational states and begins when the number of CCLKs received after $\overline{\text{INIT}}$ goes high is equal to the value of the length count field in the configuration frame and when the end of configuration frame has been written. The system design issue in the start-up phase is to ensure the user I/Os become active without inadvertently activating devices in the system or causing bus contention. A second system design concern is the timing of the release of global set/reset of the PLC latches/FFs.

There are configuration options that control the relative timing of three events: DONE going high, release of the set/reset of internal FFs, and user I/Os becoming active. Figure 51 shows the start-up timing for *ORCA* FPGAs. The system designer determines the relative timing of the I/Os becoming active, DONE going high, and the release of the set/reset of internal FFs. In the *ORCA* Series FPGA, the three events can occur in any arbitrary sequence. This means that they can occur before or after each other, or they can occur simultaneously.

There are four main start-up modes: CCLK_NOSYNC, CCLK_SYNC, UCLK_NOSYNC, and UCLK_SYNC. The only difference between the modes starting with CCLK and those starting with UCLK is that for the UCLK modes, a user clock must be supplied to the start-up logic. The timing of start-up events is then based upon this user clock, rather than CCLK. The difference between the SYNC and NOSYNC modes is that for SYNC mode, the timing of two of the start-up events, release of the set/reset of internal FFs, and the I/Os becoming active is triggered by the rise of the external DONE pin followed by a variable number of rising clock edges (either CCLK or UCLK). For the NOSYNC mode, the timing of these two events is based only on either CCLK or UCLK.

DONE is an open-drain bidirectional pin that may include an optional (enabled by default) pull-up resistor to accommodate wired ANDing. The open-drain DONE signals from multiple FPGAs can be tied together (ANDed) with a pull-up (internal or external) and used as an active-high ready signal, an active-low PROM enable, or a reset to other portions of the system. When used in SYNC mode, these ANDed DONE pins can be used to synchronize the other two start-up events, since they can all be synchronized to the same external signal. This signal will not rise until all FPGAs release their DONE pins, allowing the signal to be pulled high.

The default for *ORCA* is the CCLK_SYNC synchronized start-up mode where DONE is released on the first CCLK rising edge, C1 (see Figure 51). Since this is a synchronized start-up mode, the open-drain DONE signal can be held low externally to stop the occurrence of the other two start-up events. Once the DONE pin has been released and pulled up to a high level, the other two start-up events can be programmed individually to either happen immediately or after up to four rising edges of CCLK (Di, Di + 1, Di + 2, Di + 3, Di + 4). The default is for both events to happen immediately after DONE is released and pulled high.

A commonly used design technique is to release DONE one or more clock cycles before allowing the I/O to become active. This allows other configuration devices, such as PROMs, to be disconnected using the DONE signal so that there is no bus contention when the I/Os become active. In addition to controlling the FPGA during start-up, other start-up techniques that avoid contention include using isolation devices between the FPGA and other circuits in the system, reassigning I/O locations, and maintaining I/Os as 3-stated outputs until contentions are resolved.

Each of these start-up options can be selected during bit stream generation in ispLEVER, using Advanced Options. For more information, please see the ispLEVER documentation.

FPGA Configuration Modes

There are eight methods for configuring the FPGA. Seven of the configuration modes are selected on the M0, M1, and M2 inputs. The eighth configuration mode is accessed through the boundary-scan interface. A fourth input, M3, is used to select the frequency of the internal oscillator, which is the source for CCLK in some configuration modes. The nominal frequencies of the internal oscillator are 1.25 MHz and 10 MHz. The 1.25 MHz frequency is selected when the M3 input is unconnected or driven to a high state.

There are three basic FPGA configuration modes: master, slave, and peripheral. The configuration data can be transmitted to the FPGA serially or in parallel bytes. As a master, the FPGA provides the control signals out to strobe data in. As a slave device, a clock is generated externally and provided into the CCLK input. In the three peripheral modes, the FPGA acts as a microprocessor peripheral. Table 34 lists the functions of the configuration mode pins. Note that two configuration modes previously available on the OR2Cxx and OR2C/TxxA devices (master parallel down and synchronous peripheral) have been removed for Series 3 devices.

Table 34. Configuration Modes

M2	M1	M0	CCLK	Configuration Mode	Data
0	0	0	Output	Master Serial	Serial
0	0	1	Input	Slave Parallel	Parallel
0	1	0	Output	Microprocessor: *Motorola* PowerPC*	Parallel
0	1	1	Output	Microprocessor: *Intel i960*	Parallel
1	0	0	Output	Master Parallel	Parallel
1	0	1	Output	Async Peripheral	Parallel
1	1	0	Reserved		
1	1	1	Input	Slave Serial	Serial

* *Motorola* is a registered trademark of Motorola, Inc.

Master Parallel Mode

The master parallel configuration mode is generally used to interface to industry-standard, byte-wide memory, such as the 2764 and larger EPROMs. Figure 54 provides the connections for master parallel mode. The FPGA outputs an 18-bit address on A[17:0] to memory and reads 1 byte of configuration data on the rising edge of RCLK. The parallel bytes are internally serialized starting with the least significant bit, D0. D[7:0] of the FPGA can be connected to D[7:0] of the microprocessor only if a standard prom file format is used. If a .bit or .rbt file is used from ispLEVER, then the user must mirror the bytes in the .bit or .rbt file OR leave the .bit or .rbt file unchanged and connect D[7:0] of the FPGA to D[0:7] of the microprocessor.

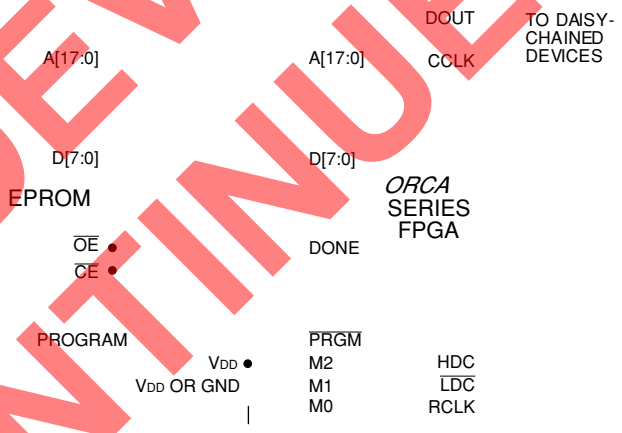
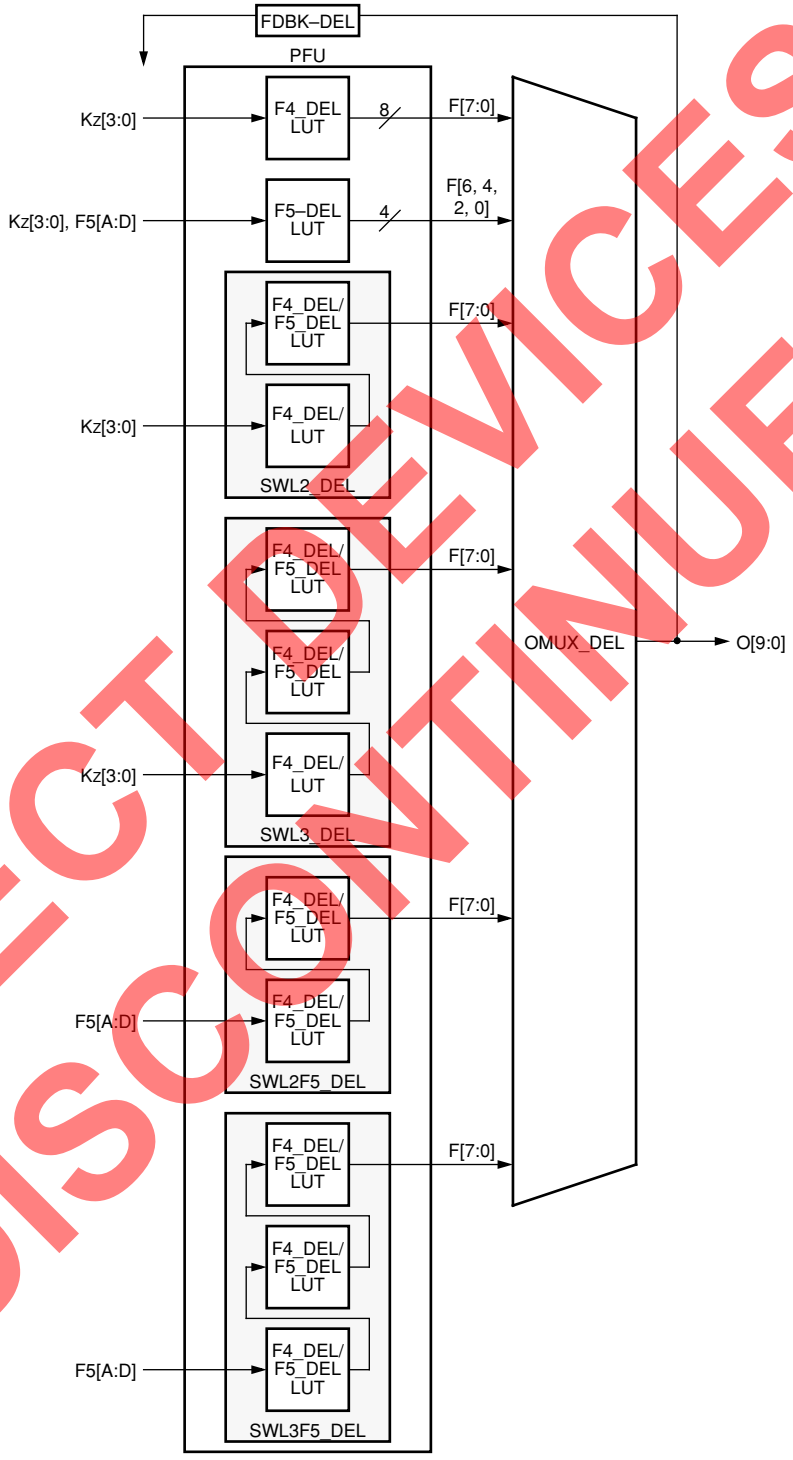


Figure 54. Master Parallel Configuration Schematic

In master parallel mode, the starting memory address is 00000 Hex, and the FPGA increments the address for each byte loaded.

One master mode FPGA can interface to the memory and provide configuration data on DOUT to additional FPGAs in a daisy-chain. The configuration data on DOUT is provided synchronously with the falling edge of CCLK. The frequency of the CCLK output is eight times that of RCLK.

Timing Characteristics (continued)



Note: See Table 46 for an explanation of FDBK_DEL and OMUX_DEL.

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Figure 64. Combinatorial PFU Timing

Timing Characteristics (continued)

Table 50. Programmable Clock Manager (PCM) Timing Characteristics

OR3Cxx Commercial: VDD = 5.0 V ± 5%, 0 °C ≤TA < 70 °C; Industrial: VDD = 5.0 V ± 10%, –40 °C < TA < +85 °C.
OR3Txxx Commercial: VDD = 3.0 V to 3.6 V, 0 °C < TA < 70 °C; Industrial: VDD = 3.0 V to 3.6 V, –40 °C < TA < +85 °C.

Parameter	Symbol	Speed								Unit
		-4		-5		-6		-7		
		Min	Max	Min	Max	Min	Max	Min	Max	
Input Clock Frequency:	FPCMI									
OR3Cxx		5	133	5	133	—	—	—	—	MHz
OR3Txxx		—	—	5	133	5	133	5	133	MHz
Output Clock Frequency:	FPCMO									
OR3Cxx		5	135	5	135	—	—	—	—	MHz
OR3Txxx		—	—	5	100	5	100	5	100	MHz
Input Clock Duty Cycle	PCMI_DUTY	30.00	70.00	30.00	70.00	30.00	70.00	30.00	70.00	%
Output Clock Duty Cycle	PCMO_DUTY	3.13	96.90	3.13	96.90	3.13	96.90	3.13	96.90	%
Input Frequency Tolerance*	FTOL	—	26400	—	26400	—	26400	—	26400	ppm
PCM Acquisition Time (CLK In to LOCK)	PCM_ACQ†	36	100	36	100	36	100	36	100	µs
PCM Off Delay (config. Done-L, WE to PCM power off)	PCMOFF_DEL	—	100.0	—	100.0	—	100.0	—	100.0	ns
PCM Delay in DLL Mode (propagation delay)	PCMDLL-DEL	—	1.95	—	1.82	—	1.63	—	1.50	ns
PCM Delay in PLL Mode (propagation delay)	PCMPLL_DEL	—	0.00	—	0.00	—	0.00	—	0.00	ns
PCM Clock In to PCM Clock Out (CLK In to ECLK)‡	PCMBYE_DEL	—	0.47	—	0.36	—	0.26	—	0.24	ns
PCM Clock In to PCM Clock Out (CLK In to SCLK)‡	PCMBYS_DEL	—	0.47	—	0.36	—	0.26	—	0.24	ns
Routed Clock-in Delay (routing to PCM phase detect, using DIV0)	RTCKD_DEL	—	1.30	—	1.10	—	0.90	—	TBD	ns
System Clock-out Delay (PCM oscillator to SCLK output at PCM)	PCMSCK_DEL	—	2.70	—	2.20	—	1.90	—	TBD	ns

Parameter	Symbol	fOUT (MHz)	PLL Mode	DLL Mode	Unit
Output Jitter	OUTJIT	5—20	250	200	ps
		21—30	210	170	ps
		31—40	180	145	ps
		41—50	155	123	ps
		51—60	130	105	ps
		61—70	110	90	ps
		71—80	95	75	ps
		81—90	80	65	ps
		91—100	70	55	ps

* Input frequency tolerance is the allowed input clock frequency change in parts per million.
† See Table 29 and Table 30 for acquisition times for individual frequencies.
‡ PLL mode, divider reg = 1111111 (input freq. = output freq.).

Timing Characteristics (continued)

Clock Timing

Table 52. ExpressCLK (ECLK) and Fast Clock (FCLK) Timing Characteristics

OR3Cxx Commercial: V_{DD} = 5.0 V ± 5%, 0 °C < T_A < 70 °C; Industrial: V_{DD} = 5.0 V ± 10%, –40 °C < T_A < +85 °C.
OR3Txxx Commercial: V_{DD} = 3.0 V to 3.6 V, 0 °C < T_A < 70 °C; Industrial: V_{DD} = 3.0 V to 3.6 V, –40 °C < T_A < +85 °C.

Device (T_J = 85 °C, V_{DD} = min)	Symbol	Speed								Unit
		-4		-5		-6		-7		
		Min	Max	Min	Max	Min	Max	Min	Max	
Clock Control Timing Delay Through CLKCNTRL (input from corner)	ECLKC_DEL	0.31	—	0.31	—	0.31	—	0.31	—	ns
Delay Through CLKCNTRL (input from internal clock controller PAD)	ECLKM_DEL	1.54	—	1.17	—	1.00	—	0.92	—	ns
Clock Shutoff Timing:										
Setup from Middle ECLK (shut off to CLK)	OFFM_SET	0.77	—	0.51	—	0.44	—	0.41	—	ns
Hold from Middle ECLK (shut off from CLK)	OFFM_HLD	0.00	—	0.00	—	0.00	—	0.00	—	ns
Setup from Corner ECLK (shut off to CLK)	OFFC_SET	0.77	—	0.51	—	0.44	—	0.41	—	ns
Hold from Corner ECLK (shut off from CLK)	OFFC_HLD	0.00	—	0.00	—	0.00	—	0.00	—	ns
ECLK Delay (middle pad):	ECLKM_DEL									
OR3T20		—	—	—	2.56	—	2.05	—	1.78	ns
OR3T30		—	—	—	2.62	—	2.08	—	1.80	ns
OR3T55		—	3.50	—	2.74	—	2.13	—	1.85	ns
OR3C/T80		—	3.67	—	2.86	—	2.19	—	1.90	ns
OR3T125		—	—	—	3.06	—	2.29	—	1.98	ns
ECLK Delay (corner pad):	ECLKC_DEL									
OR3T20		—	—	—	4.48	—	3.85	—	3.36	ns
OR3T30		—	—	—	4.53	—	3.97	—	3.47	ns
OR3T55		—	5.47	—	4.64	—	4.22	—	3.69	ns
OR3C/T80		—	5.64	—	4.77	—	4.47	—	3.92	ns
OR3T125		—	—	—	4.96	—	4.85	—	4.27	ns
FCLK Delay (middle pad):	FCLKM_DEL									
OR3T20		—	—	—	5.91	—	4.59	—	3.81	ns
OR3T30		—	—	—	6.12	—	4.66	—	3.89	ns
OR3T55		—	8.24	—	6.59	—	4.83	—	4.06	ns
OR3C/T80		—	8.87	—	7.11	—	5.01	—	4.26	ns
OR3T125		—	—	—	7.98	—	5.33	—	4.59	ns
FCLK Delay (corner pad):	FCLKC_DEL									
OR3T20		—	—	—	7.88	—	6.41	—	5.40	ns
OR3T30		—	—	—	8.11	—	6.58	—	5.58	ns
OR3T55		—	10.34	—	8.60	—	6.95	—	5.94	ns
OR3C/T80		—	11.01	—	9.15	—	7.34	—	6.33	ns
OR3T125		—	—	—	10.07	—	7.96	—	6.94	ns

Notes:
The ECLK delays are to all of the PICs on one side of the device for middle pin input, or two sides of the device for corner pin input. The delay includes both the input buffer delay and the clock routing to the PIC clock input.

The FCLK delays are for a fully routed clock tree that uses the ExpressCLK input into the fast clock network. It includes both the input buffer delay and the clock routing to the PFU CLK input. The delay will be reduced if any of the clock branches are not used.

Timing Characteristics (continued)

Table 54. OR3Cxx ExpressCLK to Output Delay (Pin-to-Pin)

OR3Cxx Commercial: V_{DD} = 5.0 V ± 5%, 0 °C < T_A < 70 °C; Industrial: V_{DD} = 5.0 V ± 10%, –40 °C < T_A < +85 °C; C_L = 50 pF.
OR3Txxx Commercial: V_{DD} = 3.0 V to 3.6 V, 0 °C < T_A < 70 °C; Industrial: V_{DD} = 3.0 V to 3.6 V, –40 °C < T_A < +85 °C; C_L = 50 pF.

Description (T_J = 85 °C, V_{DD} = min)	Device	Speed								Unit
		-4		-5		-6		-7		
		Min	Max	Min	Max	Min	Max	Min	Max	
ECLK Middle Input Pin→OUTPUT Pin (Fast)	OR3T20	—	—	—	7.78	—	5.40	—	4.38	ns
	OR3T30	—	—	—	7.84	—	5.43	—	4.40	ns
	OR3T55	—	9.93	—	7.96	—	5.48	—	4.44	ns
	OR3C/T80	—	10.10	—	8.08	—	5.54	—	4.49	ns
	OR3T125	—	—	—	8.28	—	5.64	—	4.58	ns
ECLK Middle Input Pin→OUTPUT Pin (Slewlim)	OR3T20	—	—	—	9.77	—	6.07	—	4.91	ns
	OR3T30	—	—	—	9.83	—	6.10	—	4.93	ns
	OR3T55	—	12.37	—	9.95	—	6.15	—	4.97	ns
	OR3C/T80	—	12.54	—	10.07	—	6.21	—	5.02	ns
	OR3T125	—	—	—	10.27	—	6.31	—	5.11	ns
ECLK Middle Input Pin→OUTPUT Pin (Sinklim)	OR3T20	—	—	—	11.12	—	10.92	—	9.65	ns
	OR3T30	—	—	—	11.18	—	10.95	—	9.67	ns
	OR3T55	—	13.73	—	11.30	—	11.00	—	9.71	ns
	OR3C/T80	—	13.90	—	11.42	—	11.06	—	9.76	ns
	OR3T125	—	—	—	11.62	—	11.16	—	9.85	ns
Additional Delay if ECLK Corner Pin Used	OR3T20	—	—	—	1.91	—	1.80	—	1.58	ns
	OR3T30	—	—	—	1.91	—	1.90	—	1.67	ns
	OR3T55	—	1.97	—	1.91	—	2.09	—	1.84	ns
	OR3C/T80	—	1.97	—	1.91	—	2.28	—	2.02	ns
	OR3T125	—	—	—	1.90	—	2.57	—	2.29	ns

Notes:
Timing is without the use of the programmable clock manager (PCM).

This clock delay is for a fully routed clock tree that uses the ExpressCLK network. It includes both the input buffer delay, the clock routing to the PIO CLK input, the clock→Q of the FF, and the delay through the output buffer. The given timing requires that the input clock pin be located at one of the six ExpressCLK inputs of the device, and that a PIO FF be used.

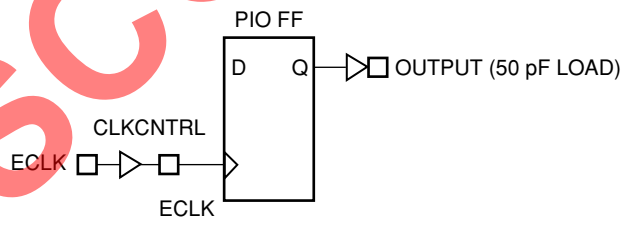

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Figure 76. ExpressCLK to Output Delay

Timing Characteristics (continued)

Table 58. OR3C/Txxx Input to Fast Clock Setup/Hold Time (Pin-to-Pin)

OR3Cxx Commercial: V_{DD} = 5.0 V ± 5%, 0 °C < T_A < 70 °C; Industrial: V_{DD} = 5.0 V ± 10%, –40 °C < T_A < +85 °C.
OR3Txxx Commercial: V_{DD} = 3.0 V to 3.6 V, 0 °C < T_A < 70 °C; Industrial: V_{DD} = 3.0 V to 3.6 V, –40 °C < T_A < +85 °C.

Description (T_J = 85 °C, V_{DD} = min)	Device	Speed								Unit
		-4		-5		-6		-7		
		Min	Max	Min	Max	Min	Max	Min	Max	
Output Not on Same Side of Device As Input Clock (Fast Clock Delays Using ExpressCLK Inputs)										
Input to FCLK Setup Time (middle ECLK pin)	OR3T20	—	—	0.00	—	0.00	—	0.00	—	ns
	OR3T30	—	—	0.00	—	0.00	—	0.00	—	ns
	OR3T55	0.00	—	0.00	—	0.00	—	0.00	—	ns
	OR3C/T80	0.00	—	0.00	—	0.00	—	0.00	—	ns
	OR3T125	—	—	0.00	—	0.00	—	0.00	—	ns
Input to FCLK Setup Time (middle ECLK pin, delayed data input)	OR3T20	—	—	0.80	—	0.58	—	2.20	—	ns
	OR3T30	—	—	0.74	—	0.55	—	2.17	—	ns
	OR3T55	0.29	—	0.62	—	0.51	—	2.11	—	ns
	OR3C/T80	0.14	—	0.50	—	0.46	—	2.06	—	ns
	OR3T125	—	—	0.22	—	0.33	—	1.90	—	ns
Input to FCLK Setup Time (corner ECLK pin)	OR3T20	—	—	0.00	—	0.00	—	0.00	—	ns
	OR3T30	—	—	0.00	—	0.00	—	0.00	—	ns
	OR3T55	0.00	—	0.00	—	0.00	—	0.00	—	ns
	OR3C/T80	0.00	—	0.00	—	0.00	—	0.00	—	ns
	OR3T125	—	—	0.00	—	0.00	—	0.00	—	ns
Input to FCLK Setup Time (corner ECLK pin, delayed data input)	OR3T20	—	—	0.00	—	0.00	—	0.00	—	ns
	OR3T30	—	—	0.00	—	0.00	—	0.00	—	ns
	OR3T55	0.00	—	0.00	—	0.00	—	0.00	—	ns
	OR3C/T80	0.00	—	0.00	—	0.00	—	0.00	—	ns
	OR3T125	—	—	0.00	—	0.00	—	0.00	—	ns
Input to FCLK Hold Time (middle ECLK pin)	OR3T20	—	—	4.29	—	3.72	—	3.27	—	ns
	OR3T30	—	—	4.50	—	3.80	—	3.35	—	ns
	OR3T55	6.33	—	4.97	—	3.96	—	3.52	—	ns
	OR3C/T80	6.95	—	5.49	—	4.15	—	3.72	—	ns
	OR3T125	—	—	6.36	—	4.47	—	4.05	—	ns

Notes:
The pin-to-pin timing parameters in this table should be used instead of results reported by ispLEVER.

The FCLK delays are for a fully routed clock tree that uses the ExpressCLK input into the fast clock network. It includes both the input buffer delay and the clock routing to the PFU CLK input. The delay will be reduced if any of the clock branches are not used.

Timing Characteristics (continued)

Table 65. Slave Parallel Configuration Mode Timing Characteristics

OR3Cxx Commercial: V_{DD} = 5.0 V ± 5%, 0 °C < T_A < 70 °C; Industrial: V_{DD} = 5.0 V ± 10%, –40 °C < T_A < +85 °C.
OR3Txxx Commercial: V_{DD} = 3.0 V to 3.6 V, 0 °C < T_A < 70 °C; Industrial: V_{DD} = 3.0 V to 3.6 V, –40 °C < T_A < +85 °C.

Parameter	Symbol	Min	Max	Unit
$\overline{CS0}$, CS1, $\overline{WR}$ Setup Time	T_{S1}	40.00	—	ns
$\overline{CS0}$, CS1, $\overline{WR}$ Hold Time	T_{H1}	20.00	—	ns
D[7:0] Setup Time: 3Cxx 3Txxx	T_{S2}	 20.00 7.00	 — —	 ns ns
D[7:0] Hold Time	T_{H2}	0.00	—	ns
CCLK High Time: 3Cxx 3Txxx	T_{CH}	 20.00 7.00	 — —	 ns ns
CCLK Low Time: 3Cxx 3Txxx	T_{CL}	 20.00 7.00	 — —	 ns ns
CCLK Frequency: 3Cxx 3Txxx	F_C	 — —	 25.00 66.00	 MHz MHz

Note: Daisy-chaining of FPGAs is not supported in this mode.

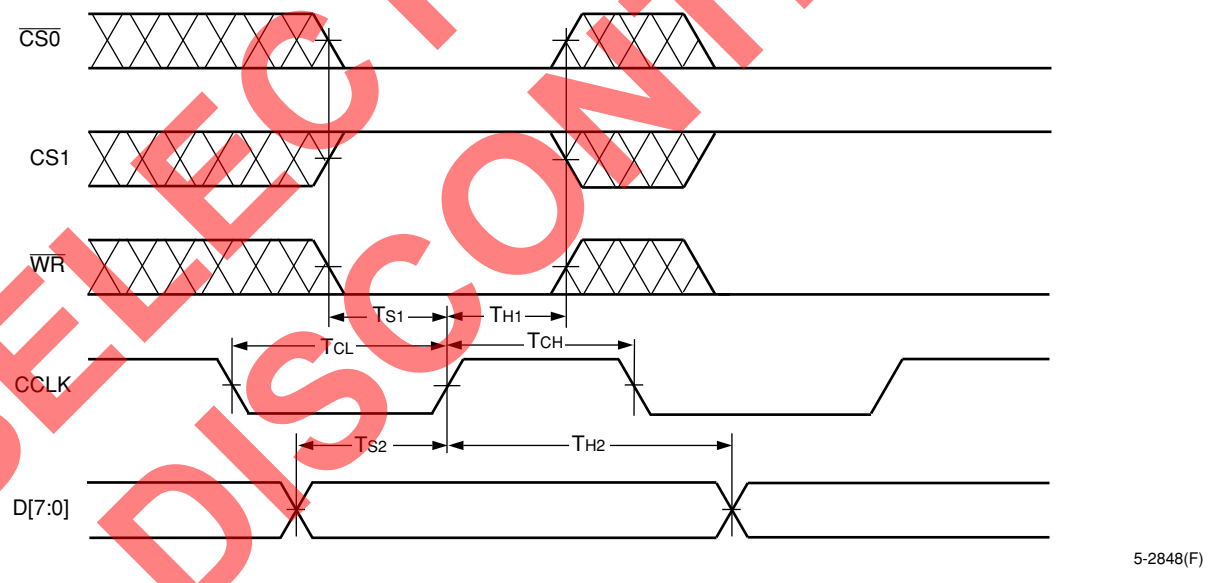

Figure 87. Slave Parallel Configuration Mode Timing Diagram

Pin Information

Pin Descriptions

This section describes the pins found on the Series 3 FPGAs. Any pin not described in this table is a user-programmable I/O. During configuration, the user-programmable I/Os are 3-stated with an internal pull-up resistor enabled. If any pin is not used (or not bonded to a package pin), it is also 3-stated with an internal pull-up resistor enabled after configuration.

Table 67. Pin Descriptions

Symbol	I/O	Description
Dedicated Pins		
VDD	—	Positive power supply.
GND	—	Ground supply.
VDD5	—	5 V tolerant select. VDD5 pin locations are shown for package compatibility with OR2TxxA devices. Connections to 5 V power sources are not used for 5 V tolerant I/Os in the OR3Txxx devices.
$\overline{\text{RESET}}$	I	During configuration, $\overline{\text{RESET}}$ forces the restart of configuration and a pull-up is enabled. After configuration, $\overline{\text{RESET}}$ can be used as a general FPGA input or as a direct input, which causes all PLC latches/FFs to be asynchronously set/reset.
CCLK	I	In the master and asynchronous peripheral modes, CCLK is an output which strobes configuration data in. In the slave or synchronous peripheral mode, CCLK is input synchronous with the data on DIN or D[7:0]. In microprocessor mode, CCLK is used internally and output for daisy-chain operation.
DONE	I	As an input, a low level on DONE delays FPGA start-up after configuration (see Note).
	O	As an active-high, open-drain output, a high level on this signal indicates that configuration is complete. DONE has an optional pull-up resistor.
$\overline{\text{PRGM}}$	I	$\overline{\text{PRGM}}$ is an active-low input that forces the restart of configuration and resets the boundary-scan circuitry. This pin always has an active pull-up.
$\overline{\text{RD\_CFG}}$	I	This pin must be held high during device initialization until the $\overline{\text{INIT}}$ pin goes high. This pin always has an active pull-up. During configuration, $\overline{\text{RD\_CFG}}$ is an active-low input that activates the TS_ALL function and 3-states all of the I/O. After configuration, $\overline{\text{RD\_CFG}}$ can be selected (via a bit stream option) to activate the TS_ALL function as described above, or, if readback is enabled via a bit stream option, a high-to-low transition on $\overline{\text{RD\_CFG}}$ will initiate readback of the configuration data, including PFU output states, starting with frame address 0.
RD_DATA/TDO	O	RD_DATA/TDO is a dual-function pin. If used for readback, RD_DATA provides configuration data out. If used in boundary scan, TDO is test data out.
Special-Purpose Pins		
M0, M1, M2	I	During powerup and initialization, M0—M2 are used to select the configuration mode with their values latched on the rising edge of $\overline{\text{INIT}}$; see Table 34 for the configuration modes. During configuration, a pull-up is enabled.
	I/O	After configuration, these pins are user-programmable I/O (see Note).

Note: The FPGA States of Operation section contains more information on how to control these signals during start-up. The timing of DONE release is controlled by one set of bit stream options, and the timing of the simultaneous release of all other configuration pins (and the activation of all user I/Os) is controlled by a second set of options.

Pin	OR3T55 Pad	OR3C/T80 Pad	OR3T125 Pad	Function
AD19	PB16A	PB19A	PB25A	I/O
AE21	PB16B	PB19B	PB25B	I/O
AC20	PB16C	PB19C	PB25C	I/O
AF21	PB16D	PB19D	PB25D	I/O
AD20	PB17A	PB20A	PB26A	I/O
AE22	PB17B	PB20B	PB26B	I/O
AF22	PB17C	PB20D	PB26D	I/O
AD21	PB17D	PB21A	PB27A	I/O
AE23	—	PB21B	PB27B	I/O
AC22	PB18A	PB21D	PB27D	I/O
AF23	PB18B	PB22A	PB28A	I/O
AD22	PB18C	PB22B	PB28B	I/O
AE24	—	PB22C	PB28C	I/O
AD23	PB18D	PB22D	PB28D	I/O
AF24	PDONE	PDONE	PDONE	DONE
AE26	$\overline{\text{PRESETN}}$	$\overline{\text{PRESETN}}$	$\overline{\text{PRESETN}}$	$\overline{\text{RESET}}$
AD25	$\overline{\text{PPRGMN}}$	$\overline{\text{PPRGMN}}$	$\overline{\text{PPRGMN}}$	$\overline{\text{PRGM}}$
AD26	PR18A	PR22A	PR28A	I/O-M0
AC25	PR18B	PR22C	PR28C	I/O
AC24	PR18C	PR22D	PR28D	I/O
AC26	PR18D	PR21A	PR27A	I/O
AB25	PR17A	PR21D	PR27D	I/O
AB23	PR17B	PR20A	PR26A	I/O
AB24	PR17C	PR20B	PR26B	I/O
AB26	PR17D	PR20D	PR26D	I/O
AA25	PR16A	PR19A	PR25A	I/O
Y23	PR16B	PR19B	PR25B	I/O
AA24	PR16C	PR19C	PR25C	I/O
AA26	PR16D	PR19D	PR24A	I/O
Y25	PR15A	PR18A	PR23A	I/O
Y26	PR15B	PR18B	PR23B	I/O
Y24	PR15C	PR18C	PR23D	I/O
W25	PR15D	PR18D	PR22D	I/O-M1
V23	PR14A	PR17A	PR21A	I/O
W26	PR14B	PR17B	PR21B	I/O
W24	PR14C	PR17C	PR21C	I/O
V25	PR14D	PR17D	PR21D	I/O
V26	PR13A	PR16A	PR20A	I/O
U25	PR13B	PR16B	PR20B	I/O
V24	PR13C	PR16C	PR20C	I/O
U26	PR13D	PR16D	PR20D	I/O
U23	PR12A	PR15A	PR19A	I/O-M2
T25	PR12B	PR15D	PR19D	I/O
U24	PR12C	PR14A	PR18A	I/O
T26	PR12D	PR14C	PR18D	I/O
R25	PR11A	PR14D	PR17A	I/O-M3