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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	-
Number of Logic Elements/Cells	2592
Total RAM Bits	43008
Number of I/O	171
Number of Gates	80000
Voltage - Supply	3V ~ 3.6V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 70°C (TA)
Package / Case	208-BFQFP
Supplier Device Package	208-PQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/or3t556s208-db

System-Level Features

System-level features reduce glue logic requirements and make a system on a chip possible. These features in the *ORCA* Series 3 include:

- Full PCI local bus compliance.
- Dual-use microprocessor interface (MPI) can be used for configuration, readback, device control, and device status, as well as for a general-purpose interface to the FPGA. Glueless interface to *i960** and *PowerPC*† processors with user-configurable address space provided.
- Parallel readback of configuration data capability with the built-in microprocessor interface.
- Programmable clock manager (PCM) adjusts clock phase and duty cycle for input clock rates from 5 MHz to 120 MHz. The PCM may be combined with FPGA logic to create complex functions, such as digital phase-locked loops (DPLL), frequency counters, and frequency synthesizers or clock doublers. Two PCMs are provided per device.
- True, internal, 3-state, bidirectional buses with simple control provided by the SLIC.
- 32 x 4 RAM per PFU, configurable as single- or dual-port at >176 MHz. Create large, fast RAM/ROM blocks (128 x 8 in only eight PFUs) using the SLIC decoders as bank drivers.

* *i960* is a registered trademark of Intel Corporation.
† *PowerPC* is a registered trademark of International Business Machines Corporation.

Table 2. *ORCA* Series 3 System Performance

Parameter	# PFUs	Speed				Unit
		-4	-5	-6	-7	
16-bit Loadable Up/Down Counter	2	78	102	131	168	MHz
16-bit Accumulator	2	78	102	131	168	MHz
8 x 8 Parallel Multiplier:						
Multiplier Mode, Unpipelined[1]	11.5	19	25	30	38	MHz
ROM Mode, Unpipelined[2]	8	51	66	80	102	MHz
Multiplier Mode, Pipelined[3]	15	76	104	127	166	MHz
32 x 16 RAM (synchronous):						
Single-port, 3-state Bus[4]	4	97	127	151	192	MHz
Dual-port[5]	4	127	166	203	253	MHz
128 x 8 RAM (synchronous):						
Single-port, 3-state Bus[4]	8	88	116	139	176	MHz
Dual-port[5]	8	88	116	139	176	MHz
8-bit Address Decode (internal):						
Using Softwired LUTs	0.25	4.87	3.66	2.58	2.03	ns
Using SLICs[6]	0	2.35	1.82	1.23	0.99	ns
32-bit Address Decode (internal):						
Using Softwired LUTs	2	16.06	12.07	9.01	7.03	ns
Using SLICs[7]	0	6.91	5.41	4.21	3.37	ns
36-bit Parity Check (internal)	2	16.06	12.07	9.01	7.03	ns

1. Implemented using 8 x 1 multiplier mode (unpipelined), register-to-register, two 8-bit inputs, one 16-bit output.
2. Implemented using two 32 x 12 ROMs and one 12-bit adder, one 8-bit input, one fixed operand, one 16-bit output.
3. Implemented using 8 x 1 multiplier mode (fully pipelined), two 8-bit inputs, one 16-bit output (7 of 15 PFUs contain only pipelining registers).
4. Implemented using 32 x 4 RAM mode with read data on 3-state buffer to bidirectional read/write bus.
5. Implemented using 32 x 4 dual-port RAM mode.
6. Implemented in one partially occupied SLIC with decoded output set up to CE in same PLC.
7. Implemented in five partially occupied SLICs.

Programmable Input/Output Cells

(continued)

Outputs

The PIC's output drivers have programmable drive capability and slew rates. Three propagation delays (fast, slewlim, sinklim) are available on output drivers. The sinklim mode has the longest propagation delay and is used to minimize system noise and minimize power consumption. The fast and slewlim modes allow critical timing to be met.

The drive current is 12 mA sink/6 mA source for the slewlim and fast output speed selections and 6 mA sink/3 mA source for the sinklim output. Two adjacent outputs can be interconnected to increase the output sink/source current to 24 mA/12 mA.

All outputs that are not speed critical should be configured as sinklim to minimize power and noise. The number of outputs that switch simultaneously in the same direction should be limited to minimize ground bounce. To minimize ground bounce problems, locate heavily loaded output buffers near the ground pads. Ground bounce is generally a function of the driving circuits, traces on the printed-circuit board, and loads and is best determined with a circuit simulation.

At powerup, the output drivers are in slewlim mode, and the input buffers are configured as TTL-level compatible (CMOS for OR3Txxx) with a pull-up. If an output is not to be driven in the selected configuration mode, it is 3-stated.

The output buffer signal can be inverted, and the 3-state control signal can be made active-high, active-low, or always enabled. In addition, this 3-state signal can be registered or nonregistered. Additionally, there is a fast, open-drain output option that directly connects the output signal to the 3-state control, allowing the output buffer to either drive to a logic 0 or 3-state, but never to drive to a logic 1. Because there is no explicit route required to create the open-drain output, its response is very fast. Like the input side of the PIO, there are two output connections from PIC routing to the output side of the PIO, OUT1, and OUT2. These connections provide for flexible routing and can be used in data manipulation in the PIO as described in subsequent paragraphs.

An FF has been added to the output path of the PIO. The register has a local set/reset and clock enable. The LSR has the option to be synchronous or asynchronous and have priority set as clock enable over LSR or LSR over clock enable. Clocking to the output FF can come from either the system clock or the ExpressCLK associated with the PIC. The input to the FF can come from either OUT1 or OUT2, or it can be tied to VDD or GND. Additionally, the input to the FF can be inverted.

Output Multiplexing

The Series 3 PIO output FF can be combined with the new PIO logic block to perform output data multiplexing with no PLC resources required. The PIO logic block has three multiplexing modes: OUT1OUTREG, OUT2OUTREG, and OUT1OUT2. OUT1OUTREG and OUT2OUTREG are equivalent except that either OUT1 or OUT2 is MUXed with the FF, where the FF data is output on the clock phase after the active edge. The simplest multiplexing mode is OUT1OUT2. In this mode, the signal at OUT1 is output to the pad while the clock is low, and the signal on OUT2 is output to the pad when the clock is high. Figure 25 shows a simple schematic of a PIO in OUT1OUT2 mode and a general timing diagram for multiplexing an address and data signal.

Often an address will be used to generate or read a data sample from memory with the goal of multiplexing the data onto a single line. In this case, the address often precedes the data by one clock cycle. OUT1OUTREG and OUT2OUTREG modes of the PIO logic can be used to address this situation.

Because OUT1OUTREG mode is equivalent to OUT2OUTREG, only OUT2OUTREG mode is described here. Figure 26 shows a simple PIO schematic in OUT2OUTREG mode and general timing for multiplexing data with a leading address. The address signal on OUT1 is registered in the PIO FF. This delays the address so that it aligns with the data signal. The PIO logic block then sends the OUTREG signal (address) to the pad when the clock is high and the OUT2 signal (data) to the pad when the clock is low, resulting in an aligned, multiplexed signal.

Clock Distribution Network

The Series 3 FPGAs provide three types of high-speed, low-skew clock distributions: system clock, fast middle clock (fast clock), and ExpressCLK. Because of the great variety of sources and distribution for clock signals in the *ORCA* Series 3, the clock mechanisms will be described here from the inside out. The clock connections to the PFU will be described, followed by clock distribution to the PLC array, clock sources to the PLC array, and finally ending with clock sources and distribution in the PICs. The ExpressCLK inputs are new, dedicated clock inputs in Series 3 FPGAs. They are mentioned in several of the clock network descriptions and are described fully later in this section.

PFU Clock Sources

Within a PLC there are five sources for the clock signal of the latches/FFs in the PFU. Two of the signals are generated off of the long lines (xL) within the PLC: one from the set of vertical long lines and one from the set of horizontal long lines. For each of these signals, any one of the ten long lines of each set, vertical or horizontal, can generate the clock signal. Two of the five PFU clock sources come from neighboring PLCs. One clock is generated from the PLC to the left or right of the current PLC, and one is generated from the PLC above or below the current PLC. The selection decision as to where these signals come from, above/below and left/right, is based on the position of the PLC in the array and has to do with the alternating nature of the source of the system clock spines (discussed later). The last of the five clock sources is also generated within the PLC. The E1 control signal, described in the PLC Routing Resources section, can drive the PFU clock. The E1 signal can come from any xBID routing resource in the PLC. The selection and switching of clock signals in a PLC is performed in the FINS. Figure 31 shows the PFU clock sources for a set of four adjacent PLCs.

Global Control Signals

The four clock signals in each PLC that are generated from the long lines (xL) in the current PLC or an adjacent PLC can also be used to drive the PFU clock enable (CE), local set/reset (LSR) and add/subtract/write enable (ASWE) signals. The clock signals generated from vertical long lines can drive CE and ASWE, and the clocks generated from horizontal long lines can drive LSR. This allows for low-skew global distribution of two of these three control signals with the clock routing while still allowing a global clock route to occur.

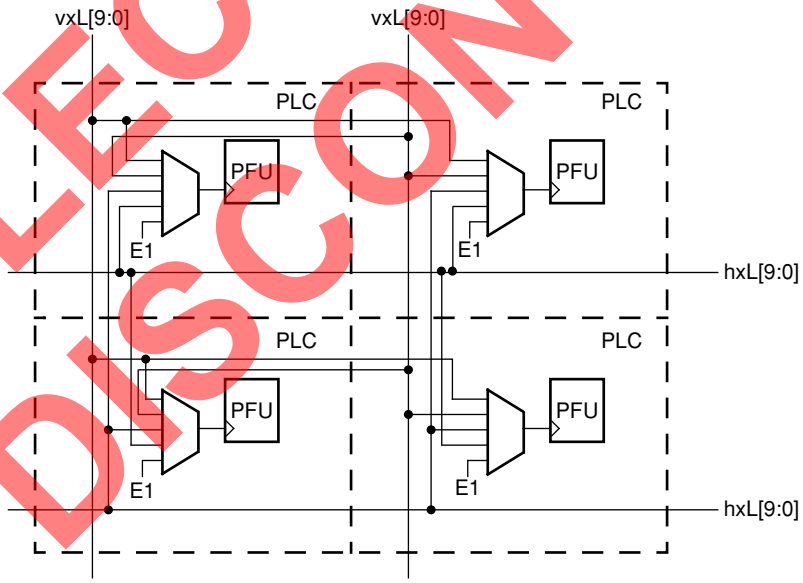

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Figure 31. PFU Clock Sources

Programmable Clock Manager (PCM)

(continued)

Delay-Locked Loop (DLL) Mode

DLL mode is used for implementing a delayed clock (phase adjustment), clock doubling, and duty cycle adjustment. All DLL functions stem from a delay line with 32 taps. The delayed input clock is pulled from various taps and processed to implement the desired result. There is no feedback clock in DLL mode, providing a very stable output and a fast lock time for the output clock.

DLL mode is selected by setting bit 0 in PCM register five to a 0. The settings for the various submodes of DLL mode are described in the following paragraphs. Divider DIV0 may be used with any of the DLL modes to divide the input clock by an integer factor of 1 to 8 prior to implementation of the DLL process.

Delayed Clock

A delayed version of the input clock can be constructed in DLL mode. The output clock can be delayed by increments of 1/32 of the input clock period. Express CLK and system CLK outputs in delay modes are selected by setting register six, bits [5:4] to 10 or 11 for ExpressCLK output, and/or bits [7:6] to 10 for system clock output. The delay value is entered in register four. See register four programming details for more information. Delay values are also shown in the second column of Table 27.

Note that when register six, bits [5:4] are set to 11, the ExpressCLK output is divided by an integer factor from 1 to 8 while the system clock cannot be divided. The ExpressCLK divider is provided so that the I/O clocking provided by the ExpressCLK can operate slower than the internal system clock. This allows for very fast internal processing while maintaining slower interface speeds off-chip for improved noise and power performance or to interoperate with slower devices in the system. The divisor of the ExpressCLK frequency is selected in register two. See the register two programming details for more information.

1x Clock Duty-Cycle Adjustment

A duty-cycle adjusted replica of the input clock can be constructed in DLL mode. The duty cycle can be adjusted in 1/32 (3.125%) increments of the input clock period. DLL 1x clock mode is selected by setting bit 4 of register five to a 1, and output clock source selection is selected by setting register six, bits [5:4] to 01 for ExpressCLK output, and/or bits [7:6] to 01 for system clock output. The duty-cycle percentage value is entered in register four. See register four programming details for more information. Duty cycle values are also shown in the third column of Table 27.

Table 27. DLL Mode Delay/1x Duty Cycle Programming Values

Register 4 [7:0] 7 6 5 4 3 2 1 0	Delay (CLK_IN/32)	Duty Cycle (% of CLK_IN)
0 0 X X X 0 0 0	1	3.125
0 0 X X X 0 0 1	2	6.250
0 0 X X X 0 1 0	3	9.375
0 0 X X X 0 1 1	4	12.500
0 0 X X X 1 0 0	5	15.625
0 0 X X X 1 0 1	6	18.750
0 0 X X X 1 1 0	7	21.875
0 0 X X X 1 1 1	8	25.000
0 1 X X X 0 0 0	9	28.125
0 1 X X X 0 0 1	10	31.250
0 1 X X X 0 1 0	11	34.375
0 1 X X X 0 1 1	12	37.500
0 1 X X X 1 0 0	13	40.625
0 1 X X X 1 0 1	14	43.750
0 1 X X X 1 1 0	15	46.875
0 1 1 1 1 X X X	16	50.000
1 0 0 0 0 X X X	17	53.125
1 0 0 0 1 X X X	18	56.250
1 0 0 1 0 X X X	19	59.375
1 0 0 1 1 X X X	20	62.500
1 0 1 0 0 X X X	21	65.625
1 0 1 0 1 X X X	22	68.750
1 0 1 1 0 X X X	23	71.875
1 0 1 1 1 X X X	24	75.000
1 1 0 0 0 X X X	25	78.125
1 1 0 0 1 X X X	26	81.250
1 1 0 1 0 X X X	27	84.375
1 1 0 1 1 X X X	28	87.500
1 1 1 0 0 X X X	29	90.625
1 1 1 0 1 X X X	30	93.750
1 1 1 1 0 X X X	31	96.875

Programmable Clock Manager (PCM)

(continued)

Table 29. PCM Oscillator Frequency Range 3Txxx

Register 4 76543210	Min (MHz)	System Clock Output Frequency (MHz) NOM	Max (MHz)	T Acquisition (µs)
00XXX010	17.00	58.50	100.00	36.00
00XXX011	16.10	52.50	89.00	37.00
00XXX100	15.17	49.00	82.80	38.00
00XXX101	14.25	45.00	76.50	39.00
00XXX110	13.33	41.50	70.30	40.00
00XXX111	12.40	38.00	64.00	41.00
01XXX000	12.20	36.75	61.30	43.75
01XXX001	12.10	35.00	58.00	46.50
01XXX010	11.90	33.00	54.30	49.25
01XXX011	11.70	31.30	51.00	52.00
01XXX100	11.10	30.00	49.40	54.75
01XXX101	10.50	29.15	47.80	57.50
01XXX110	10.00	28.10	46.20	60.25
01XXX111	9.40	27.00	44.60	63.00
10000XXX	9.20	26.25	43.30	65.40
10001XXX	9.00	25.65	42.30	67.80
10010XXX	8.80	25.00	41.30	70.10
10011XXX	8.60	24.45	40.30	72.50
10100XXX	8.40	23.70	39.00	74.90
10101XXX	8.10	22.90	37.70	77.30
10110XXX	7.90	22.20	36.50	79.60
10111XXX	7.70	21.50	35.20	82.00
11000XXX	7.60	20.80	34.00	84.30
11001XXX	7.45	20.10	32.80	86.50
11010XXX	7.30	19.45	31.60	88.80
11011XXX	7.20	18.85	30.50	91.00
11100XXX	6.60	18.30	30.00	93.30
11101XXX	6.00	17.70	29.40	95.50
11110XXX	5.50	17.10	28.60	97.80
11111XXX	5.00	16.50	28.00	100.00

Note: Use of settings in the first three rows is not recommended. X means don't care.

Table 30. PCM Oscillator Frequency Range 3Cxx

Register 4 76543210	Min (MHz)	System Clock Output Frequency (MHz) NOM	Max (MHz)	T Acquisition (µs)
00XXX010	10.50	73.00	135.00	36.00
00XXX011	10.00	68.00	126.00	37.00
00XXX100	9.50	63.00	117.00	38.00
00XXX101	9.10	58.50	108.00	39.00
00XXX110	8.60	53.80	99.00	40.00
00XXX111	8.10	49.00	90.00	41.00
01XXX000	7.80	47.70	87.50	43.80
01XXX001	7.60	46.30	85.00	46.50
01XXX010	7.30	45.00	82.50	49.30
01XXX011	7.10	43.60	80.00	52.00
01XXX100	6.80	42.10	77.50	55.00
01XXX101	6.50	40.75	75.00	57.50
01XXX110	6.30	39.40	72.50	60.30
01XXX111	6.00	38.00	70.00	63.00
10000XXX	5.90	37.40	68.80	65.40
10001XXX	5.90	36.70	67.50	67.80
10010XXX	5.80	36.00	66.30	70.10
10011XXX	5.80	35.40	65.00	72.50
10100XXX	5.70	35.00	63.80	74.90
10101XXX	5.60	34.10	62.50	77.30
10110XXX	5.60	33.50	61.30	79.60
10111XXX	5.50	32.80	60.00	82.00
11000XXX	5.40	32.10	58.80	84.30
11001XXX	5.40	31.50	57.50	86.50
11010XXX	5.30	30.70	56.30	88.80
11011XXX	5.30	30.10	55.00	91.00
11100XXX	5.20	29.50	53.80	93.30
11101XXX	5.10	28.80	52.50	95.50
11110XXX	5.10	28.20	51.30	97.80
11111XXX	5.00	27.50	50.00	100.00

Note: Use of settings in the first three rows is not recommended. X means don't care.

Programmable Clock Manager (PCM) (continued)

PCM Detailed Programming

Descriptions of bit fields and individual control bits in the PCM control registers are provided in Table 31. Refer to Figure 46 for more information on the location of the PCM elements that are discussed. In the following discussion, the duty cycle is in the percentage of the clock period where the clock is high.

Table 31. PCM Control Registers

Bit #	Function
Register 0 Divider 0 Programming	
Bits [3:0]	**4-Bit Divider, DIV0, Value**. This value enables the input clock to immediately be divided by a value from 1 to 8. A 0 value (the default) indicates that DIV0 is bypassed (no division). Bypass incurs less delay than dividing by 1. Hexadecimal values greater than 8 for bits [3:0] yield their modulo 8 value. For example, if bits [3:0] are 1001 (9 hex), the result is divide by 1 (remainder 9/8 = 1).
Bits [6:4]	**Reserved**.
Bit 7	**DIV 0 Reset Bit**. DIV0 may not be reset by GSRN depending on the value of register 7, bit 7. This bit may be set to 1 to reset DIV0 to its default value. Bit 0 must be set to 0 (the default) to remove the reset.
Register 1 Divider 1 Programming	
Bits [3:0]	**4-Bit Divider, DIV1, Value**. This value enables the feedback clock to be divided by a value from 1 to 8. A 0 value (the default) indicates that DIV1 is bypassed (no division). Bypass incurs less delay than dividing by 1. Hexadecimal values greater than 8 for bits [3:0] yield their modulo 8 value. For example, if bits [3:0] are 1001 (9 hex), the result is divide by 1 (remainder 9/8 = 1).
Bits [6:4]	**Reserved**.
Bit 7	**DIV1 Reset Bit**. DIV1 may not be reset by GSRN, depending on the value of register 7, bit 7. This bit may be set to 1 to reset DIV1 to its default value. Bit 0 must be set to 0 (the default) to remove the reset.
Register 2 Divider 2 Programming	
Bits [3:0]	**4-Bit Divider, DIV2, Value**. This value enables the tapped delay line output clock driven onto ExpressCLK to be divided by a value from 1 to 8. A 0 value (the default) indicates that DIV2 is bypassed (no division). Bypass incurs less delay than dividing by 1. Hexadecimal values greater than 8 for bits [3:0] yield their modulo 8 value. For example, if bits [3:0] are 1001 (9 hex), the result is divide by 1 (remainder 9/8 = 1).
Bits [6:4]	**Reserved**.
Bit 7	**DIV2 Reset Bit**. DIV2 may not be reset by GSRN, depending on the value of register 7, bit 7. This bit may be set to 1 to reset DIV2 to its default value. Bit 7 must be set to 0 (the default) to remove the reset.
Register 3 DLL 2x Duty-Cycle Programming	
Bits [2:0]	Duty-cycle selection for the doubled clock period associated with the input clock high. The duty cycle is (value of bit 6) * 50% + ((value of bits [2:0]) + 1) * 6.25%. See the description for bit 6.
Bits [5:3]	Duty-cycle selection for the doubled clock period associated with the input clock low. The duty cycle is (value of bit 7) * 50% + ((value of bits [2:0]) + 1) * 6.25%. See the description for bit 7.
Bit 6	Master duty-cycle control for the first clock period of the doubled clock: 0 = less than or equal to 50%, 1 = greater than 50%.
Bit 7	Master duty-cycle control for the second clock period of the doubled clock: 0 = less than or equal to 50%, 1 = greater than 50%. Example: Both clock periods having a 62.5% duty cycle, bits [7:0] are 11 001 001.

FPGA Configuration Modes (continued)

Daisy-Chaining

Multiple FPGAs can be configured by using a daisy-chain of the FPGAs. Daisy-chaining uses a lead FPGA and one or more FPGAs configured in slave serial mode. The lead FPGA can be configured in any mode except slave parallel mode. (Daisy-chaining is available with the boundary-scan ram_w instruction discussed later.)

All daisy-chained FPGAs are connected in series. Each FPGA reads and shifts the preamble and length count in on positive CCLK and out on negative CCLK edges.

An upstream FPGA that has received the preamble and length count outputs a high on DOUT until it has received the appropriate number of data frames so that downstream FPGAs do not receive frame start bit pairs. After loading and retransmitting the preamble and length count to a daisy-chain of slave devices, the lead device loads its configuration data frames.

The loading of configuration data continues after the lead device has received its configuration data if its internal frame bit counter has not reached the length count. When the configuration RAM is full and the number of bits received is less than the length count field, the FPGA shifts any additional data out on DOUT.

The configuration data is read into DIN of slave devices on the positive edge of CCLK, and shifted out DOUT on the negative edge of CCLK. Figure 63 shows the connections for loading multiple FPGAs in a daisy-chain configuration.

The generation of CCLK for the daisy-chained devices that are in slave serial mode differs depending on the configuration mode of the lead device. A master parallel mode device uses its internal timing generator to produce an internal CCLK at eight times its memory address rate (RCLK). The asynchronous peripheral mode device outputs eight CCLKs for each write cycle. If the lead device is configured in slave mode, CCLK must be routed to the lead device and to all of the daisy-chained devices.

Figure 63. Daisy-Chain Configuration Schematic

As seen in Figure 63, the $\overline{\text{INIT}}$ pins for all of the FPGAs are connected together. This is required to guarantee that powerup and initialization will work correctly. In general, the DONE pins for all of the FPGAs are also connected together as shown to guarantee that all of the FPGAs enter the start-up state simultaneously. This may not be required, depending upon the start-up sequence desired.

Electrical Characteristics

Table 37. Electrical Characteristics

OR3Cxx Commercial: V_{DD} = 5.0 V ± 5%, 0 °C < T_A < 70 °C; Industrial: V_{DD} = 5.0 V ± 10%, –40 °C < T_A < +85 °C.
OR3Txxx Commercial: V_{DD} = 3.0 V to 3.6 V, 0 °C < T_A < 70 °C; Industrial: V_{DD} = 3.0 V to 3.6 V, –40 °C < T_A < +85 °C.

Parameter	Symbol	Test Conditions	OR3Cxx		OR3Txxx		Unit
			Min	Max	Min	Max	
Input Voltage: High Low	 V_{IH} V_{IL}	Input configured as CMOS (includes OR3Txxx)	 50% V_{DD} GND – 0.5	 V_{DD} + 0.5 20% V_{DD}	 50% V_{DD} GND – 0.5	 V_{DD} + 0.5 30% V_{DD}	 V V
Input Voltage: High Low	 V_{IH} V_{IL}	OR3Txxx 5 V Tolerant	 — —	 — —	 50% V_{DD} GND – 0.5	 5.8 V 30% V_{DD}	 V V
Input Voltage: High Low	 V_{IH} V_{IL}	Input configured as TTL (not valid for OR3Txxx)	 2.0 –0.5	 V_{DD} + 0.3 0.8	 — —	 — —	 V V
Output Voltage: High Low	 V_{OH} V_{OL}	 V_{DD} = min, I_{OH} = 6 mA or 3 mA V_{DD} = min, I_{OL} = 12 mA or 6 mA	 2.4 —	 — 0.4	 2.4 —	 — 0.4	 V V
Input Leakage Current	I_L	V_{DD} = max, V_{IN} = V_{SS} or V_{DD}	–10	10	–10	10	µA
Standby Current: OR3T20 OR3T30 OR3T55 OR3C/T80 OR3T125	I_{DDSB}	OR3Cxx (T_A = 25 °C, V_{DD} = 5.0 V) OR3Txxx (T_A = 25 °C, V_{DD} = 3.3 V) internal oscillator running, no output loads, inputs V_{DD} or GND (after configuration)	 — — — — —	 — — 4.06 4.56 —	 — — — — —	 4.70 4.90 5.30 5.80 6.70	 mA mA mA mA mA
Standby Current: OR3T20 OR3T30 OR3T55 OR3C/T80 OR3T125	I_{DDSB}	OR3Cxx (T_A = 25 °C, V_{DD} = 5.0 V) OR3Txxx (T_A = 25 °C, V_{DD} = 3.3 V) internal oscillator stopped, no output loads, inputs V_{DD} or GND (after configuration)	 — — — — —	 — — 3.05 3.42 —	 — — — — —	 3.52 3.68 3.98 4.35 5.02	 mA mA mA mA mA
Powerup Current: OR3T20 OR3T30 OR3T55 OR3C/T80 OR3T125	Ipp	Power supply current @ approximately 1 V, within a recommended power supply ramp rate of 1 ms—200 ms	 — — 3.2 5.4 —	 — — — — —	 1.2 1.6 2.7 4.0 6.5	 — — — — —	 mA mA mA mA mA
Data Retention Voltage	V_{DR}	T_A = 25 °C	2.3	—	2.3	—	V
Input Capacitance	C_{IN}	OR3Cxx (T_A = 25 °C, V_{DD} = 5.0 V) OR3Txxx (T_A = 25 °C, V_{DD} = 3.3 V) Test frequency = 1 MHz	—	9	—	8	pF
Output Capacitance	C_{OUT}	OR3Cxx (T_A = 25 °C, V_{DD} = 5.0 V) OR3Txxx (T_A = 25 °C, V_{DD} = 3.3 V) Test frequency = 1 MHz	—	9	—	8	pF

Timing Characteristics (continued)

In addition to supply voltage, process variation, and operating temperature, circuit and process improvements of the *ORCA* Series FPGAs over time will result in significant improvement of the actual performance over those listed for a speed grade. Even though lower speed grades may still be available, the distribution of yield to timing parameters may be several speed grades higher than that designated on a product brand. Design practices need to consider best-case timing parameters (e.g., delays = 0), as well as worst-case timing.

The routing delays are a function of fan-out and the capacitance associated with the CIPs and metal interconnect in the path. The number of logic elements that can be driven (fan-out) by PFUs is unlimited, although the delay to reach a valid logic level can exceed timing requirements. It is difficult to make accurate routing delay estimates prior to design compilation based on fan-out. This is because the CAE software may delete redundant logic inserted by the designer to reduce fan-out, and/or it may also automatically reduce fan-out by net splitting.

The waveform test points are given in the Input/Output Buffer Measurement Conditions section of this data sheet. The timing parameters given in the electrical characteristics tables in this data sheet follow industry practices, and the values they reflect are described below.

Propagation Delay—The time between the specified reference points. The delays provided are the worst case of the tphh and tpll delays for noninverting functions, tplh and tphl for inverting functions, and tphz and tplz for 3-state enable.

Setup Time—The interval immediately preceding the transition of a clock or latch enable signal, during which the data must be stable to ensure it is recognized as the intended value.

Hold Time—The interval immediately following the transition of a clock or latch enable signal, during which the data must be held stable to ensure it is recognized as the intended value.

3-State Enable—The time from when a 3-state control signal becomes active and the output pad reaches the high-impedance state.

PFU Timing

Table 41. Combinatorial PFU Timing Characteristics

OR3Cxx Commercial: V_{DD} = 5.0 V ± 5%, 0 °C < T_A < 70 °C; Industrial: V_{DD} = 5.0 V ± 10%, –40 °C < T_A < +85 °C.
OR3Txxx Commercial: V_{DD} = 3.0 V to 3.6 V, 0 °C < T_A < 70 °C; Industrial: V_{DD} = 3.0 V to 3.6 V, –40 °C < T_A < +85 °C.

Parameter	Symbol	Speed								Unit
		-4		-5		-6		-7		
		Min	Max	Min	Max	Min	Max	Min	Max	
Combinatorial Delays (T_J = +85 °C, V_{DD} = min):										
Four-input Variables (Kz[3:0] to F[z])*	F4_DEL	—	2.34	—	1.80	—	1.32	—	1.05	ns
Five-input Variables (F5[A:D] to F[0, 2, 4, 6])	F5_DEL	—	2.11	—	1.57	—	1.23	—	0.99	ns
Two-level LUT Delay (Kz[3:0] to F w/feedbk)*	SWL2_DEL	—	4.87	—	3.66	—	2.58	—	2.03	ns
Two-level LUT Delay (F5[A:D] to F w/feedbk)	SWL2F5_DEL	—	4.69	—	3.51	—	2.48	—	1.94	ns
Three-level LUT Delay (Kz[3:0] to F w/feedbk)*	SWL3_DEL	—	6.93	—	5.15	—	3.63	—	2.82	ns
Three-level LUT Delay (F5[A:D] to F w/feedbk)	SWL3F5_DEL	—	6.89	—	5.08	—	3.54	—	2.75	ns
C_{IN} to C_{OUT} Delay (logic mode)	CO_DEL	—	3.47	—	2.65	—	1.79	—	1.43	ns

* Four-input variables' (Kz[3:0]) path delays are valid for LUTs in both F4 (four-input LUT) and F5 (five-input LUT) modes.

Timing Characteristics (continued)

Table 42. Sequential PFU Timing Characteristics

OR3Cxx Commercial: V_{DD} = 5.0 V ± 5%, 0 °C < T_A < 70 °C; Industrial: V_{DD} = 5.0 V ± 10%, –40 °C < T_A < +85 °C.
OR3Txxx Commercial: V_{DD} = 3.0 V to 3.6 V, 0 °C < T_A < 70 °C; Industrial: V_{DD} = 3.0 V to 3.6 V, –40 °C < T_A < +85 °C.

Parameter	Symbol	Speed								Unit
		-4		-5		-6		-7		
		Min	Max	Min	Max	Min	Max	Min	Max	
Input Requirements										
Clock Low Time	CLKL_MPW	3.36	—	2.07	—	0.94	—	0.72	—	ns
Clock High Time	CLKH_MPW	1.61	—	1.06	—	0.54	—	0.45	—	ns
Global S/R Pulse Width (GSRN)	GSR_MPW	3.36	—	2.07	—	0.94	—	0.72	—	ns
Local S/R Pulse Width	LSR_MPW	3.36	—	2.07	—	0.94	—	0.72	—	ns
Combinatorial Setup Times (T_J = +85 °C, V_{DD} = min):										
Four-input Variables to Clock (Kz[3:0] to CLK)*	F4_SET	1.99	—	1.47	—	1.08	—	0.85	—	ns
Five-input Variables to Clock (F5[A:D] to CLK)	F5_SET	1.79	—	1.33	—	1.03	—	0.81	—	ns
Data In to Clock (DIN[7:0] to CLK)	DIN_SET	0.47	—	0.32	—	0.18	—	0.16	—	ns
Carry-in to Clock, DIRECT to REGCOUT (CIN to CLK)	CINDIR_SET	1.25	—	0.99	—	0.71	—	0.58	—	ns
Clock Enable to Clock (CE to CLK)	CE1_SET	2.86	—	2.15	—	1.80	—	1.37	—	ns
Clock Enable to Clock (ASWE to CLK)	CE2_SET	1.68	—	1.30	—	0.95	—	0.77	—	ns
Local Set/Reset to Clock (SYNC) (LSR to CLK)	LSR_SET	1.86	—	1.36	—	0.86	—	0.68	—	ns
Data Select to Clock (SEL to CLK)	SEL_SET	1.37	—	1.00	—	0.92	—	0.70	—	ns
Two-level LUT to Clock (Kz[3:0] to CLK w/feedbk)*	SWL2_SET	3.98	—	2.99	—	2.13	—	1.63	—	ns
Two-level LUT to Clock (F5[A:D] to CLK w/feedbk)	SWL2F5_SET	4.06	—	2.97	—	2.29	—	1.68	—	ns
Three-level LUT to Clock (Kz[3:0] to CLK w/feedbk)*	SWL3_SET	6.49	—	4.81	—	3.42	—	2.64	—	ns
Three-level LUT to Clock (F5[A:D] to CLK w/feedbk)	SWL3F5_SET	6.39	—	4.73	—	3.34	—	2.57	—	ns
Combinatorial Hold Times (T_J = all, V_{DD} = all):										
Data In (DIN[7:0] from CLK)	DIN_HLD	0.00	—	0.00	—	0.00	—	0.00	—	ns
Carry-in from Clock, DIRECT to REGCOUT (CIN from CLK)	CINDIR_HLD	0.00	—	0.00	—	0.00	—	0.00	—	ns
Clock Enable (CE from CLK)	CE1_HLD	0.00	—	0.00	—	0.00	—	0.00	—	ns
Clock Enable from Clock (ASWE from CLK)	CE2_HLD	0.00	—	0.00	—	0.00	—	0.00	—	ns
Local Set/Reset from Clock (sync) (LSR from CLK)	LSR_HLD	0.00	—	0.00	—	0.00	—	0.00	—	ns
Data Select from Clock (SEL from CLK)	SEL_HLD	0.00	—	0.00	—	0.00	—	0.00	—	ns
All Others	—	0.00	—	0.00	—	0.00	—	0.00	—	ns
Output Characteristics										
Sequential Delays (T_J = +85 °C, V_{DD} = min):										
Local S/R (async) to PFU Out (LSR to Q[7:0], REGCOUT)	LSR_DEL	—	7.02	—	5.29	—	3.64	—	2.90	ns
Global S/R to PFU Out (GSRN to Q[7:0], REGCOUT)	GSR_DEL	—	5.21	—	3.90	—	2.55	—	2.00	ns
Clock to PFU Out—Register (CLK to Q[7:0], REGCOUT)	REG_DEL	—	2.38	—	1.75	—	1.26	—	0.97	ns
Clock to PFU Out—Latch (CLK to Q[7:0])	LTCH_DEL	—	2.51	—	1.88	—	1.21	—	0.96	ns
Transparent Latch (DIN[7:0] to Q[7:0])	LTCHD_DEL	—	2.73	—	2.10	—	1.38	—	1.12	ns

* Four-input variables' (Kz[3:0]) setup times are valid for LUTs in both F4 (four-input LUT) and F5 (five-input LUT) modes.

Note: The table shows worst-case delays. ispLEVER reports the delays for individual paths within a group of paths representing the same timing parameter and may accurately report delays that are less than those listed.

Timing Characteristics (continued)

PIO Timing

Table 48. Programmable I/O (PIO) Timing Characteristics

OR3Cxx Commercial: V_{DD} = 5.0 V ± 5%, 0 °C < T_A < 70 °C; Industrial: V_{DD} = 5.0 V ± 10%, –40 °C < T_A < +85 °C.
OR3Txxx Commercial: V_{DD} = 3.0 V to 3.6 V, 0 °C < T_A < 70 °C; Industrial: V_{DD} = 3.0 V to 3.6 V, –40 °C < T_A < +85 °C.

Parameter	Symbol	Speed								Unit
		-4		-5		-6		-7		
		Min	Max	Min	Max	Min	Max	Min	Max	
Input Delays (T_J = 85 °C, V_{DD} = min)										
Input Rise Time	IN_RIS	—	500	—	500	—	500	—	500	ns
Input Fall Time	IN_FAL	—	500	—	500	—	500	—	500	ns
PIO Direct Delays:										
Pad to In (pad to CLK IN)	CKIN_DEL	—	1.41	—	1.26	—	0.64	—	0.41	ns
Pad to In (pad to IN1, IN2)	IN_DEL	—	2.16	—	1.87	—	1.28	—	0.90	ns
Pad to In Delayed (pad to IN1, IN2)	IND_DEL	—	9.05	—	7.83	—	6.64	—	7.27	ns
PIO Transparent Latch Delays:										
Pad to In (pad to IN1, IN2)	LATCH_DEL	—	4.11	—	3.25	—	2.52	—	1.82	ns
Pad to In Delayed (pad to IN1, IN2)	LATCHD_DEL	—	10.58	—	9.05	—	7.67	—	7.65	ns
Input Latch/FF Setup Timing:										
Pad to ExpressCLK (fast-capture latch/FF)	INREGE_SET	5.93	—	4.82	—	3.63	—	3.23	—	ns
Pad Delayed to ExpressCLK (fast-capture latch/FF)	INREGED_SET	12.86	—	11.03	—	9.18	—	9.68	—	ns
Pad to Clock (input latch/FF)	INREG_SET	1.62	—	1.42	—	0.71	—	0.50	—	ns
Pad Delayed to Clock (input latch/FF)	INREGD_SET	8.57	—	7.36	—	5.91	—	7.06	—	ns
Clock Enable to Clock (CE to CLK)	INCE_SET	2.03	—	1.64	—	1.29	—	1.00	—	ns
Local Set/Reset (sync) to Clock (LSR to CLK)	INLSR_SET	1.79	—	1.45	—	1.14	—	0.89	—	ns
Input FF/Latch Hold Timing:										
Pad from ExpressCLK (fast-capture latch/FF)	INREGE_HLD	0.00	—	0.00	—	0.00	—	0.00	—	ns
Pad Delayed from ExpressCLK (fast-capture latch/FF)	INREGED_HLD	0.00	—	0.00	—	0.00	—	0.00	—	ns
Pad from Clock (input latch/FF)	INREG_HLD	0.00	—	0.00	—	0.00	—	0.00	—	ns
Pad Delayed from Clock (input latch/FF)	INREGD_HLD	0.00	—	0.00	—	0.00	—	0.00	—	ns
Clock Enable from Clock (CE from CLK)	INCE_HLD	0.00	—	0.00	—	0.00	—	0.00	—	ns
Local Set/Reset (sync) from Clock (LSR from CLK)	INLSR_HLD	0.00	—	0.00	—	0.00	—	0.00	—	ns
Clock-to-in Delay (FF CLK to IN1, IN2)	INREG_DEL	—	4.05	—	3.14	—	2.53	—	2.05	ns
Clock-to-in Delay (latch CLK to IN1, IN2)	INLTCH_DEL	—	4.08	—	3.19	—	2.62	—	2.14	ns
Local S/R (async) to IN (LSR to IN1, IN2)	INLSR_DEL	—	6.11	—	4.76	—	3.81	—	3.17	ns
Local S/R (async) to IN (LSR to IN1, IN2) LatchFF in Latch Mode	INLSRL_DEL	—	5.89	—	4.66	—	3.57	—	2.98	ns
Global S/R to In (GSRN to IN1, IN2)	INGSR_DEL	—	5.38	—	4.22	—	3.44	—	2.88	ns

Note: The delays for all input buffers assume an input rise/fall time of <1 V/ns.

Timing Characteristics (continued)

Table 51. Boundary-Scan Timing Characteristics

OR3Cxx Commercial: V_{DD} = 5.0 V ± 5%, 0 °C < T_A < 70 °C; Industrial: V_{DD} = 5.0 V ± 10%, –40 °C < T_A < +85 °C.
OR3Txxx Commercial: V_{DD} = 3.0 V to 3.6 V, 0 °C < T_A < 70 °C; Industrial: V_{DD} = 3.0 V to 3.6 V, –40 °C < T_A < +85 °C.

Parameter	Symbol	Min	Max	Unit
TDI/TMS to TCK Setup Time	T_S	25.0	—	ns
TDI/TMS Hold Time from TCK	T_H	0.0	—	ns
TCK Low Time	T_{CL}	50.0	—	ns
TCK High Time	T_{CH}	50.0	—	ns
TCK to TDO Delay	T_D	—	20.0	ns
TCK Frequency	T_{TCK}	—	10.0	MHz

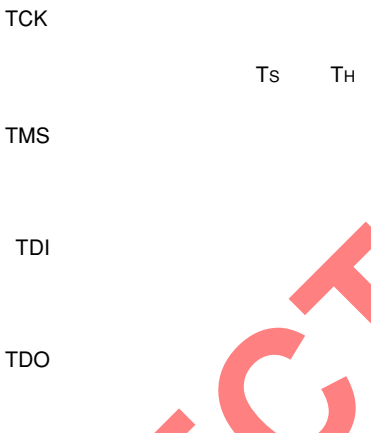

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Figure 75. Boundary-Scan Timing Diagram

Pin Information (continued)

Table 67. Pin Descriptions (continued)

Symbol	I/O	Description
Special-Purpose Pins (continued)		
M3	I	During powerup and initialization, M3 is used to select the speed of the internal oscillator during configuration with their values latched on the rising edge of $\overline{\text{INIT}}$. When M3 is low, the oscillator frequency is 10 MHz. When M3 is high, the oscillator is 1.25 MHz. During configuration, a pull-up is enabled.
	I/O	After configuration, this pin is a user-programmable I/O pin (see Note).
TDI, TCK, TMS	I	If boundary scan is used, these pins are test data in, test clock, and test mode select inputs. If boundary scan is not selected, all boundary-scan functions are inhibited once configuration is complete. Even if boundary scan is not used, either TCK or TMS must be held at logic 1 during configuration. Each pin has a pull-up enabled during configuration.
	I/O	After configuration, these pins are user-programmable I/O (see Note).
RDY/RCLK/ MPI_ALE	O	During configuration in peripheral mode, RDY/RCLK indicates another byte can be written to the FPGA. If a read operation is done when the device is selected, the same status is also available on D7 in asynchronous peripheral mode.
	O	During the master parallel configuration mode, RCLK is a read output signal to an external memory. This output is not normally used.
	I	In *i960* microprocessor mode, this pin acts as the address latch enable (ALE) input.
	I/O	After configuration, if the MPI is not used, this pin is a user-programmable I/O pin (see Note).
HDC	O	High During Configuration is output high until configuration is complete. It is used as a control output, indicating that configuration is not complete.
	I/O	After configuration, this pin is a user-programmable I/O pin (see Note).
$\overline{\text{LDC}}$	O	$\overline{\text{Low During Configuration}}$ is output low until configuration is complete. It is used as a control output, indicating that configuration is not complete.
	I/O	After configuration, this pin is a user-programmable I/O pin (see Note).
$\overline{\text{INIT}}$	I/O	$\overline{\text{INIT}}$ is a bidirectional signal before and during configuration. During configuration, a pull-up is enabled, but an external pull-up resistor is recommended. As an active-low open-drain output, $\overline{\text{INIT}}$ is held low during power stabilization and internal clearing of memory. As an active-low input, $\overline{\text{INIT}}$ holds the FPGA in the wait-state before the start of configuration.
	I/O	After configuration, this pin is a user-programmable I/O pin (see Note).

Note: The FPGA States of Operation section contains more information on how to control these signals during start-up. The timing of DONE release is controlled by one set of bit stream options, and the timing of the simultaneous release of all other configuration pins (and the activation of all user I/Os) is controlled by a second set of options.

Pin Information (continued)

Compatibility with OR2C/TxxA Series

The pinouts shown for the OR3Cxx and OR3Txxx devices are consistent with the OR2C/TxxA Series for all devices offered in the same packages. This includes the following pins: VDD, VSS, VDD5 (OR2TxxA Series only), and all configuration pins.

The following restrictions apply:

1. There are two configuration modes supported in the OR2C/TxxA Series that are **not** supported in Series 3: master parallel down and synchronous peripheral modes. The Series 3 FPGAs have two new microprocessor interface (MPI) configuration modes that are unavailable in the OR2C/TxxA Series.
2. There are four pins—one per each device side—that are user I/O in the OR2C/TxxA Series which can only be used as fast dedicated clocks or global inputs in Series 3. These pins are also used to drive the ExpressCLK to the I/O FFs on their given side of the device. These four middle ExpressCLK pins should not be used to connect to a programmable clock manager (PCM). A corner ExpressCLK input should be used instead (see item 3 below). See Table 69 for a list of these pins in each package.
3. There are two other pins that are user I/O in both the OR2C/TxxA and Series 3 but also have optional added functionality. Each of these pins drives the ExpressCLKs on two sides of the device. They also have fast connectivity to the programmable clock manager (PCM). See Table 69 for a list of these pins in each package.

Table 69. Series 3 ExpressCLK Pins

Pin Name/ Package	144-Pin TQFP	208-Pin SQFP/SQFP2	240-Pin SQFP/SQFP2	256-Pin PBGA	352-Pin PBGA	432-Pin EBGA
I-ECKL	15	22	26	K3	N2	R29
I-ECKB	55	80	91	W11	AE14	AH16
I-ECKR	92	131	152	K18	N23	T2
I-ECKT	124	178	207	B11	B14	C15
I/O-SECKLL	33	49	56	W1	AB4	AG29
I/O-SECKUR	111	159	184	A19	A25	D5

Pin	OR3T20 Pad	OR3T30 Pad	OR3T55 Pad	Function
P4	PL10A	PL11A	PL14B	I/O-A13
R3	PL11D	PL12D	PL14A	I/O
T2	PL11C	PL12C	PL15D	I/O
U1	PL11B	PL12B	PL15B	I/O
T3	PL11A	PL12A	PL16D	I/O-A14
U2	—	PL13D	PL17D	I/O
V1	PL12D	PL13C	PL17C	I/O
T4	PL12C	PL13B	PL17B	I/O
U3	—	PL13A	PL17A	I/O
V2	—	PL14D	PL18D	I/O
W1	PL12B	PL14C	PL18C	I/O-SECKLL
V3	—	PL14B	PL18B	I/O
W2	PL12A	PL14A	PL18A	I/O-A15
Y1	PCCLK	PCCLK	PCCLK	CCLK
W3	—	—	—	NC
Y2	PB1A	PB1A	PB1A	I/O-A16
W4	—	PB1C	PB1C	I/O
V4	PB1B	PB1D	PB1D	I/O
U5	PB1C	PB2A	PB2A	I/O
Y3	PB1D	PB2B	PB2B	I/O
Y4	—	PB2C	PB2C	I/O
V5	—	PB2D	PB2D	I/O
W5	PB2A	PB3A	PB3D	I/O-A17
Y5	PB2B	PB3B	PB4D	I/O
V6	PB2C	PB3C	PB5A	I/O
U7	PB2D	PB3D	PB5B	I/O
W6	PB3A	PB4A	PB5D	I/O
Y6	PB3B	PB4B	PB6A	I/O
V7	PB3C	PB4C	PB6B	I/O
W7	PB3D	PB4D	PB6D	I/O
Y7	PB4A	PB5A	PB7A	I/O
V8	PB4B	PB5B	PB7B	I/O
W8	PB4C	PB5C	PB7C	I/O
Y8	PB4D	PB5D	PB7D	I/O
U9	PB5A	PB6A	PB8A	I/O
V9	PB5B	PB6B	PB8B	I/O
W9	PB5C	PB6C	PB8C	I/O
Y9	PB5D	PB6D	PB8D	I/O
W10	PB6A	PB7A	PB9A	I/O
V10	PB6B	PB7B	PB9B	I/O
Y10	PB6C	PB7C	PB9C	I/O
Y11	PB6D	PB7D	PB9D	I/O
W11	PECKB	PECKB	PECKB	I-ECKB
V11	PB7B	PB8B	PB10B	I/O
U11	PB7C	PB8C	PB10C	I/O

Pin	OR3T20 Pad	OR3T30 Pad	OR3T55 Pad	Function
A17	PT11D	PT13B	PT16D	I/O
C16	PT11C	PT13A	PT16C	I/O
B16	PT11B	PT12D	PT16A	I/O
A16	PT11A	PT12C	PT15D	I/O-D7
C15	—	PT12B	PT15A	I/O
D14	PT10D	PT12A	PT14D	I/O
B15	PT10C	PT11D	PT14A	I/O
A15	PT10B	PT11C	PT13D	I/O
C14	PT10A	PT11B	PT13B	I/O-D6
B14	PT9D	PT11A	PT13A	I/O
A14	PT9C	PT10D	PT12D	I/O
C13	—	PT10C	PT12C	I/O
B13	PT9B	PT10B	PT12B	I/O
A13	PT9A	PT10A	PT12A	I/O-D5
D12	PT8D	PT9D	PT11D	I/O
C12	PT8C	PT9C	PT11C	I/O
B12	PT8B	PT9B	PT11B	I/O
A12	PT8A	PT9A	PT11A	I/O-D4
B11	PECKT	PECKT	PECKT	I-ECKT
C11	PT7C	PT8C	PT10C	I/O
A11	PT7B	PT8B	PT10B	I/O
A10	PT7A	PT8A	PT10A	I/O-D3
B10	PT6D	PT7D	PT9D	I/O
C10	PT6C	PT7C	PT9C	I/O
D10	PT6B	PT7B	PT9B	I/O
A9	PT6A	PT7A	PT9A	I/O-D2
B9	PT5D	PT6D	PT8D	I/O-D1
C9	PT5C	PT6C	PT8C	I/O
D9	PT5B	PT6B	PT8B	I/O
A8	PT5A	PT6A	PT8A	I/O-D0/DIN
B8	PT4D	PT5D	PT7D	I/O
C8	PT4C	PT5C	PT7C	I/O
A7	PT4B	PT5B	PT7B	I/O
B7	PT4A	PT5A	PT7A	I/O-DOUT
A6	PT3D	PT4D	PT6D	I/O
C7	PT3C	PT4C	PT6A	I/O
B6	PT3B	PT4B	PT5C	I/O
A5	PT3A	PT4A	PT5A	I/O-TDI
D7	PT2D	PT3D	PT4D	I/O
C6	PT2C	PT3C	PT4A	I/O
B5	PT2B	PT3B	PT3D	I/O
A4	PT2A	PT3A	PT3A	I/O-TMS
C5	—	PT2D	PT2D	I/O
B4	PT1D	PT2C	PT2C	I/O
A3	PT1C	PT2B	PT2B	I/O
D5	PT1B	PT2A	PT2A	I/O

Pin	OR3C/T80 Pad	OR3T125 Pad	Function
AA28	VDD	VDD	VDD
AA4	VDD	VDD	VDD
AE28	VDD	VDD	VDD
AE4	VDD	VDD	VDD
AH11	VDD	VDD	VDD
AH15	VDD	VDD	VDD
AH17	VDD	VDD	VDD
AH21	VDD	VDD	VDD
AH25	VDD	VDD	VDD
AH28	VDD	VDD	VDD
AH4	VDD	VDD	VDD
AH7	VDD	VDD	VDD
AJ29	VDD	VDD	VDD
AJ3	VDD	VDD	VDD
AK2	VDD	VDD	VDD
AK30	VDD	VDD	VDD
AL1	VDD	VDD	VDD
AL31	VDD	VDD	VDD
B2	VDD	VDD	VDD
B30	VDD	VDD	VDD
C29	VDD	VDD	VDD
C3	VDD	VDD	VDD
D11	VDD	VDD	VDD
D15	VDD	VDD	VDD
D17	VDD	VDD	VDD
D21	VDD	VDD	VDD
D25	VDD	VDD	VDD
D28	VDD	VDD	VDD
D4	VDD	VDD	VDD
D7	VDD	VDD	VDD
G28	VDD	VDD	VDD
G4	VDD	VDD	VDD
L28	VDD	VDD	VDD
L4	VDD	VDD	VDD
R28	VDD	VDD	VDD
R4	VDD	VDD	VDD
U28	VDD	VDD	VDD
U4	VDD	VDD	VDD

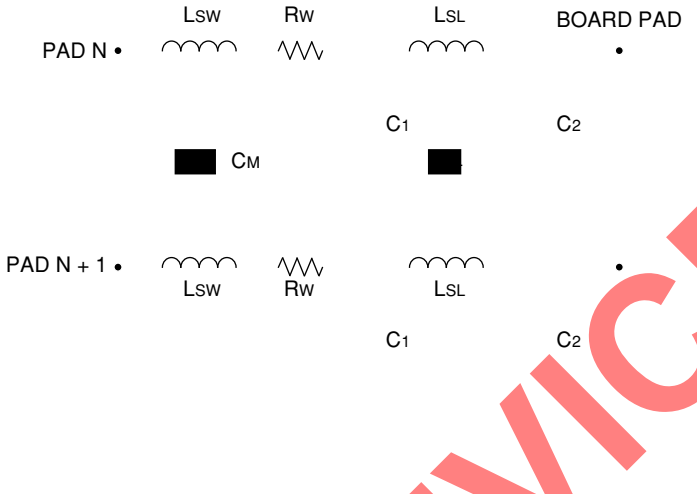

Figure 104. Package Parasitics

Package Outline Diagrams

Terms and Definitions

Basic Size (BSC): The basic size of a dimension is the size from which the limits for that dimension are derived by the application of the allowance and the tolerance.

Design Size: The design size of a dimension is the actual size of the design, including an allowance for fit and tolerance.

Typical (TYP): When specified after a dimension, this indicates the repeated design size if a tolerance is specified or repeated basic size if a tolerance is not specified.

Reference (REF): The reference dimension is an untoleranced dimension used for informational purposes only. It is a repeated dimension or one that can be derived from other values in the drawing.

Minimum (MIN) or Maximum (MAX): Indicates the minimum or maximum allowable size of a dimension.

Commercial

Device Family	Part Number	Speed Grade	Package Type	Pin/Ball Count	Grade	Packing Designator
OR3T55	OR3T557PS208-DB[1]	7	SQFP2	208	C	DB
	OR3T557S208-DB	7	SQFP	208	C	DB
	OR3T557PS240-DB[3]	7	SQFP2	240	C	DB
	OR3T557BA256-DB	7	PBGA	256	C	DB
	OR3T557BA352-DB	7	PBGA	352	C	DB
	OR3T556PS208-DB[1]	6	SQFP2	208	C	DB
	OR3T556S208-DB	6	SQFP	208	C	DB
	OR3T556PS240-DB[3]	6	SQFP2	240	C	DB
	OR3T556BA256-DB	6	PBGA	256	C	DB
	OR3T556BA352-DB	6	PBGA	352	C	DB
OR3T80	OR3T807PS208-DB[1]	7	SQFP2	208	C	DB
	OR3T807S208-DB	7	SQFP	208	C	DB
	OR3T807PS240-DB[3]	7	SQFP2	240	C	DB
	OR3T807BA352-DB	7	PBGA	352	C	DB
	OR3T807BC432-DB	7	EBGA	432	C	DB
	OR3T806PS208-DB[1]	6	SQFP2	208	C	DB
	OR3T806S208-DB	6	SQFP	208	C	DB
	OR3T806PS240-DB[3]	6	SQFP2	240	C	DB
	OR3T806BA352-DB	6	PBGA	352	C	DB
	OR3T806BC432-DB	6	EBGA	432	C	DB
OR3T125	OR3T1257PS208-DB[3]	7	SQFP2	208	C	DB
	OR3T1257PS240-DB[3]	7	SQFP2	240	C	DB
	OR3T1257BA352-DB	7	PBGA	352	C	DB
	OR3T1257BC432-DB	7	EBGA	432	C	DB
	OR3T1256PS208-DB[3]	6	SQFP2	208	C	DB
	OR3T1256PS240-DB[3]	6	SQFP2	240	C	DB
	OR3T1256BA352-DB	6	PBGA	352	C	DB
	OR3T1256BC432-DB	6	EBGA	432	C	DB

Industrial

Device Family	Part Number	Speed Grade	Package Type	Pin/Ball Count	Grade	Packing Designator
OR3C80	OR3C804PS208I-DB[2]	4	SQFP2	208	I	DB
	OR3C804BA352I-DB[2]	4	PBGA	352	I	DB
OR3T20	OR3T206S208I-DB	6	SQFP	208	I	DB
OR3T30	OR3T306S208I-DB	6	SQFP	208	I	DB
	OR3T306S240I-DB	6	SQFP	240	I	DB
	OR3T306BA256I-DB	6	PBGA	256	I	DB
OR3T55	OR3T556PS208I-DB[1]	6	SQFP2	208	I	DB
	OR3T556S208I-DB	6	SQFP	208	I	DB
	OR3T556PS240I-DB[3]	6	SQFP2	240	I	DB
	OR3T556BA256I-DB	6	PBGA	256	I	DB
	OR3T556BA352I-DB	6	PBGA	352	I	DB
OR3T80	OR3T806PS208I-DB[1]	6	SQFP2	208	I	DB
	OR3T806S208I-DB	6	SQFP	208	I	DB
	OR3T806PS240I-DB[3]	6	SQFP2	240	I	DB
	OR3T806BA352I-DB	6	PBGA	352	I	DB
	OR3T806BC432I-DB	6	EBGA	432	I	DB
OR3T125	OR3T1256PS208I-DB[3]	6	SQFP2	208	I	DB
	OR3T1256PS240I-DB[3]	6	SQFP2	240	I	DB
	OR3T1256BA352I-DB	6	PBGA	352	I	DB
	OR3T1256BC432I-DB	6	EBGA	432	I	DB

1. Converted to S208 package device per PCN#11A-06.
2. Discontinued per PCN#02-06. Contact Rochester Electronics for available inventory.
2. Discontinued per PCN#06-07. Contact Rochester Electronics for available inventory.