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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	-
Number of Logic Elements/Cells	2592
Total RAM Bits	43008
Number of I/O	171
Number of Gates	80000
Voltage - Supply	3V ~ 3.6V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 85°C (TA)
Package / Case	208-BFQFP
Supplier Device Package	208-PQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/or3t556s208i-db

Product Line	Ordering Part Number	Product Status	Reference PCN
OR3T55 (Cont'd)	OR3T557BA256-DB	Active / Orderable	
	OR3T556BA256-DB		
	OR3T556BA256I-DB		
	OR3T557BA352-DB	**Discontinued**	PCN#09-10
	OR3T556BA352-DB		
	OR3T556BA352I-DB		
OR3T80	OR3T807S208-DB	**Discontinued**	PCN#09-10
	OR3T806S208-DB		
	OR3T806S208I-DB		
	OR3T807PS240-DB	**Discontinued**	PCN#06-07
	OR3T806PS240-DB		
	OR3T806PS240I-DB		
	OR3T807BA352-DB	**Discontinued**	PCN#09-10
	OR3T806BA352-DB		
	OR3T806BA352I-DB		
	OR3T807BC432-DB		
	OR3T806BC432-DB		
	OR3T806BC432I-DB		
OR3T125	OR3T1257PS208-DB	**Discontinued**	PCN#06-07
	OR3T1256PS208-DB		
	OR3T1256PS208I-DB		
	OR3T1257PS240-DB		
	OR3T1256PS240-DB		
	OR3T1256PS240I-DB		
	OR3T1257BA352-DB		PCN#09-10
	OR3T1256BA352-DB		
	OR3T1256BA352I-DB		
	OR3T1257BC432-DB		
	OR3T1256BC432-DB		
	OR3T1256BC432I-DB		

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Internet: http://www.latticesemi.com

System-Level Features

System-level features reduce glue logic requirements and make a system on a chip possible. These features in the *ORCA* Series 3 include:

- Full PCI local bus compliance.
- Dual-use microprocessor interface (MPI) can be used for configuration, readback, device control, and device status, as well as for a general-purpose interface to the FPGA. Glueless interface to *i960** and *PowerPC*† processors with user-configurable address space provided.
- Parallel readback of configuration data capability with the built-in microprocessor interface.
- Programmable clock manager (PCM) adjusts clock phase and duty cycle for input clock rates from 5 MHz to 120 MHz. The PCM may be combined with FPGA logic to create complex functions, such as digital phase-locked loops (DPLL), frequency counters, and frequency synthesizers or clock doublers. Two PCMs are provided per device.
- True, internal, 3-state, bidirectional buses with simple control provided by the SLIC.
- 32 x 4 RAM per PFU, configurable as single- or dual-port at >176 MHz. Create large, fast RAM/ROM blocks (128 x 8 in only eight PFUs) using the SLIC decoders as bank drivers.

* *i960* is a registered trademark of Intel Corporation.
† *PowerPC* is a registered trademark of International Business Machines Corporation.

Table 2. *ORCA* Series 3 System Performance

Parameter	# PFUs	Speed				Unit
		-4	-5	-6	-7	
16-bit Loadable Up/Down Counter	2	78	102	131	168	MHz
16-bit Accumulator	2	78	102	131	168	MHz
8 x 8 Parallel Multiplier:						
Multiplier Mode, Unpipelined[1]	11.5	19	25	30	38	MHz
ROM Mode, Unpipelined[2]	8	51	66	80	102	MHz
Multiplier Mode, Pipelined[3]	15	76	104	127	166	MHz
32 x 16 RAM (synchronous):						
Single-port, 3-state Bus[4]	4	97	127	151	192	MHz
Dual-port[5]	4	127	166	203	253	MHz
128 x 8 RAM (synchronous):						
Single-port, 3-state Bus[4]	8	88	116	139	176	MHz
Dual-port[5]	8	88	116	139	176	MHz
8-bit Address Decode (internal):						
Using Softwired LUTs	0.25	4.87	3.66	2.58	2.03	ns
Using SLICs[6]	0	2.35	1.82	1.23	0.99	ns
32-bit Address Decode (internal):						
Using Softwired LUTs	2	16.06	12.07	9.01	7.03	ns
Using SLICs[7]	0	6.91	5.41	4.21	3.37	ns
36-bit Parity Check (internal)	2	16.06	12.07	9.01	7.03	ns

1. Implemented using 8 x 1 multiplier mode (unpipelined), register-to-register, two 8-bit inputs, one 16-bit output.
2. Implemented using two 32 x 12 ROMs and one 12-bit adder, one 8-bit input, one fixed operand, one 16-bit output.
3. Implemented using 8 x 1 multiplier mode (fully pipelined), two 8-bit inputs, one 16-bit output (7 of 15 PFUs contain only pipelining registers).
4. Implemented using 32 x 4 RAM mode with read data on 3-state buffer to bidirectional read/write bus.
5. Implemented using 32 x 4 dual-port RAM mode.
6. Implemented in one partially occupied SLIC with decoded output set up to CE in same PLC.
7. Implemented in five partially occupied SLICs.

Description

FPGA Overview

The *ORCA* Series 3 FPGAs are a new generation of SRAM-based FPGAs built on the successful OR2C/TxxA FPGA Series, with enhancements and innovations geared toward today's high-speed designs and tomorrow's systems on a single chip. Designed from the start to be synthesis friendly and to reduce place and route times while maintaining the complete routability of the *ORCA* 2C/2T devices, Series 3 more than doubles the logic available in each logic block and incorporates system-level features that can further reduce logic requirements and increase system speed. *ORCA* Series 3 devices contain many new patented enhancements and are offered in a variety of packages, speed grades, and temperature ranges.

The *ORCA* Series 3 FPGAs consist of three basic elements: programmable logic cells (PLCs), programmable input/output cells (PICs), and system-level features. An array of PLCs is surrounded by PICs. Each PLC contains a programmable function unit (PFU), a supplemental logic and interconnect cell (SLIC), local routing resources, and configuration RAM. Most of the FPGA logic is performed in the PFU, but decoders, *PAL*-like functions, and 3-state buffering can be performed in the SLIC. The PICs provide device inputs and outputs and can be used to register signals and to perform input demultiplexing, output multiplexing, and other functions on two output signals. Some of the system-level functions include the new microprocessor interface (MPI) and the programmable clock manager (PCM).

PLC Logic

Each PFU within a PLC contains eight 4-input (16-bit) look-up tables (LUTs), eight latches/flip-flops (FFs), and one additional flip-flop that may be used independently or with arithmetic functions.

The PFU is organized in a twin-quad fashion: two sets of four LUTs and FFs that can be controlled independently. LUTs may also be combined for use in arithmetic functions using fast-carry chain logic in either 4-bit or 8-bit modes. The carry-out of either mode may be registered in the ninth FF for pipelining. Each PFU may also be configured as a synchronous 32 x 4 single- or dual-port RAM or ROM. The FFs (or latches) may obtain input from LUT outputs or directly from invertible PFU inputs, or they can be tied high or tied low. The FFs also have programmable clock polarity, clock enables, and local set/reset.

The SLIC is connected to PLC routing resources and to the outputs of the PFU. It contains 3-state, bidirectional buffers and logic to perform up to a 10-bit AND function for decoding, or an AND-OR with optional INVERT (AOI) to perform *PAL*-like functions. The 3-state drivers in the SLIC and their direct connections to the PFU outputs make fast, true 3-state buses possible within the FPGA, reducing required routing and allowing for real-world system performance.

Programmable Logic Cells

The programmable logic cell (PLC) consists of a programmable function unit (PFU), a supplemental logic and interconnect cell (SLIC), and routing resources. All PLCs in the array are functionally identical with only minor differences in routing connectivity for improved routability. The PFU, which contains eight 4-input LUTs, eight latches/FFs, and one FF for logic implementation, is discussed in the next section, followed by discussions of the SLIC and PLC routing resources.

Programmable Function Unit

The PFUs are used for logic. Each PFU has 50 external inputs and 18 outputs and can operate in several modes. The functionality of the inputs and outputs depends on the operating mode.

The PFU uses 36 data input lines for the LUTs, eight data input lines for the latches/FFs, five control inputs (ASWE, CLK, CE, LSR, SEL), and a carry input (CIN) for fast arithmetic functions and general-purpose data input for the ninth FF. There are eight combinatorial data outputs (one from each LUT), eight latched/registered outputs (one from each latch/FF), a carry-out (COUT), and a registered carry-out (REGCOUT) that comes from the ninth FF. The carry-out signals are used principally for fast arithmetic functions.

Figure 2 and Figure 3 show high-level and detailed views of the ports in the PFU, respectively. The eight sets of LUT inputs are labeled as K0 through K7 with each of the four inputs to each LUT having a suffix of _x, where x is a number from 0 to 3. There are four F5 inputs labeled A through D. These inputs are used for a fifth LUT input for 5-input LUTs or as a selector for multiplexing two 4-input LUTs. The eight direct data inputs to the latches/FFs are labeled as DIN[7:0]. Registered LUT outputs are shown as Q[7:0], and combinatorial LUT outputs are labeled as F[7:0].

The PFU implements combinatorial logic in the LUTs and sequential logic in the latches/FFs. The LUTs are static random access memory (SRAM) and can be used for read/write or read-only memory.

Each latch/FF can accept data from its associated LUT. Alternatively, the latches/FFs can accept direct data from DIN[7:0], eliminating the LUT delay if no combinatorial function is needed. Additionally, the CIN input can be used as a direct data source for the ninth FF. The LUT outputs can bypass the latches/FFs, which reduces the delay out of the PFU. It is possible to use the LUTs and latches/FFs more or less independently, allowing, for instance, a comparator function in the LUTs simultaneously with a shift register in the FFs.

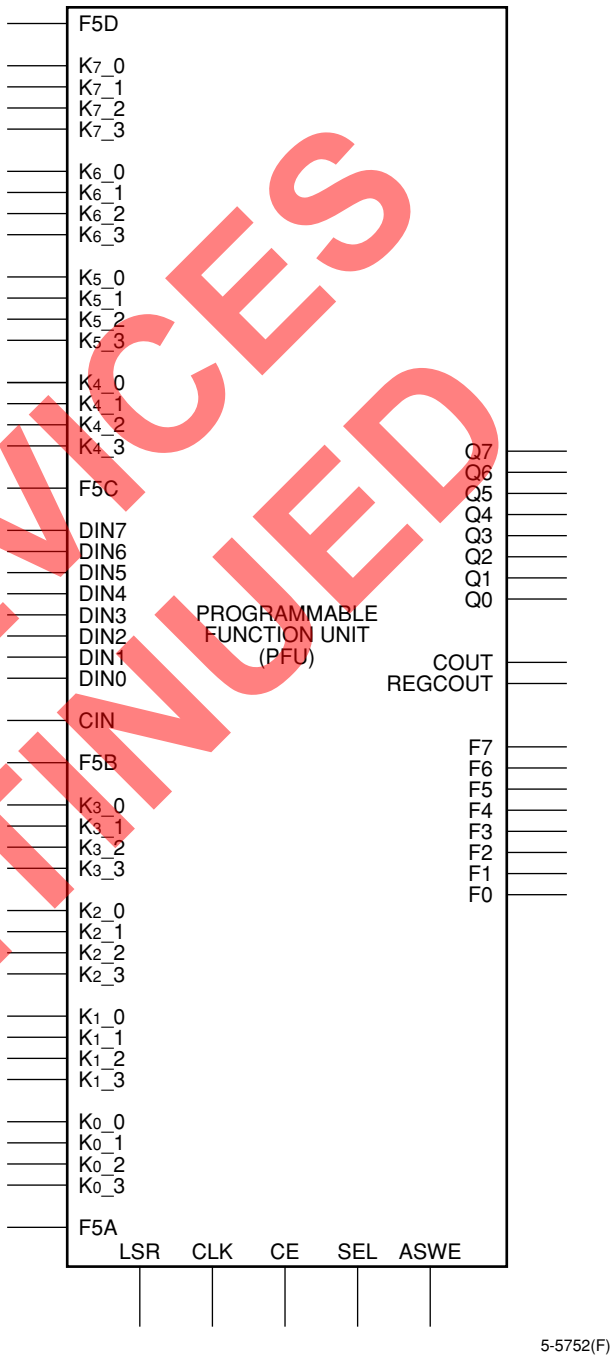


Figure 2. PFU Ports

The PFU can be configured to operate in four modes: logic mode, half-logic mode, ripple mode, and memory (RAM/ROM) mode. In addition, ripple mode has four submodes and RAM mode can be used in either a single- or dual-port memory fashion. These submodes of operation are discussed in the following sections.

Programmable Logic Cells (continued)

Intra-PLC Routing

The function of the intra-PLC routing resources is to connect the PFU's input and output ports to the routing resources used for entry to and exit from the PLC. This routing provides PFU feedback, corner turning, or switching from one type of routing resource to another.

Flexible Input Structure (FINS)

The flexible input switching structure (FINS) in each PLC of the *ORCA* Series 3 provides for the flexibility of a crossbar switch from the routing resources to the PFU inputs while taking advantage of the routability of shared inputs. Connectivity between the PLC routing resources and the PFU inputs is provided in two stages. The primary FINS switch has 50 inputs that connect the PLC routing to the 35 inputs on the secondary switch. The outputs of the second switch connect to the 50 PFU inputs. The switches are implemented to provide connectivity for bused signals and individual connections.

PFU Output Switching

The PFU outputs are switched onto PLC routing resources via the PFU output multiplexer (OMUX). The PFU output switching segments from the output multiplexer provide ten connections to the PLC routing out of 18 possible PFU outputs (F[7:0], Q[7:0], DOUT, REGCOUT). These output switching segments connect segment for segment to the SUR, SUL, SLR, and SLL switching segments described below (e.g., O4 connects only to SUR4, not SUR5). The output switching segments also feed directly into the SLIC on a segment-by-segment basis. This connectivity is also described below.

Switching Routing Segments (xSW)

There are four sets of switching routing segments in each PLC. Each set consists of ten switching elements: SUL[9:0], SUR[9:0], SLL[9:0], and SLR[9:0], traditionally labeled for the upper-left, upper-right, lower-left, and lower-right sections of the PFUs, respectively. The xSW routing segments connect to the PFU inputs and outputs as well as the BIDI routing segments, to be described later. They also connect to both the horizontal and vertical x1 and x5 routing segments (inter-PLC routing resources, described later) in their specific corner. xSW segments can be used for fast connections between adjacent PLCs or PICs without requiring the use of inter-PLC routing resources. This capability not only increases signal speed on adjacent PLC routing, but also reduces routing congestion on the principal inter-PLC routing resources. The SLL and SUR segments combine to provide connectivity to the PLCs to the left and right of the current PLC; the SLR and SUL segments combine to provide connectivity to the PLCs above and below the current PLC.

Fast routes on switching segments to diagonally adjacent PLCs/PICs are possible using the BIDI routing segments (discussed below) and the SLL and SLR switching segments. The BR BIDI routing segments combine with the SUL switching segments of the PLC below and to the right of the current PLC to connect to that PLC. The BL BIDI routing segments combine with the SLL switching segments of the PLC above and to the right of the current PLC to connect to that PLC. These fast diagonal connections provide a great amount of flexibility in routing congested areas of logic and in shifting data on a per-PLC basis such as performing implicit multiplications/divisions in routing between functional logic elements.

Switching routing segments are also the chief means by which signals are transferred between the inter-PLC routing resources and the PFU. Each set of switching segments has connectivity to the x1 routing segments, and there is varying connectivity to the x5, xH, and xL inter-PLC routing segments. Detailed information on switching segment/inter-PLC routing connectivity is provided later in this section in the Inter-PLC Routing Resources subsection.

Programmable Logic Cells (continued)

BIDI Routing and SLIC Connectivity

The SLIC is connected to the rest of the PLC by the bidirectional (BIDI) routing segments and the PFU output switching segments coming from the PFU output multiplexer. The BIDI routing segments (xBID) are labeled as BL for BIDI-left and BR for BIDI-right. Each set of BR and BL xBID segments is composed of ten bidirectional lines (note that these lines are diagramed as ten input lines to the SLIC and ten output lines from the SLIC that can be used in a mutually exclusive fashion). Because the SLIC is connected directly to the outputs of the PFU, it provides great flexibility in routing via the xBID segments. The PFU routing segments, O[9:0], only connect to their respective line in the SLL, SUL, SUR, and SLR switching segment groups. That is, O9 only connects to SLL9, SUL9, SUR9, and SLR9. The BIDI lines provide the capability to connect to the other member of the routing set. That means, for example, that O9 can be routed to BR8 or BL8. This connectivity can be used as a means to distribute or gather signals on intra-PLC routing without disturbing inter-PLC resources. As described in the Switching Routing Segments subsection, the BIDI routing segments are also used for routes to a diagonally adjacent PFU.

In addition to the intra-PLC connections, the xBID and output switching segments also have connectivity to the x1, x5, and xL inter-PLC routing resources, providing an alternate routing path rather than using PLC xSW segments. These connections also provide a path to the 3-state buffers in the SLIC without encumbering the xSW segments. In this manner, buffering or 3-state control can be added to inter-PLC routing without disturbing local functionality within a PFU.

Control Signal and Fast-Carry Routing

PFU control signal and the fast-carry routing are performed using the FINS structure and several dedicated routing paths. The fast-carry (FC) routing resources consist of a dedicated bidirectional segment between each orthogonal pair of PLCs. This means that a fast-carry can go to or come from each PLC to the right or left, above or below the subject PLC. The FINS structure is used to control the switching of these fast-carry paths between the fast-carry input (FCIN) and fast-carry output (FCOUT) ports of the PFU.

The PFU control inputs (CE, SEL, LSR, ASWE) and CIN can be reached via the FINS by two special routing segments, E1 and E2. The E1 routing segment provides connectivity between all of the xBID routing segments and the FINS. It is unidirectional from the BIDI routing to the FINS. E1 also provides connectivity to the PFU clock input via FINS for a local clock signal. The E2 segment connects the SLIC DEC output to the FINS and to a group of CIPS that provide bidirectional connectivity with all of the BIDI routing segments. This allows the DEC signal to be used in the PFU and/or routed on the BIDI segments. It also allows signals to be routed to the PFU on the xBID segments if the SLIC DEC output is not used.

There is also a dedicated routing segment from the FINS to the SLIC TRI input used for BIDI buffer 3-state control.

Programmable Logic Cells (continued)

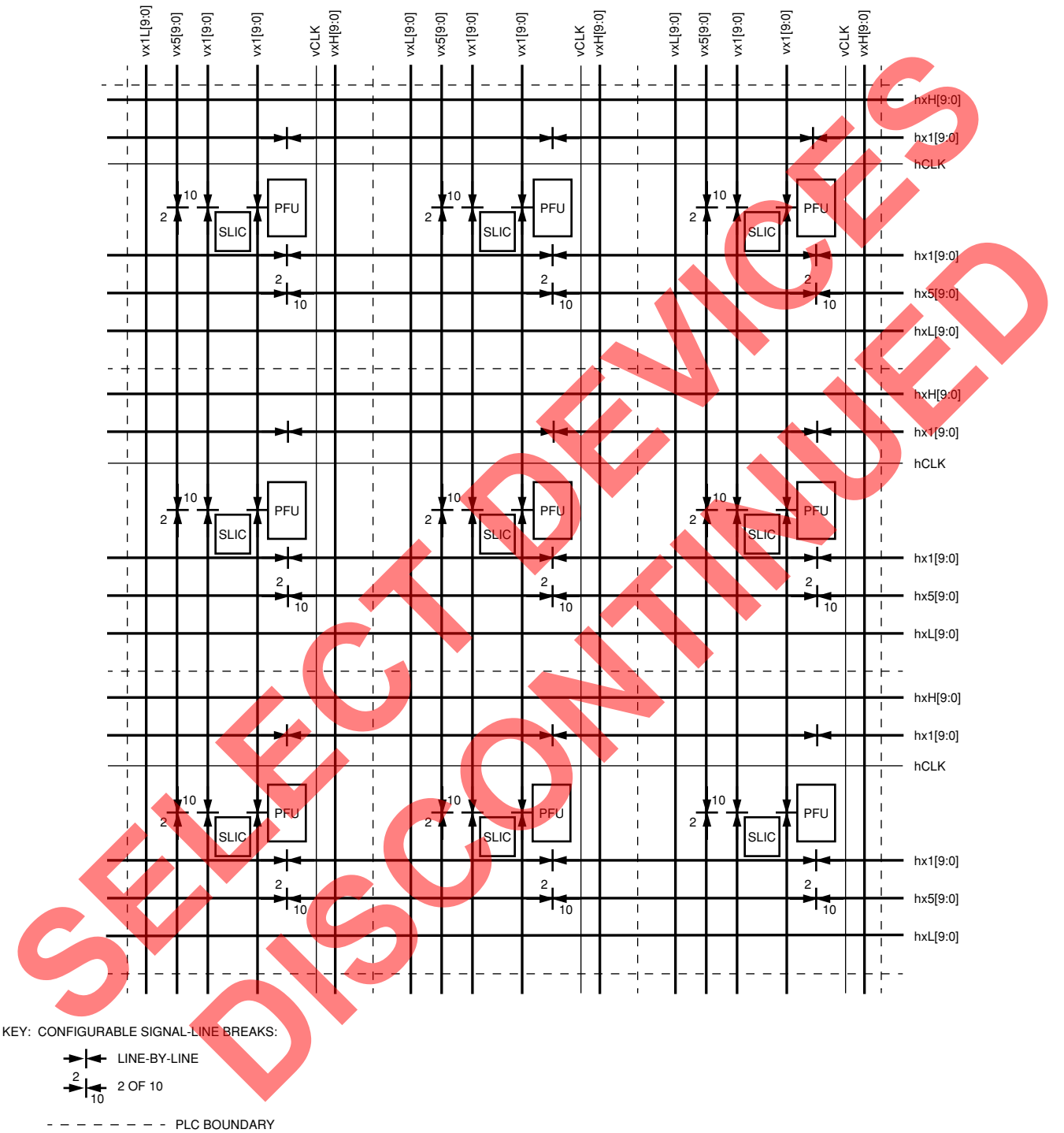


Figure 20. Multiple PLC View of Inter-PLC Routing

Programmable Logic Cells (continued)

PLC Architectural Description

Figure 21 is an architectural drawing of the PLC (as seen in ispLEVER) that reflects the PFU, the routing segments, and the CIPs. A discussion of each of the letters in the drawing follows.

A. These are switching routing segments (xSW) that give the router flexibility. In general switching theory, the more levels of indirection there are in the routing, the more routable the network is. The xSW segments can also connect to the xSW lines in adjacent PLCs.

B. These CIPs connect the x1 routing. These are located in the middle of the PLC to allow the block to connect to either the left end of the horizontal x1 segment from the right or the right end of the horizontal x1 segment from the left, or both. By symmetry, the same principle is used in the vertical direction.

C. This set of CIPs is used to connect the x1 and x5 nets to the xSW segments or to other x1 and x5 nets. The CIPs on the major diagonal allow data to be transmitted on a bit-by-bit basis from x1 nets to the xSW segments and between the x1 and x5 nets.

D. This structure is the supplemental logic and interconnect cell, or SLIC. It contains 3-statable bidirectional buffers and logic for building decoders and AND-OR-INVERT type structures.

E. These are the primary and secondary elements of the flexible input structure or FINS. FINS is a switch matrix that provides high connectivity while retaining routing capability. FINS also includes feedback paths for softwired LUT implementation.

F. This is the PFU output switch matrix. It is a complex switch network which, like the FINS at the input, provides high connectivity and maintains routability.

G. This set of CIPs allows an xBID segment to transfer a signal to/from xSW segments on each side. The BIDIs can access the PFU through the xSW segments. These CIPs allow data to be routed through the BIDIs for amplification or 3-state control and continue to another PLC. They also provide an alternative routing resource to improve routability.

H. These CIPs are used to transfer data from/to the xBID segments to/from the x1 and xL routing segments. These CIPs have been optimized to allow the BIDI buffers to drive the loads usually seen when using each type of routing segment.

I. Clock input to PFU.

J. These are the ten switched output routing segments from the PFU. They connect to the PLC switching segments and are input to the SLIC.

K. These lines deliver the auxiliary signals clock enable (CE), local set/reset (LSR), front-end select (SEL), add/subtract/write enable (ASWE), as well as the carry signals (CIN and FCIN) to the latches/FFs.

L. This is the local clock buffer. Any of the horizontal and vertical xL lines can drive the clock input of the PLC latches/FFs. The clock routing segments (vCLK and hCLK) and multiplexers/drivers are used to connect to the xL routing segments for low-skew, low-delay global signals.

M. These routing segments are used to route the fast-carry signal to/from the neighboring four PLCs. The carry-out (COUT) and registered carry-out (REGCOUT) can also be routed out of the PFU.

N. This is the E2 control routing segment. It runs from the SLIC DEC output to the FINS and also provides connectivity to all xBID segments.

O. The xH routing segments run one-half the length (width) of the array before being broken by a CIP.

P. These CIPs connect the xH segments to the xSW segments.

Q. The xBID segments are used to connect the SLIC to the xSW segments, x1 segments, x5 segments, and xL lines, as well as providing for diagonal PLC to PLC connections.

R. These CIPs provide connections from the xBID segments to the E1/E2 routing segments that feed PFU control inputs CE, LSR, CIN, ASWE, SEL, and the clock input. Alternatively, these CIPs connect the BIDI lines to the decoder (DEC) output of the SLIC, for routing the DEC signal.

S. These are clock spines (vCLK and hCLK) with the multiplexers and drivers to connect to the xL routing segments.

T. These CIPs connect xBID segments to switching segments in diagonally and orthogonally adjacent PFUs.

U. These CIPs connect xSW segments to the PFU output segments.

V. These CIPS connect xSW segments in orthogonally adjacent PFUs.

W. This is the SLIC 3-state control routing segment from the FINS to the SLIC 3-state control.

X. This is the E1 control routing segment. It provides a PFU input path from all xBID segments.

Y. These CIPs are used to select which xBID segments are connected to the E1/E2 signal as described in (R).

Programmable Input/Output Cells

The programmable input/output cells (PICs) are located along the perimeter of the device. The PIC's name is represented by a two-letter designation to indicate on which side of the device it is located followed by a number to indicate in which row or column it is located. The first letter, P, designates that the cell is a PIC and not a PLC. The second letter indicates the side of the array where the PIC is located. The four sides are left (L), right (R), top (T), and bottom (B). The individual I/O pad is indicated by a single letter (either A, B, C, or D) placed at the end of the PIC name. As an example, PL10A indicates a pad located on the left side of the array in the tenth row.

Each PIC interfaces to four bond pads and contains the necessary routing resources to provide an interface between I/O pads and the PLCs. Each PIC is composed of four programmable I/Os (PIOs) and significant routing resources. Each PIO contains input buffers, output buffers, routing resources, latches/FFs, and logic and can be configured as an input, output, or bidirectional I/O.

PICs in the Series 3 FPGAs have significant local routing resources, similar to routing in the PLCs. This new routing increases the ability to fix user pinouts prior to placement and routing of a design and still maintain routability. The flexibility provided by the routing also provides for increased signal speed due to a greater variety of signal paths possible.

Included in the PIC routing is a fast path from the input pins to the SLICs in each of the three adjacent PLCs (one orthogonal and two diagonal). This feature allows for input signals to be very quickly processed by the SLIC decoder function and used on-chip or sent back off of the FPGA. Also new to the Series 3 PIOs are latches and FFs and options for using fast, dedicated clocks called ExpressCLKs. These features will all be discussed in subsequent sections.

A diagram of a single PIO (one of four in a PIC) is shown in Figure 22. Table 9 provides an overview of the programmable functions in an I/O cell.

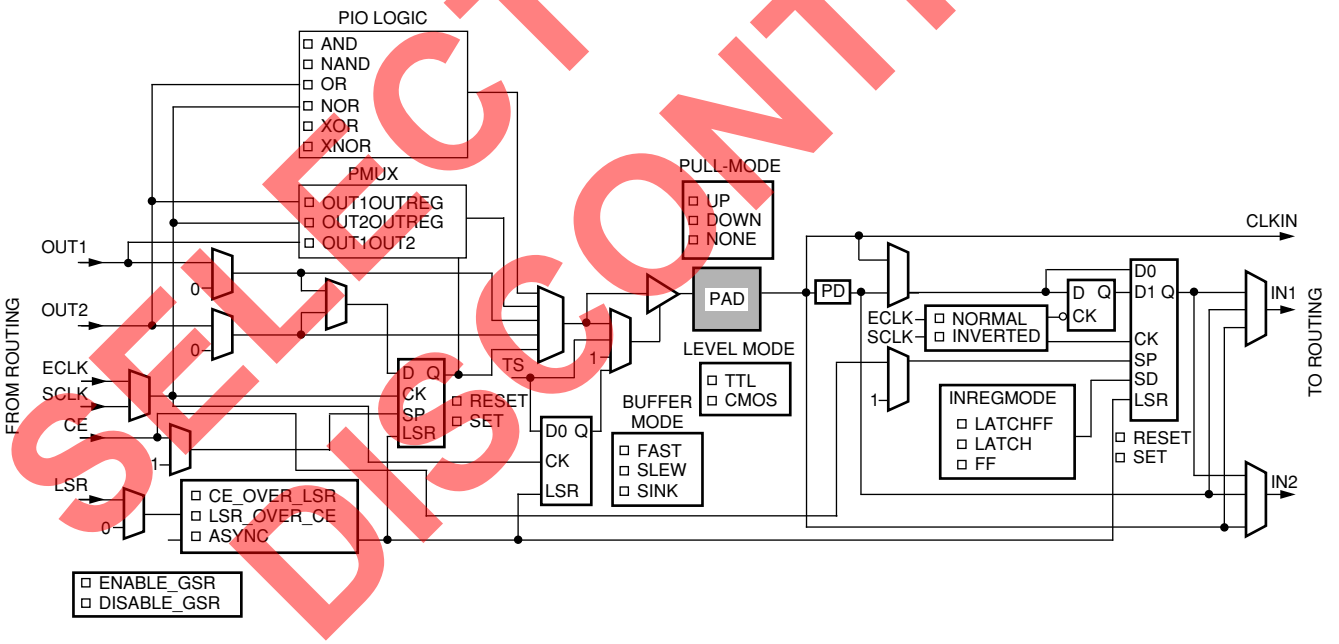


Figure 22. OR3C/Txxx Programmable Input/Output (PIO) Image from ispLEVER

Clock Distribution Network

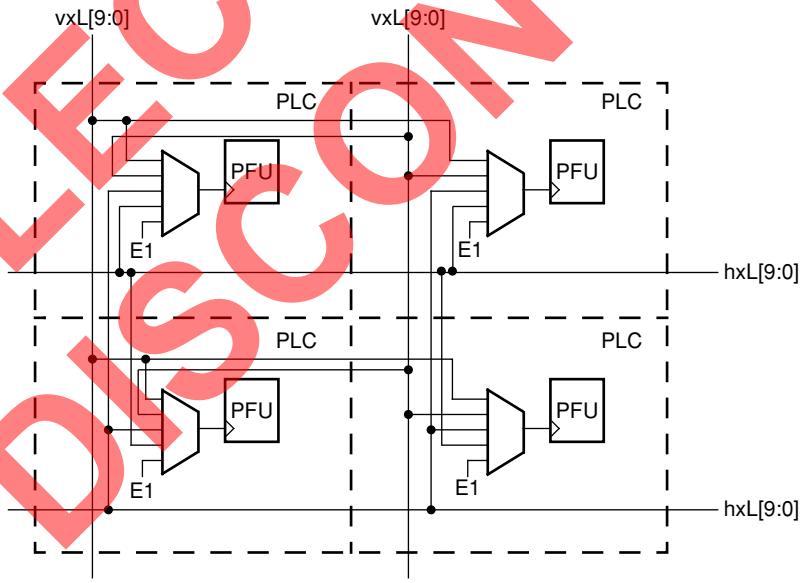
The Series 3 FPGAs provide three types of high-speed, low-skew clock distributions: system clock, fast middle clock (fast clock), and ExpressCLK. Because of the great variety of sources and distribution for clock signals in the *ORCA* Series 3, the clock mechanisms will be described here from the inside out. The clock connections to the PFU will be described, followed by clock distribution to the PLC array, clock sources to the PLC array, and finally ending with clock sources and distribution in the PICs. The ExpressCLK inputs are new, dedicated clock inputs in Series 3 FPGAs. They are mentioned in several of the clock network descriptions and are described fully later in this section.

PFU Clock Sources

Within a PLC there are five sources for the clock signal of the latches/FFs in the PFU. Two of the signals are generated off of the long lines (xL) within the PLC: one from the set of vertical long lines and one from the set of horizontal long lines. For each of these signals, any one of the ten long lines of each set, vertical or horizontal, can generate the clock signal. Two of the five PFU clock sources come from neighboring PLCs. One clock is generated from the PLC to the left or right of the current PLC, and one is generated from the PLC above or below the current PLC. The selection decision as to where these signals come from, above/below and left/right, is based on the position of the PLC in the array and has to do with the alternating nature of the source of the system clock spines (discussed later). The last of the five clock sources is also generated within the PLC. The E1 control signal, described in the PLC Routing Resources section, can drive the PFU clock. The E1 signal can come from any xBID routing resource in the PLC. The selection and switching of clock signals in a PLC is performed in the FINS. Figure 31 shows the PFU clock sources for a set of four adjacent PLCs.

Global Control Signals

The four clock signals in each PLC that are generated from the long lines (xL) in the current PLC or an adjacent PLC can also be used to drive the PFU clock enable (CE), local set/reset (LSR) and add/subtract/write enable (ASWE) signals. The clock signals generated from vertical long lines can drive CE and ASWE, and the clocks generated from horizontal long lines can drive LSR. This allows for low-skew global distribution of two of these three control signals with the clock routing while still allowing a global clock route to occur.



5-6054(F)

Figure 31. PFU Clock Sources

Timing Characteristics (continued)

Table 45. Synchronous Memory Read Characteristics

OR3Cxx Commercial: VDD = 5.0 V ± 5%, 0 °C < TA < 70 °C; Industrial: VDD = 5.0 V ± 10%, –40 °C < TA < +85 °C.
OR3Txxx Commercial: VDD = 3.0 V to 3.6 V, 0 °C < TA < 70 °C; Industrial: VDD = 3.0 V to 3.6 V, –40 °C < TA < +85 °C.

Parameter (TJ = 85 °C, VDD = min)	Symbol	Speed								Unit
		-4		-5		-6		-7		
		Min	Max	Min	Max	Min	Max	Min	Max	
Read Operation:										
Data Valid After Address (Kz[3:0] to F[6, 4, 2, 0])	RA_DEL	—	2.34	—	1.80	—	1.32	—	1.05	ns
Data Valid After Address (F5[A:D] to F[6, 4, 2, 0])	RA4_DEL	—	2.11	—	1.57	—	1.23	—	0.99	ns
Read Operation, Clocking Data into Latch/FF:										
Address to Clock Setup Time (Kz[3:0] to CLK)	RA_SET	1.99	—	1.47	—	1.08	—	0.85	—	ns
Address to Clock Setup Time (F5[A:D] to CLK)	RA4_SET	1.79	—	1.33	—	1.03	—	0.81	—	ns
Address from Clock Hold Time (Kz[3:0] from CLK)	RA_HLD	0.00	—	0.00	—	0.00	—	0.00	—	ns
Address from Clock Hold Time (F5[A:D] from CLK)	RA4_HLD	0.00	—	0.00	—	0.00	—	0.00	—	ns
Clock to PFU Output—Register (CLK to Q[6, 4, 2, 0])	REG_DEL	—	2.38	—	1.75	—	1.26	—	0.97	ns
Read Cycle Delay	SMRD_CYC	—	10.48	—	7.66	—	7.53	—	5.78	ns

Note: The table shows worst-case delays. ispLEVER reports the delays for individual paths within a group of paths representing the same timing parameter and may accurately report delays that are less than those listed.

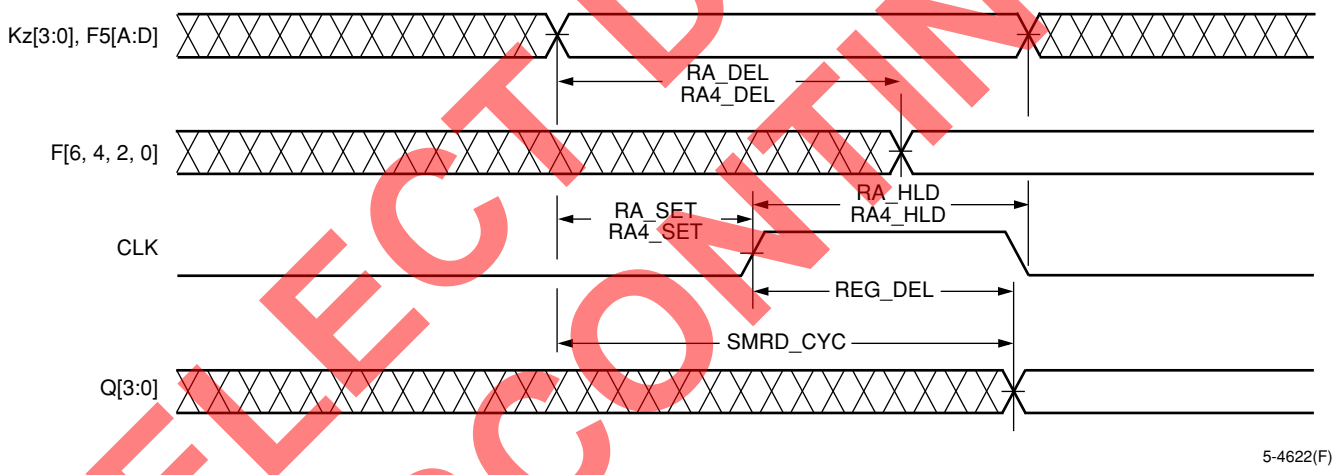


Figure 66. Synchronous Memory Read Cycle

Timing Characteristics (continued)

Table 53. General-Purpose Clock Timing Characteristics (Internally Generated Clock)

OR3Cxx Commercial: V_{DD} = 5.0 V ± 5%, 0 °C < T_A < 70 °C; Industrial: V_{DD} = 5.0 V ± 10%, –40 °C < T_A < +85 °C.
OR3Txxx Commercial: V_{DD} = 3.0 V to 3.6 V, 0 °C < T_A < 70 °C; Industrial: V_{DD} = 3.0 V to 3.6 V, –40 °C < T_A < +85 °C.

Device (T_J = 85 °C, V_{DD} = min)	Symbol	Speed								Unit
		-4		-5		-6		-7		
		Min	Max	Min	Max	Min	Max	Min	Max	
OR3T20	CLK_DEL	—	—	—	4.22	—	3.46	—	2.84	ns
OR3T30	CLK_DEL	—	—	—	4.29	—	3.48	—	2.87	ns
OR3T55	CLK_DEL	—	5.34	—	4.41	—	3.53	—	2.93	ns
OR3C/T80	CLK_DEL	—	5.49	—	4.52	—	3.57	—	2.98	ns
OR3T125	CLK_DEL	—	—	—	4.80	—	3.71	—	3.13	ns

Notes:
This table represents the delay for an internally generated clock from the clock tree input in one of the four middle PICs (using pSW routing) on any side of the device which is then distributed to the PFU/PIO clock inputs. If the clock tree input used is located at any other PIC, see the results reported by ispLEVER.

This clock delay is for a fully routed clock tree that uses the general clock network. The delay will be reduced if any of the clock branches are not used. See pin-to-pin timing in Table 56 for clock delays of clocks input on general I/O pins.

Timing Characteristics (continued)

Table 55. OR3Cxx Fast Clock (FCLK) to Output Delay (Pin-to-Pin)

OR3Cxx Commercial: V_{DD} = 5.0 V ± 5%, 0 °C < T_A < 70 °C; Industrial: V_{DD} = 5.0 V ± 10%, –40 °C < T_A < +85 °C; C_L = 50 pF.
OR3Txxx Commercial: V_{DD} = 3.0 V to 3.6 V, 0 °C < T_A < 70 °C; Industrial: V_{DD} = 3.0 V to 3.6 V, –40 °C < T_A < +85 °C; C_L = 50 pF.

Description (T_J = 85 °C, V_{DD} = min)	Device	Speed								Unit
		-4		-5		-6		-7		
		Min	Max	Min	Max	Min	Max	Min	Max	
Output Not on Same Side of Device As Input Clock (Fast Clock Delays Using ExpressCLK Inputs)										
ECLK Middle Input Pin →OUTPUT Pin (Fast)	OR3T20	—	—	—	11.13	—	7.94	—	6.40	ns
	OR3T30	—	—	—	11.35	—	8.01	—	6.48	ns
	OR3T55	—	14.68	—	11.81	—	8.18	—	6.66	ns
	OR3C/T80	—	15.30	—	12.33	—	8.36	—	6.85	ns
	OR3T125	—	—	—	13.20	—	8.68	—	7.19	ns
ECLK Middle Input Pin →OUTPUT Pin (Slewlim)	OR3T20	—	—	—	13.12	—	8.61	—	6.93	ns
	OR3T30	—	—	—	13.33	—	8.68	—	7.01	ns
	OR3T55	—	17.11	—	13.80	—	8.85	—	7.19	ns
	OR3C/T80	—	17.74	—	14.32	—	9.04	—	7.38	ns
	OR3T125	—	—	—	15.19	—	9.35	—	7.72	ns
ECLK Middle Input Pin →OUTPUT Pin (Sinklim)	OR3T20	—	—	—	14.47	—	13.46	—	11.67	ns
	OR3T30	—	—	—	14.68	—	13.53	—	11.75	ns
	OR3T55	—	18.47	—	15.15	—	13.70	—	11.93	ns
	OR3C/T80	—	19.10	—	15.67	—	13.88	—	12.12	ns
	OR3T125	—	—	—	16.54	—	14.20	—	12.46	ns
Additional Delay if ECLK Corner Pin Used	OR3T20	—	—	—	1.97	—	1.82	—	1.60	ns
	OR3T30	—	—	—	1.99	—	1.92	—	1.69	ns
	OR3T55	—	2.10	—	2.01	—	2.12	—	1.88	ns
	OR3C/T80	—	2.14	—	2.04	—	2.33	—	2.07	ns
	OR3T125	—	—	—	2.09	—	2.63	—	2.39	ns

Notes:
Timing is without the use of the programmable clock manager (PCM).

This clock delay is for a fully routed clock tree that uses the primary clock network. It includes both the input buffer delay, the clock→Q of the FF, and the delay through the output buffer. The delay will be reduced if any of the clock branches are not used. The given timing requires that the input clock pin be located at one of the six ExpressCLK inputs of the device and that a PIO FF be used.

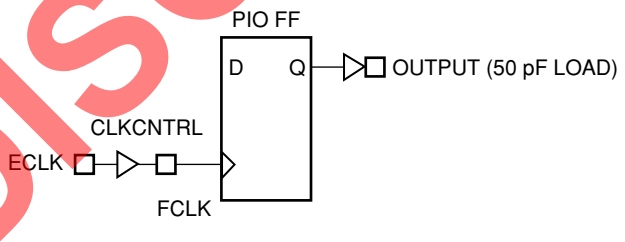


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Figure 77. Fast Clock to Output Delay

Timing Characteristics (continued)

Table 57. OR3C/Txxx Input to ExpressCLK (ECLK) Fast-Capture Setup/Hold Time (Pin-to-Pin)

OR3Cxx Commercial: V_{DD} = 5.0 V ± 5%, 0 °C < T_A < 70 °C; Industrial: V_{DD} = 5.0 V ± 10%, –40 °C < T_A < +85 °C.
OR3Txxx Commercial: V_{DD} = 3.0 V to 3.6 V, 0 °C < T_A < 70 °C; Industrial: V_{DD} = 3.0 V to 3.6 V, –40 °C < T_A < +85 °C.

Description (T_J = 85 °C, V_{DD} = min)	Device	Speed								Unit
		-4		-5		-6		-7		
		Min	Max	Min	Max	Min	Max	Min	Max	
Input to ECLK Setup Time (middle ECLK pin)	OR3T20	—	—	1.34	—	0.88	—	0.83	—	ns
	OR3T30	—	—	1.30	—	0.86	—	0.82	—	ns
	OR3T55	1.36	—	1.22	—	0.83	—	0.80	—	ns
	OR3C/T80	1.25	—	1.14	—	0.80	—	0.77	—	ns
	OR3T125	—	—	1.03	—	0.76	—	0.74	—	ns
Input to ECLK Setup Time (middle ECLK pin, delayed data input)	OR3T20	—	—	6.30	—	5.32	—	5.98	—	ns
	OR3T30	—	—	6.27	—	5.30	—	5.97	—	ns
	OR3T55	6.91	—	6.19	—	5.27	—	5.95	—	ns
	OR3C/T80	6.79	—	6.11	—	5.24	—	5.93	—	ns
	OR3T125	—	—	6.00	—	5.20	—	5.90	—	ns
Input to ECLK Setup Time (corner ECLK pin)	OR3T20	—	—	0.00	—	0.00	—	0.00	—	ns
	OR3T30	—	—	0.00	—	0.00	—	0.00	—	ns
	OR3T55	0.00	—	0.00	—	0.00	—	0.00	—	ns
	OR3C/T80	0.00	—	0.00	—	0.00	—	0.00	—	ns
	OR3T125	—	—	0.00	—	0.00	—	0.00	—	ns
Input to ECLK Setup Time (corner ECLK pin, delayed data input)	OR3T20	—	—	4.39	—	3.51	—	4.41	—	ns
	OR3T30	—	—	4.35	—	3.40	—	4.31	—	ns
	OR3T55	4.94	—	4.28	—	3.18	—	4.11	—	ns
	OR3C/T80	4.82	—	4.21	—	2.98	—	3.91	—	ns
	OR3T125	—	—	4.10	—	2.63	—	3.61	—	ns
Input to ECLK Hold Time (middle ECLK pin)	OR3T20	—	—	0.00	—	0.00	—	0.00	—	ns
	OR3T30	—	—	0.00	—	0.00	—	0.00	—	ns
	OR3T55	0.00	—	0.00	—	0.00	—	0.00	—	ns
	OR3C/T80	0.00	—	0.00	—	0.00	—	0.00	—	ns
	OR3T125	—	—	0.00	—	0.00	—	0.00	—	ns
Input to ECLK Hold Time (middle ECLK pin, delayed data input)	OR3T20	—	—	0.00	—	0.00	—	0.00	—	ns
	OR3T30	—	—	0.00	—	0.00	—	0.00	—	ns
	OR3T55	0.00	—	0.00	—	0.00	—	0.00	—	ns
	OR3C/T80	0.00	—	0.00	—	0.00	—	0.00	—	ns
	OR3T125	—	—	0.00	—	0.00	—	0.00	—	ns

Note:
The pin-to-pin timing parameters in this table should be used instead of results reported by ispLEVER.

The ECLK delays are to all of the PIOs on one side of the device for middle pin input, or two sides of the device for corner pin input. The delay includes both the input buffer delay and the clock routing to the PIO clock input.

Pin Information (continued)

Compatibility with OR2C/TxxA Series

The pinouts shown for the OR3Cxx and OR3Txxx devices are consistent with the OR2C/TxxA Series for all devices offered in the same packages. This includes the following pins: VDD, VSS, VDD5 (OR2TxxA Series only), and all configuration pins.

The following restrictions apply:

1. There are two configuration modes supported in the OR2C/TxxA Series that are **not** supported in Series 3: master parallel down and synchronous peripheral modes. The Series 3 FPGAs have two new microprocessor interface (MPI) configuration modes that are unavailable in the OR2C/TxxA Series.
2. There are four pins—one per each device side—that are user I/O in the OR2C/TxxA Series which can only be used as fast dedicated clocks or global inputs in Series 3. These pins are also used to drive the ExpressCLK to the I/O FFs on their given side of the device. These four middle ExpressCLK pins should not be used to connect to a programmable clock manager (PCM). A corner ExpressCLK input should be used instead (see item 3 below). See Table 69 for a list of these pins in each package.
3. There are two other pins that are user I/O in both the OR2C/TxxA and Series 3 but also have optional added functionality. Each of these pins drives the ExpressCLKs on two sides of the device. They also have fast connectivity to the programmable clock manager (PCM). See Table 69 for a list of these pins in each package.

Table 69. Series 3 ExpressCLK Pins

Pin Name/ Package	144-Pin TQFP	208-Pin SQFP/SQFP2	240-Pin SQFP/SQFP2	256-Pin PBGA	352-Pin PBGA	432-Pin EBGA
I-ECKL	15	22	26	K3	N2	R29
I-ECKB	55	80	91	W11	AE14	AH16
I-ECKR	92	131	152	K18	N23	T2
I-ECKT	124	178	207	B11	B14	C15
I/O-SECKLL	33	49	56	W1	AB4	AG29
I/O-SECKUR	111	159	184	A19	A25	D5

Pin	OR3T20 Pad	OR3T30 Pad	OR3T55 Pad	OR3C/T80 Pad	OR3T125 Pad	Function
86	PB8B	PB9B	PB11B	PB13B	PB16D	I/O
87	PB8C	PB9C	PB11C	PB13C	PB17A	I/O
88	PB8D	PB9D	PB11D	PB14A	PB17D	I/O
89	PB9A	PB10A	PB12A	PB14B	PB18A	I/O-HDC
90	PB9B	PB10B	PB12B	PB14D	PB18D	I/O
91	PB9C	PB10C	PB12C	PB15A	PB19A	I/O
92	PB9D	PB10D	PB12D	PB15D	PB19D	I/O
93	VDD	VDD	VDD	VDD	VDD	VDD
94	PB10A	PB11A	PB13A	PB16A	PB20A	I/O-$\overline{\text{LDC}}$
95	PB10B	PB11D	PB13D	PB16D	PB21D	I/O
96	PB10C	PB12A	PB14A	PB17A	PB22A	I/O
97	PB10D	PB12B	PB14D	PB17D	PB23D	I/O
98	PB11A	PB12C	PB15A	PB18A	PB24A	I/O-$\overline{\text{INIT}}$
99	PB11C	PB12D	PB16A	PB19A	PB25A	I/O
100	PB11D	PB13A	PB17A	PB20A	PB26A	I/O
101	PB12A	PB13D	PB18A	PB21D	PB27D	I/O
102	PB12D	PB14D	PB18D	PB22D	PB28D	I/O
103	VSS	VSS	VSS	VSS	VSS	VSS
104	PDONE	PDONE	PDONE	PDONE	PDONE	DONE
105	VSS	VSS	VSS	VSS	VSS	VSS
106	$\overline{\text{PRESETN}}$	$\overline{\text{PRESETN}}$	$\overline{\text{PRESETN}}$	$\overline{\text{PRESETN}}$	$\overline{\text{PRESETN}}$	$\overline{\text{RESET}}$
107	$\overline{\text{PPRGMN}}$	$\overline{\text{PPRGMN}}$	$\overline{\text{PPRGMN}}$	$\overline{\text{PPRGMN}}$	$\overline{\text{PPRGMN}}$	$\overline{\text{PRGM}}$
108	PR12A	PR14A	PR18A	PR22A	PR28A	I/O-M0
109	PR12D	PR13A	PR18D	PR21A	PR27A	I/O
110	PR11A	PR13D	PR17B	PR20A	PR26A	I/O
111	PR11B	PR12A	PR16A	PR19A	PR25A	I/O
112	PR10A	PR11A	PR15D	PR18D	PR22D	I/O-M1
113	PR10B	PR11B	PR14A	PR17A	PR21A	I/O
114	PR10C	PR11C	PR14D	PR17D	PR21D	I/O
115	PR10D	PR11D	PR13A	PR16A	PR20A	I/O
116	VDD	VDD	VDD	VDD	VDD	VDD
117	PR9A	PR10A	PR12A	PR15A	PR19A	I/O-M2
118	PR9B	PR10B	PR12B	PR15D	PR19D	I/O
119	PR9C	PR10C	PR12C	PR14A	PR18A	I/O
120	PR9D	PR10D	PR12D	PR14C	PR18D	I/O
121	PR8A	PR9A	PR11A	PR14D	PR17A	I/O-M3
122	PR8B	PR9B	PR11B	PR13A	PR17D	I/O
123	PR8C	PR9C	PR11C	PR13B	PR16A	I/O
124	PR8D	PR9D	PR11D	PR13D	PR16D	I/O
125	VSS	VSS	VSS	VSS	VSS	VSS
126	PR7A	PR8A	PR10A	PR12A	PR15A	I/O
127	PR7B	PR8B	PR10B	PR12B	PR15B	I/O

Pin	OR3T20 Pad	OR3T30 Pad	OR3T55 Pad	Function
P4	PL10A	PL11A	PL14B	I/O-A13
R3	PL11D	PL12D	PL14A	I/O
T2	PL11C	PL12C	PL15D	I/O
U1	PL11B	PL12B	PL15B	I/O
T3	PL11A	PL12A	PL16D	I/O-A14
U2	—	PL13D	PL17D	I/O
V1	PL12D	PL13C	PL17C	I/O
T4	PL12C	PL13B	PL17B	I/O
U3	—	PL13A	PL17A	I/O
V2	—	PL14D	PL18D	I/O
W1	PL12B	PL14C	PL18C	I/O-SECKLL
V3	—	PL14B	PL18B	I/O
W2	PL12A	PL14A	PL18A	I/O-A15
Y1	PCCLK	PCCLK	PCCLK	CCLK
W3	—	—	—	NC
Y2	PB1A	PB1A	PB1A	I/O-A16
W4	—	PB1C	PB1C	I/O
V4	PB1B	PB1D	PB1D	I/O
U5	PB1C	PB2A	PB2A	I/O
Y3	PB1D	PB2B	PB2B	I/O
Y4	—	PB2C	PB2C	I/O
V5	—	PB2D	PB2D	I/O
W5	PB2A	PB3A	PB3D	I/O-A17
Y5	PB2B	PB3B	PB4D	I/O
V6	PB2C	PB3C	PB5A	I/O
U7	PB2D	PB3D	PB5B	I/O
W6	PB3A	PB4A	PB5D	I/O
Y6	PB3B	PB4B	PB6A	I/O
V7	PB3C	PB4C	PB6B	I/O
W7	PB3D	PB4D	PB6D	I/O
Y7	PB4A	PB5A	PB7A	I/O
V8	PB4B	PB5B	PB7B	I/O
W8	PB4C	PB5C	PB7C	I/O
Y8	PB4D	PB5D	PB7D	I/O
U9	PB5A	PB6A	PB8A	I/O
V9	PB5B	PB6B	PB8B	I/O
W9	PB5C	PB6C	PB8C	I/O
Y9	PB5D	PB6D	PB8D	I/O
W10	PB6A	PB7A	PB9A	I/O
V10	PB6B	PB7B	PB9B	I/O
Y10	PB6C	PB7C	PB9C	I/O
Y11	PB6D	PB7D	PB9D	I/O
W11	PECKB	PECKB	PECKB	I-ECKB
V11	PB7B	PB8B	PB10B	I/O
U11	PB7C	PB8C	PB10C	I/O

Table 74. OR3T55, OR3C/T80, and OR3T125 352-Pin PBGA Pinout

Pin	OR3T55 Pad	OR3C/T80 Pad	OR3T125 Pad	Function
B1	PL1D	PL1D	PL1D	I/O
C2	PL1C	PL1C	PL1C	I/O
C1	PL1B	PL1B	PL1B	I/O
D2	PL1A	PL1A	PL1A	I/O
D3	PL2D	PL2D	PL2D	I/O-A0/$\overline{\text{MPI\_BE0}}$
D1	PL2C	PL2A	PL2A	I/O
E2	PL2B	PL3D	PL3D	I/O
E4	—	PL3B	PL3B	I/O
E3	PL2A	PL3A	PL3A	I/O
E1	PL3D	PL4D	PL4D	I/O
F2	PL3C	PL4C	PL4C	I/O
G4	PL3B	PL4B	PL4B	I/O
F3	PL3A	PL4A	PL5D	I/O
F1	PL4D	PL5D	PL6D	I/O
G2	PL4C	PL5C	PL6C	I/O
G1	PL4B	PL5B	PL6B	I/O
G3	PL4A	PL5A	PL7D	I/O-A1/$\overline{\text{MPI\_BE1}}$
H2	PL5D	PL6D	PL8D	I/O
J4	PL5C	PL6C	PL8C	I/O
H1	PL5B	PL6B	PL8B	I/O
H3	PL5A	PL6A	PL8A	I/O-A2
J2	PL6D	PL7D	PL9D	I/O
J1	PL6C	PL7C	PL9C	I/O
K2	PL6B	PL7B	PL9B	I/O
J3	PL6A	PL7A	PL9A	I/O-A3
K1	PL7D	PL8D	PL10D	I/O
K4	PL7C	PL8A	PL10A	I/O
L2	PL7B	PL9D	PL11D	I/O
K3	PL7A	PL9B	PL11A	I/O-A4
L1	PL8D	PL9A	PL12D	I/O-A5
M2	PL8C	PL10C	PL12A	I/O
M1	PL8B	PL10B	PL13D	I/O
L3	PL8A	PL10A	PL13A	I/O-A6
N2	PECKL	PECKL	PECKL	I-ECKL
M4	PL9C	PL11C	PL14C	I/O
N1	PL9B	PL11B	PL14B	I/O
M3	PL9A	PL11A	PL14A	I/O-A7/MPI_CLK
P2	PL10D	PL12D	PL15D	I/O
P4	PL10C	PL12C	PL15C	I/O
P1	PL10B	PL12B	PL15B	I/O
N3	PL10A	PL12A	PL15A	I/O-A8/MPI_RW
R2	PL11D	PL13D	PL16D	I/O-A9/$\overline{\text{MPI\_ACK}}$
P3	PL11C	PL13B	PL16A	I/O
R1	PL11B	PL13A	PL17D	I/O
T2	PL11A	PL14C	PL17A	I/O-A10/$\overline{\text{MPI\_BI}}$

ψJC

This JEDEC designated parameter correlates the junction temperature to the case temperature. It is generally used to infer the junction temperature while the device is operating in the system. It is not considered a true thermal resistance, and it is defined by:

$$\psi_{JC} = \frac{T_J - T_C}{Q}$$

where T_C is the case temperature at top dead center, T_J is the junction temperature, and Q is the chip power. During the Θ_{JA} measurements described above, besides the other parameters measured, an additional temperature reading, T_C, is made with a thermocouple attached at top-dead-center of the case. ψ_{JC} is also expressed in units of °C/watt.

ΘJC

This is the thermal resistance from junction to case. It is most often used when attaching a heat sink to the top of the package. It is defined by:

$$\Theta_{JC} = \frac{T_J - T_C}{Q}$$

The parameters in this equation have been defined above. However, the measurements are performed with the case of the part pressed against a water-cooled heat sink so as to draw most of the heat generated by the chip out the top of the package. It is this difference in the measurement process that differentiates Θ_{JC} from ψ_{JC}. Θ_{JC} is a true thermal resistance and is expressed in units of °C/watt.

ΘJB

This is the thermal resistance from junction to board (a.k.a. Θ_{JL}). It is defined by:

$$\Theta_{JB} = \frac{T_J - T_B}{Q}$$

where T_B is the temperature of the board adjacent to a lead measured with a thermocouple. The other parameters on the right-hand side have been defined above. This is considered a true thermal resistance, and the measurement is made with a water-cooled heat sink pressed against the board so as to draw most of the heat out of the leads. Note that Θ_{JB} is expressed in units of °C/watt, and that this parameter and the way it is measured is still in JEDEC committee.

Package Outline Diagrams (continued)

240-Pin SQFP2

Dimensions are in millimeters.

DETAIL C (SQFP2 CHIP-UP)

5-3825(F).a