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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	-
Number of Logic Elements/Cells	2592
Total RAM Bits	43008
Number of I/O	171
Number of Gates	80000
Voltage - Supply	3V ~ 3.6V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 70°C (TA)
Package / Case	208-BFQFP
Supplier Device Package	208-PQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/or3t557s208-db

Product Line	Ordering Part Number	Product Status	Reference PCN
OR3T55 (Cont'd)	OR3T557BA256-DB	Active / Orderable	
	OR3T556BA256-DB		
	OR3T556BA256I-DB		
	OR3T557BA352-DB	**Discontinued**	PCN#09-10
	OR3T556BA352-DB		
	OR3T556BA352I-DB		
OR3T80	OR3T807S208-DB	**Discontinued**	PCN#09-10
	OR3T806S208-DB		
	OR3T806S208I-DB		
	OR3T807PS240-DB	**Discontinued**	PCN#06-07
	OR3T806PS240-DB		
	OR3T806PS240I-DB		
	OR3T807BA352-DB	**Discontinued**	PCN#09-10
	OR3T806BA352-DB		
	OR3T806BA352I-DB		
	OR3T807BC432-DB		
	OR3T806BC432-DB		
	OR3T806BC432I-DB		
OR3T125	OR3T1257PS208-DB	**Discontinued**	PCN#06-07
	OR3T1256PS208-DB		
	OR3T1256PS208I-DB		
	OR3T1257PS240-DB		
	OR3T1256PS240-DB		
	OR3T1256PS240I-DB		
	OR3T1257BA352-DB		PCN#09-10
	OR3T1256BA352-DB		
	OR3T1256BA352I-DB		
	OR3T1257BC432-DB		
	OR3T1256BC432-DB		
	OR3T1256BC432I-DB		

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Architecture (continued)

5-4489(F)

Figure 1. OR3T55 Array

Programmable Logic Cells (continued)

BIDI Routing and SLIC Connectivity

The SLIC is connected to the rest of the PLC by the bidirectional (BIDI) routing segments and the PFU output switching segments coming from the PFU output multiplexer. The BIDI routing segments (xBID) are labeled as BL for BIDI-left and BR for BIDI-right. Each set of BR and BL xBID segments is composed of ten bidirectional lines (note that these lines are diagramed as ten input lines to the SLIC and ten output lines from the SLIC that can be used in a mutually exclusive fashion). Because the SLIC is connected directly to the outputs of the PFU, it provides great flexibility in routing via the xBID segments. The PFU routing segments, O[9:0], only connect to their respective line in the SLL, SUL, SUR, and SLR switching segment groups. That is, O9 only connects to SLL9, SUL9, SUR9, and SLR9. The BIDI lines provide the capability to connect to the other member of the routing set. That means, for example, that O9 can be routed to BR8 or BL8. This connectivity can be used as a means to distribute or gather signals on intra-PLC routing without disturbing inter-PLC resources. As described in the Switching Routing Segments subsection, the BIDI routing segments are also used for routes to a diagonally adjacent PFU.

In addition to the intra-PLC connections, the xBID and output switching segments also have connectivity to the x1, x5, and xL inter-PLC routing resources, providing an alternate routing path rather than using PLC xSW segments. These connections also provide a path to the 3-state buffers in the SLIC without encumbering the xSW segments. In this manner, buffering or 3-state control can be added to inter-PLC routing without disturbing local functionality within a PFU.

Control Signal and Fast-Carry Routing

PFU control signal and the fast-carry routing are performed using the FINS structure and several dedicated routing paths. The fast-carry (FC) routing resources consist of a dedicated bidirectional segment between each orthogonal pair of PLCs. This means that a fast-carry can go to or come from each PLC to the right or left, above or below the subject PLC. The FINS structure is used to control the switching of these fast-carry paths between the fast-carry input (FCIN) and fast-carry output (FCOUT) ports of the PFU.

The PFU control inputs (CE, SEL, LSR, ASWE) and CIN can be reached via the FINS by two special routing segments, E1 and E2. The E1 routing segment provides connectivity between all of the xBID routing segments and the FINS. It is unidirectional from the BIDI routing to the FINS. E1 also provides connectivity to the PFU clock input via FINS for a local clock signal. The E2 segment connects the SLIC DEC output to the FINS and to a group of CIPS that provide bidirectional connectivity with all of the BIDI routing segments. This allows the DEC signal to be used in the PFU and/or routed on the BIDI segments. It also allows signals to be routed to the PFU on the xBID segments if the SLIC DEC output is not used.

There is also a dedicated routing segment from the FINS to the SLIC TRI input used for BIDI buffer 3-state control.

Clock Distribution Network (continued)

Clock Distribution in the PLC Array

System Clock (SCLK)

The clock distribution network, or clock spine network, within the PLC array is designed to minimize clock skew while maximizing clock flexibility. Clock flexibility is expressed in two ways: the ease with which a single clock is routed to the entire array, and the capability to provide multiple clocks to the PLC array.

There is one horizontal and one vertical clock spine passing through each PLC. The horizontal clock spine is sourced from the PIC in the same row on either the left- or right-hand side of the array, with the source side (left or right) alternating for each row. The vertical clock spines are similarly sourced from the PICs alternating from the top or bottom of a column. Each clock spine is capable of driving one of the ten xL routing segments that run orthogonal to it within each PLC. Full connectivity to all PFUs is maintained due to the connectivity from the xL lines to the PFU clock signals described in the previous section; however, only an xL line in every other row (column) needs to be driven to allow the given clock signal to be distributed to every PFU. Figure 32 is a high-level diagram of the Series 3 system clock spine network with sample xL line connections for a 4 x 4 array of PLCs.

The clock spine structure previously described provides for complete distribution of a clock from any I/O pin to the entire PLC array by means of a single clock spine and long lines (xL). This distribution system also provides a means to have many different clocks routed to many different and dispersed locations in the PLC array. Each spine can carry a different clock signal, so for the OR3T55 (which has an 18 x 18 array of PLCs, implying nine clock spines per side), 36 input clock signals can be supported using the system clock network.

Fast Clock

Fast clocks are high-speed, low-skew clock spines that originate from the CLKCNTRL special function blocks (described later). There are four fast clock spines—one originating on the middle of each edge of the array. The spines run in the interquad region of the PLC array from their source side of the device to the last row or column on the opposite side of the device. The fast clocks connect to two long lines, xL[8] and xL[9], that run orthogonal to the spine direction in each PLC. These long lines can then be connected to the PFU clock input in the same manner as the general system clocks, and, like the system clock connections, xL lines are only needed in every other row (column) to distribute a clock to every PFU. The limited number of long-line connections and the low skew of the CLKCNTRL source combine to make the fast clocks a very robust, low-skew clock source.

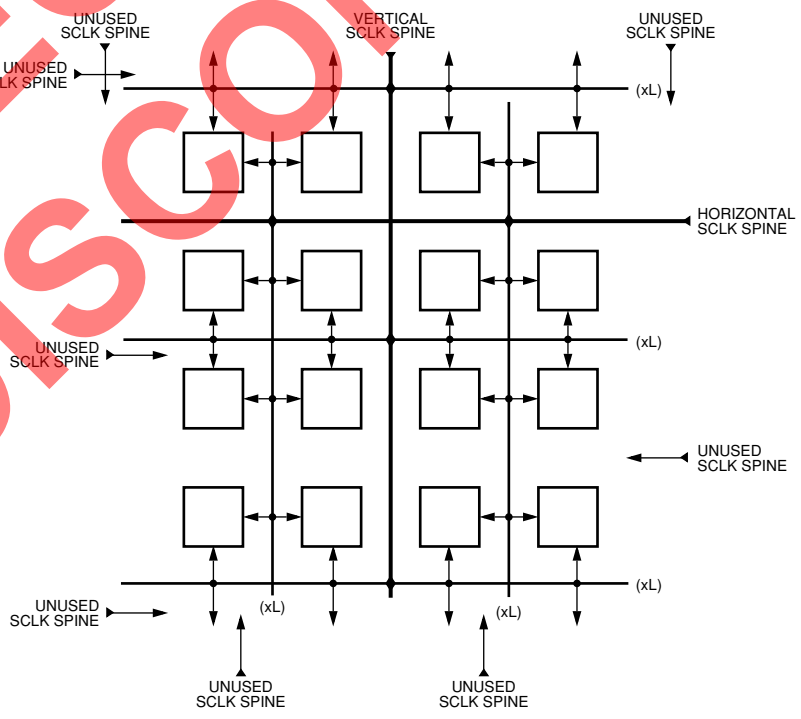

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Figure 32. *ORCA* Series 3 System Clock Distribution Overview

Special Function Blocks (continued)

Boundary-Scan Timing

To ensure race-free operation, data changes on specific clock edges. The TMS and TDI inputs are clocked in on the rising edge of TCK, while changes on TDO occur on the falling edge of TCK. In the execution of an EXTEST instruction, parallel data is output from the BSR to the FPGA pads on the falling edge of TCK. The maximum frequency allowed for TCK is 10 MHz.

Figure 41 shows timing waveforms for an instruction scan operation. The diagram shows the use of TMS to sequence the TAPC through states. The test host (or BSM) changes data on the falling edge of TCK, and it is clocked into the DUT on the rising edge.

Figure 41. Instruction Register Scan Timing Diagram

Microprocessor Interface (MPI)

The Series 3 FPGAs have a dedicated synchronous microprocessor interface function block (see Figure 42). The MPI is programmable to operate with *PowerPC* MPC800 series microprocessors and *Intel* i960** J core processors; see Table 16 and Table 17, respectively, for compatible processors. The MPI implements an 8-bit interface to the host processor (*PowerPC* or *i960*) that can be used for configuration and readback of the FPGA as well as for user-defined data processing and general monitoring of FPGA function. In addition to dedicated-function registers, the microprocessor interface allows for the control of up to 16 user registers (RAM or flip-flops) in the FPGA logic. A synchronous/asynchronous handshake procedure is used to control transactions with user logic in the FPGA array. There is also capability for the FPGA logic to interrupt the host processor either by a hard interrupt or by having the host processor poll the microprocessor interface.

The control portion of the microprocessor interface is available following powerup of the FPGA if the mode pins specify MPI mode, even if the FPGA is not yet configured. The mode pin (M[2:0]) settings can be found in the FPGA Configuration Modes section of this data sheet, and the setup and use of the MPI for configuration is discussed in the MPI Setup and Control subsection. For postconfiguration use, the MPI must be included in the configuration bit stream by using an MPI library element in your design from the *ORCA* macro library, or by setting the MP_USER bit of the MPI configuration control register prior to the start of configuration (MPI registers are discussed later).

* *Intel* and *i960* are registered trademarks of Intel Corporation.

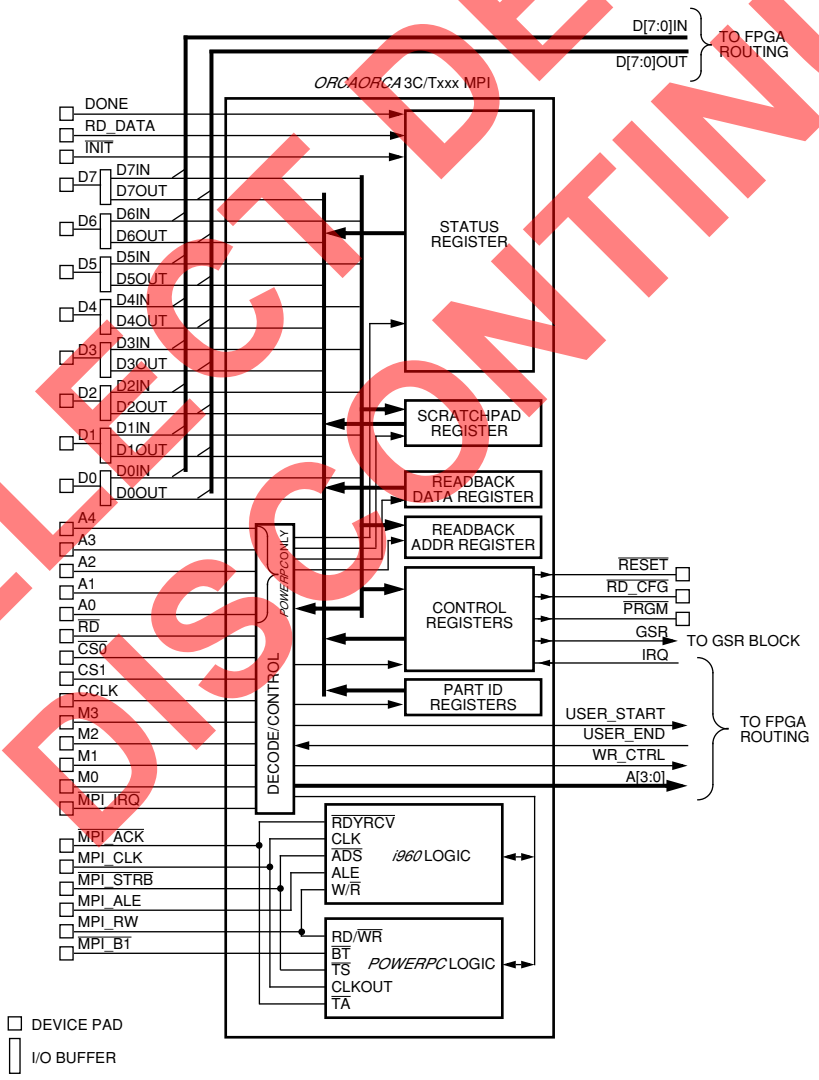

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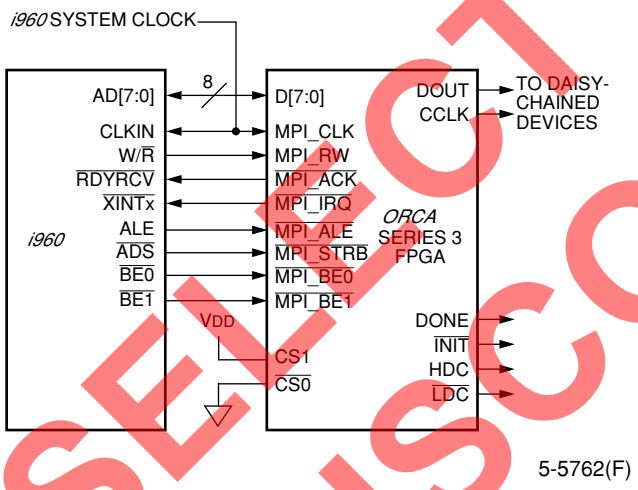
Figure 42. MPI Block Diagram

Microprocessor Interface (MPI) (continued)

i960 System

Figure 44 shows a schematic for connecting the *ORCA* MPI to supported *i960* processors. In the figure, the FPGA is shown as the only peripheral, with the FPGA chip select lines, $\overline{CS0}$ and CS1, tied low and high, respectively. The *i960* address and data are multiplexed onto the same bus. This precludes memory mapping of the FPGA in the *i960* memory space of a multiperipheral system without some form of address latching to capture and hold the address signals to drive the $\overline{CS0}$ and/or CS1 signals. Multiple address signals could also be decoded and latched to drive the $\overline{CS0}$ and/or CS1 signals. If the MPI is not used for FPGA configuration, decoding/latching logic can be implemented internal or external to the FPGA. If logic internal to the FPGA is used, the chip selects must be routed out an output pin and then connected externally to $\overline{CS0}$ and/or CS1. If the MPI is to be used for configuration, any decode/latch logic used must be implemented external to the FPGA since the FPGA logic has not been configured yet.



Note: FPGA shown as only system peripheral with fixed-chip select signals. For multiperipheral systems, address decoding and/or latching can be used to implement chip selects.

Figure 44. *i960*/MPI

The basic flow of a transaction on the *i960*/MPI interface is given below. Pin descriptions are shown in Table 17, and timing is shown in the *ORCA* Timing Characteristics section of this data sheet. For both read and write transactions, the address latch enable (ALE) is set up by the *i960* at the FPGA to the falling edge of the clock. The address, byte enables, chip selects, and read/write (read low, write high) signals are normally set up at the FPGA pins by the *i960* at the next rising edge of the clock. At this same rising clock edge, the *i960* asserts its address/data strobe ($\overline{ADS}$) low. Data is available to the MPI during a write at the rising clock edge of the following clock cycle. The transfer is acknowledged to the *i960* by the low assertion of the ready/recover ($\overline{RDYRCV}$) signal. The same process applies to a read from the MPI except that the read data is expected at the FPGA data pins by the *i960* at the rising edge of the clock when $\overline{RDYRCV}$ is low. The MPI only drives $\overline{RDYRCV}$ low for one clock cycle.

Interrupts can be sent to the *i960* asynchronously to the read/write process. Interrupt requests are sourced by the user-logic in the FPGA. The MPI will assert the request to the *i960* as a direct interrupt signal and/or a pollable bit in the MPI status register (discussed in the MPI Setup and Control section). The MPI will continue to assert the interrupt request until the user-logic deasserts its interrupt request signal.

Table 17. *i960*/MPI Configuration

i960 Signal	*ORCA* Pin Name	MPI I/O	Function
AD[7:0]	D[7:0]	I/O	Multiplexed 5-bit address/ 8-bit data bus. The address appears on D[4:0].
ALE	RDY/RCLK/ $\overline{MPI\_ALE}$	I	Address latch enable used to capture address from AD[4:0] on falling edge of clock.
$\overline{ADS}$	$\overline{RD}$/ $\overline{MPI\_STRB}$	I	Address/data strobe to indicate start of transaction.
—	$\overline{CS0}$	I	Active-low MPI select.
—	CS1	I	Active-high MPI select.
System Clock	A7/ MPI_CLK	I	*i960* system clock. This clock is sourced by the system and not the *i960*.
W/$\overline{R}$	A8/MPI_RW	I	Write (high)/read (low) signal.
$\overline{RDYRCV}$	A9/ $\overline{MPI\_ACK}$	O	Active-low ready/recover signal indicating acknowledgment of the transaction.
Any of $\overline{XINT}$[7:0]	A11/ $\overline{MPI\_IRQ}$	O	Active-low interrupt request signal.
$\overline{BE0}$	A0/ $\overline{MPI\_BE0}$	I	Byte-enable 0 used as address bit 0 in *i960* 8-bit mode.
$\overline{BE1}$	A1/ $\overline{MPI\_BE1}$	I	Byte-enable 1 used as address bit 1 in *i960* 8-bit mode.

Microprocessor Interface (MPI) (continued)

Scratchpad Register

The MPI scratchpad register is an 8-bit read/write register with no defined operation. It may be used for any user-defined function.

Control Register 2

The MPI control register 2 is a read/write register. The host processor writes a control byte to configure the MPI. It is readable by the host processor to verify the status of control bits it had previously written.

Table 21. MPI Control Register 2

Bit #	Bit Name	Description
Bit 0	EN_IRQ_CFG	**Enable $\overline{\text{IRQ}}$ for Configuration Data Request in Daisy-Chain Configuration Mode**. Setting this bit to a 1 prior to configuration enables the $\overline{\text{IRQ}}$ signal to go active when new data is requested for configuration writes or is available for configuration reads to/from the configuration data register. A 0 clears the $\overline{\text{IRQ}}$ enable. This bit is only valid for daisy-chain configuration. Default = 0.
Bit 1	EN_IRQ_ERR	**Enable $\overline{\text{IRQ}}$ for Bit Stream Error**. Setting this bit to a 1 prior to configuration enables the $\overline{\text{IRQ}}$ signal to go active on the occurrence of a bit stream error during configuration. A 0 clears the $\overline{\text{IRQ}}$ enable. This bit only has effect while in configuration mode. Default = 0.
Bit 2	EN_IRQ_USR	**Enable $\overline{\text{IRQ}}$ from the User FPGA Space**. Setting this bit to a 1 allows user-defined circuitry in the FPGA to generate an interrupt to the host processor by sourcing a logic low on the $\overline{\text{UIRQ}}$ signal in the user logic. Default = 0.
Bit 3	MP_DAISY	**MPI Daisy-Chain Output Enable**. Setting this bit to a 1 enables daisy-chain output of the configuration data. See the Configuration section of this data sheet for daisy-chain configuration details. Default = 0.
Bit 4	MP_HOLD_BUS	**Enable Bus Holding During Daisy-Chain Configuration Mode**. Setting this bit to a 1 will cause the MPI to wait until the FPGA configuration logic has serialized a byte of configuration data before acknowledging the transaction. The data is only serialized if the MP_DAISY (bit 3 above) control bit is set to 1. If MP_HOLD_BUS is set to 0, the MPI will immediately acknowledge a configuration data byte transfer. Immediate acknowledgment allows the host processor to perform other tasks during FPGA configuration by polling the MPI status register (or by interrupt) and only write configuration data when the FPGA is ready. Default = 0.
Bit 5	MP_USER	**MPI User Mode Enable**. Setting this bit to a 1 will enable the MPI for user mode operation. MP_USER must be set prior to the FPGA DONE signal going high during configuration. The MPI may also be enabled for user operation via the configuration bit stream. Default = 0.
Bit 6	Reserved	—
Bit 7	Reserved	—

Programmable Clock Manager (PCM) (continued)

Table 31. PCM Control Registers (continued)

Bit #	Function
Bits [5:4]	**ExpressCLK Output Source Selector**. Default is 00. 00: PCM input clock, bypass path through PCM 01: DLL output 10: tapped delay line output 11: divided (DIV2) delay line output
Bits [7:6]	**System Clock Output Source Selector**. Default is 00. 00: PCM input clock, bypass path through PCM 01: DLL output 10: tapped delay line output 11: reserved
Register 7 PCM Control Programming	
Bit 0	**PCM Analog Power Supply Switch**. 1 = power supply on, 0 = power supply off.
Bit 1	**PCM Reset**. A value of 1 resets all PCM logic for PLL and DLL modes.
Bit 2	**DLL Reset**. A value of 1 resets the clock generation logic for DLL mode. No dividers or user registers are affected.
Bits [5:3]	**Reserved**.
Bit 6	**PCM Configuration Operation Enable Bit**. 0 = normal configuration operation. During configuration (DONE = 0), the PCM analog power supply will be off, the PCM output data bus is 3-stated, and the LOCK signal is asserted to logic 0. The PCM will power up when DONE = 1. 1 = PCM operation during configuration. The PCM may be powered up (see bit 0) and begin operation, or continue operation. The setup of the PCM can be performed via the configuration bit stream.
Bit 7	**PCM GSRN Enable Bit**. 0 = normal GSRN operation. 1 = GSRN has no effect on PCM logic, so clock processing will not be interrupted by a chip reset. Default is 0.

Timing Characteristics

Description

To define speed grades, the *ORCA* Series part number designation (see Ordering Information) uses a single-digit number to designate a speed grade. This number is not related to any single ac parameter. Higher numbers indicate a faster set of timing parameters. The actual speed sorting is based on testing the delay in a path consisting of an input buffer, combinatorial delay through all PLCs in a row, and an output buffer. Other tests are then done to verify other delay parameters, such as routing delays, setup times to FFs, etc.

The most accurate timing characteristics are reported by the timing analyzer in the ispLEVER Development System. A timing report provided by the development system after layout divides path delays into logic and routing delays. The timing analyzer can also provide logic delays prior to layout. While this allows routing budget estimates, there is wide variance in routing delays associated with different layouts.

The logic timing parameters noted in the Electrical Characteristics section of this data sheet are the same as those in the design tools. In the PFU timing given in Table 41—Table 48, symbol names are generally a concatenation of the PFU operating mode (as defined in Table 3) and the parameter type. The setup, hold, and propagation delay parameters, defined below, are designated in the symbol name by the SET, HLD, and DEL characters, respectively.

The values given for the parameters are the same as those used during production testing and speed binning of the devices. The junction temperature and supply voltage used to characterize the devices are listed in the delay tables. Actual delays at nominal temperature and voltage for best-case processes can be much better than the values given.

It should be noted that the junction temperature used in the tables is generally 85 °C. The junction temperature for the FPGA depends on the power dissipated by the device, the package thermal characteristics (Θ_{JA}), and the ambient temperature, as calculated in the following equation and as discussed further in the Package Thermal Characteristics section:

$$T_{Jmax} = T_{Amax} + (P \bullet \Theta_{JA})\ ^{\circ}C$$

Note: The user must determine this junction temperature to see if the delays from ispLEVER should be derated based on the following derating tables.

Table 38 and Table 39 provide approximate power supply and junction temperature derating for OR3Cxx commercial and industrial devices. Table 40 provides the same information for the OR3Txxx devices (both commercial and industrial). The delay values in this data sheet and reported by ispLEVER are shown as **1.00** in the tables. The method for determining the maximum junction temperature is defined in the Package Thermal Characteristics section. Taken cumulatively, the range of parameter values for best-case vs. worst-case processing, supply voltage, and junction temperature can approach 3 to 1.

Table 38. Derating for Commercial Devices (OR3Cxx)

TJ (¡C)	Power Supply Voltage		
	4.75 V	5.0 V	5.25 V
0	0.81	0.79	0.77
25	0.85	0.83	0.81
85	**1.00**	0.97	0.95
100	1.05	1.02	1.00
125	1.12	1.09	1.07

Table 39. Derating for Industrial Devices (OR3Cxx)

TJ (¡C)	Power Supply Voltage				
	4.5 V	4.75 V	5.0 V	5.25 V	5.5 V
—40	0.71	0.70	0.68	0.66	0.65
0	0.80	0.78	0.76	0.74	0.73
25	0.84	0.82	0.80	0.78	0.77
85	**1.00**	0.97	0.94	0.93	0.91
100	1.05	1.01	0.99	0.97	0.95
125	1.12	1.09	1.06	1.04	1.02

Table 40. Derating for Commercial/Industrial Devices (OR3Txxx)

TJ (¡C)	Power Supply Voltage		
	3.0 V	3.3 V	3.6 V
—40	0.73	0.66	0.61
0	0.82	0.73	0.68
25	0.87	0.78	0.72
85	**1.00**	0.90	0.83
100	1.04	0.94	0.87
125	1.10	1.00	0.92

Note: The derating tables shown above are for a typical critical path that contains 33% logic delay and 66% routing delay. Since the routing delay derates at a higher rate than the logic delay, paths with more than 66% routing delay will derate at a higher rate than shown in the table. The approximate derating values vs. temperature are 0.26% per °C for logic delay and 0.45% per °C for routing delay. The approximate derating values vs. voltage are 0.13% per mV for both logic and routing delays at 25 °C.

Timing Characteristics (continued)

In addition to supply voltage, process variation, and operating temperature, circuit and process improvements of the *ORCA* Series FPGAs over time will result in significant improvement of the actual performance over those listed for a speed grade. Even though lower speed grades may still be available, the distribution of yield to timing parameters may be several speed grades higher than that designated on a product brand. Design practices need to consider best-case timing parameters (e.g., delays = 0), as well as worst-case timing.

The routing delays are a function of fan-out and the capacitance associated with the CIPs and metal interconnect in the path. The number of logic elements that can be driven (fan-out) by PFUs is unlimited, although the delay to reach a valid logic level can exceed timing requirements. It is difficult to make accurate routing delay estimates prior to design compilation based on fan-out. This is because the CAE software may delete redundant logic inserted by the designer to reduce fan-out, and/or it may also automatically reduce fan-out by net splitting.

The waveform test points are given in the Input/Output Buffer Measurement Conditions section of this data sheet. The timing parameters given in the electrical characteristics tables in this data sheet follow industry practices, and the values they reflect are described below.

Propagation Delay—The time between the specified reference points. The delays provided are the worst case of the tphh and tpll delays for noninverting functions, tplh and tphl for inverting functions, and tphz and tplz for 3-state enable.

Setup Time—The interval immediately preceding the transition of a clock or latch enable signal, during which the data must be stable to ensure it is recognized as the intended value.

Hold Time—The interval immediately following the transition of a clock or latch enable signal, during which the data must be held stable to ensure it is recognized as the intended value.

3-State Enable—The time from when a 3-state control signal becomes active and the output pad reaches the high-impedance state.

PFU Timing

Table 41. Combinatorial PFU Timing Characteristics

OR3Cxx Commercial: V_{DD} = 5.0 V ± 5%, 0 °C < T_A < 70 °C; Industrial: V_{DD} = 5.0 V ± 10%, –40 °C < T_A < +85 °C.
OR3Txxx Commercial: V_{DD} = 3.0 V to 3.6 V, 0 °C < T_A < 70 °C; Industrial: V_{DD} = 3.0 V to 3.6 V, –40 °C < T_A < +85 °C.

Parameter	Symbol	Speed								Unit
		-4		-5		-6		-7		
		Min	Max	Min	Max	Min	Max	Min	Max	
Combinatorial Delays (T_J = +85 °C, V_{DD} = min):										
Four-input Variables (Kz[3:0] to F[z])*	F4_DEL	—	2.34	—	1.80	—	1.32	—	1.05	ns
Five-input Variables (F5[A:D] to F[0, 2, 4, 6])	F5_DEL	—	2.11	—	1.57	—	1.23	—	0.99	ns
Two-level LUT Delay (Kz[3:0] to F w/feedbk)*	SWL2_DEL	—	4.87	—	3.66	—	2.58	—	2.03	ns
Two-level LUT Delay (F5[A:D] to F w/feedbk)	SWL2F5_DEL	—	4.69	—	3.51	—	2.48	—	1.94	ns
Three-level LUT Delay (Kz[3:0] to F w/feedbk)*	SWL3_DEL	—	6.93	—	5.15	—	3.63	—	2.82	ns
Three-level LUT Delay (F5[A:D] to F w/feedbk)	SWL3F5_DEL	—	6.89	—	5.08	—	3.54	—	2.75	ns
C_{IN} to C_{OUT} Delay (logic mode)	CO_DEL	—	3.47	—	2.65	—	1.79	—	1.43	ns

* Four-input variables' (Kz[3:0]) path delays are valid for LUTs in both F4 (four-input LUT) and F5 (five-input LUT) modes.

Timing Characteristics (continued)

PIO Timing

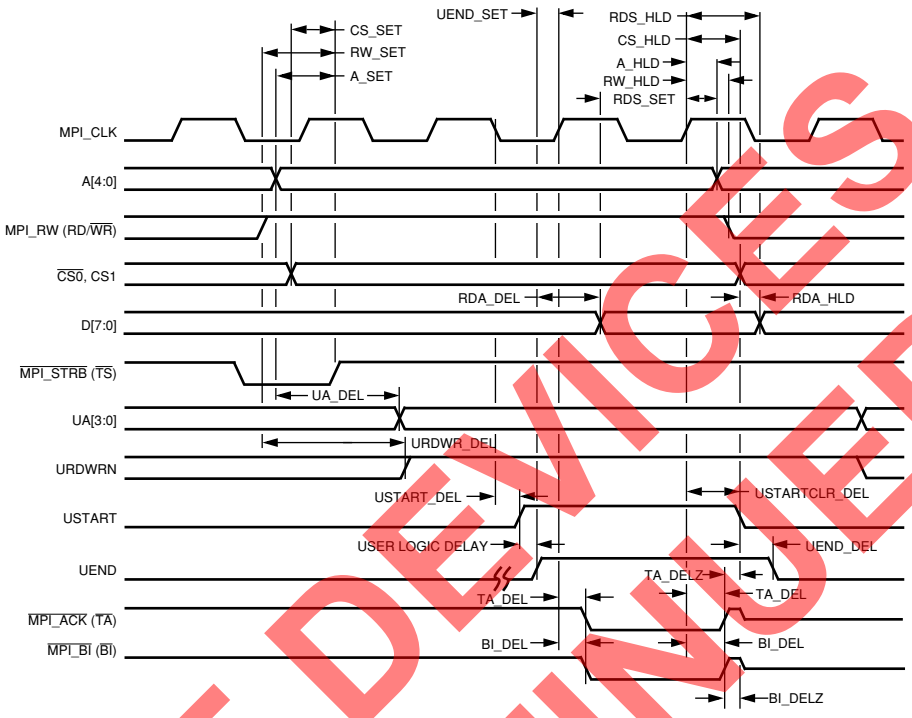
Table 48. Programmable I/O (PIO) Timing Characteristics

OR3Cxx Commercial: V_{DD} = 5.0 V ± 5%, 0 °C < T_A < 70 °C; Industrial: V_{DD} = 5.0 V ± 10%, –40 °C < T_A < +85 °C.
OR3Txxx Commercial: V_{DD} = 3.0 V to 3.6 V, 0 °C < T_A < 70 °C; Industrial: V_{DD} = 3.0 V to 3.6 V, –40 °C < T_A < +85 °C.

Parameter	Symbol	Speed								Unit
		-4		-5		-6		-7		
		Min	Max	Min	Max	Min	Max	Min	Max	
Input Delays (T_J = 85 °C, V_{DD} = min)										
Input Rise Time	IN_RIS	—	500	—	500	—	500	—	500	ns
Input Fall Time	IN_FAL	—	500	—	500	—	500	—	500	ns
PIO Direct Delays:										
Pad to In (pad to CLK IN)	CKIN_DEL	—	1.41	—	1.26	—	0.64	—	0.41	ns
Pad to In (pad to IN1, IN2)	IN_DEL	—	2.16	—	1.87	—	1.28	—	0.90	ns
Pad to In Delayed (pad to IN1, IN2)	IND_DEL	—	9.05	—	7.83	—	6.64	—	7.27	ns
PIO Transparent Latch Delays:										
Pad to In (pad to IN1, IN2)	LATCH_DEL	—	4.11	—	3.25	—	2.52	—	1.82	ns
Pad to In Delayed (pad to IN1, IN2)	LATCHD_DEL	—	10.58	—	9.05	—	7.67	—	7.65	ns
Input Latch/FF Setup Timing:										
Pad to ExpressCLK (fast-capture latch/FF)	INREGE_SET	5.93	—	4.82	—	3.63	—	3.23	—	ns
Pad Delayed to ExpressCLK (fast-capture latch/FF)	INREGED_SET	12.86	—	11.03	—	9.18	—	9.68	—	ns
Pad to Clock (input latch/FF)	INREG_SET	1.62	—	1.42	—	0.71	—	0.50	—	ns
Pad Delayed to Clock (input latch/FF)	INREGD_SET	8.57	—	7.36	—	5.91	—	7.06	—	ns
Clock Enable to Clock (CE to CLK)	INCE_SET	2.03	—	1.64	—	1.29	—	1.00	—	ns
Local Set/Reset (sync) to Clock (LSR to CLK)	INLSR_SET	1.79	—	1.45	—	1.14	—	0.89	—	ns
Input FF/Latch Hold Timing:										
Pad from ExpressCLK (fast-capture latch/FF)	INREGE_HLD	0.00	—	0.00	—	0.00	—	0.00	—	ns
Pad Delayed from ExpressCLK (fast-capture latch/FF)	INREGED_HLD	0.00	—	0.00	—	0.00	—	0.00	—	ns
Pad from Clock (input latch/FF)	INREG_HLD	0.00	—	0.00	—	0.00	—	0.00	—	ns
Pad Delayed from Clock (input latch/FF)	INREGD_HLD	0.00	—	0.00	—	0.00	—	0.00	—	ns
Clock Enable from Clock (CE from CLK)	INCE_HLD	0.00	—	0.00	—	0.00	—	0.00	—	ns
Local Set/Reset (sync) from Clock (LSR from CLK)	INLSR_HLD	0.00	—	0.00	—	0.00	—	0.00	—	ns
Clock-to-in Delay (FF CLK to IN1, IN2)	INREG_DEL	—	4.05	—	3.14	—	2.53	—	2.05	ns
Clock-to-in Delay (latch CLK to IN1, IN2)	INLTCH_DEL	—	4.08	—	3.19	—	2.62	—	2.14	ns
Local S/R (async) to IN (LSR to IN1, IN2)	INLSR_DEL	—	6.11	—	4.76	—	3.81	—	3.17	ns
Local S/R (async) to IN (LSR to IN1, IN2) LatchFF in Latch Mode	INLSRL_DEL	—	5.89	—	4.66	—	3.57	—	2.98	ns
Global S/R to In (GSRN to IN1, IN2)	INGSR_DEL	—	5.38	—	4.22	—	3.44	—	2.88	ns

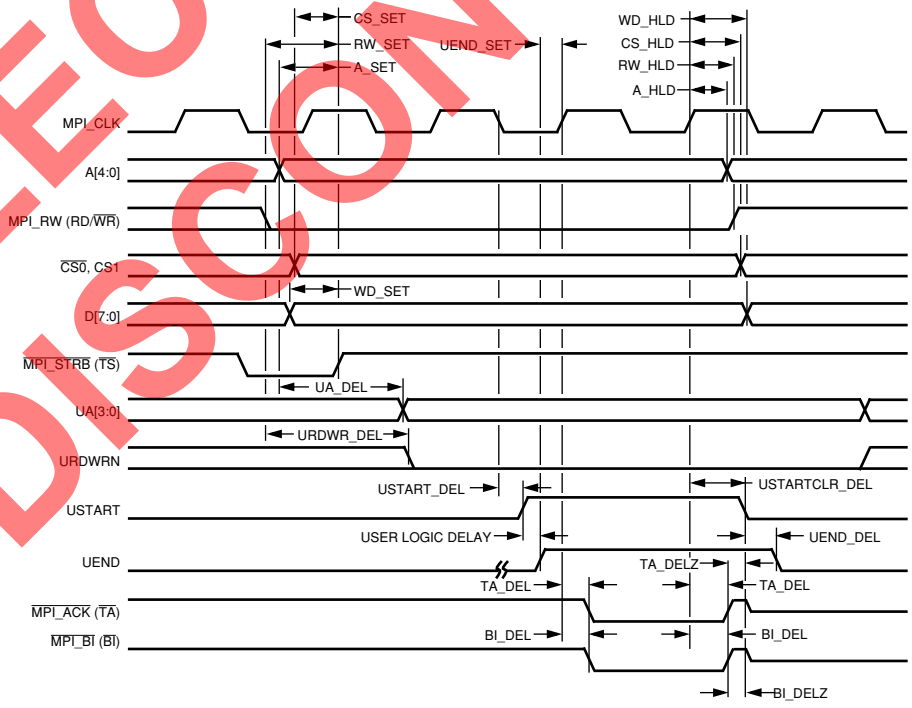
Note: The delays for all input buffers assume an input rise/fall time of <1 V/ns.

Timing Characteristics (continued)



5-5832(F)

Figure 67. MPI *PowerPC* User Space Read Timing



5-5840(F)

Figure 68. MPI *PowerPC* User Space Write Timing

Timing Characteristics (continued)

Clock Timing

Table 52. ExpressCLK (ECLK) and Fast Clock (FCLK) Timing Characteristics

OR3Cxx Commercial: V_{DD} = 5.0 V ± 5%, 0 °C < T_A < 70 °C; Industrial: V_{DD} = 5.0 V ± 10%, –40 °C < T_A < +85 °C.
OR3Txxx Commercial: V_{DD} = 3.0 V to 3.6 V, 0 °C < T_A < 70 °C; Industrial: V_{DD} = 3.0 V to 3.6 V, –40 °C < T_A < +85 °C.

Device (T_J = 85 °C, V_{DD} = min)	Symbol	Speed								Unit
		-4		-5		-6		-7		
		Min	Max	Min	Max	Min	Max	Min	Max	
Clock Control Timing Delay Through CLKCNTRL (input from corner)	ECLKC_DEL	0.31	—	0.31	—	0.31	—	0.31	—	ns
Delay Through CLKCNTRL (input from internal clock controller PAD)	ECLKM_DEL	1.54	—	1.17	—	1.00	—	0.92	—	ns
Clock Shutoff Timing:										
Setup from Middle ECLK (shut off to CLK)	OFFM_SET	0.77	—	0.51	—	0.44	—	0.41	—	ns
Hold from Middle ECLK (shut off from CLK)	OFFM_HLD	0.00	—	0.00	—	0.00	—	0.00	—	ns
Setup from Corner ECLK (shut off to CLK)	OFFC_SET	0.77	—	0.51	—	0.44	—	0.41	—	ns
Hold from Corner ECLK (shut off from CLK)	OFFC_HLD	0.00	—	0.00	—	0.00	—	0.00	—	ns
ECLK Delay (middle pad):	ECLKM_DEL									
OR3T20		—	—	—	2.56	—	2.05	—	1.78	ns
OR3T30		—	—	—	2.62	—	2.08	—	1.80	ns
OR3T55		—	3.50	—	2.74	—	2.13	—	1.85	ns
OR3C/T80		—	3.67	—	2.86	—	2.19	—	1.90	ns
OR3T125		—	—	—	3.06	—	2.29	—	1.98	ns
ECLK Delay (corner pad):	ECLKC_DEL									
OR3T20		—	—	—	4.48	—	3.85	—	3.36	ns
OR3T30		—	—	—	4.53	—	3.97	—	3.47	ns
OR3T55		—	5.47	—	4.64	—	4.22	—	3.69	ns
OR3C/T80		—	5.64	—	4.77	—	4.47	—	3.92	ns
OR3T125		—	—	—	4.96	—	4.85	—	4.27	ns
FCLK Delay (middle pad):	FCLKM_DEL									
OR3T20		—	—	—	5.91	—	4.59	—	3.81	ns
OR3T30		—	—	—	6.12	—	4.66	—	3.89	ns
OR3T55		—	8.24	—	6.59	—	4.83	—	4.06	ns
OR3C/T80		—	8.87	—	7.11	—	5.01	—	4.26	ns
OR3T125		—	—	—	7.98	—	5.33	—	4.59	ns
FCLK Delay (corner pad):	FCLKC_DEL									
OR3T20		—	—	—	7.88	—	6.41	—	5.40	ns
OR3T30		—	—	—	8.11	—	6.58	—	5.58	ns
OR3T55		—	10.34	—	8.60	—	6.95	—	5.94	ns
OR3C/T80		—	11.01	—	9.15	—	7.34	—	6.33	ns
OR3T125		—	—	—	10.07	—	7.96	—	6.94	ns

Notes:
The ECLK delays are to all of the PICs on one side of the device for middle pin input, or two sides of the device for corner pin input. The delay includes both the input buffer delay and the clock routing to the PIC clock input.

The FCLK delays are for a fully routed clock tree that uses the ExpressCLK input into the fast clock network. It includes both the input buffer delay and the clock routing to the PFU CLK input. The delay will be reduced if any of the clock branches are not used.

Timing Characteristics (continued)

Table 53. General-Purpose Clock Timing Characteristics (Internally Generated Clock)

OR3Cxx Commercial: V_{DD} = 5.0 V ± 5%, 0 °C < T_A < 70 °C; Industrial: V_{DD} = 5.0 V ± 10%, –40 °C < T_A < +85 °C.
OR3Txxx Commercial: V_{DD} = 3.0 V to 3.6 V, 0 °C < T_A < 70 °C; Industrial: V_{DD} = 3.0 V to 3.6 V, –40 °C < T_A < +85 °C.

Device (T_J = 85 °C, V_{DD} = min)	Symbol	Speed								Unit
		-4		-5		-6		-7		
		Min	Max	Min	Max	Min	Max	Min	Max	
OR3T20	CLK_DEL	—	—	—	4.22	—	3.46	—	2.84	ns
OR3T30	CLK_DEL	—	—	—	4.29	—	3.48	—	2.87	ns
OR3T55	CLK_DEL	—	5.34	—	4.41	—	3.53	—	2.93	ns
OR3C/T80	CLK_DEL	—	5.49	—	4.52	—	3.57	—	2.98	ns
OR3T125	CLK_DEL	—	—	—	4.80	—	3.71	—	3.13	ns

Notes:
This table represents the delay for an internally generated clock from the clock tree input in one of the four middle PICs (using pSW routing) on any side of the device which is then distributed to the PFU/PIO clock inputs. If the clock tree input used is located at any other PIC, see the results reported by ispLEVER.

This clock delay is for a fully routed clock tree that uses the general clock network. The delay will be reduced if any of the clock branches are not used. See pin-to-pin timing in Table 56 for clock delays of clocks input on general I/O pins.

Timing Characteristics (continued)

Configuration Timing

Table 60. General Configuration Mode Timing Characteristics

OR3Cxx Commercial: V_{DD} = 5.0 V ± 5%, 0 °C < T_A < 70 °C; Industrial: V_{DD} = 5.0 V ± 10%, –40 °C < T_A < +85 °C.
OR3Txxx Commercial: V_{DD} = 3.0 V to 3.6 V, 0 °C < T_A < 70 °C; Industrial: V_{DD} = 3.0 V to 3.6 V, –40 °C < T_A < +85 °C.

Parameter	Symbol	Min	Max	Unit
All Configuration Modes				
M[3:0] Setup Time to $\overline{INIT}$ High	TSMODE	0.00	—	ns
M[3:0] Hold Time from $\overline{INIT}$ High	THMODE	600.00	—	ns
$\overline{RESET}$ Pulse Width Low to Start Reconfiguration	TRW	50.00	—	ns
$\overline{PRGM}$ Pulse Width Low to Start Reconfiguration	TPGW	50.00	—	ns
Master and Asynchronous Peripheral Modes				
Power-on Reset Delay	TPO	15.70	52.40	ms
CCLK Period (M3 = 0)	TCCLK	60.00	200.00	ns
(M3 = 1)		480.00	1600.00	ns
Configuration Latency (autoincrement mode):	TCL			
OR3T20 (M3 = 0)		11.50	38.40*	ms
(M3 = 1)		92.10	307.00*	ms
OR3T30 (M3 = 0)		15.10	50.40*	ms
(M3 = 1)		121.00	403.30*	ms
OR3T55 (M3 = 0)		23.20	77.40*	ms
(M3 = 1)		185.00	619.00*	ms
OR3C/T80 (M3 = 0)		33.70	113.00*	ms
(M3 = 1)		270.00	900.00*	ms
OR3T125 (M3 = 0)		52.30	175.00*	ms
(M3 = 1)		418.00	1395.00*	ms
Microprocessor (MPI) Mode				
Power-on Reset Delay	TPO	15.70	52.40	ms
Configuration Latency (autoincrement mode):	TCL			
OR3T20		27413	—	write cycles
OR3T30		35445	—	write cycles
OR3T55		53341	—	write cycles
OR3C/T80		76317	—	write cycles
OR3T125		116581	—	write cycles
Partial Reconfiguration (explicit mode):	TPR			
OR3T20		32	—	write cycles
OR3T30		36	—	write cycles
OR3T55		43	—	write cycles
OR3C/T80		51	—	write cycles
OR3T125		62	—	write cycles
Slave Serial Mode				
Power-on Reset Delay	TPO	3.90	13.10	ms
CCLK Period	TCCLK			
OR3Cxx		40	—	ns
OR3Txxx		15	—	ns
Configuration Latency (autoincrement mode):	TCL			
OR3T20		2.80	—	ms
OR3T30		3.80	—	ms
OR3T55		5.80	—	ms
OR3C80		22.50	—	ms
OR3T80		8.40	—	ms
OR3T125		13.09	—	ms

* Not applicable to asynchronous peripheral mode.

Pin Information (continued)

Table 67. Pin Descriptions (continued)

Symbol	I/O	Description
Special-Purpose Pins (continued)		
$\overline{CS0}$, CS1	I	$\overline{CS0}$ and CS1 are used in the asynchronous peripheral, slave parallel, and microprocessor configuration modes. The FPGA is selected when $\overline{CS0}$ is low and CS1 is high. During configuration, a pull-up is enabled.
	I/O	After configuration, these pins are user-programmable I/O pins (see Note).
$\overline{RD}$/ $\overline{MPI\_STRB}$	I	$\overline{RD}$ is used in the asynchronous peripheral configuration mode. A low on $\overline{RD}$ changes D7 into a status output. As a status indication, a high indicates ready, and a low indicates busy. $\overline{WR}$ and $\overline{RD}$ should not be used simultaneously. If they are, the write strobe overrides.
	I	This pin is also used as the microprocessor interface (MPI) data transfer strobe. For *PowerPC*, it is the transfer start (TS). For *i960*, it is the address/data strobe ($\overline{ADS}$).
	I/O	After configuration, if the MPI is not used, this pin is a user-programmable I/O pin (see Note).
$\overline{WR}$	I	$\overline{WR}$ is used in the asynchronous peripheral configuration mode. When the FPGA is selected, a low on the write strobe, $\overline{WR}$, loads the data on D[7:0] inputs into an internal data buffer. $\overline{WR}$ and $\overline{RD}$ should not be used simultaneously. If they are, the write strobe overrides.
	I/O	After configuration, this pin is a user-programmable I/O pin (see Note).
A[17:0]	O	During master parallel configuration mode, A[17:0] address the configuration EPROM. In microprocessor interface (MPI) mode, many of the A[n] pins have alternate uses as described below. See the Special Function Blocks section for more MPI information. During configuration, if not in master parallel or an MPI configuration mode, these pins are 3-stated with a pull-up enabled.
	I/O	After configuration, the pins are user-programmable I/O pins (see Note).

Note: The FPGA States of Operation section contains more information on how to control these signals during start-up. The timing of DONE release is controlled by one set of bit stream options, and the timing of the simultaneous release of all other configuration pins (and the activation of all user I/Os) is controlled by a second set of options.

Table 70. OR3T20 144-Pin TQFP Pinout

Pin	OR3T20 Pad	Function
1	VDD	VDD
2	VSS	VSS
3	PL1A	I/O-A0/$\overline{\text{MPI\_BE0}}$
4	PL2D	I/O
5	PL2A	I/O-A1/$\overline{\text{MPI\_BE1}}$
6	PL3D	I/O-A2
7	PL3A	I/O-A3
8	PL4D	I/O
9	PL4C	I/O
10	PL4A	I/O-A4
11	PL5D	I/O-A5
12	PL5C	I/O
13	PL5A	I/O-A6
14	VSS	VSS
15	PECKL	I-ECKL
16	PL6C	I/O
17	PL6A	I/O-A7/MPI_CLK
18	VDD	VDD
19	PL7D	I/O
20	PL7C	I/O
21	PL7A	I/O-A8/MPI_RW
22	VSS	VSS
23	PL8D	I/O-A9/$\overline{\text{MPI\_ACK}}$
24	PL8A	I/O-A10/$\overline{\text{MPI\_BI}}$
25	PL9D	I/O
26	PL9C	I/O
27	PL9A	I/O-A11/$\overline{\text{MPI\_IRQ}}$
28	PL10D	I/O-A12
29	PL10C	I/O
30	PL10A	I/O-A13
31	PL11A	I/O-A14
32	PL12D	I/O
33	PL12B	I/O-SECKLL
34	PL12A	I/O-A15
35	VSS	VSS
36	PCCLK	CCLK
37	VDD	VDD
38	VSS	VSS
39	PB1A	I/O-A16
40	PB1D	I/O
41	PB2A	I/O-A17
42	PB3A	I/O

Pin	OR3C/T80 Pad	OR3T125 Pad	Function
B19	PT9B	PT11D	I/O
D18	PT9C	PT12A	I/O-D0/DIN
A19	PT9D	PT12C	I/O
C18	PT10A	PT12D	I/O
B18	PT10B	PT13A	I/O
A18	PT10C	PT13C	I/O
C17	PT10D	PT13D	I/O-D1
B17	PT11A	PT14A	I/O-D2
A17	PT11B	PT14B	I/O
B16	PT11C	PT14C	I/O
D16	PT11D	PT14D	I/O
C16	PT12A	PT15A	I/O-D3
A15	PT12B	PT15B	I/O
B15	PT12C	PT15C	I/O
C15	PECKT	PECKT	I-ECKT
A14	PT13A	PT16A	I/O-D4
B14	PT13B	PT16B	I/O
C14	PT13C	PT16D	I/O
A13	PT13D	PT17A	I/O
D14	PT14A	PT17B	I/O
B13	PT14B	PT17D	I/O
C13	PT14C	PT18A	I/O-D5
B12	PT14D	PT18B	I/O
D13	PT15A	PT18D	I/O
C12	PT15B	PT19A	I/O
A11	PT15D	PT19D	I/O
B11	PT16A	PT20A	I/O
D12	PT16B	PT20D	I/O-D6
C11	PT16C	PT21A	I/O
A10	PT16D	PT21D	I/O
B10	PT17A	PT22D	I/O
C10	PT17B	PT23B	I/O
A9	PT17C	PT23C	I/O
B9	PT17D	PT23D	I/O
D10	PT18A	PT24A	I/O
C9	PT18B	PT24B	I/O
B8	PT18C	PT24C	I/O
C8	PT18D	PT24D	I/O-D7
D9	PT19A	PT25A	I/O
A7	PT19B	PT25B	I/O
B7	PT19C	PT25C	I/O
C7	PT19D	PT25D	I/O
D8	PT20A	PT26A	I/O
A6	PT20B	PT26B	I/O
B6	PT20C	PT26C	I/O
C6	PT20D	PT26D	I/O
A5	PT21A	PT27A	I/O-RDY/RCLK/MPI_ALE
B5	PT21B	PT27B	I/O
C5	PT21C	PT27C	I/O
D6	PT21D	PT27D	I/O

Pin	OR3C/T80 Pad	OR3T125 Pad	Function
A4	PT22A	PT28A	I/O
B4	PT22B	PT28B	I/O
C4	PT22C	PT28C	I/O
D5	PT22D	PT28D	I/O-SECKUR
A12	VSS	VSS	VSS
A16	VSS	VSS	VSS
A2	VSS	VSS	VSS
A20	VSS	VSS	VSS
A24	VSS	VSS	VSS
A29	VSS	VSS	VSS
A3	VSS	VSS	VSS
A30	VSS	VSS	VSS
A8	VSS	VSS	VSS
AD1	VSS	VSS	VSS
AD31	VSS	VSS	VSS
AJ1	VSS	VSS	VSS
AJ2	VSS	VSS	VSS
AJ30	VSS	VSS	VSS
AJ31	VSS	VSS	VSS
AK1	VSS	VSS	VSS
AK29	VSS	VSS	VSS
AK3	VSS	VSS	VSS
AK31	VSS	VSS	VSS
AL12	VSS	VSS	VSS
AL16	VSS	VSS	VSS
AL2	VSS	VSS	VSS
AL20	VSS	VSS	VSS
AL24	VSS	VSS	VSS
AL29	VSS	VSS	VSS
AL3	VSS	VSS	VSS
AL30	VSS	VSS	VSS
AL8	VSS	VSS	VSS
B1	VSS	VSS	VSS
B29	VSS	VSS	VSS
B3	VSS	VSS	VSS
B31	VSS	VSS	VSS
C1	VSS	VSS	VSS
C2	VSS	VSS	VSS
C30	VSS	VSS	VSS
C31	VSS	VSS	VSS
H1	VSS	VSS	VSS
H31	VSS	VSS	VSS
M1	VSS	VSS	VSS
M31	VSS	VSS	VSS
T1	VSS	VSS	VSS
T31	VSS	VSS	VSS
Y1	VSS	VSS	VSS
Y31	VSS	VSS	VSS
A1	VDD	VDD	VDD
A31	VDD	VDD	VDD

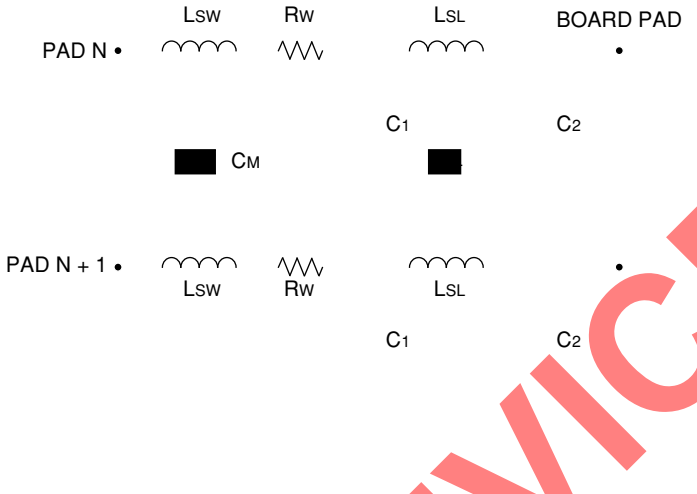


Figure 104. Package Parasitics

Package Outline Diagrams

Terms and Definitions

Basic Size (BSC): The basic size of a dimension is the size from which the limits for that dimension are derived by the application of the allowance and the tolerance.

Design Size: The design size of a dimension is the actual size of the design, including an allowance for fit and tolerance.

Typical (TYP): When specified after a dimension, this indicates the repeated design size if a tolerance is specified or repeated basic size if a tolerance is not specified.

Reference (REF): The reference dimension is an untoleranced dimension used for informational purposes only. It is a repeated dimension or one that can be derived from other values in the drawing.

Minimum (MIN) or Maximum (MAX): Indicates the minimum or maximum allowable size of a dimension.