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Details

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Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	40 MIPs
Connectivity	CANbus, I ² C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, Motor Control PWM, POR, PWM, QEI, WDT
Number of I/O	85
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 24x10/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TQFP
Supplier Device Package	100-TQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33fj128mc510a-e-pt

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1.0 DEVICE OVERVIEW

- Note 1: This data sheet summarizes the features of the dsPIC33FJXXXMCX06A/X08A/ X10A family of devices. However, it is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the *"dsPIC33F/PIC24H Family Reference Manual"*. Please see the Microchip web site (www.microchip.com) for the latest dsPIC33F/PIC24H Family Reference Manual sections.
 - 2: Some registers and associated bits described in this section may not be available on all devices. Refer to Section 4.0 "Memory Organization" in this data sheet for device-specific register and bit information.

This document contains device-specific information for the following devices:

- dsPIC33FJ64MC506A
- dsPIC33FJ64MC508A
- dsPIC33FJ64MC510A
- dsPIC33FJ64MC706A
- dsPIC33FJ64MC710A
- dsPIC33FJ128MC506A
- dsPIC33FJ128MC510A
- dsPIC33FJ128MC706A
- dsPIC33FJ128MC708A
- dsPIC33FJ128MC710A
- dsPIC33FJ256MC510A
- dsPIC33FJ256MC710A

The dsPIC33FJXXXMCX06A/X08A/X10A includes devices with a wide range of pin counts (64, 80 and 100), different program memory sizes (64 Kbytes, 128 Kbytes and 256 Kbytes) and different RAM sizes (8 Kbytes, 16 Kbytes and 30 Kbytes).

These features make this family suitable for a wide variety of high-performance, digital signal control applications. The devices are pin compatible with the PIC24H family of devices, and also share a very high degree of compatibility with the dsPIC30F family devices. This allows easy migration between device families as may be necessitated by the specific functionality, computational resource and system cost requirements of the application.

The dsPIC33FJXXXMCX06A/X08A/X10A family of devices employs a powerful 16-bit architecture that seamlessly integrates the control features of a Microcontroller (MCU) with the computational capabilities of a Digital Signal Processor (DSP). The resulting functionality is ideal for applications that rely on high-speed, repetitive computations, as well as control.

The DSP engine, dual 40-bit accumulators, hardware support for division operations, barrel shifter, 17 x 17 multiplier, a large array of 16-bit working registers and a wide variety of data addressing modes, together, the dsPIC33FJXXXMCX06A/X08A/X10A provide Central Processing Unit (CPU) with extensive mathematical processing capability. Flexible and deterministic interrupt handling, coupled with a powerful array of peripherals, renders the dsPIC33FJXXXMCX06A/X08A/X10A devices suitable for control applications. Further, Direct Memory Access (DMA) enables overhead-free transfer of data between several peripherals and a dedicated DMA RAM. Reliable, field programmable Flash program memory ensures scalability of applications that use dsPIC33FJXXXMCX06A/X08A/X10A devices.



	-/.																	
SFR Name	SFR Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
IC1BUF	0140	Input 1 Capture Register												xxxx				
IC1CON	0142	_	_	ICSIDL	_	_	_	_	_	ICTMR	ICI<	1:0>	ICOV	ICBNE		ICM<2:0>		0000
IC2BUF	0144		Input 2 Capture Register												xxxx			
IC2CON	0146	_	_	ICSIDL	_	_	_	_	_	ICTMR	ICI<	1:0>	ICOV	ICBNE		ICM<2:0>		0000
IC3BUF	0148	Input 3 Capture Register												xxxx				
IC3CON	014A	_	—	ICSIDL	—	—	_	—	_	ICTMR	ICI<	1:0>	ICOV	ICBNE		ICM<2:0>		0000
IC4BUF	014C								Input 4 Ca	pture Regis	ter							xxxx
IC4CON	014E	—	—	ICSIDL	—	—	_	_	_	ICTMR	ICI<	1:0>	ICOV	ICBNE		ICM<2:0>		0000
IC5BUF	0150								Input 5 Ca	pture Regis	ter							xxxx
IC5CON	0152	—	—	ICSIDL	—	—	_	_	_	ICTMR	ICI<	1:0>	ICOV	ICBNE		ICM<2:0>		0000
IC6BUF	0154								Input 6 Ca	pture Regis	ter							xxxx
IC6CON	0156	—	—	ICSIDL	—	—	_	_	_	ICTMR	ICI<	1:0>	ICOV	ICBNE		ICM<2:0>		0000
IC7BUF	0158								Input 7 Ca	pture Regis	ter							xxxx
IC7CON	015A	—	—	ICSIDL	—	—	_	_	_	ICTMR	ICI<	1:0>	ICOV	ICBNE		ICM<2:0>		0000
IC8BUF	015C								Input 8 Ca	pture Regis	ter							xxxx
IC8CON	015E	_	_	ICSIDL	—	_	_	_	_	ICTMR	ICI<	1:0>	ICOV	ICBNE		ICM<2:0>		0000

TABLE 4-7: INPUT CAPTURE REGISTER MAP

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-22: ECAN1 REGISTER MAP WHEN WIN (C1CTRL<0>) = 1

File Name	Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
	0400- 041E		See definition when WIN = x															
C1BUFPNT1	0420		F3BP<3:0> F2BP<3:0>								F1BP	<3:0>			F0BP	<3:0>		0000
C1BUFPNT2	0422		F7BF	P<3:0>			F6BF	><3:0>			F5BP	<3:0>			F4BP	<3:0>		0000
C1BUFPNT3	0424		F11B	P<3:0>			F10B	P<3:0>			F9BP	<3:0>			F8BP	<3:0>	0000	
C1BUFPNT4	0426		F15B	P<3:0>			F14B	P<3:0>			F13BF	P<3:0>			F12BF	<3:0>		0000
C1RXM0SID	0430				SID<	:10:3>					SID<2:0>		—	MIDE		EID<1	17:16>	xxxx
C1RXM0EID	0432				EID<	:15:8>							EID<	7:0>				xxxx
C1RXM1SID	0434				SID<	:10:3>					SID<2:0>		—	MIDE	_	EID<1	17:16>	xxxx
C1RXM1EID	0436				EID<	:15:8>							EID<	7:0>		_		xxxx
C1RXM2SID	0438				SID<	:10:3>					SID<2:0>		—	MIDE	_	EID<1	17:16>	xxxx
C1RXM2EID	043A				EID<	:15:8>							EID<	7:0>				xxxx
C1RXF0SID	0440				SID<	:10:3>					SID<2:0>		—	EXIDE	_	EID<1	17:16>	xxxx
C1RXF0EID	0442				EID<	:15:8>				EID<7:0>						xxxx		
C1RXF1SID	0444				SID<	:10:3>					SID<2:0>		—	EXIDE		EID<1	17:16>	xxxx
C1RXF1EID	0446				EID<	:15:8>							EID<	7:0>				xxxx
C1RXF2SID	0448				SID<	:10:3>					SID<2:0>		—	EXIDE		EID<1	17:16>	xxxx
C1RXF2EID	044A				EID<	:15:8>							EID<	7:0>				xxxx
C1RXF3SID	044C				SID<	:10:3>					SID<2:0>		—	EXIDE		EID<1	17:16>	xxxx
C1RXF3EID	044E				EID≤	:15:8>				EID<7:0>							xxxx	
C1RXF4SID	0450				SID<	:10:3>				SID<2:0> — EXIDE — EID<				EID<1	17:16>	xxxx		
C1RXF4EID	0452				EID<	:15:8>				EID<7:0>							xxxx	
C1RXF5SID	0454				SID<	:10:3>					SID<2:0>		—	EXIDE	_	EID<1	17:16>	xxxx
C1RXF5EID	0456				EID<	:15:8>							EID<	7:0>				xxxx
C1RXF6SID	0458				SID<	:10:3>					SID<2:0>		—	EXIDE	_	EID<1	17:16>	xxxx
C1RXF6EID	045A				EID<	:15:8>							EID<	7:0>				xxxx
C1RXF7SID	045C				SID<	:10:3>					SID<2:0>		—	EXIDE		EID<1	17:16>	xxxx
C1RXF7EID	045E				EID<	:15:8>							EID<	7:0>				xxxx
C1RXF8SID	0460				SID<	:10:3>					SID<2:0>		—	EXIDE	_	EID<1	17:16>	xxxx
C1RXF8EID	0462				EID<	:15:8>							EID<	7:0>				xxxx
C1RXF9SID	0464				SID<	:10:3>					SID<2:0>		—	EXIDE	_	EID<1	17:16>	xxxx
C1RXF9EID	0466				EID<	:15:8>							EID<	7:0>				xxxx
C1RXF10SID	0468				SID<	:10:3>					SID<2:0>		—	EXIDE	—	EID<1	17:16>	xxxx
C1RXF10EID	046A		EID<15:8>								EID<7:0>						xxxx	

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-22:	ECAN1 REGISTER MAP WHEN WIN (C1CTRL<0>) = 1 (CONTINUED)
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File Name	Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
C1RXF11SID	046C		SID<10:3>								SID<2:0>		_	EXIDE	—	EID<1	7:16>	xxxx
C1RXF11EID	046E				EID<	:15:8>				EID<7:0>								xxxx
C1RXF12SID	0470		SID<10:3>								SID<2:0>		_	EXIDE	_	EID<1	7:16>	xxxx
C1RXF12EID	0472				EID<	:15:8>				EID<7:0>							xxxx	
C1RXF13SID	0474				SID<	:10:3>					SID<2:0>		_	EXIDE	_	EID<1	7:16>	xxxx
C1RXF13EID	0476				EID<	:15:8>				EID<7:0>							xxxx	
C1RXF14SID	0478				SID<	:10:3>					SID<2:0>		_	EXIDE	_	EID<1	7:16>	xxxx
C1RXF14EID	047A				EID<	:15:8>							EID<	7:0>				xxxx
C1RXF15SID	047C		SID<10:3>						SID<2:0>		_	EXIDE	_	EID<1	7:16>	xxxx		
C1RXF15EID	047E				EID<	:15:8>				EID<7:0>							xxxx	

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Addressing Mode	Description
File Register Direct	The address of the file register is specified explicitly.
Register Direct	The contents of a register are accessed directly.
Register Indirect	The contents of Wn forms the EA.
Register Indirect Post-Modified	The contents of Wn forms the EA. Wn is post-modified (incremented or decremented) by a constant value.
Register Indirect Pre-Modified	Wn is pre-modified (incremented or decremented) by a signed constant value to form the EA.
Register Indirect with Register Offset	The sum of Wn and Wb forms the EA.
Register Indirect with Literal Offset	The sum of Wn and a literal forms the EA.

TABLE 4-36: FUNDAMENTAL ADDRESSING MODES SUPPORTED

4.3.3 MOVE AND ACCUMULATOR INSTRUCTIONS

Move instructions and the DSP accumulator class of instructions provide a greater degree of addressing flexibility than other instructions. In addition to the Addressing modes supported by most MCU instructions, move and accumulator instructions also support Register Indirect with Register Offset Addressing mode, also referred to as Register Indexed mode.

Note:	For the MOV instructions, the addressing mode specified in the instruction can differ										
	for the source and destination EA										
	IOI THE SOULCE AND DESTINATION EA.										
	However, the 4-bit Wb (register offset)										
	field is shared between both source and										
	destination (but typically only used by										
	one).										

In summary, the following addressing modes are supported by move and accumulator instructions:

- Register Direct
- Register Indirect
- Register Indirect Post-modified
- Register Indirect Pre-modified
- Register Indirect with Register Offset (Indexed)
- Register Indirect with Literal Offset
- 8-Bit Literal
- 16-Bit Literal

Note: Not all instructions support all the addressing modes given above. Individual instructions may support different subsets of these addressing modes.

4.3.4 MAC INSTRUCTIONS

The dual source operand DSP instructions (CLR, ED, EDAC, MAC, MPY, MPY.N, MOVSAC and MSC), also referred to as MAC instructions, utilize a simplified set of addressing modes to allow the user to effectively manipulate the Data Pointers through register indirect tables.

The 2-source operand prefetch registers must be members of the set {W8, W9, W10, W11}. For data reads, W8 and W9 are always directed to the X RAGU, and W10 and W11 will always be directed to the Y AGU. The Effective Addresses generated (before and after modification) must, therefore, be valid addresses within X data space for W8 and W9, and Y data space for W10 and W11.

Note: Register Indirect with Register Offset Addressing mode is only available for W9 (in X space) and W11 (in Y space).

In summary, the following addressing modes are supported by the ${\tt MAC}$ class of instructions:

- · Register Indirect
- Register Indirect Post-Modified by 2
- Register Indirect Post-Modified by 4
- Register Indirect Post-Modified by 6
- Register Indirect with Register Offset (Indexed)

4.3.5 OTHER INSTRUCTIONS

Besides the various addressing modes outlined above, some instructions use literal constants of various sizes. For example, BRA (branch) instructions use 16-bit signed literals to specify the branch destination directly, whereas the DISI instruction uses a 14-bit unsigned literal field. In some instructions, such as ADD Acc, the source of an operand or result is implied by the opcode itself. Certain operations, such as NOP, do not have any operands.

4.4 Modulo Addressing

Modulo Addressing mode is a method of providing an automated means to support circular data buffers using hardware. The objective is to remove the need for software to perform data address boundary checks when executing tightly looped code, as is typical in many DSP algorithms.

7.0 INTERRUPT CONTROLLER

- Note 1: This data sheet summarizes the features of the dsPIC33FJXXXMCX06A/ X08A/X10A family of devices. However, it is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to Section 6. "Interrupts" (DS70184) in the "dsPIC33F/PIC24H Family Reference Manual", which is available from the Microchip web site (www.microchip.com).
 - 2: Some registers and associated bits described in this section may not be available on all devices. Refer to Section 4.0 "Memory Organization" in this data sheet for device-specific register and bit information.

The interrupt controller for the dsPIC33FJXXXMCX06A/X08A/X10A family of devices reduces the numerous peripheral interrupt request signals to a single interrupt request signal to the dsPIC33FJXXXMCX06A/X08A/X10A CPU. It has the following features:

- Up to eight processor exceptions and software traps
- Seven user-selectable priority levels
- Interrupt Vector Table (IVT) with up to 118 vectors
- A unique vector for each interrupt or exception source
- Fixed priority within a specified user priority level
- Alternate Interrupt Vector Table (AIVT) for debug support
- Fixed interrupt entry and return latencies

7.1 Interrupt Vector Table

The Interrupt Vector Table (IVT) is shown in Figure 7-1. The IVT resides in program memory, starting at location 000004h. The IVT contains 126 vectors consisting of eight nonmaskable trap vectors plus up to 118 sources of interrupt. In general, each interrupt source has its own vector. Each interrupt vector contains a 24-bit wide address. The value programmed into each interrupt vector location is the starting address of the associated Interrupt Service Routine (ISR).

Interrupt vectors are prioritized in terms of their natural priority; this priority is linked to their position in the vector table. All other things being equal, lower addresses have a higher natural priority. For example, the interrupt associated with vector 0 will take priority over interrupts at any other vector address. The dsPIC33FJXXXMCX06A/X08A/X10A family of devices implement up to 67 unique interrupts and five nonmaskable traps. These are summarized in Table 7-1 and Table 7-2.

7.1.1 ALTERNATE INTERRUPT VECTOR TABLE

The Alternate Interrupt Vector Table (AIVT) is located after the IVT, as shown in Figure 7-1. Access to the AIVT is provided by the ALTIVT control bit (INTCON2<15>). If the ALTIVT bit is set, all interrupt and exception processes use the alternate vectors instead of the default vectors. The alternate vectors are organized in the same manner as the default vectors.

The AIVT supports debugging by providing a means to switch between an application and a support environment without requiring the interrupt vectors to be reprogrammed. This feature also enables switching between applications for evaluation of different software algorithms at run time. If the AIVT is not needed, the AIVT should be programmed with the same addresses used in the IVT.

7.2 Reset Sequence

A device Reset is not a true exception because the interrupt controller is not involved in the Reset process. The dsPIC33FJXXXMCX06A/X08A/X10A device clears its registers in response to a Reset, which forces the PC to zero. The digital signal controller then begins program execution at location 0x000000. The user programs a GOTO instruction at the Reset address, which redirects program execution to the appropriate start-up routine.

Note: Any unimplemented or unused vector locations in the IVT and AIVT should be programmed with the address of a default interrupt handler routine that contains a RESET instruction.

REGISTER 7-5: IFS0: INTERRUPT FLAG STATUS REGISTER 0 (CONTINUED)

bit 2	OC1IF: Output Compare Channel 1 Interrupt Flag Status bit
	1 = Interrupt request has occurred
	0 = Interrupt request has not occurred
bit 1	IC1IF: Input Capture Channel 1 Interrupt Flag Status bit
	1 = Interrupt request has occurred
	0 = Interrupt request has not occurred
bit 0	INTOIF: External Interrupt 0 Flag Status bit

- 1 = Interrupt request has occurred
- 0 = Interrupt request has not occurred

11.2 Open-Drain Configuration

In addition to the PORT, LAT and TRIS registers for data control, some port pins can also be individually configured for either digital or open-drain output. This is controlled by the Open-Drain Control register, ODCx, associated with each port. Setting any of the bits configures the corresponding pin to act as an open-drain output.

The open-drain feature allows the generation of outputs higher than VDD (e.g., 5V) on any desired 5V tolerant pins by using external pull-up resistors. The maximum open-drain voltage allowed is the same as the maximum VIH specification.

See the "**Pin Diagrams**" section for the available pins and their functionality.

11.3 Configuring Analog Port Pins

The ADxPCFGH, ADxPCFGL and TRIS registers control the operation of the ADC port pins. The port pins that are desired as analog inputs must have their corresponding TRIS bit set (input). If the TRIS bit is cleared (output), the digital output level (VOH or VOL) is converted.

Clearing any bit in the ADxPCFGH or ADxPCFGL register configures the corresponding bit to be an analog pin. This is also the Reset state of any I/O pin that has an analog (ANx) function associated with it.

Note:	In devices with two ADC modules, if the
	corresponding PCFG bit in either
	AD1PCFGH(L) and AD2PCFGH(L) is
	cleared, the pin is configured as an analog
	input.

When reading the PORT register, all pins configured as analog input channels will read as cleared (a low level).

Pins configured as digital inputs will not convert an analog input. Analog levels on any pin that is defined as a digital input (including the ANx pins) can cause the input buffer to consume current that exceeds the device specifications.

Note:	The voltage on an analog input pin can be
	between -0.3V to (VDD + 0.3 V).

11.4 I/O Port Write/Read Timing

One instruction cycle is required between a port direction change or port write operation and a read operation of the same port. Typically, this instruction would be a NOP.

11.5 Input Change Notification

The input change notification function of the I/O ports allows the dsPIC33FJXXXMCX06A/X08A/X10A devices to generate interrupt requests to the processor in response to a change-of-state on selected input pins. This feature is capable of detecting input change-of-states even in Sleep mode, when the clocks are disabled. Depending on the device pin count, there are up to 24 external signals (CN0 through CN23) that can be selected (enabled) for generating an interrupt request on a change-of-state.

There are four control registers associated with the CN module. The CNEN1 and CNEN2 registers contain the CN Interrupt Enable (CNxIE) control bits for each of the CN input pins. Setting any of these bits enables a CN interrupt for the corresponding pins.

Each CN pin also has a weak pull-up connected to it. The pull-ups act as a current source that is connected to the pin and eliminate the need for external resistors when push button or keypad devices are connected. The pull-ups are enabled separately using the CNPU1 and CNPU2 registers, which contain the Weak Pull-up Enable bits (CNxPUE) for each of the CN pins. Setting any of the control bits enables the weak pull-ups for the corresponding pins.

Note: Pull-ups on change notification pins should always be disabled whenever the port pin is configured as a digital output.

EXAMPLE 11-1: PORT WRITE/READ EXAMPLE

MOV	OxFF00, WO	; Configure PORTB<15:8> as inputs
MOV	W0, TRISBB	; and PORTB<7:0> as outputs
NOP		; Delay 1 cycle
btss	PORTB, #13	; Next Instruction

REGISTER 16-2: PxTMR: PWMx TIMER COUNT VALUE REGISTER

R-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0		
PTDIR				PTMR<14:8>	>				
bit 15	-						bit 8		
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0		
			PTM	R<7:0>					
bit 7							bit 0		
Legend:									
R = Readable	bit	W = Writable	bit	U = Unimpler	nented bit, rea	ad as '0'			
-n = Value at F	POR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unkr	x = Bit is unknown		
				o					

bit 14-0	PTMR <14:0>: PWM Time Base Register Count Value bits
	0 = PWM time base is counting up
	1 = PWM time base is counting down
Dit 15	PIDIR: PWM Time Base Count Direction Status bit (read-only)

REGISTER 16-3: PxTPER: PWMx TIME BASE PERIOD REGISTER

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—				PTPER<14:8	>		
bit 15							bit 8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			PTPE	ER<7:0>			
bit 7							bit 0
Legend:							
R = Readable	bit	W = Writable b	it	U = Unimplen	nented bit, rea	id as '0'	
-n = Value at F	POR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unkr	nown

bit 15 Unimplemented: Read as '0'

bit 14-0 PTPER<14:0>: PWM Time Base Period Value bits

REGISTER 21-31: CiTRBnSTAT: ECAN™ RECEIVE BUFFER n STATUS (n = 0, 1, ..., 31)

U-0	U-0	U-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x		
—	—	_		FILHIT<4:0>					
bit 15							bit 8		
U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0		
—	—	—	—	—	—	—	—		
bit 7							bit 0		
Legend:									
R = Readable	bit	W = Writable I	bit U = Unimplemented bit, read as '0'						
-n = Value at P	OR	'1' = Bit is set		'0' = Bit is cleared x = Bit is unknown			nown		

bit 15-13 Unimplemented: Read as '0'

bit 12-8 **FILHIT<4:0>:** Filter Hit Code bits (only written by module for receive buffers, unused for transmit buffers) Encodes number of filter that resulted in writing this buffer.

bit 7-0 Unimplemented: Read as '0'

TABLE 26-32: SPIx MAXIMUM DATA/CLOCK RATE SUMMARY

AC CHARA	CTERISTICS		Standard Operating (unless otherwise s Operating temperate	g Conditions: stated) ure $-40^{\circ}C \le -40^{\circ}C \le 10^{\circ}$	3.0V to 3.6V TA \leq +85°C for TA \leq +125°C for	Industrial or Extended
Maximum Data Rate	Master Transmit Only (Half-Duplex)	Master Transmit/Receive (Full-Duplex)	Slave Transmit/Receive (Full-Duplex)	СКЕ	СКР	SMP
15 MHz	Table 26-33		—	0,1	0,1	0,1
10 MHz	—	Table 26-34	—	1	0,1	1
10 MHz	—	Table 26-35	—	0	0,1	1
15 MHz	—		Table 26-36	1	0	0
11 MHz	—	_	Table 26-37	1	1	0
15 MHz	_		Table 26-38	0	1	0
11 MHz			Table 26-39	0	0	0

FIGURE 26-14: SPIX MASTER MODE (HALF-DUPLEX, TRANSMIT ONLY CKE = 0) TIMING CHARACTERISTICS



FIGURE 26-15: SPIX MASTER MODE (HALF-DUPLEX, TRANSMIT ONLY CKE = 1) TIMING CHARACTERISTICS



АС СНА	ARACTER	ISTICS		Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)Operating temperature $-40^{\circ}C \le TA \le +85^{\circ}C$ for Industrial $-40^{\circ}C \le TA \le +125^{\circ}C$ for Extended			<pre>V to 3.6V ≤ +85°C for Industrial +125°C for Extended</pre>
Param No.	Symbol	Characteristic		Min ⁽¹⁾	Max	Units	Conditions
IM10	TLO:SCL	Clock Low Time	100 kHz mode	Tcy/2 (BRG + 1)	—	μs	—
			400 kHz mode	Tcy/2 (BRG + 1)	—	μs	—
			1 MHz mode ⁽²⁾	Tcy/2 (BRG + 1)	—	μS	—
IM11	THI:SCL	Clock High Time	100 kHz mode	Tcy/2 (BRG + 1)	—	μs	—
			400 kHz mode	Tcy/2 (BRG + 1)	—	μS	—
			1 MHz mode ⁽²⁾	Tcy/2 (BRG + 1)	—	μs	—
IM20	TF:SCL	SDAx and SCLx	100 kHz mode	—	300	ns	CB is specified to be
		Fall Time	400 kHz mode	20 + 0.1 Св	300	ns	from 10 to 400 pF
			1 MHz mode ⁽²⁾	—	100	ns	
IM21	TR:SCL	SDAx and SCLx	100 kHz mode	_	1000	ns	CB is specified to be
		Rise Time	400 kHz mode	20 + 0.1 Св	300	ns	from 10 to 400 pF
			1 MHz mode ⁽²⁾	_	300	ns	
IM25	TSU:DAT	Data Input	100 kHz mode	250		ns	—
	Setup Time	400 kHz mode	100	_	ns		
			1 MHz mode ⁽²⁾	40	_	ns	
IM26	IM26 THD:DAT	Data Input	100 kHz mode	0	_	μs	_
	Hold Time	400 kHz mode	0	0.9	μs		
			1 MHz mode ⁽²⁾	0.2		μS	
IM30	TSU:STA	Start Condition	100 kHz mode	Tcy/2 (BRG + 1)	_	μs	Only relevant for
		Setup Time	400 kHz mode	Tcy/2 (BRG + 1)		μS	Repeated Start
			1 MHz mode ⁽²⁾	Tcy/2 (BRG + 1)	_	μs	condition
IM31	THD:STA	Start Condition	100 kHz mode	Tcy/2 (BRG + 1)		μs	After this period the
		Hold Time	400 kHz mode	Tcy/2 (BRG + 1)	_	μs	first clock pulse is
			1 MHz mode ⁽²⁾	Tcy/2 (BRG + 1)		μs	generated
IM33	Tsu:sto	Stop Condition	100 kHz mode	Tcy/2 (BRG + 1)	—	μS	—
		Setup Time	400 kHz mode	Tcy/2 (BRG + 1)	—	μs	-
			1 MHz mode ⁽²⁾	Tcy/2 (BRG + 1)	—	μS	-
IM34	THD:STO	Stop Condition	100 kHz mode	Tcy/2 (BRG + 1)	—	ns	—
	Hold ⁻	Hold Time	400 kHz mode	Tcy/2 (BRG + 1)	_	ns	
			1 MHz mode ⁽²⁾	Tcy/2 (BRG + 1)		ns	
IM40	TAA:SCL	Output Valid	100 kHz mode		3500	μs	
		From Clock	400 kHz mode	_	1000	μS	_
			1 MHz mode ⁽²⁾		400	μS	_
IM45	TBF:SDA	Bus Free Time	100 kHz mode	4.7		μS	Time the bus must be
			400 kHz mode	1.3	—	μs	free before a new
			1 MHz mode ⁽²⁾	0.5	—	μS	transmission can start
IM50	Св	Bus Capacitive L	oading	—	400	pF	—
IM51	Tpgd	Pulse Gobbler De	elay	65	390	ns	See Note 3
· · · · · ·				•	•		

TABLE 26-40: I2Cx BUS DATA TIMING REQUIREMENTS (MASTER MODE)

Note 1: BRG is the value of the I²C[™] Baud Rate Generator. Refer to Section 19. "Inter-Integrated Circuit (I²C[™])" (DS70195) in the "dsPIC33F/PIC24H Family Reference Manual".

2: Maximum pin capacitance = 10 pF for all I2Cx pins (for 1 MHz mode only).

3: Typical value for this parameter is 130 ns.

FIGURE 26-24: I2Cx BUS START/STOP BITS TIMING CHARACTERISTICS (SLAVE MODE)





27.0 HIGH TEMPERATURE ELECTRICAL CHARACTERISTICS

This section provides an overview of dsPIC33FJXXXMCX06A/X08A/X10A electrical characteristics for devices operating in an ambient temperature range of -40°C to +150°C.

The specifications between -40° C to $+150^{\circ}$ C are identical to those shown in **Section 26.0** "**Electrical Characteristics**" for operation between -40° C to $+125^{\circ}$ C, with the exception of the parameters listed in this section.

Parameters in this section begin with an H, which denotes High temperature. For example, parameter DC10 in **Section 26.0 "Electrical Characteristics"** is the Industrial and Extended temperature equivalent of HDC10.

Absolute maximum ratings for the dsPIC33FJXXXMCX06A/X08A/X10A high temperature devices are listed below. Exposure to these maximum rating conditions for extended periods can affect device reliability. Functional operation of the device at these or any other conditions above the parameters indicated in the operation listings of this specification is not implied.

Absolute Maximum Ratings⁽¹⁾

Ambient temperature under bias ⁽⁴⁾	40°C to +150°C
Storage temperature	65°C to +160°C
Voltage on VDD with respect to Vss	-0.3V to +4.0V
Voltage on any pin that is not 5V tolerant with respect to Vss ⁽⁵⁾	0.3V to (VDD + 0.3V)
Voltage on any 5V tolerant pin with respect to Vss when $VDD < 3.0V^{(5)}$	0.3V to (VDD + 0.3V)
Voltage on any 5V tolerant pin with respect to Vss when VDD $\geq 3.0 V^{(5)}$	0.3V to 5.6V
Voltage on VCAP with respect to Vss	2.25V to 2.75V
Maximum current out of Vss pin	60 mA
Maximum current into VDD pin ⁽²⁾	60 mA
Maximum junction temperature	+155°C
Maximum current sourced/sunk by any 2x I/O pin ⁽³⁾	2 mA
Maximum current sourced/sunk by any 4x I/O pin ⁽³⁾	4 mA
Maximum current sourced/sunk by any 8x I/O pin ⁽³⁾	8 mA
Maximum current sunk by all ports combined	10 mA
Maximum current sourced by all ports combined ⁽²⁾	10 mA

- **Note 1:** Stresses above those listed under "Absolute Maximum Ratings" can cause permanent damage to the device. This is a stress rating only, and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods can affect device reliability.
 - 2: Maximum allowable current is a function of device maximum power dissipation (see Table 27-2).
 - **3:** Unlike devices at 125°C and below, the specifications in this section also apply to the CLKOUT, VREF+, VREF-, SCLx, SDAx, PGECx, and PGEDx pins.
 - 4: AEC-Q100 reliability testing for devices intended to operate at 150°C is 1,000 hours. Any design in which the total operating time from 125°C to 150°C will be greater than 1,000 hours is not warranted without prior written approval from Microchip Technology Inc.
 - 5: Refer to the "Pin Diagrams" section for 5V tolerant pins.

DC CHARACTERISTICS Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +150°C for High Temperation				W to 3.6V ≤ +150°C for High Temperature			
Parameter No.	Typical	Мах	Units	Conditions			
Power-Down (Current (IPD)						
HDC61c	3	5	μA	+150°C	3.3V	Watchdog Timer Current: ΔIWDT ^(2,4)	

Note 1: Base IPD is measured with all peripherals and clocks shut down. All I/Os are configured as inputs and pulled to Vss. WDT, etc., are all switched off, and VREGS (RCON<8>) = 1.

- 2: The ∆ current is the additional current consumed when the module is enabled. This current should be added to the base IPD current.
- 3: These currents are measured on the device containing the most memory in this family.
- 4: These parameters are characterized, but are not tested in manufacturing.

TABLE 27-5: DC CHARACTERISTICS: DOZE CURRENT (IDOZE)

DC CHARACTERISTICS			Standard O (unless oth Operating te	perating erwise s emperatu	Conditions tated) re -40°C ≤	: 3.0V to 3.6 Ta ≤ +150°C	V C for High Temperature
Parameter No.	Typical ⁽¹⁾	Max	Doze Ratio	Units		Condi	tions
HDC72a	39	45	1:2	mA			
HDC72f	18	25	1:64	mA	+150°C	3.3V	20 MIPS
HDC72g	18	25	1:128	mA			

Note 1: Parameters with Doze ratios of 1:2 and 1:64 are characterized, but are not tested in manufacturing.

28.0 DC AND AC DEVICE CHARACTERISTICS GRAPHS

Note: The graphs provided following this note are a statistical summary based on a limited number of samples and are provided for design guidance purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore, outside the warranted range.



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Q

Quadrature Encoder Interface (C	QEI)
Quadrature Encoder Interface (C	QEI) Module
Register Map	

R

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