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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

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Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	40 MIPs
Connectivity	CANbus, I ² C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, Motor Control PWM, POR, PWM, QEI, WDT
Number of I/O	85
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 24x10/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33fj128mc710a-e-pf

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Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

2.0 GUIDELINES FOR GETTING STARTED WITH 16-BIT DIGITAL SIGNAL CONTROLLERS

- Note 1: This data sheet summarizes the features of the dsPIC33FJXXXMCX06A/X08A/ X10A family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the "dsPIC33F/ PIC24H Family Reference Manual", which is available from the Microchip web site (www.microchip.com).
 - Some registers and associated bits described in this section may not be available on all devices. Refer to Section 4.0 "Memory Organization" in this data sheet for device-specific register and bit information.

2.1 Basic Connection Requirements

Getting started with the dsPIC33FJXXXMCX06A/X08A/X10A family of 16-bit Digital Signal Controllers (DSC) requires attention to a minimal set of device pin connections before proceeding with development. The following is a list of pin names, which must always be connected:

- All VDD and Vss pins (see Section 2.2 "Decoupling Capacitors")
- All AVDD and AVSS pins (regardless if ADC module is not used)
- (see Section 2.2 "Decoupling Capacitors")
 VCAP
- (see Section 2.3 "CPU Logic Filter Capacitor Connection (VCAP)")
- MCLR pin (see Section 2.4 "Master Clear (MCLR) Pin")
- PGECx/PGEDx pins used for In-Circuit Serial Programming[™] (ICSP[™]) and debugging purposes (see Section 2.5 "ICSP Pins")
- OSC1 and OSC2 pins when external oscillator source is used

(see Section 2.6 "External Oscillator Pins")

Additionally, the following pins may be required:

• VREF+/VREF- pins used when external voltage reference for ADC module is implemented

Note:	The	AVdd	and	AVss	pins	mu	st be
	conn	ected	ted independen		of	the	ADC
	volta	ge refe					

2.2 Decoupling Capacitors

The use of decoupling capacitors on every pair of power supply pins, such as VDD, VSS, AVDD and AVSS is required.

Consider the following criteria when using decoupling capacitors:

- Value and type of capacitor: Recommendation of 0.1 μ F (100 nF), 10-20V. This capacitor should be a low-ESR and have resonance frequency in the range of 20 MHz and higher. It is recommended that ceramic capacitors be used.
- Placement on the printed circuit board: The decoupling capacitors should be placed as close to the pins as possible. It is recommended to place the capacitors on the same side of the board as the device. If space is constricted, the capacitor can be placed on another layer on the PCB using a via; however, ensure that the trace length from the pin to the capacitor is within one-quarter inch (6 mm) in length.
- Handling high-frequency noise: If the board is experiencing high-frequency noise, upward of tens of MHz, add a second ceramic type capacitor in parallel to the above described decoupling capacitor. The value of the second capacitor can be in the range of 0.01 μ F to 0.001 μ F. Place this second capacitor next to the primary decoupling capacitor. In high-speed circuit designs, consider implementing a decade pair of capacitances as close to the power and ground pins as possible. For example, 0.1 μ F in parallel with 0.001 μ F.
- **Maximizing performance:** On the board layout from the power supply circuit, run the power and return traces to the decoupling capacitors first, and then to the device pins. This ensures that the decoupling capacitors are first in the power chain. Equally important is to keep the trace length between the capacitor and the power pins to a minimum, thereby reducing PCB track inductance.

3.6.1 MULTIPLIER

The 17-bit x 17-bit multiplier is capable of signed or unsigned operation and can multiplex its output using a scaler to support either 1.31 fractional (Q31) or 32-bit integer results. Unsigned operands are zero-extended into the 17th bit of the multiplier input value. Signed operands are sign-extended into the 17th bit of the multiplier input value. Signed operands are sign-extended into the 17th bit of the multiplier/scaler is a 33-bit value which is sign-extended to 40 bits. Integer data is inherently represented as a signed two's complement value, where the MSb is defined as a sign bit. Generally speaking, the range of an N-bit two's complement integer is -2^{N-1} to $2^{N-1} - 1$. For a 16-bit integer, the data range is -32768 (0x8000) to 32767 (0x7FFF) including 0. For a 32-bit integer, the data range is -2,147,483,648 (0x8000 0000) to 2,147,483,647 (0x7FFF FFFF).

When the multiplier is configured for fractional multiplication, the data is represented as a two's complement fraction, where the MSb is defined as a sign bit and the radix point is implied to lie just after the sign bit (QX format). The range of an N-bit two's complement fraction with this implied radix point is -1.0 to $(1 - 2^{1-N})$. For a 16-bit fraction, the Q15 data range is -1.0 (0x8000) to 0.999969482 (0x7FFF) including 0 and has a precision of 3.01518 x 10⁻⁵. In Fractional mode, the 16 x 16 multiply operation generates a 1.31 product which has a precision of 4.65661 x 10⁻¹⁰.

The same multiplier is used to support the MCU multiply instructions which include integer 16-bit signed, unsigned and mixed sign multiplies.

The MUL instruction may be directed to use byte or word-sized operands. Byte operands will direct a 16-bit result, and word operands will direct a 32-bit result to the specified register(s) in the W array.

3.6.2 DATA ACCUMULATORS AND ADDER/SUBTRACTER

The data accumulator consists of a 40-bit adder/ subtracter with automatic sign extension logic. It can select one of two accumulators (A or B) as its pre-accumulation source and post-accumulation destination. For the ADD and LAC instructions, the data to be accumulated or loaded can be optionally scaled via the barrel shifter prior to accumulation.

3.6.2.1 Adder/Subtracter, Overflow and Saturation

The adder/subtracter is a 40-bit adder with an optional zero input into one side, and either true, or complement data into the other input. In the case of addition, the Carry/Borrow input is active-high and the other input is true data (not complemented); whereas in the case of subtraction, the Carry/Borrow input is active-low and the other input is complemented. The adder/subtracter generates Overflow Status bits, SA/SB and OA/OB, which are latched and reflected in the STATUS register:

- Overflow from bit 39: this is a catastrophic overflow in which the sign of the accumulator is destroyed.
- Overflow into guard bits 32 through 39: this is a recoverable overflow. This bit is set whenever all the guard bits are not identical to each other.

The adder has an additional saturation block which controls accumulator data saturation, if selected. It uses the result of the adder, the Overflow Status bits described above and the SAT<A:B> (CORCON<7:6>) and ACCSAT (CORCON<4>) mode control bits to determine when and to what value to saturate.

Six STATUS register bits have been provided to support saturation and overflow; they are:

- 1. OA: AccA overflowed into guard bits
- OB: AccB overflowed into guard bits
- 3. SA:

AccA saturated (bit 31 overflow and saturation) or

AccA overflowed into guard bits and saturated (bit 39 overflow and saturation)

- 4. SB:
 - AccB saturated (bit 31 overflow and saturation) or

AccB overflowed into guard bits and saturated (bit 39 overflow and saturation)

5. OAB:

Logical OR of OA and OB

6. SAB:

Logical OR of SA and SB

The OA and OB bits are modified each time data passes through the adder/subtracter. When set, they indicate that the most recent operation has overflowed into the accumulator guard bits (bits 32 through 39). The OA and OB bits can also optionally generate an arithmetic warning trap when they and the corresponding Overflow Trap Flag Enable bits (OVATE, OVBTE) in the INTCON1 register (refer to **Section 7.0 "Interrupt Controller"**) are set. This allows the user to take immediate action, for example, to correct system gain.

The SA and SB bits are modified each time data passes through the adder/subtracter, but can only be cleared by the user. When set, they indicate that the accumulator has overflowed its maximum range (bit 31 for 32-bit saturation or bit 39 for 40-bit saturation) and will be saturated (if saturation is enabled). When saturation is not enabled, SA and SB default to bit 39 overflow, and thus, indicate that a catastrophic overflow has occurred. If the COVTE bit in the INTCON1 register is set, SA and SB bits will generate an arithmetic warning trap when saturation is disabled.

The Overflow and Saturation Status bits can optionally be viewed in the STATUS Register (SR) as the logical OR of OA and OB (in bit OAB), and the logical OR of SA and SB (in bit SAB). This allows programmers to check one bit in the STATUS register to determine if either accumulator has overflowed or one bit to determine if either accumulator has saturated. This would be useful for complex number arithmetic, which typically uses both the accumulators.

The device supports three Saturation and Overflow modes:

1. Bit 39 Overflow and Saturation:

When bit 39 overflow and saturation occurs, the saturation logic loads the maximally positive 9.31 (0x7FFFFFFFF) or maximally negative 9.31 value (0x800000000) into the target accumulator. The SA or SB bit is set and remains set until cleared by the user. This is referred to as 'super saturation' and provides protection against erroneous data or unexpected algorithm problems (e.g., gain calculations).

- 2. Bit 31 Overflow and Saturation: When bit 31 overflow and saturation occurs, the saturation logic then loads the maximally positive 1.31 value (0x007FFFFFF) or maximally negative 1.31 value (0x0080000000) into the target accumulator. The SA or SB bit is set and remains set until cleared by the user. When this Saturation mode is in effect, the guard bits are not used (so the OA, OB or OAB bits are never set).
- 3. Bit 39 Catastrophic Overflow:

The bit 39 Overflow Status bit from the adder is used to set the SA or SB bit, which remains set until cleared by the user. No saturation operation is performed and the accumulator is allowed to overflow (destroying its sign). If the COVTE bit in the INTCON1 register is set, a catastrophic overflow can initiate a trap exception.

3.6.2.2 Accumulator 'Write Back'

The MAC class of instructions (with the exception of MPY, MPY.N, ED and EDAC) can optionally write a rounded version of the high word (bits 31 through 16) of the accumulator that is not targeted by the instruction into data space memory. The write is performed across the X bus into combined X and Y address space. The following addressing modes are supported:

- 1. W13, Register Direct: The rounded contents of the non-target accumulator are written into W13 as a 1.15 fraction.
- [W13]+ = 2, Register Indirect with Post-Increment: The rounded contents of the non-target accumulator are written into the address pointed to by W13 as a 1.15 fraction. W13 is then incremented by 2 (for a word write).

3.6.2.3 Round Logic

The round logic is a combinational block which performs a conventional (biased) or convergent (unbiased) round function during an accumulator write (store). The Round mode is determined by the state of the RND bit in the CORCON register. It generates a 16-bit, 1.15 data value which is passed to the data space write saturation logic. If rounding is not indicated by the instruction, a truncated 1.15 data value is stored and the least significant word is simply discarded.

Conventional rounding zero-extends bit 15 of the accumulator and adds it to the ACCxH word (bits 16 through 31 of the accumulator). If the ACCxL word (bits 0 through 15 of the accumulator) is between 0x8000 and 0xFFFF (0x8000 included), ACCxH is incremented. If ACCxL is between 0x0000 and 0x7FFF, ACCxH is left unchanged. A consequence of this algorithm is that over a succession of random rounding operations, the value tends to be biased slightly positive.

Convergent (or unbiased) rounding operates in the same manner as conventional rounding, except when ACCxL equals 0x8000. In this case, the Least Significant bit (bit 16 of the accumulator) of ACCxH is examined. If it is '1', ACCxH is incremented. If it is '0', ACCxH is not modified. Assuming that bit 16 is effectively random in nature, this scheme removes any rounding bias that may accumulate.

The SAC and SAC.R instructions store either a truncated (SAC) or rounded (SAC.R) version of the contents of the target accumulator to data memory via the X bus, subject to data saturation (see **Section 3.6.2.4 "Data Space Write Saturation"**). For the MAC class of instructions, the accumulator write-back operation will function in the same manner, addressing combined MCU (X and Y) data space though the X bus. For this class of instructions, the data is always subject to rounding.

FIGURE 4-4: DATA MEMORY MAP FOR dsPIC33FJXXXMCX06A/X08A/X10A DEVICES WITH 16-Kbyte RAM



5.4.1 PROGRAMMING ALGORITHM FOR FLASH PROGRAM MEMORY

The user can program one row of program Flash memory at a time. To do this, it is necessary to erase the 8-row erase page that contains the desired row. The general process is as follows:

- 1. Read eight rows of program memory (512 instructions) and store it in data RAM.
- 2. Update the program data in RAM with the desired new data.
- 3. Erase the block (see Example 5-1):
 - a) Set the NVMOP bits (NVMCON<3:0>) to ⁽⁰⁰¹⁰⁾ to configure for block erase. Set the ERASE (NVMCON<6>) and WREN (NVMCON<14>) bits.
 - b) Write the starting address of the page to be erased into the TBLPAG and W registers.
 - c) Write 0x55 to NVMKEY.
 - d) Write 0xAA to NVMKEY.
 - e) Set the WR bit (NVMCON<15>). The erase cycle begins and the CPU stalls for the duration of the erase cycle. When the erase is done, the WR bit is cleared automatically.

- 4. Write the first 64 instructions from data RAM into the program memory buffers (see Example 5-2).
- 5. Write the program block to Flash memory:
 - a) Set the NVMOP bits to '0001' to configure for row programming. Clear the ERASE bit and set the WREN bit.
 - b) Write 0x55 to NVMKEY.
 - c) Write 0xAA to NVMKEY.
 - d) Set the WR bit. The programming cycle begins and the CPU stalls for the duration of the write cycle. When the write to Flash memory is done, the WR bit is cleared automatically.
- Repeat steps 4 and 5 using the next available 64 instructions from the block in data RAM by incrementing the value in TBLPAG until all 512 instructions are written back to Flash memory.

For protection against accidental operations, the write initiate sequence for NVMKEY must be used to allow any erase or program operation to proceed. After the programming command has been executed, the user must wait for the programming time until programming is complete. The two instructions following the start of the programming sequence should be NOPS, as shown in Example 5-3.

EXAMPLE 5-1: ERASING A PROGRAM MEMORY PAGE

; Set up NVMCC	ON for block erase operation		
MOV	#0x4042, W0	;	
MOV	W0, NVMCON	;	Initialize NVMCON
; Init pointer	r to row to be ERASED		
MOV	<pre>#tblpage(PROG_ADDR), W0</pre>	;	
MOV	W0, TBLPAG	;	Initialize PM Page Boundary SFR
MOV	<pre>#tbloffset(PROG_ADDR), W0</pre>	;	Initialize in-page EA[15:0] pointer
TBLWTL	W0, [W0]	;	Set base address of erase block
DISI	#5	;	Block all interrupts with priority <7
		;	for next 5 instructions
MOV	#0x55, W0		
MOV	W0, NVMKEY	;	Write the 55 key
MOV	#0xAA, W1	;	
MOV	W1, NVMKEY	;	Write the AA key
BSET	NVMCON, #WR	;	Start the erase sequence
NOP		;	Insert two NOPs after the erase
NOP		;	command is asserted

REGISTER 7-11: IEC1: INTERRUPT ENABLE CONTROL REGISTER 1 (CONTINUED)

bit 3	CNIE: Input Change Notification Interrupt Enable bit 1 = Interrupt request enabled 0 = Interrupt request not enabled
bit 2	Unimplemented: Read as '0'
bit 1	MI2C1IE: I2C1 Master Events Interrupt Enable bit
	1 = Interrupt request enabled
	0 = Interrupt request not enabled
bit 0	SI2C1IE: I2C1 Slave Events Interrupt Enable bit
	1 = Interrupt request enabled

0 = Interrupt request not enabled

REGISTER 8-7: DMACS0: DMA CONTROLLER STATUS REGISTER 0 (CONTINUED)

bit 3	XWCOL3: Channel 3 DMA RAM Write Collision Flag bit 1 = Write collision detected
bit 2	0 = No write collision detected XWCOL2: Channel 2 DMA RAM Write Collision Flag bit
	 1 = Write collision detected 0 = No write collision detected
bit 1	XWCOL1: Channel 1 DMA RAM Write Collision Flag bit 1 = Write collision detected 0 = No write collision detected
bit 0	XWCOL0: Channel 0 DMA RAM Write Collision Flag bit 1 = Write collision detected 0 = No write collision detected

REGISTER 8-9: DSADR: MOST RECENT DMA RAM ADDRESS

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
			DSAD)R<15:8>			
bit 15							bit 8
R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
			DSAI	DR<7:0>			
bit 7							bit 0
Legend:							
R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'							
-n = Value at POR (1' = Bit is set (0' = Bit is cleared x = Bit is unknown						nown	

bit 15-0 DSADR<15:0>: Most Recent DMA RAM Address Accessed by DMA Controller bits

12.0 TIMER1

- Note 1: This data sheet summarizes the features of the dsPIC33FJXXXMCX06A/ X08A/X10A family of devices. However, it is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 11. "Timers"** (DS70205) in the *"dsPIC33F/PIC24H Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com).
 - Some registers and associated bits described in this section may not be available on all devices. Refer to Section 4.0 "Memory Organization" in this data sheet for device-specific register and bit information.

The Timer1 module is a 16-bit timer, which can serve as the time counter for the Real-Time Clock (RTC) or operate as a free-running interval timer/counter. Timer1 can operate in three modes:

- 16-Bit Timer
- 16-Bit Synchronous Counter
- 16-Bit Asynchronous Counter

Timer1 also supports the following features:

- Timer gate operation
- · Selectable prescaler settings
- Timer operation during CPU Idle and Sleep modes
- Interrupt on 16-bit Period register match or falling edge of external gate signal

Figure 12-1 presents a block diagram of the 16-bit timer module.

To configure Timer1 for operation, do the following:

- 1. Set the TON bit (= 1) in the T1CON register.
- 2. Select the timer prescaler ratio using the TCKPS<1:0> bits in the T1CON register.
- 3. Set the Clock and Gating modes using the TCS and TGATE bits in the T1CON register.
- 4. Set or clear the TSYNC bit in T1CON to select synchronous or asynchronous operation.
- 5. Load the timer period value into the PR1 register.
- 6. If interrupts are required, set the interrupt enable bit, T1IE. Use the priority bits, T1IP<2:0>, to set the interrupt priority.



FIGURE 12-1: 16-BIT TIMER1 MODULE BLOCK DIAGRAM

REGISTER 21-14: CIBUFPNT3: ECAN™ FILTER 8-11 BUFFER POINTER REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	F11BF	P<3:0>			F10E	3P<3:0>	
bit 15							bit 8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	F9BP<3:0> F8BP<3:0>						
bit 7							bit 0
Legend:							
R = Readable	bit	W = Writable	bit	U = Unimplen	nented bit. rea	ad as '0'	
-n = Value at I	POR	'1' = Bit is set		'0' = Bit is clea	ared	x = Bit is unkr	nown
bit 15-12	F11BP<3:0> 1111 = Filter 1110 = Filter	: RX Buffer Writ hits received ir hits received ir	tten when Fill n RX FIFO bu n RX Buffer 1	ter 11 Hits bits iffer 4			
	•						
	•						
	0001 = Filter 0000 = Filter	hits received in hits received ir	n RX Buffer 1 n RX Buffer 0				
bit 11-8	F10BP<3:0> 1111 = Filter 1110 = Filter	: RX Buffer Writh hits received in hits received in	tten when Fil n RX FIFO bu n RX Buffer 1	ter 10 Hits bits iffer 4			
	•						
	•						
	• 0001 = Filter 0000 = Filter	hits received ir hits received ir	n RX Buffer 1 n RX Buffer 0				
bit 7-4	F9BP<3:0>: 1111 = Filter 1110 = Filter	RX Buffer Writt hits received in hits received in	en when Filte n RX FIFO bu n RX Buffer 1	er 9 Hits bits Iffer 4			
	•						
	0001 = Filter 0000 = Filter	hits received in hits received ir	n RX Buffer 1 n RX Buffer 0				
bit 3-0	F8BP<3:0>: 1111 = Filter 1110 = Filter	RX Buffer Writt hits received in hits received in	en when Filte n RX FIFO bu n RX Buffer 1	er 8 Hits bits Iffer 4			
	•						
	0001 = Filter 0000 = Filter	hits received ir hits received ir	n RX Buffer 1 n RX Buffer 0				

REGISTER 21-16: CIRXFnSID: ECAN™ ACCEPTANCE FILTER n STANDARD IDENTIFIER (n = 0, 1, ...,15)

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
			SID<	<10:3>			
bit 15							bit 8
R/W-x	R/W-x	R/W-x	U-0	R/W-x	U-0	R/W-x	R/W-x
	SID<2:0>		_	EXIDE	—	EID<1	17:16>
bit 7							bit 0
Legend:							
R = Readable	e bit	W = Writable I	oit	U = Unimpler	nented bit, reac	l as '0'	
-n = Value at	POR	'1' = Bit is set		'0' = Bit is cleared x = Bit is unknown			
bit 15-5	SID<10:0>: S	tandard Identifi	er bits				
	1 = Message 0 = Message	address bit, SII address bit, SII	Dx, must be ' Dx, must be '	1' to match filte 0' to match filte	er er		
bit 4	Unimplemen	ted: Read as 'd)'				
bit 3	EXIDE: Exte	nded Identifier I	Enable bit				
	If MIDE = 1, t	hen:					
	1 = Match on 0 = Match on	ly messages wi ly messages wi	th extended i th standard io	dentifier addres dentifier addres	sses ses		
	<u>If MIDE = 0, t</u> Ignore EXIDE	hen: bit.					
bit 2	Unimplemen	ted: Read as 'o)'				
bit 1-0	EID<17:16>:	Extended Iden	tifier bits				
	1 = Message 0 = Message	address bit, Ell address bit, Ell	Dx, must be ' Dx, must be '	1' to match filte	er er		

REGISTER 21-17: CIRXFnEID: ECAN™ ACCEPTANCE FILTER n EXTENDED IDENTIFIER (n = 0, 1, ..., 15)

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
			EID	<15:8>			
bit 15							bit 8
R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
			EID	<7:0>			
bit 7							bit 0
Legend:							
R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'							
-n = Value at P	I = Value at POR (1' = Bit is set (0' = Bit is cleared x = Bit is unknown					nown	

bit 15-0 EID<15:0>: Extended Identifier bits

1 = Message address bit, EIDx, must be '1' to match filter

0 = Message address bit, EIDx, must be '0' to match filter

REGISTER 21-20: CiRXMnSID: ECAN™ ACCEPTANCE FILTER MASK n STANDARD IDENTIFIER

r								
R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	
			SID	<10:3>				
bit 15							bit 8	
R/W-x	R/W-x	R/W-x	U-0	R/W-x	U-0	R/W-x	R/W-x	
	SID<2:0>		—	MIDE	_	EID<1	17:16>	
bit 7							bit 0	
Legend:								
R = Readabl	e bit	W = Writable	bit	U = Unimple	mented bit, rea	d as '0'		
-n = Value at	POR	'1' = Bit is set		'0' = Bit is cleared x = Bit is unknown				
bit 15-5	SID<10:0>:	Standard Identi	fier bits					
	1 = Include b	oit, SIDx, in filter	comparison					
	0 = Bit, SIDx	, is a don't care	in filter comp	barison				
bit 4	Unimpleme	nted: Read as '	0'					
bit 3	MIDE: Ident	ifier Receive Mo	ode bit					
	1 = Match or	nly message typ	es (standard	or extended ad	dress) that corre	espond to the E>	KIDE bit in filter	
	0 = Match e	ither standard o	r extended a	ddress messag	e if filters matc	h		
	(i.e., if (l	Filter SID) = (Me	essage SID)	or if (Filter SID/	EID) = (Messag	ge SID/EID))		
bit 2	Unimpleme	nted: Read as '	0'					
bit 1-0	EID<17:16>:	Extended Iden	tifier bits					
	1 = Include	bit, EIDx, in filte	r comparisor	1				
	0 = Bit, EID	k, is a don't care	e in filter com	parison				

REGISTER 21-21: CIRXMnEID: ECAN™ ACCEPTANCE FILTER MASK n EXTENDED IDENTIFIER

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
			EID	<15:8>			
bit 15							bit 8
R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
			EID	<7:0>			
bit 7							bit 0
Legend:							
R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'							
-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown					nown		

bit 15-0 EID<15:0>: Extended Identifier bits

1 = Include bit, EIDx, in filter comparison

0 = Bit, EIDx, is a don't care in filter comparison

U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	
—	_	—	—	_	CH123	NB<1:0>	CH123SB	
bit 15				•			bit 8	
U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	
		<u> </u>	—	—	CH123	NA<1:0>	CH123SA	
bit 7							bit 0	
Legend:								
R = Readable	e bit	W = Writable b	oit	U = Unimple	mented bit, rea	ad as '0'		
-n = Value at	POR	'1' = Bit is set		'0' = Bit is cle	eared	x = Bit is unk	nown	
bit 15-11	Unimplemen	ted: Read as 'o)'					
bit 10-9	CH123NB<1:	0>: Channel 1,	2, 3 Negative	e Input Select f	or Sample B bi	ts		
	When AD12E	B = 1, CHxNB is	s: U-0, Unimp	plemented, Re	ead as '0'.			
	11 = CH1 neg 10 = CH1 neg	ative input is A	N9; CH2 nega	ative input is A	NTU; CH3 neg	ative input is Ai tive input is AN	N11 8	
	0x = CH1, CH	12, CH3 negativ	/e input is VR	EF-	intr, erie negu		0	
bit 8	CH123SB: Ch	nannel 1, 2, 3 P	ositive Input S	Select for Sam	ple B bit			
	When AD12E	B = 1, CHxSB is	s: U-0, Unimp	plemented, Re	ead as '0'.			
	1 = CH1 posit	ive input is AN	3; CH2 positiv	e input is AN4	; CH3 positive	input is AN5		
	0 = CH1 posit	ive input is AN	J; CH2 positiv	e input is AN1	; CH3 positive	input is AN2		
bit 7-3	Unimplement	ted: Read as '0)'					
bit 2-1	CH123NA<1:	0>: Channel 1,	2, 3 Negative	Input Select f	or Sample A bi	ts		
	When AD12E	B = 1, CHXNA is	S: U-0, Unimp	plemented, Re	ad as '0'.	ative input is Al	N11	
	10 = CH1 neg	ative input is A	N6: CH2 neg	ative input is A	N7: CH3 nega	tive input is AN	8	
	0x = CH1, CH	12, CH3 negativ	ve input is VR	EF-	,	-	-	
bit 0	CH123SA: Cl	nannel 1, 2, 3 P	ositive Input S	Select for Sam	ple A bit			
	When AD12E	B = 1, CHxSA is	s: U-0, Unimp	plemented, Re	ad as '0'.			
	1 = CH1 posit	ive input is AN	3; CH2 positiv	e input is AN4	; CH3 positive	input is AN5		
	0 = CH1 positive input is AN0; CH2 positive input is AN1; CH3 positive input is AN2							

REGISTER 22-5: ADxCHS123: ADCx INPUT CHANNEL 1, 2, 3 SELECT REGISTER

Bit Field	Register	RTSP Effect	Description
BWRP	FBS	Immediate	Boot Segment Program Flash Write Protection bit 1 = Boot segment may be written 0 = Boot segment is write-protected
BSS<2:0>	FBS	Immediate	Boot Segment Program Flash Code Protection Size bits x11 = No boot program Flash segment Boot space is 1K IW less VS: 110 = Standard security; boot program Flash segment starts at end of VS, ends at 0007FEh 010 = High security; boot program Flash segment starts at end of VS, ends at 0007FEh Boot space is 4K IW less VS: 101 = Standard security; boot program Flash segment starts at end of VS, ends at 0017FEh 001 = High security; boot program Flash segment starts at end of VS, ends at 001FFEh 001 = High security; boot program Flash segment starts at end of VS, ends at 001FFEh 001 = High security; boot program Flash segment starts at end of VS, ends at 001FFEh 000 = Standard security; boot program Flash segment starts at end of VS, ends at 003FFEh 000 = High security; boot program Flash segment starts at end of VS, ends at 003FFEh
RBS<1:0>	FBS	Immediate	Boot Segment RAM Code Protection bits 11 = No boot RAM defined 10 = Boot RAM is 128 bytes 01 = Boot RAM is 256 bytes 00 = Boot RAM is 1024 bytes
SWRP	FSS	Immediate	Secure Segment Program Flash Write Protection bit 1 = Secure segment may be written 0 = Secure segment is write-protected

TABLE 23-2: CONFIGURATION BITS DESCRIPTION

DC CHARACTERISTICS			$\begin{array}{l} \mbox{Standard Operating Conditions: 3.0V to 3.6V} \\ \mbox{(unless otherwise stated)} \\ \mbox{Operating temperature} & -40^{\circ}C \leq TA \leq +85^{\circ}C \mbox{ for Industrial} \\ & -40^{\circ}C \leq TA \leq +125^{\circ}C \mbox{ for Extended} \end{array}$				
Parameter No.	Typical ⁽²⁾	Мах	Doze Ratio Units Conditions				
Doze Current	t (IDOZE) ⁽¹⁾						
DC73a	11	35	1:2	mA			
DC73f	11	30	1:64	mA	-40°C	3.3V	40 MIPS
DC73g	11	30	1:128	mA			
DC70a	42	50	1:2	mA			
DC70f	26	30	1:64	mA	+25°C	3.3V	40 MIPS
DC70g	25	30	1:128	mA			
DC71a	41	50	1:2	mA			
DC71f	25	30	1:64	mA	+85°C	3.3V	40 MIPS
DC71g	24	30	1:128	mA			
DC72a	42	50	1:2	mA			
DC72f	26	30	1:64	mA	+125°C	3.3V	40 MIPS
DC72g	25	30	1:128	mA]		

TABLE 26-8: DC CHARACTERISTICS: DOZE CURRENT (IDOZE)

Note 1: IDOZE is primarily a function of the operating voltage and frequency. Other factors, such as I/O pin loading and switching rate, oscillator type, internal code execution pattern and temperature, also have an impact on the current consumption. The test conditions for all IDOZE measurements are as follows:

- Oscillator is configured in EC mode and external clock active, OSC1 is driven with external square wave from rail-to-rail with overshoot/undershoot < 250 mV
- CLKO is configured as an I/O input pin in the Configuration word
- · All I/O pins are configured as inputs and pulled to Vss
- MCLR = VDD, WDT and FSCM are disabled
- CPU, SRAM, program memory and data memory are operational
- No peripheral modules are operating; however, every peripheral is being clocked (defined PMDx bits are set to zero and unimplemented PMDx bits are set to one)
- CPU executing while(1) statement
- JTAG is disabled
- 2: Data in the "Typ" column is at 3.3V, +25°C unless otherwise stated.



TABLE 26-29: QUADRATURE DECODER TIMING REQUIREMENTS

AC CHARACTERISTICS			$\begin{tabular}{lllllllllllllllllllllllllllllllllll$				
Param No.	Symbol	Characteristic ⁽¹⁾		Тур ⁽²⁾	Max	Units	Conditions
TQ30	TQUL	Quadrature Input Low Time		6 Тсү	_	ns	—
TQ31	ΤουΗ	Quadrature Input High Time		6 TCY	—	ns	—
TQ35	ΤουΙΝ	Quadrature Input Period		12 TCY	—	ns	—
TQ36	ΤουΡ	Quadrature Phase Period		3 TCY	—	ns	—
TQ40	TQUFL	Filter Time to Recognize Low with Digital Filter		3 * N * Tcy	—	ns	N = 1, 2, 4, 16, 32, 64, 128 and 256 (Note 3)
TQ41	TQUFH	Filter Time to Recognize Hig with Digital Filter	h	3 * N * Tcy		ns	N = 1, 2, 4, 16, 32, 64, 128 and 256 (Note 3)

Note 1: These parameters are characterized but not tested in manufacturing.

2: Data in "Typ" column is at 3.3V, 25°C unless otherwise stated.

3: N = Index Channel Digital Filter Clock Divide Select bits. Refer to **Section 15. "Quadrature Encoder Interface (QEI)"** (DS70208) in the "*dsPIC33F/PIC24H Family Reference Manual*".

AC CHARACTERISTICS			$\begin{tabular}{lllllllllllllllllllllllllllllllllll$				
Param No.	Symbol	Characteristic		Min	Max	Units	Conditions
IS10	TLO:SCL	Clock Low Time	100 kHz mode	4.7	—	μS	Device must operate at a minimum of 1.5 MHz
			400 kHz mode	1.3	_	μs	Device must operate at a minimum of 10 MHz
			1 MHz mode ⁽¹⁾	0.5		μS	—
IS11	THI:SCL	Clock High Time	100 kHz mode	4.0	—	μs	Device must operate at a minimum of 1.5 MHz
			400 kHz mode	0.6	_	μS	Device must operate at a minimum of 10 MHz
			1 MHz mode ⁽¹⁾	0.5	_	μS	_
IS20	TF:SCL	SDAx and SCLx	100 kHz mode	—	300	ns	CB is specified to be from
		Fall Time	400 kHz mode	20 + 0.1 Св	300	ns	10 to 400 pF
			1 MHz mode ⁽¹⁾	—	100	ns	
IS21	TR:SCL	SDAx and SCLx	100 kHz mode	—	1000	ns	CB is specified to be from
		Rise Time	400 kHz mode	20 + 0.1 Св	300	ns	10 to 400 pF
			1 MHz mode ⁽¹⁾	—	300	ns	
IS25	TSU:DAT	Data Input	100 kHz mode	250		ns	—
		Setup Time	400 kHz mode	100		ns	
			1 MHz mode ⁽¹⁾	100	_	ns	
IS26	THD:DAT	Data Input	100 kHz mode	0	_	μs	—
		Hold Time	400 kHz mode	0	0.9	μs	
			1 MHz mode ⁽¹⁾	0	0.3	μs	
IS30	TSU:STA	Start Condition	100 kHz mode	4.7	—	μs	Only relevant for Repeated
		Setup Time	400 kHz mode	0.6	_	μs	Start condition
			1 MHz mode ⁽¹⁾	0.25	_	μS	
IS31 THD:STA		Start Condition	100 kHz mode	4.0	_	μS	After this period, the first
		Hold Time	400 kHz mode	0.6	_	μS	clock pulse is generated
			1 MHz mode ⁽¹⁾	0.25		μS	
IS33	TSU:STO	Stop Condition	100 kHz mode	4.7		μs	_
		Setup Time	400 kHz mode	0.6		μS	
			1 MHz mode ⁽¹⁾	0.6		μs	
IS34 THD:STO	Stop Condition	100 kHz mode	4000		ns	_	
		Hold Time	400 kHz mode	600	—	ns	
			1 MHz mode ⁽¹⁾	250		ns	
IS40 TAA:SCL		Output Valid	100 kHz mode	0	3500	ns	
		From Clock	400 kHz mode	0	1000	ns	
			1 MHz mode ⁽¹⁾	0	350	ns	
IS45	TBF:SDA	Bus Free Time	100 kHz mode	4.7	—	μS	Time the bus must be free
			400 kHz mode	1.3	—	μS	before a new transmission
			1 MHz mode ⁽¹⁾	0.5	—	μS	Can Start
IS50	Св	Bus Capacitive Lo		400	pF	—	

TABLE 26-41: I2Cx BUS DATA TIMING REQUIREMENTS (SLAVE MODE)

Note 1: Maximum pin capacitance = 10 pF for all I2Cx pins (for 1 MHz mode only).

29.1 Package Marking Information (Continued)

100-Lead TQFP (12x12x1 mm)





100-Lead TQFP (14x14x1mm)





Legend	: XXX Y YY WW NNN (63) *	Customer-specific information Year code (last digit of calendar year) Year code (last 2 digits of calendar year) Week code (week of January 1 is week '01') Alphanumeric traceability code Pb-free JEDEC designator for Matte Tin (Sn) This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.			
Note:	In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.				

Revision C (March 2011)

This revision includes typographical and formatting changes throughout the data sheet text. In addition, all instances of VDDCORE have been removed.

All other major changes are referenced by their respective section in the following table.

TABLE B-2:	MAJOR	SECTION	UPDATES
		02011011	0. 5/1150

Section Name	Update Description
Section 2.0 "Guidelines for Getting Started with 16-bit Digital Signal Controllers"	Updated the title of Section 2.3 "CPU Logic Filter Capacitor Connection (VCAP)".
	The frequency limitation for device PLL start-up conditions was updated in Section 2.7 " Oscillator Value Conditions on Device Start-up ".
	The second paragraph in Section 2.9 "Unused I/Os" was updated.
Section 4.0 "Memory Organization"	The All Resets values for the following SFRs in the Timer Register Map were changed (see Table 4-6): • TMR1 • TMR2 • TMR3 • TMR4 • TMR5 • TMR6 • TMR7 • TMR8 • TMR9
Section 9.0 "Oscillator Configuration"	Added Note 3 to the OSCCON: Oscillator Control Register (see Register 9-1).
	Added Note 2 to the CLKDIV: Clock Divisor Register (see Register 9-2).
	Added Note 1 to the PLLFBD: PLL Feedback Divisor Register (see Register 9-3).
	Added Note 2 to the OSCTUN: FRC Oscillator Tuning Register (see Register 9-4).
Section 22.0 "10-bit/12-bit Analog-to-Digital Converter (ADC)"	Updated the VREFL references in the ADC1 module block diagram (see Figure 22-1).
Section 23.0 "Special Features"	Added a new paragraph and removed the third paragraph in Section 23.1 "Configuration Bits" .
	Added the column "RTSP Effects" to the Configuration Bits Descriptions (see Table 23-2).

NOTES: