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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	40 MIPS
Connectivity	CANbus, I <sup>2</sup> C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, Motor Control PWM, POR, PWM, QEI, WDT
Number of I/O	85
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	30K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 24x10/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TQFP
Supplier Device Package	100-TQFP (12x12)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/microchip-technology/dspic33fj256mc710a-i-pt">https://www.e-xfl.com/product-detail/microchip-technology/dspic33fj256mc710a-i-pt</a>

# dsPIC33FJXXXMCX06A/X08A/X10A

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**TABLE 4-2: CHANGE NOTIFICATION REGISTER MAP FOR dsPIC33FJXXXMCX10A DEVICES**

SFR Name	SFR Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
CNEN1	0060	CN15IE	CN14IE	CN13IE	CN12IE	CN11IE	CN10IE	CN9IE	CN8IE	CN7IE	CN6IE	CN5IE	CN4IE	CN3IE	CN2IE	CN1IE	CN0IE	0000
CNEN2	0062	—	—	—	—	—	—	—	—	CN23IE	CN22IE	CN21IE	CN20IE	CN19IE	CN18IE	CN17IE	CN16IE	0000
CNPU1	0068	CN15PUE	CN14PUE	CN13PUE	CN12PUE	CN11PUE	CN10PUE	CN9PUE	CN8PUE	CN7PUE	CN6PUE	CN5PUE	CN4PUE	CN3PUE	CN2PUE	CN1PUE	CN0PUE	0000
CNPU2	006A	—	—	—	—	—	—	—	—	CN23PUE	CN22PUE	CN21PUE	CN20PUE	CN19PUE	CN18PUE	CN17PUE	CN16PUE	0000

**Legend:** x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**TABLE 4-3: CHANGE NOTIFICATION REGISTER MAP FOR dsPIC33FJXXXMCX08A DEVICES**

SFR Name	SFR Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
CNEN1	0060	CN15IE	CN14IE	CN13IE	CN12IE	CN11IE	CN10IE	CN9IE	CN8IE	CN7IE	CN6IE	CN5IE	CN4IE	CN3IE	CN2IE	CN1IE	CN0IE	0000
CNEN2	0062	—	—	—	—	—	—	—	—	—	—	CN21IE	CN20IE	CN19IE	CN18IE	CN17IE	CN16IE	0000
CNPU1	0068	CN15PUE	CN14PUE	CN13PUE	CN12PUE	CN11PUE	CN10PUE	CN9PUE	CN8PUE	CN7PUE	CN6PUE	CN5PUE	CN4PUE	CN3PUE	CN2PUE	CN1PUE	CN0PUE	0000
CNPU2	006A	—	—	—	—	—	—	—	—	—	—	CN21PUE	CN20PUE	CN19PUE	CN18PUE	CN17PUE	CN16PUE	0000

**Legend:** x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**TABLE 4-4: CHANGE NOTIFICATION REGISTER MAP FOR dsPIC33FJXXXMCX06A DEVICES**

SFR Name	SFR Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
CNEN1	0060	CN15IE	CN14IE	CN13IE	CN12IE	CN11IE	CN10IE	CN9IE	CN8IE	CN7IE	CN6IE	CN5IE	CN4IE	CN3IE	CN2IE	CN1IE	CN0IE	0000
CNEN2	0062	—	—	—	—	—	—	—	—	—	—	CN21IE	CN20IE	—	CN18IE	CN17IE	CN16IE	0000
CNPU1	0068	CN15PUE	CN14PUE	CN13PUE	CN12PUE	CN11PUE	CN10PUE	CN9PUE	CN8PUE	CN7PUE	CN6PUE	CN5PUE	CN4PUE	CN3PUE	CN2PUE	CN1PUE	CN0PUE	0000
CNPU2	006A	—	—	—	—	—	—	—	—	—	—	CN21PUE	CN20PUE	—	CN18PUE	CN17PUE	CN16PUE	0000

**Legend:** x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

# dsPIC33FJXXXMCX06A/X08A/X10A

## 5.2 RTSP Operation

The dsPIC33FJXXXMCX06A/X08A/X10A Flash program memory array is organized into rows of 64 instructions or 192 bytes. RTSP allows the user to erase a page of memory at a time, which consists of eight rows (512 instructions), and to program one row or one word at a time. Table 26-12 shows typical erase and programming times. The 8-row erase pages and single row write rows are edge-aligned, from the beginning of program memory, on boundaries of 1536 bytes and 192 bytes, respectively.

The program memory implements holding buffers that can contain 64 instructions of programming data. Prior to the actual programming operation, the write data must be loaded into the buffers in sequential order. The instruction words loaded must always be from a group of 64 boundaries.

The basic sequence for RTSP programming is to set up a Table Pointer, then do a series of TBLWT instructions to load the buffers. Programming is performed by setting the control bits in the NVMCON register. A total of 64 TBLWTL and TBLWTH instructions are required to load the instructions.

All of the table write operations are single-word writes (two instruction cycles), because only the buffers are written. A programming cycle is required for programming each row.

## 5.3 Programming Operations

A complete programming sequence is necessary for programming or erasing the internal Flash in RTSP mode. The processor stalls (waits) until the programming operation is finished.

The programming time depends on the FRC accuracy (see Table 26-19) and the value of the FRC Oscillator Tuning register (see Register 9-4). Use the following formula to calculate the minimum and maximum values for the row write time, page erase time and word write cycle time parameters (see Table 26-12).

### EQUATION 5-1: PROGRAMMING TIME

$$T = \frac{1}{7.37 \text{ MHz} \times (\text{FRC Accuracy})\% \times (\text{FRC Tuning})\%}$$

For example, if the device is operating at +125°C, the FRC accuracy will be ±5%. If the TUN<5:0> bits (see Register 9-4) are set to 'b1111111, the minimum row write time is equal to Equation 5-2.

### EQUATION 5-2: MINIMUM ROW WRITE TIME

$$T_{RW} = \frac{11064 \text{ Cycles}}{7.37 \text{ MHz} \times (1 + 0.05) \times (1 - 0.00375)} = 1.435 \text{ ms}$$

The maximum row write time is equal to Equation 5-3.

### EQUATION 5-3: MAXIMUM ROW WRITE TIME

$$T_{RW} = \frac{11064 \text{ Cycles}}{7.37 \text{ MHz} \times (1 - 0.05) \times (1 - 0.00375)} = 1.586 \text{ ms}$$

Setting the WR bit (NVMCON<15>) starts the operation and the WR bit is automatically cleared when the operation is finished.

## 5.4 Control Registers

There are two SFRs used to read and write the program Flash memory: NVMCON and NVMKEY.

The NVMCON register (Register 5-1) controls which blocks are to be erased, which memory type is to be programmed and the start of the programming cycle.

NVMKEY is a write-only register that is used for write protection. To start a programming or erase sequence, the user must consecutively write 0x55 and 0xAA to the NVMKEY register. Refer to **Section 5.3 “Programming Operations”** for further details.

# dsPIC33FJXXMCMX06A/X08A/X10A

**TABLE 7-1: INTERRUPT VECTORS**

Vector Number	Interrupt Request (IRQ) Number	IVT Address	AIVT Address	Interrupt Source
8	0	0x000014	0x000114	INT0 – External Interrupt 0
9	1	0x000016	0x000116	IC1 – Input Capture 1
10	2	0x000018	0x000118	OC1 – Output Compare 1
11	3	0x00001A	0x00011A	T1 – Timer1
12	4	0x00001C	0x00011C	DMA0 – DMA Channel 0
13	5	0x00001E	0x00011E	IC2 – Input Capture 2
14	6	0x000020	0x000120	OC2 – Output Compare 2
15	7	0x000022	0x000122	T2 – Timer2
16	8	0x000024	0x000124	T3 – Timer3
17	9	0x000026	0x000126	SPI1E – SPI1 Error
18	10	0x000028	0x000128	SPI1 – SPI1 Transfer Done
19	11	0x00002A	0x00012A	U1RX – UART1 Receiver
20	12	0x00002C	0x00012C	U1TX – UART1 Transmitter
21	13	0x00002E	0x00012E	ADC1 – ADC 1
22	14	0x000030	0x000130	DMA1 – DMA Channel 1
23	15	0x000032	0x000132	Reserved
24	16	0x000034	0x000134	SI2C1 – I2C1 Slave Events
25	17	0x000036	0x000136	MI2C1 – I2C1 Master Events
26	18	0x000038	0x000138	Reserved
27	19	0x00003A	0x00013A	Change Notification Interrupt
28	20	0x00003C	0x00013C	INT1 – External Interrupt 1
29	21	0x00003E	0x00013E	ADC2 – ADC 2
30	22	0x000040	0x000140	IC7 – Input Capture 7
31	23	0x000042	0x000142	IC8 – Input Capture 8
32	24	0x000044	0x000144	DMA2 – DMA Channel 2
33	25	0x000046	0x000146	OC3 – Output Compare 3
34	26	0x000048	0x000148	OC4 – Output Compare 4
35	27	0x00004A	0x00014A	T4 – Timer4
36	28	0x00004C	0x00014C	T5 – Timer5
37	29	0x00004E	0x00014E	INT2 – External Interrupt 2
38	30	0x000050	0x000150	U2RX – UART2 Receiver
39	31	0x000052	0x000152	U2TX – UART2 Transmitter
40	32	0x000054	0x000154	SPI2E – SPI2 Error
41	33	0x000056	0x000156	SPI1 – SPI1 Transfer Done
42	34	0x000058	0x000158	C1RX – ECAN1 Receive Data Ready
43	35	0x00005A	0x00015A	C1 – ECAN1 Event
44	36	0x00005C	0x00015C	DMA3 – DMA Channel 3
45	37	0x00005E	0x00015E	IC3 – Input Capture 3
46	38	0x000060	0x000160	IC4 – Input Capture 4
47	39	0x000062	0x000162	IC5 – Input Capture 5
48	40	0x000064	0x000164	IC6 – Input Capture 6
49	41	0x000066	0x000166	OC5 – Output Compare 5
50	42	0x000068	0x000168	OC6 – Output Compare 6
51	43	0x00006A	0x00016A	OC7 – Output Compare 7
52	44	0x00006C	0x00016C	OC8 – Output Compare 8
53	45	0x00006E	0x00016E	Reserved

# dsPIC33FJXXMCX06A/X08A/X10A

## REGISTER 7-3: INTCON1: INTERRUPT CONTROL REGISTER 1

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
NSTDIS	OVAERR	OVBERR	COVAERR	COVBERR	OVATE	OVATE	COVTE
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0
SFTACERR	DIV0ERR	DMACERR	MATHERR	ADDRERR	STKERR	OSCFAIL	—
bit 7							bit 0

### Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

- bit 15      **NSTDIS:** Interrupt Nesting Disable bit  
1 = Interrupt nesting is disabled  
0 = Interrupt nesting is enabled
- bit 14      **OVAERR:** Accumulator A Overflow Trap Flag bit  
1 = Trap was caused by overflow of Accumulator A  
0 = Trap was not caused by overflow of Accumulator A
- bit 13      **OVBERR:** Accumulator B Overflow Trap Flag bit  
1 = Trap was caused by overflow of Accumulator B  
0 = Trap was not caused by overflow of Accumulator B
- bit 12      **COVAERR:** Accumulator A Catastrophic Overflow Trap Flag bit  
1 = Trap was caused by catastrophic overflow of Accumulator A  
0 = Trap was not caused by catastrophic overflow of Accumulator A
- bit 11      **COVBERR:** Accumulator B Catastrophic Overflow Trap Flag bit  
1 = Trap was caused by catastrophic overflow of Accumulator B  
0 = Trap was not caused by catastrophic overflow of Accumulator B
- bit 10      **OVATE:** Accumulator A Overflow Trap Enable bit  
1 = Trap overflow of Accumulator A  
0 = Trap disabled
- bit 9        **OVATE:** Accumulator B Overflow Trap Enable bit  
1 = Trap overflow of Accumulator B  
0 = Trap disabled
- bit 8        **COVTE:** Catastrophic Overflow Trap Enable bit  
1 = Trap on catastrophic overflow of Accumulator A or B enabled  
0 = Trap disabled
- bit 7        **SFTACERR:** Shift Accumulator Error Status bit  
1 = Math error trap was caused by an invalid accumulator shift  
0 = Math error trap was not caused by an invalid accumulator shift
- bit 6        **DIV0ERR:** Arithmetic Error Status bit  
1 = Math error trap was caused by a divide by zero  
0 = Math error trap was not caused by a divide by zero
- bit 5        **DMACERR:** DMA Controller Error Status bit  
1 = DMA controller error trap has occurred  
0 = DMA controller error trap has not occurred
- bit 4        **MATHERR:** Arithmetic Error Status bit  
1 = Math error trap has occurred  
0 = Math error trap has not occurred

# dsPIC33FJXXXMCX06A/X08A/X10A

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## REGISTER 8-7:     DMACS0: DMA CONTROLLER STATUS REGISTER 0 (CONTINUED)

- bit 3           **XWCOL3:** Channel 3 DMA RAM Write Collision Flag bit  
                  1 = Write collision detected  
                  0 = No write collision detected
- bit 2           **XWCOL2:** Channel 2 DMA RAM Write Collision Flag bit  
                  1 = Write collision detected  
                  0 = No write collision detected
- bit 1           **XWCOL1:** Channel 1 DMA RAM Write Collision Flag bit  
                  1 = Write collision detected  
                  0 = No write collision detected
- bit 0           **XWCOL0:** Channel 0 DMA RAM Write Collision Flag bit  
                  1 = Write collision detected  
                  0 = No write collision detected

# dsPIC33FJXXXMCX06A/X08A/X10A

**REGISTER 9-4: OSCTUN: FRC OSCILLATOR TUNING REGISTER<sup>(2)</sup>**

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15						bit 8	

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	TUN<5:0> <sup>(1)</sup>					
bit 7							bit 0

**Legend:**

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-6

**Unimplemented:** Read as '0'

bit 5-0

**TUN<5:0>:** FRC Oscillator Tuning bits<sup>(1)</sup>

011111 = Center frequency + 11.625% (8.23 MHz)

011110 = Center frequency + 11.25% (8.20 MHz)

•

•

•

000001 = Center frequency + 0.375% (7.40 MHz)

000000 = Center frequency (7.37 MHz nominal)

111111 = Center frequency – 0.375% (7.345 MHz)

•

•

•

100001 = Center frequency – 11.625% (6.52 MHz)

100000 = Center frequency – 12% (6.49 MHz)

**Note 1:** OSCTUN functionality has been provided to help customers compensate for temperature effects on the FRC frequency over a wide range of temperatures. The tuning step size is an approximation and is neither characterized nor tested.

**2:** This register is reset only on a Power-on Reset (POR).



# dsPIC33FJXXXMCX06A/X08A/X10A

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## REGISTER 10-1: PMD1: PERIPHERAL MODULE DISABLE CONTROL REGISTER 1 (CONTINUED)

bit 3	<b>SPI1MD:</b> SPI1 Module Disable bit 1 = SPI1 module is disabled 0 = SPI1 module is enabled
bit 2	<b>C2MD:</b> ECAN2 Module Disable bit 1 = ECAN2 module is disabled 0 = ECAN2 module is enabled
bit 1	<b>C1MD:</b> ECAN1 Module Disable bit 1 = ECAN1 module is disabled 0 = ECAN1 module is enabled
bit 0	<b>AD1MD:</b> ADC1 Module Disable bit <sup>(1)</sup> 1 = ADC1 module is disabled 0 = ADC1 module is enabled

**Note 1:** The PCFGx bits have no effect if the ADC module is disabled by setting this bit. In this case, all port pins multiplexed with ANx will be in Digital mode.

# dsPIC33FJXXXMCX06A/X08A/X10A

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NOTES:

# dsPIC33FJXXMCX06A/X08A/X10A

## REGISTER 16-12: PxDC1: PWMx DUTY CYCLE REGISTER 1

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PDC1<15:8>							
bit 15							
bit 8							

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PDC1<7:0>							
bit 7							
bit 0							

### Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-0      **PDC1<15:0>**: PWM Duty Cycle #1 Value bits

## REGISTER 16-13: PxDC2: PWMx DUTY CYCLE REGISTER 2

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PDC2<15:8>							
bit 15							
bit 8							

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PDC2<7:0>							
bit 7							
bit 0							

### Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-0      **PDC2<15:0>**: PWM Duty Cycle #2 Value bits

# dsPIC33FJXXMCX06A/X08A/X10A

## 17.0 QUADRATURE ENCODER INTERFACE (QEI) MODULE

**Note 1:** This data sheet summarizes the features of the dsPIC33FJXXMCX06A/X08A/X10A family of devices. However, it is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 15. “Quadrature Encoder Interface (QEI)”** (DS70208) in the “dsPIC33F/PIC24H Family Reference Manual”, which is available from the Microchip web site ([www.microchip.com](http://www.microchip.com)).

**2:** Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 “Memory Organization”** in this data sheet for device-specific register and bit information.

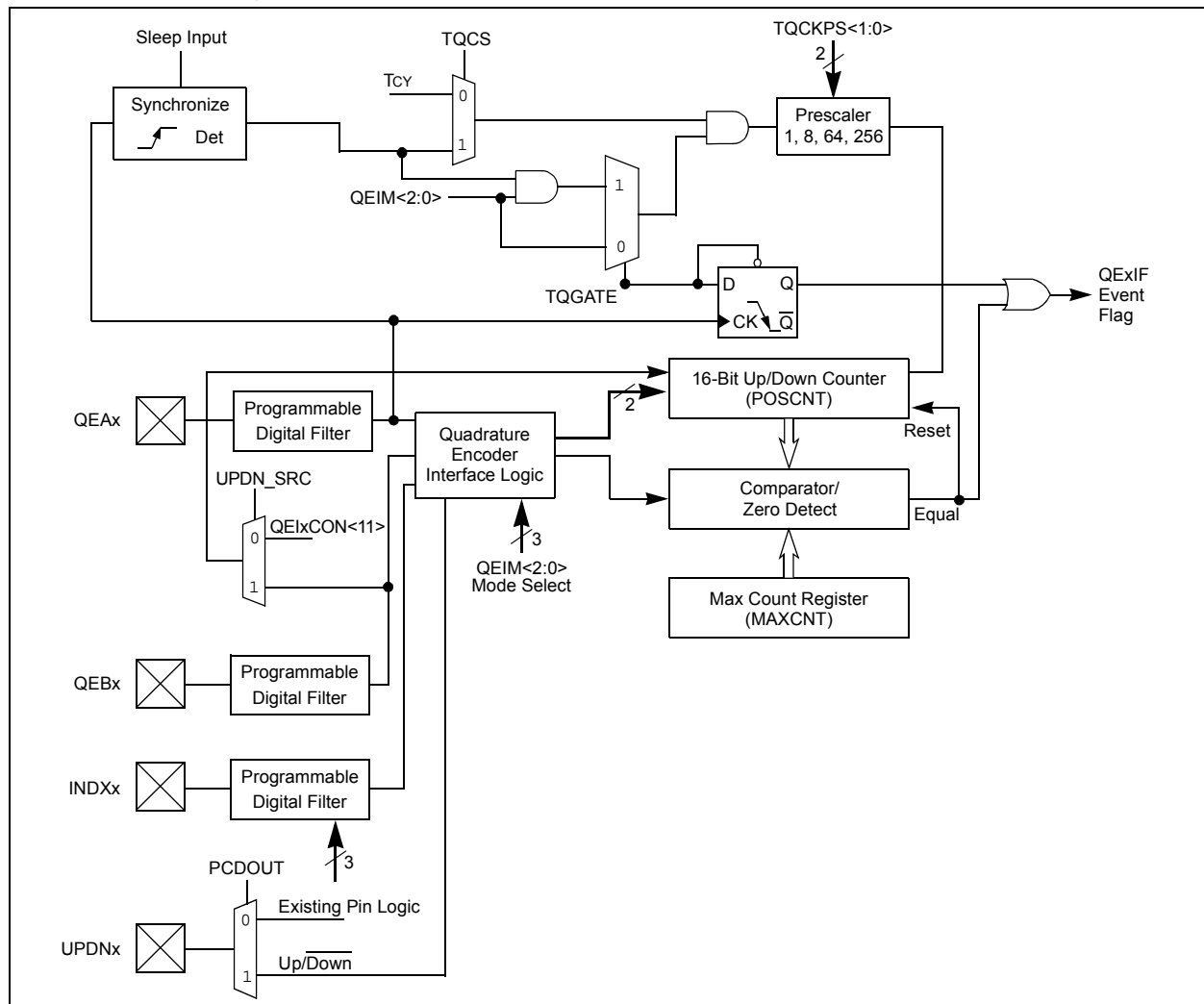
This section describes the Quadrature Encoder Interface (QEI) module and associated operational modes. The QEI module provides the interface to incremental encoders for obtaining mechanical position data.

The operational features of the QEI include the following:

- Three input channels for two phase signals and an index pulse
- 16-bit up/down position counter
- Count direction status
- Position Measurement (x2 and x4) mode
- Programmable digital noise filters on inputs
- Alternate 16-Bit Timer/Counter mode
- Quadrature Encoder Interface interrupts

The QEI module’s operating mode is determined by setting the appropriate bits, QEIM<2:0> (QEIXCON<10:8>). Figure 17-1 depicts the Quadrature Encoder Interface block diagram.

**FIGURE 17-1: QUADRATURE ENCODER INTERFACE BLOCK DIAGRAM**



# dsPIC33FJXXMCX06A/X08A/X10A

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## REGISTER 20-2: UxSTA: UARTx STATUS AND CONTROL REGISTER (CONTINUED)

bit 7-6	<b>URXISEL&lt;1:0&gt;</b> : Receive Interrupt Mode Selection bits 11 = Interrupt is set on the UxRSR transfer, making the receive buffer full (i.e., has 4 data characters) 10 = Interrupt is set on the UxRSR transfer, making the receive buffer 3/4 full (i.e., has 3 data characters) 0x = Interrupt is set when any character is received and transferred from the UxRSR to the receive buffer. Receive buffer has one or more characters
bit 5	<b>ADDEN</b> : Address Character Detect bit (bit 8 of received data = 1) 1 = Address Detect mode enabled. If 9-bit mode is not selected, this does not take effect. 0 = Address Detect mode disabled
bit 4	<b>RIDLE</b> : Receiver Idle bit (read-only) 1 = Receiver is Idle 0 = Receiver is active
bit 3	<b>PERR</b> : Parity Error Status bit (read-only) 1 = Parity error has been detected for the current character (character at the top of the receive FIFO) 0 = Parity error has not been detected
bit 2	<b>FERR</b> : Framing Error Status bit (read-only) 1 = Framing error has been detected for the current character (character at the top of the receive FIFO) 0 = Framing error has not been detected
bit 1	<b>OERR</b> : Receive Buffer Overrun Error Status bit (read/clear only) 1 = Receive buffer has overflowed 0 = Receive buffer has not overflowed. Clearing a previously set OERR bit (1 → 0 transition) will reset the receiver buffer and the UxRSR to the empty state.
bit 0	<b>URXDA</b> : Receive Buffer Data Available bit (read-only) 1 = Receive buffer has data, at least one more character can be read 0 = Receive buffer is empty

**Note 1:** Refer to **Section 17. “UART”** (DS70188) in the “*dsPIC33F/PIC24H Family Reference Manual*” for information on enabling the UART module for transmit operation.

# dsPIC33FJXXMCX06A/X08A/X10A

## REGISTER 21-2: CICTRL2: ECAN™ CONTROL REGISTER 2

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	R-0	R-0	R-0	R-0	R-0
—	—	—	DNCNT<4:0>				
bit 7							bit 0

### Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-5

**Unimplemented:** Read as '0'

bit 4-0

**DNCNT<4:0>:** DeviceNet™ Filter Bit Number bits

10010–11111 = Invalid selection

10001 = Compare up to data byte 3, bit 6 with EID<17>

- 
- 
- 

00001 = Compare up to data byte 1, bit 7 with EID<0>

00000 = Do not compare data bytes

# dsPIC33FJXXMCMC06A/X08A/X10A

## REGISTER 22-7: ADxCSSH: ADCx INPUT SCAN SELECT REGISTER HIGH<sup>(1,2)</sup>

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CSS31	CSS30	CSS29	CSS28	CSS27	CSS26	CSS25	CSS24
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CSS23	CSS22	CSS21	CSS20	CSS19	CSS18	CSS17	CSS16
bit 7							bit 0

### Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-0 **CSS<31:16>**: ADC Input Scan Selection bits

1 = Select ANx for input scan

0 = Skip ANx for input scan

**Note 1:** On devices without 32 analog inputs, all ADxCSSH bits may be selected by user. However, inputs selected for scan without a corresponding input on the device will convert VREFL.

**2:** CSSx = ANx, where x = 16 through 31.

## REGISTER 22-8: ADxCSSL: ADCx INPUT SCAN SELECT REGISTER LOW<sup>(1,2)</sup>

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CSS15	CSS14	CSS13	CSS12	CSS11	CSS10	CSS9	CSS8
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CSS7	CSS6	CSS5	CSS4	CSS3	CSS2	CSS1	CSS0
bit 7							bit 0

### Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-0 **CSS<15:0>**: ADC Input Scan Selection bits

1 = Select ANx for input scan

0 = Skip ANx for input scan

**Note 1:** On devices without 16 analog inputs, all ADxCSSL bits may be selected by user. However, inputs selected for scan without a corresponding input on the device will convert VREF-.

**2:** CSSx = ANx, where x = 0 through 15.

# dsPIC33FJXXMCX06A/X08A/X10A

## 23.2 On-Chip Voltage Regulator

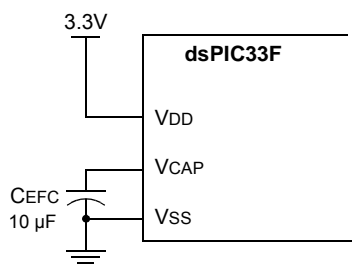
All of the dsPIC33FJXXMCX06A/X08A/X10A devices power their core digital logic at a nominal 2.5V. This may create an issue for designs that are required to operate at a higher typical voltage, such as 3.3V. To simplify system design, all devices in the dsPIC33FJXXMCX06A/X08A/X10A family incorporate an on-chip regulator that allows the device to run its core logic from VDD.

The regulator provides power to the core from the other VDD pins. The regulator requires that a low-ESR (less than 5 ohms) capacitor (such as tantalum or ceramic) be connected to the VCAP pin (Figure 23-1). This helps to maintain the stability of the regulator. The recommended value for the filter capacitor is provided in Table 26-13 of **Section 26.1 “DC Characteristics”**.

**Note:** It is important for the low-ESR capacitor to be placed as close as possible to the VCAP pin.

On a POR, it takes approximately 20  $\mu$ s for the on-chip voltage regulator to generate an output voltage. During this time, designated as TSTARTUP, code execution is disabled. TSTARTUP is applied every time the device resumes operation after any power-down.

**FIGURE 23-1: CONNECTIONS FOR THE ON-CHIP VOLTAGE REGULATOR<sup>(1,2,3)</sup>**



- Note 1:** These are typical operating voltages. Refer to **TABLE 26-13: “Internal Voltage Regulator Specifications”** located in **Section 26.1 “DC Characteristics”** for the full operating ranges of VDD and VCAP.
- Note 2:** It is important for the low-ESR capacitor to be placed as close as possible to the VCAP pin.
- Note 3:** Typical VCAP pin voltage = 2.5V when VDD  $\geq$  VDDMIN.

## 23.3 BOR: Brown-out Reset

The BOR (Brown-out Reset) module is based on an internal voltage reference circuit that monitors the regulated supply voltage, VCAP. The main purpose of the BOR module is to generate a device Reset when a brown-out condition occurs. Brown-out conditions are generally caused by glitches on the AC mains (i.e., missing portions of the AC cycle waveform due to bad power transmission lines or voltage sags due to excessive current draw when a large inductive load is turned on).

A BOR will generate a Reset pulse which will reset the device. The BOR will select the clock source, based on the device Configuration bit values (FNOSC<2:0> and POSCMD<1:0>). Furthermore, if an oscillator mode is selected, the BOR will activate the Oscillator Start-up Timer (OST). The system clock is held until OST expires. If the PLL is used, then the clock will be held until the LOCK bit (OSCCON<5>) is '1'.

Concurrently, the PWRT time-out (TPWRT) will be applied before the internal Reset is released. If TPWRT = 0 and a crystal oscillator is being used, then a nominal delay of TFSCM = 100 is applied. The total delay in this case is TFSCM.

The BOR Status bit (RCON<1>) will be set to indicate that a BOR has occurred. The BOR circuit continues to operate while in Sleep or Idle modes and will reset the device should VDD fall below the BOR threshold voltage.



# dsPIC33FJXXMXX06A/X08A/X10A

**TABLE 26-11: ELECTRICAL CHARACTERISTICS: BOR**

DC CHARACTERISTICS		Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended					
Param.	Symbol	Characteristic <sup>(1)</sup>	Min <sup>(1)</sup>	Typ	Max <sup>(1)</sup>	Units	Conditions
BO10	VBOR	BOR Event on VDD Transition High-to-Low	2.40	—	2.55	V	VDD

**Note 1:** Parameters are for design guidance only and are not tested in manufacturing.

**TABLE 26-12: DC CHARACTERISTICS: PROGRAM MEMORY**

DC CHARACTERISTICS		Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended					
Param No.	Symbol	Characteristic	Min	Typ <sup>(1)</sup>	Max	Units	Conditions
		<b>Program Flash Memory</b>					
D130	EP	Cell Endurance	10,000	—	—	E/W	—
D131	VPR	VDD for Read	V <sub>MIN</sub>	—	3.6	V	V <sub>MIN</sub> = Minimum operating voltage
D132b	VPEW	VDD for Self-Timed Write	V <sub>MIN</sub>	—	3.6	V	V <sub>MIN</sub> = Minimum operating voltage
D134	TRETD	Characteristic Retention	20	—	—	Year	Provided no other specifications are violated
D135	IDDP	Supply Current during Programming	—	10	—	mA	—
D136a	TRW	Row Write Time	1.32	—	1.74	ms	TRW = 11064 FRC cycles, TA = +85°C, see <b>Note 2</b>
D136b	TRW	Row Write Time	1.28	—	1.79	ms	TRW = 11064 FRC cycles, TA = +150°C, see <b>Note 2</b>
D137a	TPE	Page Erase Time	20.1	—	26.5	ms	TPE = 168517 FRC cycles, TA = +85°C, see <b>Note 2</b>
D137b	TPE	Page Erase Time	19.5	—	27.3	ms	TPE = 168517 FRC cycles, TA = +150°C, see <b>Note 2</b>
D138a	TWW	Word Write Cycle Time	42.3	—	55.9	μs	TWW = 355 FRC cycles, TA = +85°C, see <b>Note 2</b>
D138b	TWW	Word Write Cycle Time	41.1	—	57.6	μs	TWW = 355 FRC cycles, TA = +150°C, see <b>Note 2</b>

**Note 1:** Data in “Typ” column is at 3.3V, 25°C unless otherwise stated.

- 2:** Other conditions: FRC = 7.37 MHz, TUN<5:0> = b'011111 (for Min), TUN<5:0> = b'100000 (for Max). This parameter depends on the FRC accuracy (see Table 26-19) and the value of the FRC Oscillator Tuning register (see Register 9-4). For complete details on calculating the Minimum and Maximum time, see **Section 5.3 “Programming Operations”**.

**TABLE 26-13: INTERNAL VOLTAGE REGULATOR SPECIFICATIONS**

Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended							
Param.	Symbol	Characteristics	Min	Typ	Max	Units	Comments
—	CEFC	External Filter Capacitor Value	4.7	10	—	μF	Capacitor must be low series resistance (< 5 ohms)

# dsPIC33FJXXMXX06A/X08A/X10A

**TABLE 26-23: TIMER2, TIMER4, TIMER6 AND TIMER8 EXTERNAL CLOCK TIMING REQUIREMENTS**

AC CHARACTERISTICS				Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for Extended				
Param No.	Symbol	Characteristic		Min	Typ	Max	Units	Conditions
TB10	TtxH	TxCK High Time	Synchronous mode	Greater of 20 or (Tcy + 20)/N	—	—	ns	Must also meet parameter TB15 N = prescale value (1, 8, 64, 256)
					—	—	ns	
TB11	TtxL	TxCK Low Time	Synchronous mode	Greater of 20 or (Tcy + 20)/N	—	—	ns	Must also meet parameter TB15 N = prescale value (1, 8, 64, 256)
					—	—	ns	
TB15	TtxP	TxCK Input Period	Synchronous mode	Greater of 40 or (2Tcy + 40)/N	—	—	ns	N = prescale value (1, 8, 64, 256)
TB20	TCKEXT-MRL	Delay from External TxCK Clock Edge to Timer Increment		0.75 Tcy + 40	—	1.75 Tcy + 40	ns	—

**Note 1:** These parameters are characterized, but are not tested in manufacturing.

**TABLE 26-24: TIMER3, TIMER5, TIMER7 AND TIMER9 EXTERNAL CLOCK TIMING REQUIREMENTS**

AC CHARACTERISTICS				Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for Extended				
Param No.	Symbol	Characteristic		Min	Typ	Max	Units	Conditions
TC10	TtxH	TxCK High Time	Synchronous	$T_{CY} + 20$	—	—	ns	Must also meet parameter TC15
TC11	TtxL	TxCK Low Time	Synchronous	$T_{CY} + 20$	—	—	ns	Must also meet parameter TC15
TC15	TtxP	TxCK Input Period	Synchronous with prescaler	$2 T_{CY} + 40$	—	—	ns	N = prescale value (1, 8, 64, 256)
TC20	TCKEXTMRL	Delay from External TxCK Clock Edge to Timer Increment		$0.75 T_{CY} + 40$	—	$1.75 T_{CY} + 40$	—	—

**Note 1:** These parameters are characterized, but are not tested in manufacturing.

# dsPIC33FJXXMCMC06A/X08A/X10A

**TABLE 26-46: ADC CONVERSION (12-BIT MODE) TIMING REQUIREMENTS**

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	Symbol	Characteristic	Min.	Typ	Max.	Units	Conditions
<b>Clock Parameters</b>							
AD50a	TAD	ADC Clock Period	117.6	—	—	ns	—
AD51a	trc	ADC Internal RC Oscillator Period	—	250	—	ns	—
<b>Conversion Rate</b>							
AD55a	tCONV	Conversion Time	—	14 TAD	—	—	—
AD56a	FCNV	Throughput Rate	—	—	500	ksps	—
AD57a	TSAMP	Sample Time	3.0 TAD	—	—	—	—
<b>Timing Parameters</b>							
AD60a	tPCS	Conversion Start from Sample Trigger <sup>(1,2)</sup>	2.0 TAD	—	3.0 TAD	—	—
AD61a	tPSS	Sample Start from Setting Sample (SAMP) bit <sup>(1,2)</sup>	2.0 TAD	—	3.0 TAD	—	—
AD62a	tCSS	Conversion Completion to Sample Start (ASAM = 1) <sup>(1,2)</sup>	—	0.5 TAD	—	—	—
AD63a	tDPU	Time to Stabilize Analog Stage from ADC Off to ADC On <sup>(1,2,3)</sup>	—	—	20	μs	—

- Note 1:** Because the sample caps will eventually lose charge, clock rates below 10 kHz can affect linearity performance, especially at elevated temperatures.
- 2:** These parameters are characterized but not tested in manufacturing.
- 3:** tDPU is the time required for the ADC module to stabilize when it is turned on (AD1CON1<ADON> = 1). During this time, the ADC result is indeterminate.

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**TABLE 27-6: DC CHARACTERISTICS: I/O PIN OUTPUT SPECIFICATIONS**

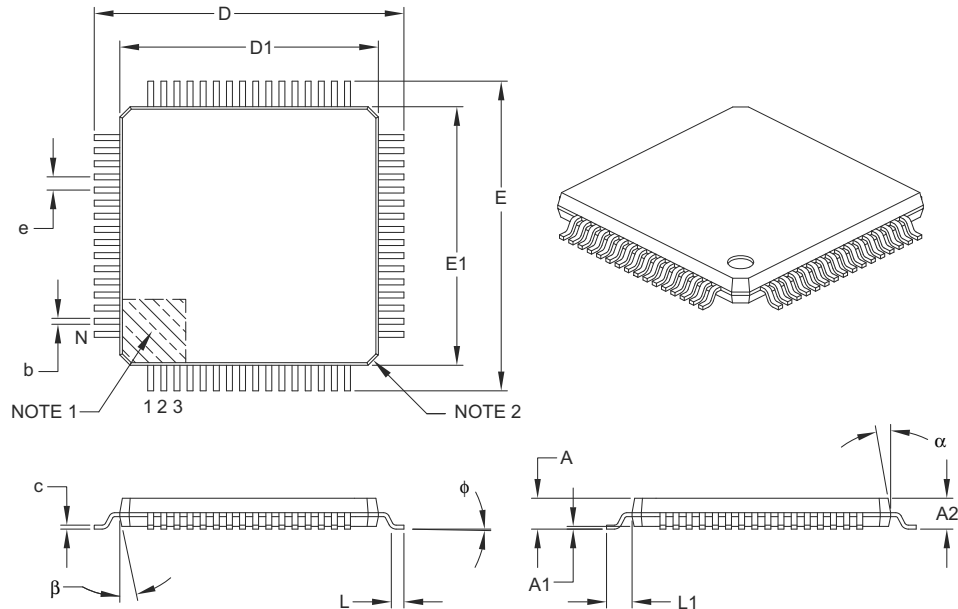
DC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for High Temperature				
Param.	Symbol	Characteristic	Min.	Typ.	Max.	Units	Conditions
HDO10	VOL	<b>Output Low Voltage</b> I/O Pins: 2x Sink Driver Pins - All pins not defined by 4x or 8x driver pins	—	—	0.4	V	$I_{OL} \leq 1.8 \text{ mA}$ , $V_{DD} = 3.3\text{V}$ See <b>Note 1</b>
		<b>Output Low Voltage</b> I/O Pins: 4x Sink Driver Pins - RA2, RA3, RA9, RA10, RA14, RA15, RB0, RB1, RB11, RF4, RF5, RG2, RG3	—	—	0.4	V	$I_{OL} \leq 3.6 \text{ mA}$ , $V_{DD} = 3.3\text{V}$ See <b>Note 1</b>
		<b>Output Low Voltage</b> I/O Pins: 8x Sink Driver Pins - OSC2, CLKO, RC15	—	—	0.4	V	$I_{OL} \leq 6 \text{ mA}$ , $V_{DD} = 3.3\text{V}$ See <b>Note 1</b>
HDO20	VOH	<b>Output High Voltage</b> I/O Pins: 2x Source Driver Pins - All pins not defined by 4x or 8x driver pins	2.4	—	—	V	$I_{OH} \geq -1.8 \text{ mA}$ , $V_{DD} = 3.3\text{V}$ See <b>Note 1</b>
		<b>Output High Voltage</b> I/O Pins: 4x Source Driver Pins - RA2, RA3, RA9, RA10, RA14, RA15, RB0, RB1, RB11, RF4, RF5, RG2, RG3	2.4	—	—	V	$I_{OH} \geq -3 \text{ mA}$ , $V_{DD} = 3.3\text{V}$ See <b>Note 1</b>
		<b>Output High Voltage</b> I/O Pins: 8x Source Driver Pins - OSC2, CLKO, RC15	2.4	—	—	V	$I_{OH} \geq -6 \text{ mA}$ , $V_{DD} = 3.3\text{V}$ See <b>Note 1</b>
HDO20A	VOH1	<b>Output High Voltage</b> I/O Pins: 2x Source Driver Pins - All pins not defined by 4x or 8x driver pins	1.5	—	—	V	$I_{OH} \geq -1.9 \text{ mA}$ , $V_{DD} = 3.3\text{V}$ See <b>Note 1</b>
			2.0	—	—		$I_{OH} \geq -1.85 \text{ mA}$ , $V_{DD} = 3.3\text{V}$ See <b>Note 1</b>
			3.0	—	—		$I_{OH} \geq -1.4 \text{ mA}$ , $V_{DD} = 3.3\text{V}$ See <b>Note 1</b>
		<b>Output High Voltage</b> 4x Source Driver Pins - RA2, RA3, RA9, RA10, RA14, RA15, RB0, RB1, RB11, RF4, RF5, RG2, RG3	1.5	—	—	V	$I_{OH} \geq -3.9 \text{ mA}$ , $V_{DD} = 3.3\text{V}$ See <b>Note 1</b>
			2.0	—	—		$I_{OH} \geq -3.7 \text{ mA}$ , $V_{DD} = 3.3\text{V}$ See <b>Note 1</b>
			3.0	—	—		$I_{OH} \geq -2 \text{ mA}$ , $V_{DD} = 3.3\text{V}$ See <b>Note 1</b>
		<b>Output High Voltage</b> 8x Source Driver Pins - OSC2, CLKO, RC15	1.5	—	—	V	$I_{OH} \geq -7.5 \text{ mA}$ , $V_{DD} = 3.3\text{V}$ See <b>Note 1</b>
			2.0	—	—		$I_{OH} \geq -6.8 \text{ mA}$ , $V_{DD} = 3.3\text{V}$ See <b>Note 1</b>
			3.0	—	—		$I_{OH} \geq -3 \text{ mA}$ , $V_{DD} = 3.3\text{V}$ See <b>Note 1</b>

**Note 1:** Parameters are characterized, but not tested.

# dsPIC33FJXXXMCX06A/X08A/X10A

## 64-Lead Plastic Thin Quad Flatpack (PT) – 10x10x1 mm Body, 2.00 mm [TQFP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Number of Leads	N	64		
Lead Pitch	e	0.50 BSC		
Overall Height	A	–	–	1.20
Molded Package Thickness	A2	0.95	1.00	1.05
Standoff	A1	0.05	–	0.15
Foot Length	L	0.45	0.60	0.75
Footprint	L1	1.00 REF		
Foot Angle	$\phi$	0°	3.5°	7°
Overall Width	E	12.00 BSC		
Overall Length	D	12.00 BSC		
Molded Package Width	E1	10.00 BSC		
Molded Package Length	D1	10.00 BSC		
Lead Thickness	c	0.09	–	0.20
Lead Width	b	0.17	0.22	0.27
Mold Draft Angle Top	$\alpha$	11°	12°	13°
Mold Draft Angle Bottom	$\beta$	11°	12°	13°

### Notes:

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- Chamfers at corners are optional; size may vary.
- Dimensions D1 and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.25 mm per side.
- Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-085B