



Welcome to [E-XFL.COM](#)

What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	40 MIPS
Connectivity	CANbus, I ² C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, Motor Control PWM, POR, PWM, QEI, WDT
Number of I/O	53
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 16x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-VQFN Exposed Pad
Supplier Device Package	64-VQFN (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33fj64mc506a-i-mr

dsPIC33FJXXXMCX06A/X08A/X10A

Referenced Sources

This device data sheet is based on the following individual chapters of the “dsPIC33F/PIC24H Family Reference Manual”. These documents should be considered as the general reference for the operation of a particular module or device feature.

Note: To access the documents listed below, browse to the documentation section of the dsPIC33FJ256MC710A product page on the Microchip web site (www.microchip.com) or select a family reference manual section from the following list.

In addition to parameters, features, and other documentation, the resulting page provides links to the related family reference manual sections.

- **Section 1. “Introduction”** (DS70197)
- **Section 2. “CPU”** (DS70204)
- **Section 3. “Data Memory”** (DS70202)
- **Section 4. “Program Memory”** (DS70203)
- **Section 5. “Flash Programming”** (DS70191)
- **Section 6. “Interrupts”** (DS70184)
- **Section 7. “Oscillator”** (DS70186)
- **Section 8. “Reset”** (DS70192)
- **Section 9. “Watchdog Timer and Power-Saving Modes”** (DS70196)
- **Section 10. “I/O Ports”** (DS70193)
- **Section 11. “Timers”** (DS70205)
- **Section 12. “Input Capture”** (DS70198)
- **Section 13. “Output Compare”** (DS70209)
- **Section 14. “Motor Control PWM”** (DS70187)
- **Section 15. “Quadrature Encoder Interface (QEI)”** (DS70208)
- **Section 16. “Analog-to-Digital Converter (ADC)”** (DS70183)
- **Section 17. “UART”** (DS70188)
- **Section 18. “Serial Peripheral Interface (SPI)”** (DS70206)
- **Section 19. “Inter-Integrated Circuit™ (I2C™)”** (DS70195)
- **Section 20. “Data Converter Interface (DCI)”** (DS70288)
- **Section 21. “Enhanced Controller Area Network (ECAN™)”** (DS70185)
- **Section 22. “Direct Memory Access (DMA)”** (DS70182)
- **Section 23. “CodeGuard™ Security”** (DS70199)
- **Section 24. “Programming and Diagnostics”** (DS70207)
- **Section 25. “Device Configuration”** (DS70194)

dsPIC33FJXXXMCX06A/X08A/X10A

1.0 DEVICE OVERVIEW

Note 1: This data sheet summarizes the features of the dsPIC33FJXXXMCX06A/X08A/X10A family of devices. However, it is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the “dsPIC33F/PIC24H Family Reference Manual”. Please see the Microchip web site (www.microchip.com) for the latest dsPIC33F/PIC24H Family Reference Manual sections.

2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 “Memory Organization”** in this data sheet for device-specific register and bit information.

This document contains device-specific information for the following devices:

- dsPIC33FJ64MC506A
- dsPIC33FJ64MC508A
- dsPIC33FJ64MC510A
- dsPIC33FJ64MC706A
- dsPIC33FJ64MC710A
- dsPIC33FJ128MC506A
- dsPIC33FJ128MC510A
- dsPIC33FJ128MC706A
- dsPIC33FJ128MC708A
- dsPIC33FJ128MC710A
- dsPIC33FJ256MC510A
- dsPIC33FJ256MC710A

The dsPIC33FJXXXMCX06A/X08A/X10A includes devices with a wide range of pin counts (64, 80 and 100), different program memory sizes (64 Kbytes, 128 Kbytes and 256 Kbytes) and different RAM sizes (8 Kbytes, 16 Kbytes and 30 Kbytes).

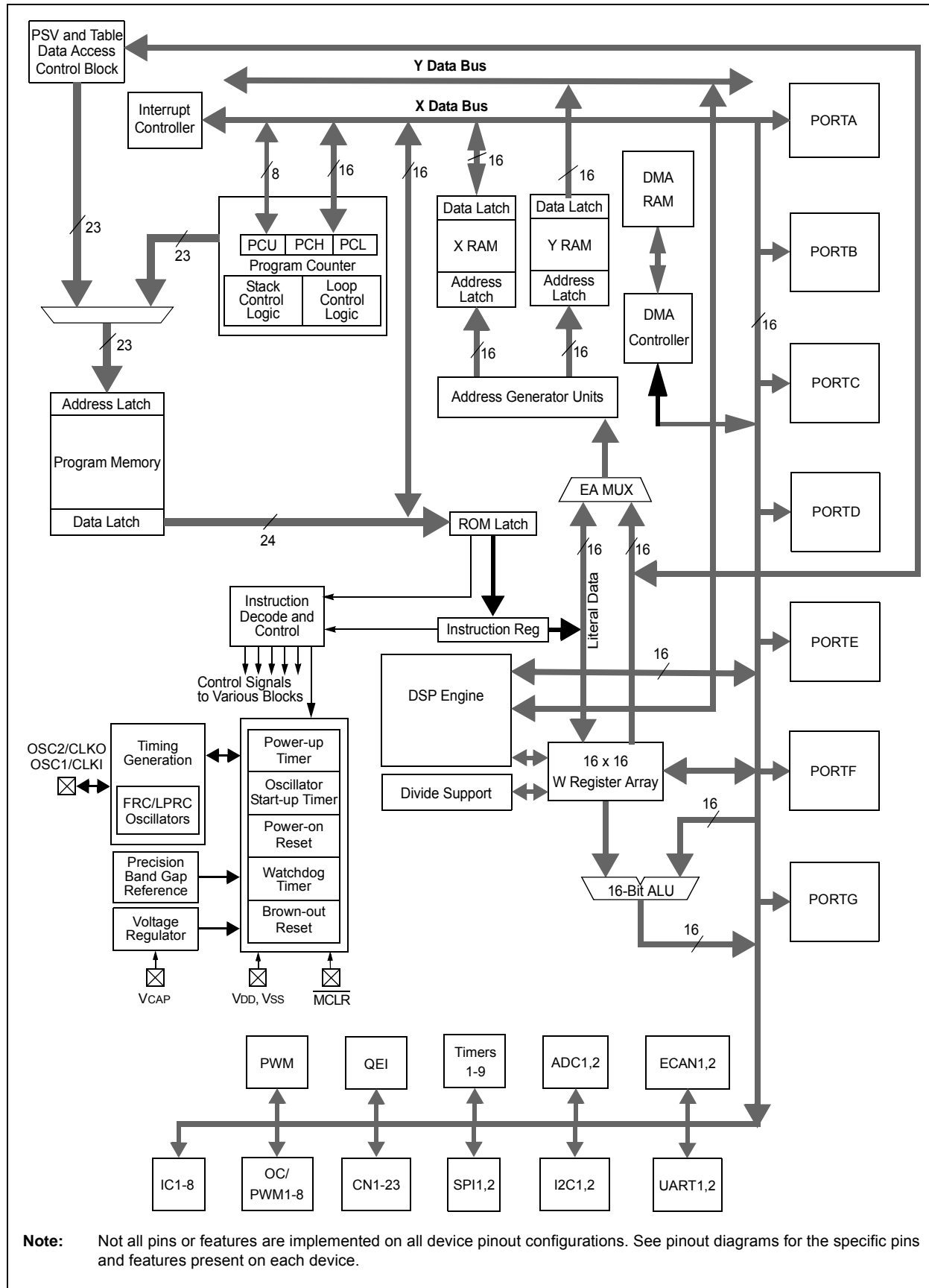
These features make this family suitable for a wide variety of high-performance, digital signal control applications. The devices are pin compatible with the PIC24H family of devices, and also share a very high degree of compatibility with the dsPIC30F family devices. This allows easy migration between device families as may be necessitated by the specific functionality, computational resource and system cost requirements of the application.

The dsPIC33FJXXXMCX06A/X08A/X10A family of devices employs a powerful 16-bit architecture that seamlessly integrates the control features of a Microcontroller (MCU) with the computational capabilities of a Digital Signal Processor (DSP). The resulting functionality is ideal for applications that rely on high-speed, repetitive computations, as well as control.

The DSP engine, dual 40-bit accumulators, hardware support for division operations, barrel shifter, 17 x 17 multiplier, a large array of 16-bit working registers and a wide variety of data addressing modes, together, provide the dsPIC33FJXXXMCX06A/X08A/X10A Central Processing Unit (CPU) with extensive mathematical processing capability. Flexible and deterministic interrupt handling, coupled with a powerful array of peripherals, renders the dsPIC33FJXXXMCX06A/X08A/X10A devices suitable for control applications. Further, Direct Memory Access (DMA) enables overhead-free transfer of data between several peripherals and a dedicated DMA RAM. Reliable, field programmable Flash program memory ensures scalability of applications that use dsPIC33FJXXXMCX06A/X08A/X10A devices.

dsPIC33FJXXXMCX06A/X08A/X10A

FIGURE 1-1: dsPIC33FJXXXMCX06A/X08A/X10A GENERAL BLOCK DIAGRAM



dsPIC33FJXXMCX06A/X08A/X10A

3.0 CPU

Note 1: This data sheet summarizes the features of the dsPIC33FJXXMCX06A/X08A/X10A family of devices. However, it is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 2. “CPU”** (DS70204) in the “dsPIC33F/PIC24H Family Reference Manual”, which is available from the Microchip web site (www.microchip.com).

2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 “Memory Organization”** in this data sheet for device-specific register and bit information.

The dsPIC33FJXXMCX06A/X08A/X10A CPU module has a 16-bit (data) modified Harvard architecture with an enhanced instruction set, including significant support for DSP. The CPU has a 24-bit instruction word with a variable length opcode field. The Program Counter (PC) is 23 bits wide and addresses up to 4M x 24 bits of user program memory space. The actual amount of program memory implemented varies by device. A single-cycle instruction prefetch mechanism is used to help maintain throughput and provides predictable execution. All instructions execute in a single cycle, with the exception of instructions that change the program flow, the double word move (MOV.D) instruction and the table instructions. Overhead-free program loop constructs are supported using the DO and REPEAT instructions, both of which are interruptible at any point.

The dsPIC33FJXXMCX06A/X08A/X10A devices have sixteen, 16-bit working registers in the programmer's model. Each of the working registers can serve as a data, address or address offset register. The 16th working register (W15) operates as a software Stack Pointer (SP) for interrupts and calls.

The dsPIC33FJXXMCX06A/X08A/X10A instruction set has two classes of instructions: MCU and DSP. These two instruction classes are seamlessly integrated into a single CPU. The instruction set includes many addressing modes and is designed for optimum 'C' compiler efficiency. For most instructions, the dsPIC33FJXXMCX06A/X08A/X10A devices are capable of executing a data (or program data) memory read, a working register (data) read, a data memory write and a program (instruction) memory read per instruction cycle. As a result, three parameter instructions can be supported, allowing $A + B = C$ operations to be executed in a single cycle.

A block diagram of the CPU is shown in Figure 3-1 and the programmer's model for the dsPIC33FJXXMCX06A/X08A/X10A is shown in Figure 3-2.

3.1 Data Addressing Overview

The data space can be addressed as 32K words or 64 Kbytes, and is split into two blocks referred to as X and Y data memory. Each memory block has its own independent Address Generation Unit (AGU). The MCU class of instructions operates solely through the X memory AGU, which accesses the entire memory map as one linear data space. Certain DSP instructions operate through the X and Y AGUs to support dual operand reads, which splits the data address space into two parts. The X and Y data space boundary is device-specific.

Overhead-free circular buffers (Modulo Addressing mode) are supported in both X and Y address spaces. The Modulo Addressing removes the software boundary checking overhead for DSP algorithms. Furthermore, the X AGU circular addressing can be used with any of the MCU class of instructions. The X AGU also supports Bit-Reversed Addressing to greatly simplify input or output data reordering for radix-2 FFT algorithms.

The upper 32 Kbytes of the data space memory map can optionally be mapped into program space at any 16K program word boundary defined by the 8-bit Program Space Visibility Page register (PSVPAG). The program to data space mapping feature lets any instruction access program space as if it were data space.

The data space also includes 2 Kbytes of DMA RAM, which is primarily used for DMA data transfers but may be used as general purpose RAM.

3.2 DSP Engine Overview

The DSP engine features a high-speed, 17-bit by 17-bit multiplier, a 40-bit ALU, two 40-bit saturating accumulators and a 40-bit bidirectional barrel shifter. The barrel shifter is capable of shifting a 40-bit value up to 16 bits right or left in a single cycle. The DSP instructions operate seamlessly with all other instructions and have been designed for optimal real-time performance. The MAC instruction and other associated instructions can concurrently fetch two data operands from memory while multiplying two W registers, and accumulating and optionally saturating the result in the same cycle. This instruction functionality requires that the RAM memory data space be split for these instructions and linear for all others. Data space partitioning is achieved in a transparent and flexible manner through dedicating certain working registers to each address space.

dsPIC33FJXXXMCX06A/X08A/X10A

REGISTER 3-2: CORCON: CORE CONTROL REGISTER

U-0	U-0	U-0	R/W-0	R/W-0	R-0	R-0	R-0
—	—	—	US	EDT ⁽¹⁾	DL<2:0>		
bit 15			bit 8				

R/W-0	R/W-0	R/W-1	R/W-0	R/C-0	R/W-0	R/W-0	R/W-0
SATA	SATB	SATDW	ACCSAT	IPL3 ⁽²⁾	PSV	RND	IF
bit 7							
							bit 0

Legend:	C = Clearable bit		
R = Readable bit	W = Writable bit	-n = Value at POR	'1' = Bit is set
0' = Bit is cleared	'x' = Bit is unknown	U = Unimplemented bit, read as '0'	

- bit 15-13 **Unimplemented:** Read as '0'
- bit 12 **US:** DSP Multiply Unsigned/Signed Control bit
 1 = DSP engine multiplies are unsigned
 0 = DSP engine multiplies are signed
- bit 11 **EDT:** Early DO Loop Termination Control bit⁽¹⁾
 1 = Terminate executing DO loop at end of current loop iteration
 0 = No effect
- bit 10-8 **DL<2:0>:** DO Loop Nesting Level Status bits
 111 = 7 DO loops active
 .
 .
 .
 001 = 1 DO loop active
 000 = 0 DO loops active
- bit 7 **SATA:** AccA Saturation Enable bit
 1 = Accumulator A saturation enabled
 0 = Accumulator A saturation disabled
- bit 6 **SATB:** AccB Saturation Enable bit
 1 = Accumulator B saturation enabled
 0 = Accumulator B saturation disabled
- bit 5 **SATDW:** Data Space Write from DSP Engine Saturation Enable bit
 1 = Data space write saturation enabled
 0 = Data space write saturation disabled
- bit 4 **ACCSAT:** Accumulator Saturation Mode Select bit
 1 = 9.31 saturation (super saturation)
 0 = 1.31 saturation (normal saturation)
- bit 3 **IPL3:** CPU Interrupt Priority Level Status bit 3⁽²⁾
 1 = CPU interrupt priority level is greater than 7
 0 = CPU interrupt priority level is 7 or less
- bit 2 **PSV:** Program Space Visibility in Data Space Enable bit
 1 = Program space visible in data space
 0 = Program space not visible in data space
- bit 1 **RND:** Rounding Mode Select bit
 1 = Biased (conventional) rounding enabled
 0 = Unbiased (convergent) rounding enabled
- bit 0 **IF:** Integer or Fractional Multiplier Mode Select bit
 1 = Integer mode enabled for DSP multiply ops
 0 = Fractional mode enabled for DSP multiply ops

Note 1: This bit will always read as '0'.

2: The IPL3 bit is concatenated with the IPL<2:0> bits (SR<7:5>) to form the CPU interrupt priority level.

TABLE 4-5: INTERRUPT CONTROLLER REGISTER MAP

SFR Name	SFR Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
INTCON1	0080	NSTDIS	OVAERR	OVBERR	COVAERR	COVBERR	OVATE	OVBTE	COVTE	SFTACERR	DIV0ERR	DMACERR	MATHERR	ADDRRERR	STKERR	OSCFAIL	—	0000
INTCON2	0082	ALTIVT	DISI	—	—	—	—	—	—	—	—	—	INT4EP	INT3EP	INT2EP	INT1EP	INT0EP	0000
IFS0	0084	—	DMA1IF	AD1IF	U1TXIF	U1RXIF	SPI1IF	SPI1EIF	T3IF	T2IF	OC2IF	IC2IF	DMA0IF	T1IF	OC1IF	IC1IF	INT0IF	0000
IFS1	0086	U2TXIF	U2RXIF	INT2IF	T5IF	T4IF	OC4IF	OC3IF	DMA2IF	IC8IF	IC7IF	AD2IF	INT1IF	CNIF	—	MI2C1IF	SI2C1IF	0000
IFS2	0088	T6IF	DMA4IF	—	OC8IF	OC7IF	OC6IF	OC5IF	IC6IF	IC5IF	IC4IF	IC3IF	DMA3IF	C1IF	C1RXIF	SPI2IF	SPI2EIF	0000
IFS3	008A	FLTAIF	—	DMA5IF	—	—	QEIIF	PWMIF	C2IF	C2RXIF	INT4IF	INT3IF	T9IF	T8IF	MI2C2IF	SI2C2IF	T7IF	0000
IFS4	008C	—	—	—	—	—	—	—	—	C2TXIF	C1TXIF	DMA7IF	DMA6IF	—	U2EIF	U1EIF	FLTBIF	0000
IEC0	0094	—	DMA1IE	AD1IE	U1TXIE	U1RXIE	SPI1IE	SPI1EIE	T3IE	T2IE	OC2IE	IC2IE	DMA0IE	T1IE	OC1IE	IC1IE	INT0IE	0000
IEC1	0096	U2TXIE	U2RXIE	INT2IE	T5IE	T4IE	OC4IE	OC3IE	DMA2IE	IC8IE	IC7IE	AD2IE	INT1IE	CNIE	—	MI2C1IE	SI2C1IE	0000
IEC2	0098	T6IE	DMA4IE	—	OC8IE	OC7IE	OC6IE	OC5IE	IC6IE	IC5IE	IC4IE	IC3IE	DMA3IE	C1IE	C1RXIE	SPI2IE	SPI2EIE	0000
IEC3	009A	FLTAIE	—	DMA5IE	—	—	QEIE	PWMIE	C2IE	C2RXIE	INT4IE	INT3IE	T9IE	T8IE	MI2C2IE	SI2C2IE	T7IE	0000
IEC4	009C	—	—	—	—	—	—	—	—	C2TXIE	C1TXIE	DMA7IE	DMA6IE	—	U2EIE	U1EIE	FLTBIE	0000
IPC0	00A4	—	T1IP<2:0>			—	OC1IP<2:0>			—	IC1IP<2:0>			—	INT0IP<2:0>			4444
IPC1	00A6	—	T2IP<2:0>			—	OC2IP<2:0>			—	IC2IP<2:0>			—	DMA0IP<2:0>			4444
IPC2	00A8	—	U1RXIP<2:0>			—	SPI1IP<2:0>			—	SPI1EIP<2:0>			—	T3IP<2:0>			4444
IPC3	00AA	—	—	—	—	—	DMA1IP<2:0>			—	AD1IP<2:0>			—	U1TXIP<2:0>			0444
IPC4	00AC	—	CNIP<2:0>			—	—	—	—	—	MI2C1IP<2:0>			—	SI2C1IP<2:0>			4044
IPC5	00AE	—	IC8IP<2:0>			—	IC7IP<2:0>			—	AD2IP<2:0>			—	INT1IP<2:0>			4444
IPC6	00B0	—	T4IP<2:0>			—	OC4IP<2:0>			—	OC3IP<2:0>			—	DMA2IP<2:0>			4444
IPC7	00B2	—	U2TXIP<2:0>			—	U2RXIP<2:0>			—	INT2IP<2:0>			—	T5IP<2:0>			4444
IPC8	00B4	—	C1IP<2:0>			—	C1RXIP<2:0>			—	SPI2IP<2:0>			—	SPI2EIP<2:0>			4444
IPC9	00B6	—	IC5IP<2:0>			—	IC4IP<2:0>			—	IC3IP<2:0>			—	DMA3IP<2:0>			4444
IPC10	00B8	—	OC7IP<2:0>			—	OC6IP<2:0>			—	OC5IP<2:0>			—	IC6IP<2:0>			4444
IPC11	00BA	—	T6IP<2:0>			—	DMA4IP<2:0>			—	—	—	—	—	OC8IP<2:0>			4404
IPC12	00BC	—	T8IP<2:0>			—	MI2C2IP<2:0>			—	SI2C2IP<2:0>			—	T7IP<2:0>			4444
IPC13	00BE	—	C2RXIP<2:0>			—	INT4IP<2:0>			—	INT3IP<2:0>			—	T9IP<2:0>			4444
IPC14	00C0	—	—	—	—	—	QEIIP<2:0>			—	PWMIP<2:0>			—	C2IP<2:0>			0444
IPC15	00C2	—	FLTAIP<2:0>			—	—	—	—	—	DMA5IP<2:0>			—	—	—	—	4040
IPC16	00C4	—	—	—	—	—	U2EIP<2:0>			—	U1EIP<2:0>			—	FLTBIP<2:0>			0444
IPC17	00C6	—	C2TXIP<2:0>			—	C1TXIP<2:0>			—	DMA7IP<2:0>			—	DMA6IP<2:0>			4444
INTTREG	00E0	—	—	—	—	ILR<3:0>				—	VECNUM<6:0>							0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-6: TIMER REGISTER MAP

SFR Name	SFR Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TMR1	0100	Timer1 Register																0000
PR1	0102	Period Register 1																FFFF
T1CON	0104	TON	—	TSIDL	—	—	—	—	—	—	TGATE	TCKPS<1:0>	—	TSYNC	TCS	—	0000	
TMR2	0106	Timer2 Register																0000
TMR3HLD	0108	Timer3 Holding Register (for 32-bit timer operations only)																xxxx
TMR3	010A	Timer3 Register																0000
PR2	010C	Period Register 2																FFFF
PR3	010E	Period Register 3																FFFF
T2CON	0110	TON	—	TSIDL	—	—	—	—	—	—	TGATE	TCKPS<1:0>	T32	—	TCS	—	0000	
T3CON	0112	TON	—	TSIDL	—	—	—	—	—	—	TGATE	TCKPS<1:0>	—	—	TCS	—	0000	
TMR4	0114	Timer4 Register																0000
TMR5HLD	0116	Timer5 Holding Register (for 32-bit operations only)																xxxx
TMR5	0118	Timer5 Register																0000
PR4	011A	Period Register 4																FFFF
PR5	011C	Period Register 5																FFFF
T4CON	011E	TON	—	TSIDL	—	—	—	—	—	—	TGATE	TCKPS<1:0>	T32	—	TCS	—	0000	
T5CON	0120	TON	—	TSIDL	—	—	—	—	—	—	TGATE	TCKPS<1:0>	—	—	TCS	—	0000	
TMR6	0122	Timer6 Register																0000
TMR7HLD	0124	Timer7 Holding Register (for 32-bit operations only)																xxxx
TMR7	0126	Timer7 Register																0000
PR6	0128	Period Register 6																FFFF
PR7	012A	Period Register 7																FFFF
T6CON	012C	TON	—	TSIDL	—	—	—	—	—	—	TGATE	TCKPS<1:0>	T32	—	TCS	—	0000	
T7CON	012E	TON	—	TSIDL	—	—	—	—	—	—	TGATE	TCKPS<1:0>	—	—	TCS	—	0000	
TMR8	0130	Timer8 Register																0000
TMR9HLD	0132	Timer9 Holding Register (for 32-bit operations only)																xxxx
TMR9	0134	Timer9 Register																0000
PR8	0136	Period Register 8																FFFF
PR9	0138	Period Register 9																FFFF
T8CON	013A	TON	—	TSIDL	—	—	—	—	—	—	TGATE	TCKPS<1:0>	T32	—	TCS	—	0000	
T9CON	013C	TON	—	TSIDL	—	—	—	—	—	—	TGATE	TCKPS<1:0>	—	—	TCS	—	0000	

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

dsPIC33FJXXMXX06A/X08A/X10A

Modulo Addressing can operate in either data or program space (since the Data Pointer mechanism is essentially the same for both). One circular buffer can be supported in each of the X (which also provides the pointers into program space) and Y data spaces. Modulo Addressing can operate on any W register pointer. However, it is not advisable to use W14 or W15 for Modulo Addressing, since these two registers are used as the Stack Frame Pointer and Stack Pointer, respectively.

In general, any particular circular buffer can only be configured to operate in one direction, as there are certain restrictions on the buffer start address (for incrementing buffers) or end address (for decrementing buffers), based upon the direction of the buffer.

The only exception to the usage restrictions is for buffers which have a power-of-2 length. As these buffers satisfy the start and end address criteria, they may operate in a bidirectional mode (i.e., address boundary checks will be performed on both the lower and upper address boundaries).

4.4.1 START AND END ADDRESS

The Modulo Addressing scheme requires that a starting and ending address be specified and loaded into the 16-bit Modulo Buffer Address registers: XMODSRT, XMODEND, YMODSRT and YMODEND (see Table 4-1).

Note: Y space Modulo Addressing EA calculations assume word-sized data (LSb of every EA is always clear).

The length of a circular buffer is not directly specified. It is determined by the difference between the corresponding start and end addresses. The maximum possible length of the circular buffer is 32K words (64 Kbytes).

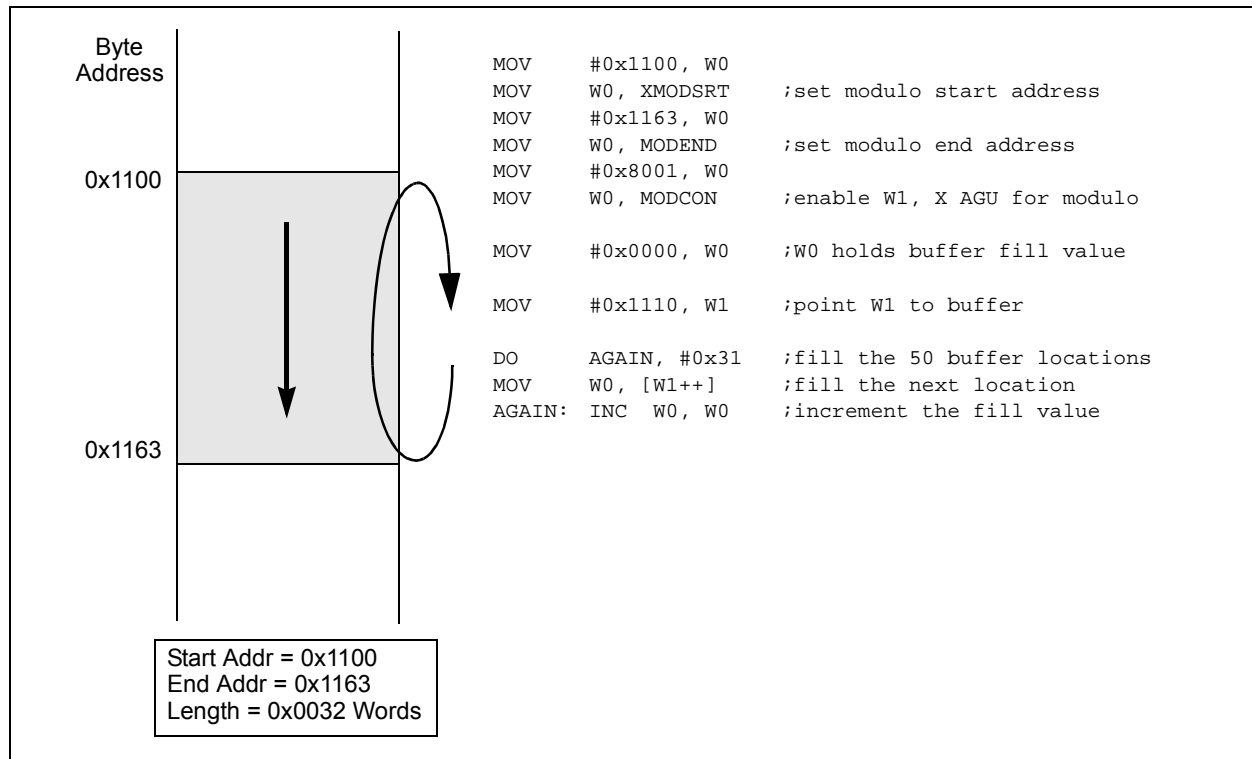
4.4.2 W ADDRESS REGISTER SELECTION

The Modulo and Bit-Reversed Addressing Control register, MODCON<15:0>, contains enable flags as well as a W register field to specify the W Address registers. The XWM and YWM fields select which registers will operate with Modulo Addressing. If XWM = 15, X RAGU and X WAGU Modulo Addressing are disabled. Similarly, if YWM = 15, Y AGU Modulo Addressing is disabled.

The X Address Space Pointer W register (XWM) to which Modulo Addressing is to be applied is stored in MODCON<3:0> (see Table 4-1). Modulo Addressing is enabled for X data space when XWM is set to any value other than 15 and the XMODEN bit is set at MODCON<15>.

The Y Address Space Pointer W register (YWM) to which Modulo Addressing is to be applied is stored in MODCON<7:4>. Modulo Addressing is enabled for Y data space when YWM is set to any value other than 15 and the YMODEN bit is set at MODCON<14>.

FIGURE 4-7: MODULO ADDRESSING OPERATION EXAMPLE



dsPIC33FJXXMCX06A/X08A/X10A

6.0 RESET

Note 1: This data sheet summarizes the features of the dsPIC33FJXXMCX06A/X08A/X10A family of devices. However, it is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 8. “Reset”** (DS70192) in the “dsPIC33F/PIC24H Family Reference Manual”, which is available from the Microchip web site (www.microchip.com).

2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 “Memory Organization”** in this data sheet for device-specific register and bit information.

The Reset module combines all Reset sources and controls the device Master Reset Signal, $\overline{\text{SYSRST}}$. The following is a list of device Reset sources:

- POR: Power-on Reset
- BOR: Brown-out Reset
- MCLR: Master Clear Pin Reset
- SWR: RESET Instruction
- WDT: Watchdog Timer Reset
- TRAPR: Trap Conflict Reset
- IOPUWR: Illegal Opcode and Uninitialized W Register Reset

A simplified block diagram of the Reset module is shown in Figure 6-1.

Any active source of Reset will make the $\overline{\text{SYSRST}}$ signal active. Many registers associated with the CPU and peripherals are forced to a known Reset state. Most registers are unaffected by a Reset; their status is unknown on POR and unchanged by all other Resets.

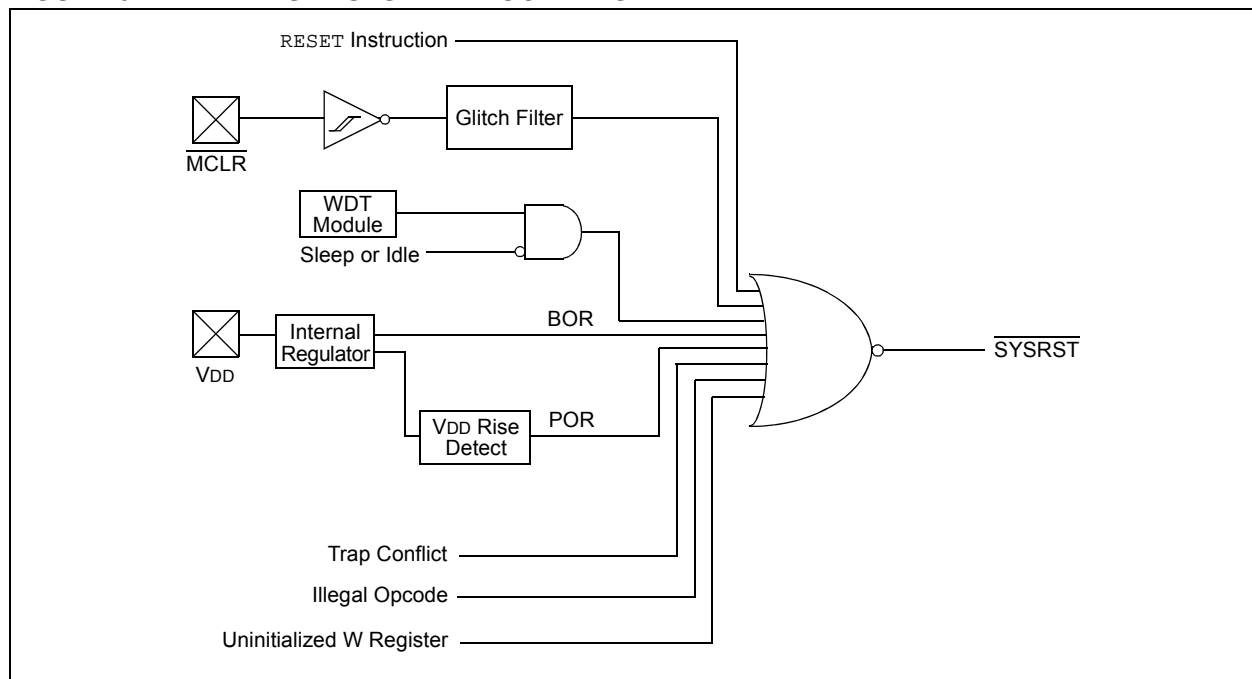
Note: Refer to the specific peripheral or CPU section of this data sheet for register Reset states.

All types of device Reset will set a corresponding status bit in the RCON register to indicate the type of Reset (see Register 6-1). A POR will clear all bits except for the POR bit ($\text{RCON}<0>$), which is set. The user can set or clear any bit at any time during code execution. The RCON bits only serve as status bits. Setting a particular Reset status bit in software does not cause a device Reset to occur.

The RCON register also has other bits associated with the Watchdog Timer and device power-saving states. The function of these bits is discussed in other sections of this manual.

Note: The status bits in the RCON register should be cleared after they are read so that the next RCON register value after a device Reset will be meaningful.

FIGURE 6-1: RESET SYSTEM BLOCK DIAGRAM



dsPIC33FJXXMCX06A/X08A/X10A

10.0 POWER-SAVING FEATURES

Note 1: This data sheet summarizes the features of the dsPIC33FJXXMCX06A/X08A/X10A family of devices. However, it is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 9. “Watchdog Timer and Power-Saving Modes”** (DS70196) in the “dsPIC33F/PIC24H Family Reference Manual”, which is available from the Microchip web site (www.microchip.com).

2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 “Memory Organization”** in this data sheet for device-specific register and bit information.

The dsPIC33FJXXMCX06A/X08A/X10A devices provide the ability to manage power consumption by selectively managing clocking to the CPU and the peripherals. In general, a lower clock frequency and a reduction in the number of circuits being clocked constitutes lower consumed power. dsPIC33FJXXMCX06A/X08A/X10A devices can manage power consumption in four different ways:

- Clock frequency
- Instruction-based Sleep and Idle modes
- Software-controlled Doze mode
- Selective peripheral control in software

Combinations of these methods can be used to selectively tailor an application's power consumption while still maintaining critical application features, such as timing-sensitive communications.

10.1 Clock Frequency and Clock Switching

dsPIC33FJXXMCX06A/X08A/X10A devices allow a wide range of clock frequencies to be selected under application control. If the system clock configuration is not locked, users can choose low-power or high-precision oscillators by simply changing the NOSC bits (OSCCON<10:8>). The process of changing a system clock during operation, as well as limitations to the process, are discussed in more detail in **Section 9.0 “Oscillator Configuration”**.

10.2 Instruction-Based Power-Saving Modes

dsPIC33FJXXMCX06A/X08A/X10A devices have two special power-saving modes that are entered through the execution of a special PWRSAV instruction. Sleep mode stops clock operation and halts all code execution. Idle mode halts the CPU and code execution, but allows peripheral modules to continue operation. The assembly syntax of the PWRSAV instruction is shown in Example 10-1.

Note: SLEEP_MODE and IDLE_MODE are constants defined in the assembler include file for the selected device.

Sleep and Idle modes can be exited as a result of an enabled interrupt, WDT time-out or a device Reset. When the device exits these modes, it is said to “wake-up”.

10.2.1 SLEEP MODE

Sleep mode has the following features:

- The system clock source is shut down. If an on-chip oscillator is used, it is turned off.
- The device current consumption is reduced to a minimum, provided that no I/O pin is sourcing current.
- The Fail-Safe Clock Monitor does not operate during Sleep mode since the system clock source is disabled.
- The LPRC clock continues to run in Sleep mode if the WDT is enabled.
- The WDT, if enabled, is automatically cleared prior to entering Sleep mode.
- Some device features or peripherals may continue to operate in Sleep mode. This includes items such as the input change notification on the I/O ports and peripherals that use an external clock input. Any peripheral that requires the system clock source for its operation is disabled in Sleep mode.

The device will wake-up from Sleep mode on any of the following events:

- Any interrupt source that is individually enabled
- Any form of device Reset
- A WDT time-out

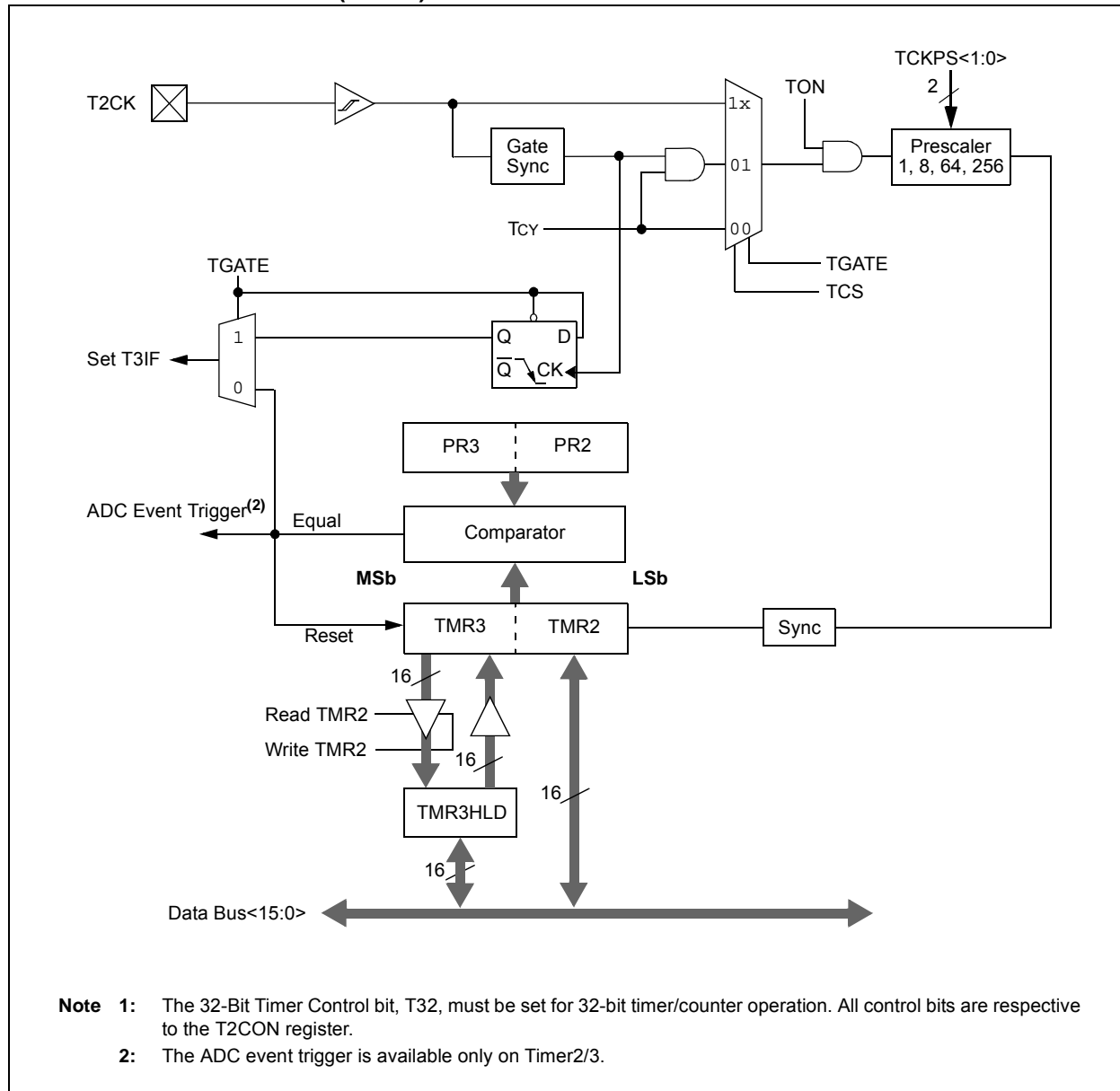
On wake-up from Sleep, the processor restarts with the same clock source that was active when Sleep mode was entered.

EXAMPLE 10-1: PWRSAV INSTRUCTION SYNTAX

```
PWRSAV #SLEEP_MODE    ; Put the device into SLEEP mode
PWRSAV #IDLE_MODE      ; Put the device into IDLE mode
```

dsPIC33FJXXXMCX06A/X08A/X10A

FIGURE 13-1: TIMER2/3 (32-BIT) BLOCK DIAGRAM⁽¹⁾



dsPIC33FJXXXMCX06A/X08A/X10A

REGISTER 21-9: CiCFG1: ECAN™ BAUD RATE CONFIGURATION REGISTER 1

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
SJW<1:0>		BRP<5:0>					
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-8 **Unimplemented:** Read as '0'

bit 7-6 **SJW<1:0>:** Synchronization Jump Width bits

11 = Length is 4 x TQ

10 = Length is 3 x TQ

01 = Length is 2 x TQ

00 = Length is 1 x TQ

bit 5-0 **BRP<5:0>:** Baud Rate Prescaler bits

11 1111 = TQ = 2 x 64 x 1/FCAN

•

•

•

00 0010 = TQ = 2 x 3 x 1/FCAN

00 0001 = TQ = 2 x 2 x 1/FCAN

00 0000 = TQ = 2 x 1 x 1/FCAN

dsPIC33FJXXXMCX06A/X08A/X10A

REGISTER 22-2: ADxCON2: ADCx CONTROL REGISTER 2 (CONTINUED) (where x = 1 or 2)

bit 0 **ALTS:** Alternate Input Sample Mode Select bit
1 = Uses channel input selects for Sample A on first sample and Sample B on next sample
0 = Always uses channel input selects for Sample A

dsPIC33FJXXMCMC06A/X08A/X10A

23.0 SPECIAL FEATURES

- Note 1:** This data sheet summarizes the features of the dsPIC33FJXXMCMC06A/X08A/X10A family of devices. However, it is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 23. “CodeGuard™ Security”** (DS70199), **Section 24. “Programming and Diagnostics”** (DS70207) and **Section 25. “Device Configuration”** (DS70194) in the “dsPIC33F/PIC24H Family Reference Manual”, which are available from the Microchip web site (www.microchip.com).
- 2:** Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 “Memory Organization”** in this data sheet for device-specific register and bit information.

dsPIC33FJXXMCMC06A/X08A/X10A devices include several features intended to maximize application flexibility and reliability, and minimize cost through elimination of external components. These are:

- Flexible Configuration
- Watchdog Timer (WDT)
- Code Protection and CodeGuard™ Security
- JTAG Boundary Scan Interface
- In-Circuit Serial Programming™ (ICSP™)
- In-Circuit Emulation

23.1 Configuration Bits

dsPIC33FJXXMCMC06A/X08A/X10A devices provide nonvolatile memory implementation for device configuration bits. Refer to **Section 25. “Device Configuration”** (DS70194) of the “dsPIC33F/PIC24H Family Reference Manual”, for more information on this implementation.

The Configuration bits can be programmed (read as ‘0’), or left unprogrammed (read as ‘1’), to select various device configurations. These bits are mapped starting at program memory location 0xF80000.

The device Configuration register map is shown in Table 23-1.

The individual Configuration bit descriptions for the Configuration registers are shown in Table 23-2.

Note that address, 0xF80000, is beyond the user program memory space. In fact, it belongs to the configuration memory space (0x800000-0xFFFFF) which can only be accessed using table reads and table writes.

TABLE 23-1: DEVICE CONFIGURATION REGISTER MAP

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0xF80000	FBS	RBS<1:0>		—	—	BSS<2:0>			BWRP
0xF80002	FSS	RSS<1:0>		—	—	SSS<2:0>			SWRP
0xF80004	FGS	—	—	—	—	—	GSS1	GSS0	GWRP
0xF80006	FOSCSEL	IESO	Reserved ⁽²⁾	—	—	—	FNOSC<2:0>		
0xF80008	FOSC	FCKSM<1:0>		—	—	—	OSCIOFNC	POSCMD<1:0>	
0xF8000A	FWDT	FWDTEN	WINDIS	PLLKEN ⁽³⁾	WDTPRE	WDTPOST<3:0>			
0xF8000C	FPOR	PWMPIN	HPOL	LPOL	—	—	FPWRT<2:0>		
0xF8000E	FICD	Reserved ⁽¹⁾		JTAGEN	—	—	—	ICS<1:0>	
0xF80010	FUID0	User Unit ID Byte 0							
0xF80012	FUID1	User Unit ID Byte 1							
0xF80014	FUID2	User Unit ID Byte 2							
0xF80016	FUID3	User Unit ID Byte 3							

Legend: — = unimplemented bit, reads as ‘0’.

Note 1: These bits are reserved for use by development tools and must be programmed as ‘1’.

2: When read, this bit returns the current programmed value.

3: This bit is unimplemented on dsPIC33FJ64MCMC06A/X08A/X10A and dsPIC33FJ128MCMC06A/X08A/X10A devices and reads as ‘0’.

dsPIC33FJXXMCX06A/X08A/X10A

26.0 ELECTRICAL CHARACTERISTICS

This section provides an overview of dsPIC33FJXXMCX06A/X08A/X10A electrical characteristics. Additional information will be provided in future revisions of this document as it becomes available.

Absolute maximum ratings for the dsPIC33FJXXMCX06A/X08A/X10A family are listed below. Exposure to these maximum rating conditions for extended periods may affect device reliability. Functional operation of the device at these or any other conditions above the parameters indicated in the operation listings of this specification is not implied.

Absolute Maximum Ratings

(See Note 1)

Ambient temperature under bias	-40°C to +125°C
Storage temperature	-65°C to +160°C
Voltage on VDD with respect to VSS	-0.3V to +4.0V
Voltage on any pin that is not 5V tolerant with respect to VSS ⁽⁴⁾	-0.3V to (VDD + 0.3V)
Voltage on any 5V tolerant pin with respect to VSS when VDD ≥ 3.0V ⁽⁴⁾	-0.3V to +5.6V
Voltage on any 5V tolerant pin with respect to VSS when VDD < 3.0V ⁽⁴⁾	-0.3V to 3.6V
Maximum current out of VSS pin	300 mA
Maximum current into VDD pin ⁽²⁾	250 mA
Maximum current sourced/sunk by any 2x I/O pin ⁽³⁾	8 mA
Maximum current sourced/sunk by any 4x I/O pin ⁽³⁾	15 mA
Maximum current sourced/sunk by any 8x I/O pin ⁽³⁾	25 mA
Maximum current sunk by all ports	200 mA
Maximum current sourced by all ports ⁽²⁾	200 mA

Note 1: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

2: Maximum allowable current is a function of device maximum power dissipation (see Table 26-2).

3: Exceptions are CLKOUT, which is able to sink/source 25 mA, and the VREF+, VREF-, SCLx, SDAX, PGECx and PGEDx pins, which are able to sink/source 12 mA.

4: See the “Pin Diagrams” section for 5V tolerant pins.

dsPIC33FJXXMCX06A/X08A/X10A

FIGURE 26-16: SPIx MASTER MODE (FULL-DUPLEX, CKE = 1, CKP = x, SMP = 1) TIMING CHARACTERISTICS

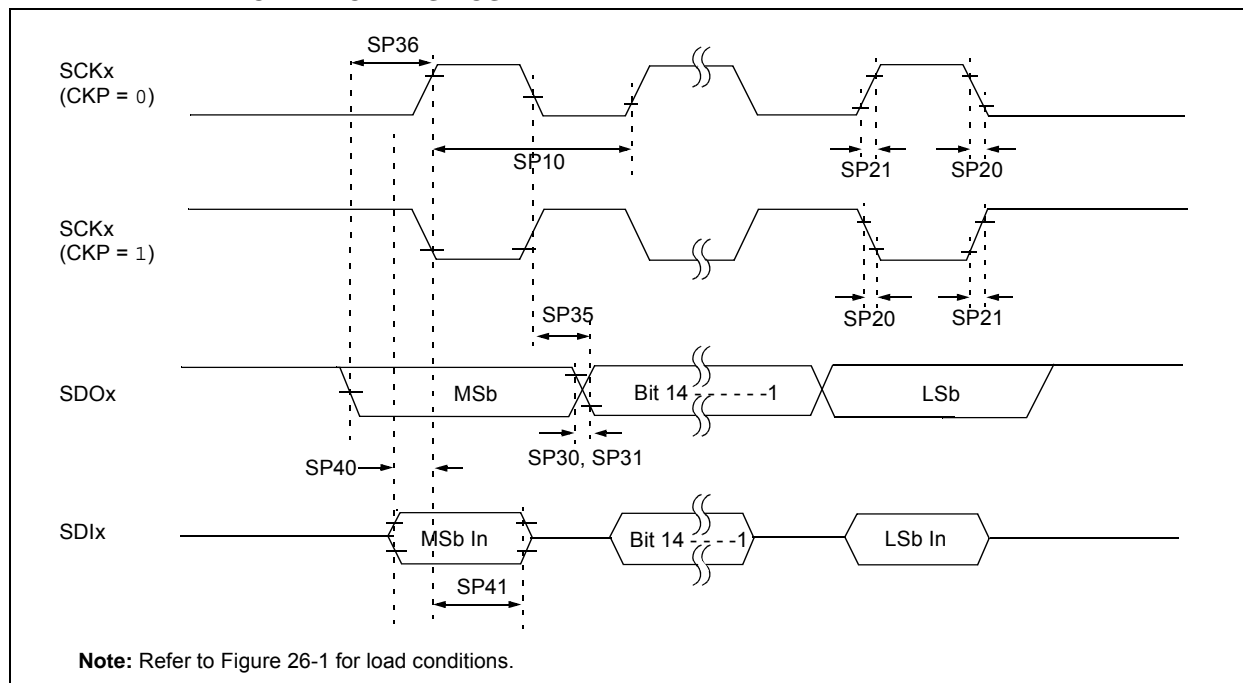


TABLE 26-34: SPIx MASTER MODE (FULL-DUPLEX, CKE = 1, CKP = x, SMP = 1) TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	Symbol	Characteristic ⁽¹⁾	Min	Typ ⁽²⁾	Max	Units	Conditions
SP10	TscP	Maximum SCK Frequency	—	—	10	MHz	See Note 3
SP20	TscF	SCKx Output Fall Time	—	—	—	ns	See parameter DO32 and Note 4
SP21	TscR	SCKx Output Rise Time	—	—	—	ns	See parameter DO31 and Note 4
SP30	TdoF	SDOx Data Output Fall Time	—	—	—	ns	See parameter DO32 and Note 4
SP31	TdoR	SDOx Data Output Rise Time	—	—	—	ns	See parameter DO31 and Note 4
SP35	Tsch2doV, TscL2doV	SDOx Data Output Valid after SCKx Edge	—	6	20	ns	—
SP36	TdoV2sc, TdoV2scL	SDOx Data Output Setup to First SCKx Edge	30	—	—	ns	—
SP40	TdiV2scH, TdiV2scL	Setup Time of SDIx Data Input to SCKx Edge	30	—	—	ns	—
SP41	Tsch2diL, TscL2diL	Hold Time of SDIx Data Input to SCKx Edge	30	—	—	ns	—

Note 1: These parameters are characterized, but are not tested in manufacturing.

2: Data in "Typ" column is at 3.3V, 25°C unless otherwise stated.

3: The minimum clock period for SCKx is 100 ns. The clock generated in Master mode must not violate this specification.

4: Assumes 50 pF load on all SPIx pins.

dsPIC33FJXXXMCX06A/X08A/X10A

FIGURE 26-22: I2Cx BUS START/STOP BITS TIMING CHARACTERISTICS (MASTER MODE)

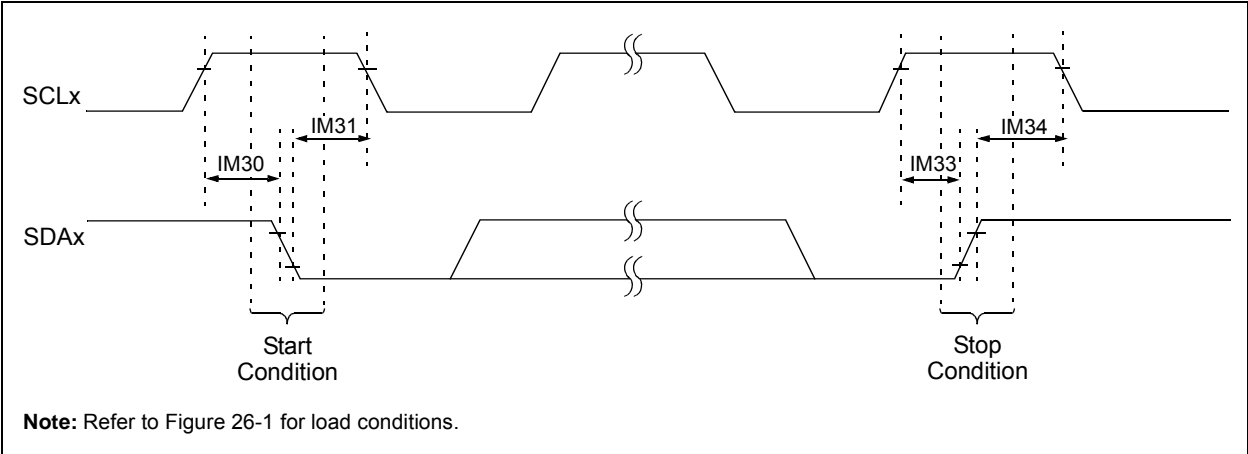
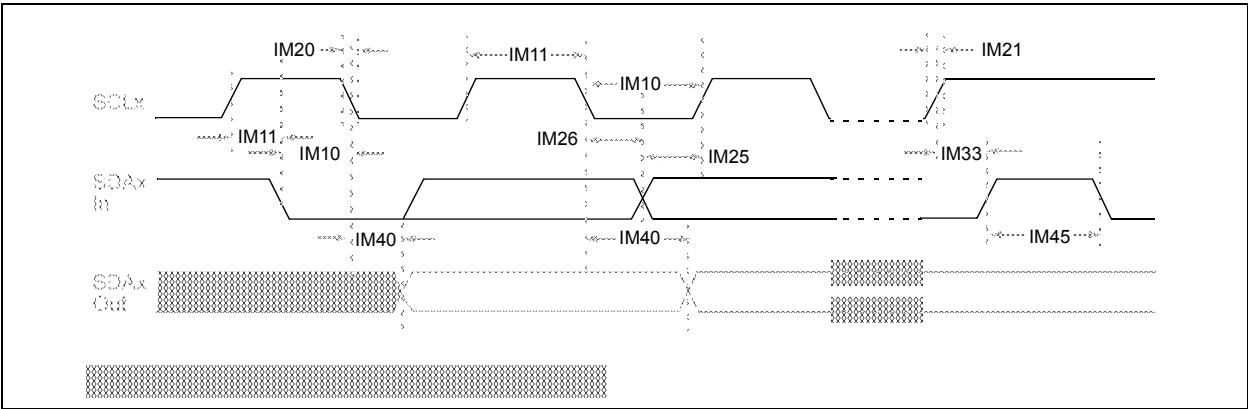


FIGURE 26-23: I2Cx BUS DATA TIMING CHARACTERISTICS (MASTER MODE)



dsPIC33FJXXMCX06A/X08A/X10A

27.0 HIGH TEMPERATURE ELECTRICAL CHARACTERISTICS

This section provides an overview of dsPIC33FJXXMCX06A/X08A/X10A electrical characteristics for devices operating in an ambient temperature range of -40°C to +150°C.

The specifications between -40°C to +150°C are identical to those shown in **Section 26.0 “Electrical Characteristics”** for operation between -40°C to +125°C, with the exception of the parameters listed in this section.

Parameters in this section begin with an H, which denotes High temperature. For example, parameter DC10 in **Section 26.0 “Electrical Characteristics”** is the Industrial and Extended temperature equivalent of HDC10.

Absolute maximum ratings for the dsPIC33FJXXMCX06A/X08A/X10A high temperature devices are listed below. Exposure to these maximum rating conditions for extended periods can affect device reliability. Functional operation of the device at these or any other conditions above the parameters indicated in the operation listings of this specification is not implied.

Absolute Maximum Ratings⁽¹⁾

Ambient temperature under bias ⁽⁴⁾	-40°C to +150°C
Storage temperature	-65°C to +160°C
Voltage on VDD with respect to VSS	-0.3V to +4.0V
Voltage on any pin that is not 5V tolerant with respect to VSS ⁽⁵⁾	-0.3V to (VDD + 0.3V)
Voltage on any 5V tolerant pin with respect to VSS when VDD < 3.0V ⁽⁵⁾	-0.3V to (VDD + 0.3V)
Voltage on any 5V tolerant pin with respect to VSS when VDD ≥ 3.0V ⁽⁵⁾	-0.3V to 5.6V
Voltage on VCAP with respect to VSS	2.25V to 2.75V
Maximum current out of VSS pin	60 mA
Maximum current into VDD pin ⁽²⁾	60 mA
Maximum junction temperature	+155°C
Maximum current sourced/sunk by any 2x I/O pin ⁽³⁾	2 mA
Maximum current sourced/sunk by any 4x I/O pin ⁽³⁾	4 mA
Maximum current sourced/sunk by any 8x I/O pin ⁽³⁾	8 mA
Maximum current sunk by all ports combined	10 mA
Maximum current sourced by all ports combined ⁽²⁾	10 mA

Note 1: Stresses above those listed under “Absolute Maximum Ratings” can cause permanent damage to the device. This is a stress rating only, and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods can affect device reliability.

2: Maximum allowable current is a function of device maximum power dissipation (see Table 27-2).

3: Unlike devices at 125°C and below, the specifications in this section also apply to the CLKOUT, VREF+, VREF-, SCLx, SDAx, PGECx, and PGEDx pins.

4: AEC-Q100 reliability testing for devices intended to operate at 150°C is 1,000 hours. Any design in which the total operating time from 125°C to 150°C will be greater than 1,000 hours is not warranted without prior written approval from Microchip Technology Inc.

5: Refer to the “Pin Diagrams” section for 5V tolerant pins.

dsPIC33FJXXMCX06A/X08A/X10A

TABLE 27-14: ADC MODULE SPECIFICATIONS

AC CHARACTERISTICS		Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +150^{\circ}\text{C}$ for High Temperature					
Param No.	Symbol	Characteristic	Min	Typ	Max	Units	Conditions
Reference Inputs							
HAD08	IREF	Current Drain	—	250	600	μA	ADC operating, See Note 1
			—	—	50	μA	ADC off, See Note 1

Note 1: These parameters are not characterized or tested in manufacturing.

TABLE 27-15: ADC MODULE SPECIFICATIONS (12-BIT MODE)⁽³⁾

AC CHARACTERISTICS		Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +150^{\circ}\text{C}$ for High Temperature					
Param No.	Symbol	Characteristic	Min	Typ	Max	Units	Conditions
ADC Accuracy (12-bit Mode) – Measurements with external VREF+/VREF- ⁽¹⁾							
AD23a	GERR	Gain Error	—	5	10	LSb	VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3.6V
AD24a	EOFF	Offset Error	—	2	5	LSb	VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3.6V
ADC Accuracy (12-bit Mode) – Measurements with internal VREF+/VREF- ⁽¹⁾							
AD23a	GERR	Gain Error	2	10	20	LSb	VINL = AVSS = 0V, AVDD = 3.6V
AD24a	EOFF	Offset Error	2	5	10	LSb	VINL = AVSS = 0V, AVDD = 3.6V
Dynamic Performance (12-bit Mode) ⁽²⁾							
HAD33a	FNYQ	Input Signal Bandwidth	—	—	200	kHz	—

Note 1: These parameters are characterized, but are tested at 20 ksp/s only.

2: These parameters are characterized by similarity, but are not tested in manufacturing.

3: Injection currents $> |0|$ can affect the ADC results by approximately 4-6 counts.

TABLE 27-16: ADC MODULE SPECIFICATIONS (10-BIT MODE)⁽³⁾

AC CHARACTERISTICS		Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +150^{\circ}\text{C}$ for High Temperature					
Param No.	Symbol	Characteristic	Min	Typ	Max	Units	Conditions
ADC Accuracy (12-bit Mode) – Measurements with external VREF+/VREF- ⁽¹⁾							
AD23b	GERR	Gain Error	—	3	6	LSb	VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3.6V
AD24b	EOFF	Offset Error	—	2	5	LSb	VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3.6V
ADC Accuracy (12-bit Mode) – Measurements with internal VREF+/VREF- ⁽¹⁾							
AD23b	GERR	Gain Error	—	7	15	LSb	VINL = AVSS = 0V, AVDD = 3.6V
AD24b	EOFF	Offset Error	—	3	7	LSb	VINL = AVSS = 0V, AVDD = 3.6V
Dynamic Performance (10-bit Mode) ⁽²⁾							
HAD33b	FNYQ	Input Signal Bandwidth	—	—	400	kHz	—

Note 1: These parameters are characterized, but are tested at 20 ksp/s only.

2: These parameters are characterized by similarity, but are not tested in manufacturing.

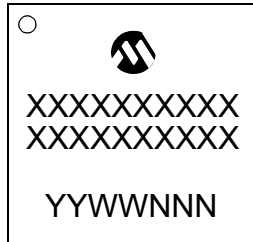
3: Injection currents $> |0|$ can affect the ADC results by approximately 4-6 counts.

dsPIC33FJXXXMCX06A/X08A/X10A

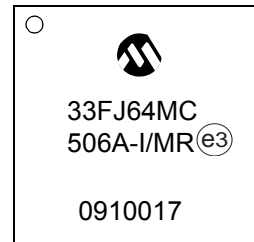
29.0 PACKAGING INFORMATION

29.1 Package Marking Information

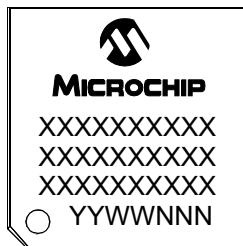
64-Lead QFN (9x9x0.9mm)



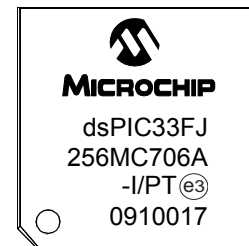
Example



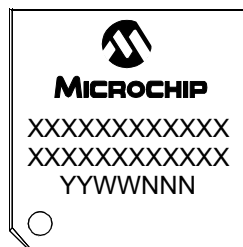
64-Lead TQFP (10x10x1 mm)



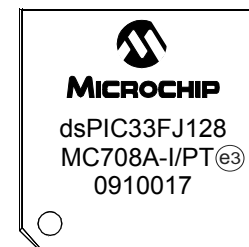
Example



80-Lead TQFP (12x12x1 mm)



Example



Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator (e3) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.