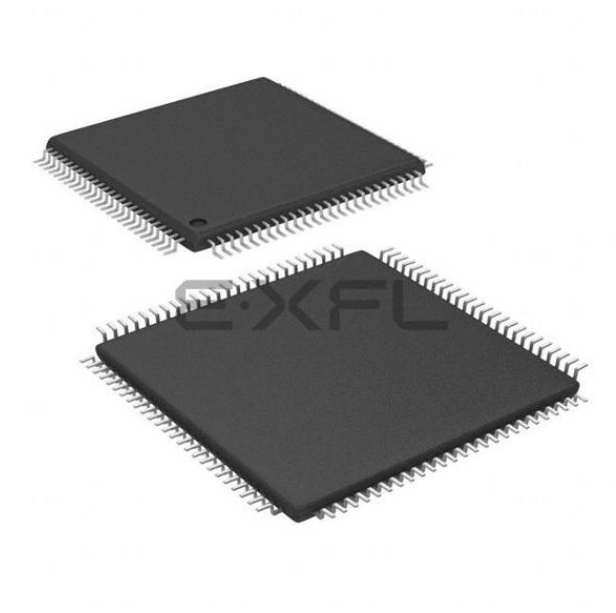
# Microchip Technology - DSPIC33FJ64MC710A-E/PF Datasheet



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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | dsPIC |
| Core Size | 16-Bit |
| Speed | 40 MIPs |
| Connectivity | CANbus, I²C, IrDA, LINbus, SPI, UART/USART |
| Peripherals | Brown-out Detect/Reset, DMA, Motor Control PWM, POR, PWM, QEI, WDT |
| Number of I/O | 85 |
| Program Memory Size | 64KB (64K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 16K x 8 |
| Voltage - Supply (Vcc/Vdd) | 3V ~ 3.6V |
| Data Converters | A/D 24x10/12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 125°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 100-TQFP |
| Supplier Device Package | 100-TQFP (14x14) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/dspic33fj64mc710a-e-pf |

**REGISTER 3-2: CORCON: CORE CONTROL REGISTER**

| U-0 | U-0 | U-0 | R/W-0 | R/W-0 | R-0 | R-0 | R-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | US | EDT(1) | DL<2:0> | | |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-1 | R/W-0 | R/C-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| SATA | SATB | SATDW | ACCSAT | IPL3(2) | PSV | RND | IF |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | C = Clearable bit | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | -n = Value at POR | '1' = Bit is set |
| 0' = Bit is cleared | 'x = Bit is unknown | U = Unimplemented bit, read as '0' | |

bit 15-13 **Unimplemented:** Read as '0'

bit 12 **US:** DSP Multiply Unsigned/Signed Control bit
1 = DSP engine multiplies are unsigned
0 = DSP engine multiplies are signed

bit 11 **EDT:** Early DO Loop Termination Control bit(1)
1 = Terminate executing DO loop at end of current loop iteration
0 = No effect

bit 10-8 **DL<2:0>:** DO Loop Nesting Level Status bits
111 = 7 DO loops active
.
.
.
001 = 1 DO loop active
000 = 0 DO loops active

bit 7 **SATA:** AccA Saturation Enable bit
1 = Accumulator A saturation enabled
0 = Accumulator A saturation disabled

bit 6 **SATB:** AccB Saturation Enable bit
1 = Accumulator B saturation enabled
0 = Accumulator B saturation disabled

bit 5 **SATDW:** Data Space Write from DSP Engine Saturation Enable bit
1 = Data space write saturation enabled
0 = Data space write saturation disabled

bit 4 **ACCSAT:** Accumulator Saturation Mode Select bit
1 = 9.31 saturation (super saturation)
0 = 1.31 saturation (normal saturation)

bit 3 **IPL3:** CPU Interrupt Priority Level Status bit 3(2)
1 = CPU interrupt priority level is greater than 7
0 = CPU interrupt priority level is 7 or less

bit 2 **PSV:** Program Space Visibility in Data Space Enable bit
1 = Program space visible in data space
0 = Program space not visible in data space

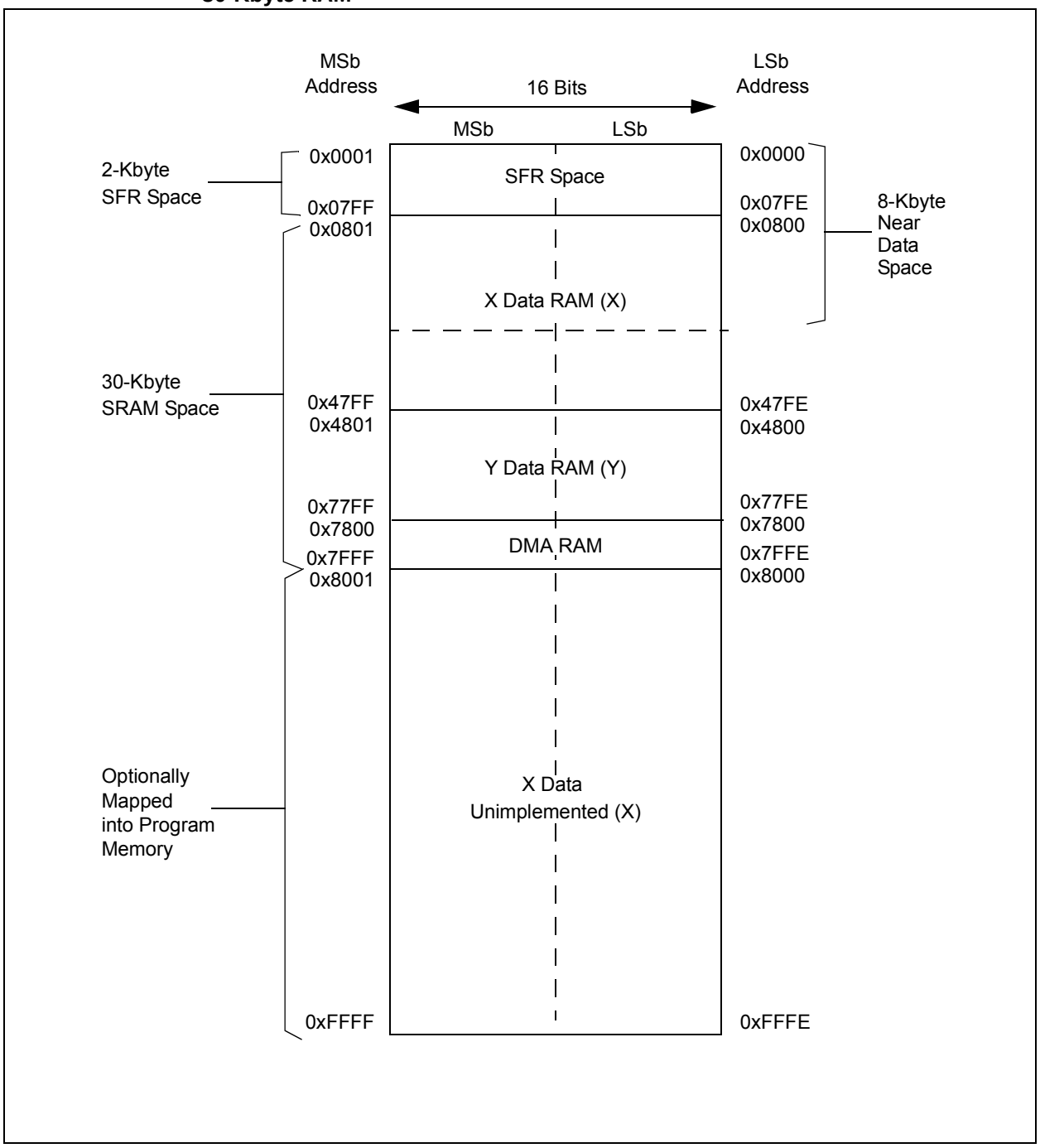
bit 1 **RND:** Rounding Mode Select bit
1 = Biased (conventional) rounding enabled
0 = Unbiased (convergent) rounding enabled

bit 0 **IF:** Integer or Fractional Multiplier Mode Select bit
1 = Integer mode enabled for DSP multiply ops
0 = Fractional mode enabled for DSP multiply ops

**Note 1:** This bit will always read as '0'.
**2:** The IPL3 bit is concatenated with the IPL<2:0> bits (SR<7:5>) to form the CPU interrupt priority level.

**NOTES:**

**FIGURE 4-5: DATA MEMORY MAP FOR dsPIC33FJXXXMCX06A/X08A/X10A DEVICES WITH 30-Kbyte RAM**



### 4.6.3 READING DATA FROM PROGRAM MEMORY USING PROGRAM SPACE VISIBILITY

The upper 32 Kbytes of data space may optionally be mapped into any 16K word page of the program space. This option provides transparent access of stored constant data from the data space without the need to use special instructions (i.e., TBLRDL/H).

Program space access through the data space occurs if the Most Significant bit of the data space EA is '1' and program space visibility is enabled by setting the PSV bit in the Core Control register (CORCON<2>). The location of the program memory space to be mapped into the data space is determined by the Program Space Visibility Page register (PSVPAG). This 8-bit register defines any one of 256 possible pages of 16K words in program space. In effect, PSVPAG functions as the upper 8 bits of the program memory address, with the 15 bits of the EA functioning as the lower bits. Note that by incrementing the PC by 2 for each program memory word, the lower 15 bits of data space addresses directly map to the lower 15 bits in the corresponding program space addresses.

Data reads to this area add an additional cycle to the instruction being executed, since two program memory fetches are required.

Although each data space address, 8000h and higher, maps directly into a corresponding program memory address (see Figure 4-11), only the lower 16 bits of the 24-bit program word are used to contain the data. The upper 8 bits of any program space location used as data should be programmed with '1111 1111' or '0000 0000' to force a NOP. This prevents possible issues should the area of code ever be accidentally executed.

| **Note:** | PSV access is temporarily disabled during table reads/writes. |
|---|---|

For operations that use PSV and are executed outside a REPEAT loop, the MOV and MOV.D instructions require one instruction cycle in addition to the specified execution time. All other instructions require two instruction cycles in addition to the specified execution time.

For operations that use PSV and are executed inside a REPEAT loop, there will be some instances that require two instruction cycles in addition to the specified execution time of the instruction:

- Execution in the first iteration
- Execution in the last iteration
- Execution prior to exiting the loop due to an interrupt
- Execution upon re-entering the loop after an interrupt is serviced

Any other iteration of the REPEAT loop will allow the instruction accessing data using PSV to execute in a single cycle.

**FIGURE 4-11: PROGRAM SPACE VISIBILITY OPERATION**

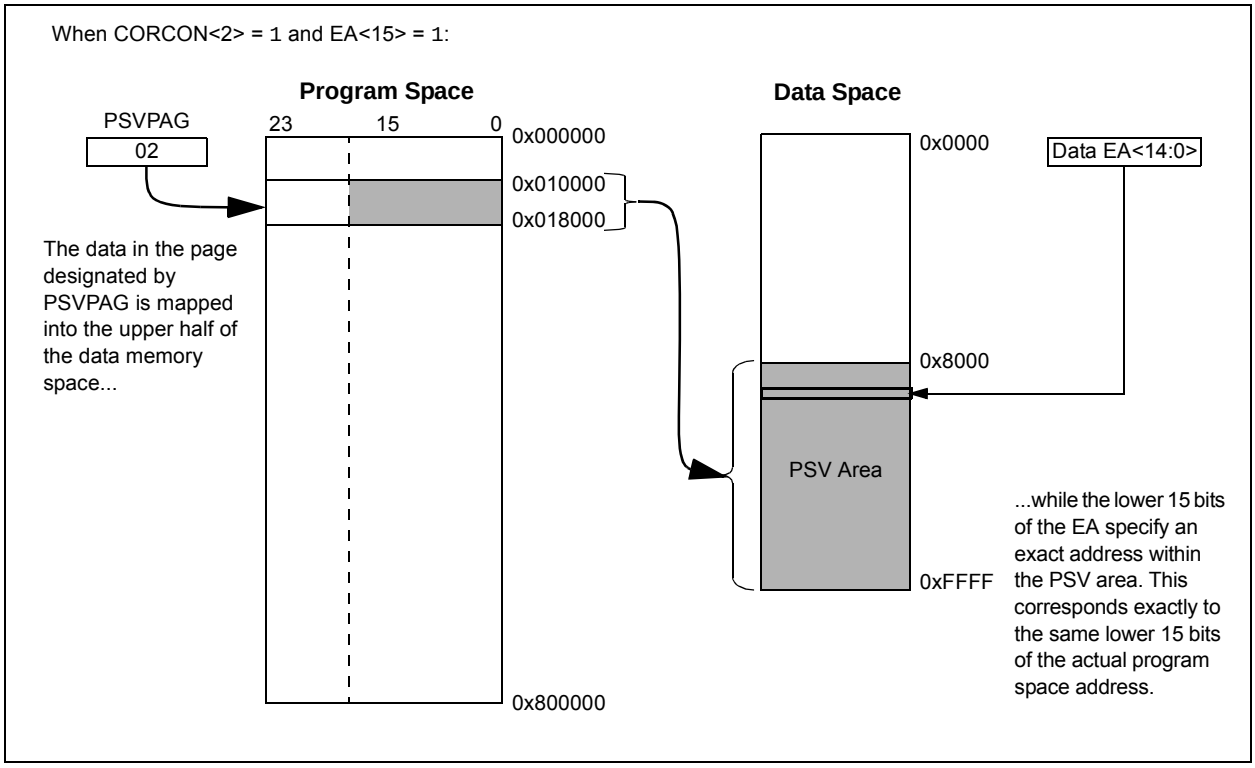


**TABLE 7-1: INTERRUPT VECTORS (CONTINUED)**

| Vector Number | Interrupt Request (IRQ) Number | IVT Address | AIVT Address | Interrupt Source |
|---|---|---|---|---|
| 54 | 46 | 0x000070 | 0x000170 | DMA4 – DMA Channel 4 |
| 55 | 47 | 0x000072 | 0x000172 | T6 – Timer6 |
| 56 | 48 | 0x000074 | 0x000174 | T7 – Timer7 |
| 57 | 49 | 0x000076 | 0x000176 | SI2C2 – I2C2 Slave Events |
| 58 | 50 | 0x000078 | 0x000178 | MI2C2 – I2C2 Master Events |
| 59 | 51 | 0x00007A | 0x00017A | T8 – Timer8 |
| 60 | 52 | 0x00007C | 0x00017C | T9 – Timer9 |
| 61 | 53 | 0x00007E | 0x00017E | INT3 – External Interrupt 3 |
| 62 | 54 | 0x000080 | 0x000180 | INT4 – External Interrupt 4 |
| 63 | 55 | 0x000082 | 0x000182 | C2RX – ECAN2 Receive Data Ready |
| 64 | 56 | 0x000084 | 0x000184 | C2 – ECAN2 Event |
| 65 | 57 | 0x000086 | 0x000186 | PWM – PWM Period Match |
| 66 | 58 | 0x000088 | 0x000188 | QEI – Position Counter Compare |
| 69 | 61 | 0x00008E | 0x00018E | DMA5 – DMA Channel 5 |
| 70 | 62 | 0x000090 | 0x000190 | Reserved |
| 71 | 63 | 0x000092 | 0x000192 | $\overline{\text{FLTA}}$ – MCPWM Fault A |
| 72 | 64 | 0x000094 | 0x000194 | $\overline{\text{FLTB}}$ – MCPWM Fault B |
| 73 | 65 | 0x000096 | 0x000196 | U1E – UART1 Error |
| 74 | 66 | 0x000098 | 0x000198 | U2E – UART2 Error |
| 75 | 67 | 0x00009A | 0x00019A | Reserved |
| 76 | 68 | 0x00009C | 0x00019C | DMA6 – DMA Channel 6 |
| 77 | 69 | 0x00009E | 0x00019E | DMA7 – DMA Channel 7 |
| 78 | 70 | 0x0000A0 | 0x0001A0 | C1TX – ECAN1 Transmit Data Request |
| 79 | 71 | 0x0000A2 | 0x0001A2 | C2TX – ECAN2 Transmit Data Request |
| 80-125 | 72-117 | 0x0000A4-0x0000FE | 0x0001A4-0x0001FE | Reserved |

**TABLE 7-2: TRAP VECTORS**

| Vector Number | IVT Address | AIVT Address | Trap Source |
|---|---|---|---|
| 0 | 0x000004 | 0x000104 | Reserved |
| 1 | 0x000006 | 0x000106 | Oscillator Failure |
| 2 | 0x000008 | 0x000108 | Address Error |
| 3 | 0x00000A | 0x00010A | Stack Error |
| 4 | 0x00000C | 0x00010C | Math Error |
| 5 | 0x00000E | 0x00010E | DMA Error Trap |
| 6 | 0x000010 | 0x000110 | Reserved |
| 7 | 0x000012 | 0x000112 | Reserved |

**REGISTER 7-12: IEC2: INTERRUPT ENABLE CONTROL REGISTER 2**

| R/W-0 | R/W-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| T6IE | DMA4IE | — | OC8IE | OC7IE | OC6IE | OC5IE | IC6IE |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| IC5IE | IC4IE | IC3IE | DMA3IE | C1IE | C1RXIE | SPI2IE | SPI2EIE |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15 **T6IE:** Timer6 Interrupt Enable bit
1 = Interrupt request enabled
0 = Interrupt request not enabled

bit 14 **DMA4IE:** DMA Channel 4 Data Transfer Complete Interrupt Enable bit
1 = Interrupt request enabled
0 = Interrupt request not enabled

bit 13 **Unimplemented:** Read as '0'

bit 12 **OC8IE:** Output Compare Channel 8 Interrupt Enable bit
1 = Interrupt request enabled
0 = Interrupt request not enabled

bit 11 **OC7IE:** Output Compare Channel 7 Interrupt Enable bit
1 = Interrupt request enabled
0 = Interrupt request not enabled

bit 10 **OC6IE:** Output Compare Channel 6 Interrupt Enable bit
1 = Interrupt request enabled
0 = Interrupt request not enabled

bit 9 **OC5IE:** Output Compare Channel 5 Interrupt Enable bit
1 = Interrupt request enabled
0 = Interrupt request not enabled

bit 8 **IC6IE:** Input Capture Channel 6 Interrupt Enable bit
1 = Interrupt request enabled
0 = Interrupt request not enabled

bit 7 **IC5IE:** Input Capture Channel 5 Interrupt Enable bit
1 = Interrupt request enabled
0 = Interrupt request not enabled

bit 6 **IC4IE:** Input Capture Channel 4 Interrupt Enable bit
1 = Interrupt request enabled
0 = Interrupt request not enabled

bit 5 **IC3IE:** Input Capture Channel 3 Interrupt Enable bit
1 = Interrupt request enabled
0 = Interrupt request not enabled

bit 4 **DMA3IE:** DMA Channel 3 Data Transfer Complete Interrupt Enable bit
1 = Interrupt request enabled
0 = Interrupt request not enabled

bit 3 **C1IE:** ECAN1 Event Interrupt Enable bit
1 = Interrupt request enabled
0 = Interrupt request not enabled

**REGISTER 7-14: IEC4: INTERRUPT ENABLE CONTROL REGISTER 4**

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | — | — |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | U-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| C2TXIE | C1TXIE | DMA7IE | DMA6IE | — | U2EIE | U1EIE | FLTBIE |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-8 **Unimplemented:** Read as '0'

bit 7 **C2TXIE:** ECAN2 Transmit Data Request Interrupt Enable bit
1 = Interrupt request enabled
0 = Interrupt request not enabled

bit 6 **C1TXIE:** ECAN1 Transmit Data Request Interrupt Enable bit
1 = Interrupt request enabled
0 = Interrupt request not enabled

bit 5 **DMA7IE:** DMA Channel 7 Data Transfer Complete Enable Status bit
1 = Interrupt request enabled
0 = Interrupt request not enabled

bit 4 **DMA6IE:** DMA Channel 6 Data Transfer Complete Enable Status bit
1 = Interrupt request enabled
0 = Interrupt request not enabled

bit 3 **Unimplemented:** Read as '0'

bit 2 **U2EIE:** UART2 Error Interrupt Enable bit
1 = Interrupt request enabled
0 = Interrupt request not enabled

bit 1 **U1EIE:** UART1 Error Interrupt Enable bit
1 = Interrupt request enabled
0 = Interrupt request not enabled

bit 0 **FLTBIE:** PWM Fault B Interrupt Enable bit
1 = Interrupt request enabled
0 = Interrupt request not enabled

**REGISTER 7-30: IPC15: INTERRUPT PRIORITY CONTROL REGISTER 15**

| U-0 | R/W-1 | R/W-0 | R/W-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | FLTAIP<2:0> | | | — | — | — | — |
| bit 15 | | | | | | | bit 8 |

| U-0 | R/W-1 | R/W-0 | R/W-0 | U-0 | U-1 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | DMA5IP<2:0> | | | — | — | — | — |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 15 **Unimplemented:** Read as ‘0’

bit 14-12 **FLTAIP<2:0>:** PWM Fault A Interrupt Priority bits
111 = Interrupt is priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is priority 1
000 = Interrupt source is disabled

bit 11-7 **Unimplemented:** Read as ‘0’

bit 6-4 **DMA5IP<2:0>:** DMA Channel 5 Data Transfer Complete Interrupt Priority bits
111 = Interrupt is priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is priority 1
000 = Interrupt source is disabled

bit 3-0 **Unimplemented:** Read as ‘0’

**REGISTER 13-2: TyCON (T3CON, T5CON, T7CON OR T9CON) CONTROL REGISTER**

| R/W-0 | U-0 | R/W-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| TON(1) | — | TSIDL(2) | — | — | — | — | — |
| bit 15 | | | | | | | bit 8 |

| U-0 | R/W-0 | R/W-0 | R/W-0 | U-0 | U-0 | R/W-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | TGATE(1) | TCKPS<1:0>(1) | | — | — | TCS(1,3) | — |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15 **TON:** Timery On bit(1)
1 = Starts 16-bit Timery
0 = Stops 16-bit Timery

bit 14 **Unimplemented:** Read as '0'

bit 13 **TSIDL:** Stop in Idle Mode bit(2)
1 = Discontinue module operation when device enters Idle mode
0 = Continue module operation in Idle mode

bit 12-7 **Unimplemented:** Read as '0'

bit 6 **TGATE:** Timery Gated Time Accumulation Enable bit(1)
When TCS = 1:
This bit is ignored.
When TCS = 0:
1 = Gated time accumulation enabled
0 = Gated time accumulation disabled

bit 5-4 **TCKPS<1:0>:** Timer3 Input Clock Prescale Select bits(1)
11 = 1:256
10 = 1:64
01 = 1:8
00 = 1:1

bit 3-2 **Unimplemented:** Read as '0'

bit 1 **TCS:** Timery Clock Source Select bit(1,3)
1 = External clock from TyCK pin (on the rising edge)
0 = Internal clock (FCY)

bit 0 **Unimplemented:** Read as '0'

**Note 1:** When 32-bit operation is enabled (T2CON<3> = 1), these bits have no effect on Timery operation; all timer functions are set through T2CON.

**2:** When 32-bit timer operation is enabled (T32 = 1) in the Timer Control register (TxCON<3>), the TSIDL bit must be cleared to operate the 32-bit timer in Idle mode.

**3:** The TyCK pin is not available on all timers. Refer to the **"Pin Diagrams"** section for the available pins.

**REGISTER 16-10: PxFLTBCON: PWMx FAULT B CONTROL REGISTER**

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| FBOV4H | FBOV4L | FBOV3H | FBOV3L | FBOV2H | FBOV2L | FBOV1H | FBOV1L |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| FLTBM | — | — | — | FBEN4(1) | FBEN3(1) | FBEN2(1) | FBEN1(1) |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 15-8 **FBOVxH<4:1>:FBOVxL<4:1>:** Fault Input B PWM Override Value bits
1 = The PWM output pin is driven active on an external Fault input event
0 = The PWM output pin is driven inactive on an external Fault input event

bit 7 **FLTBM:** Fault B Mode bit
1 = The Fault B input pin functions in the Cycle-by-Cycle mode
0 = The Fault B input pin latches all control pins to the states programmed in FLTBCON<15:8>

bit 6-4 **Unimplemented:** Read as ‘0’

bit 3 **FBEN4:** Fault Input B Enable bit(1)
1 = PWM4H/PWM4L pin pair is controlled by Fault Input B
0 = PWM4H/PWM4L pin pair is not controlled by Fault Input B

bit 2 **FBEN3:** Fault Input B Enable bit(1)
1 = PWM3H/PWM3L pin pair is controlled by Fault Input B
0 = PWM3H/PWM3L pin pair is not controlled by Fault Input B

bit 1 **FBEN2:** Fault Input B Enable bit(1)
1 = PWM2H/PWM2L pin pair is controlled by Fault Input B
0 = PWM2H/PWM2L pin pair is not controlled by Fault Input B

bit 0 **FBEN1:** Fault Input B Enable bit(1)
1 = PWM1H/PWM1L pin pair is controlled by Fault Input B
0 = PWM1H/PWM1L pin pair is not controlled by Fault Input B

**Note 1:** Fault A pin has priority over Fault B pin, if enabled.

## 25.2 MPLAB C Compilers for Various Device Families

The MPLAB C Compiler code development systems are complete ANSI C compilers for Microchip's PIC18, PIC24 and PIC32 families of microcontrollers and the dsPIC30 and dsPIC33 families of digital signal controllers. These compilers provide powerful integration capabilities, superior code optimization and ease of use.

For easy source level debugging, the compilers provide symbol information that is optimized to the MPLAB IDE debugger.

## 25.3 HI-TECH C for Various Device Families

The HI-TECH C Compiler code development systems are complete ANSI C compilers for Microchip's PIC family of microcontrollers and the dsPIC family of digital signal controllers. These compilers provide powerful integration capabilities, omniscient code generation and ease of use.

For easy source level debugging, the compilers provide symbol information that is optimized to the MPLAB IDE debugger.

The compilers include a macro assembler, linker, preprocessor, and one-step driver, and can run on multiple platforms.

## 25.4 MPASM Assembler

The MPASM Assembler is a full-featured, universal macro assembler for PIC10/12/16/18 MCUs.

The MPASM Assembler generates relocatable object files for the MPLINK Object Linker, Intel® standard HEX files, MAP files to detail memory usage and symbol reference, absolute LST files that contain source lines and generated machine code and COFF files for debugging.

The MPASM Assembler features include:

- Integration into MPLAB IDE projects
- User-defined macros to streamline assembly code
- Conditional assembly for multi-purpose source files
- Directives that allow complete control over the assembly process

## 25.5 MPLINK Object Linker/ MPLIB Object Librarian

The MPLINK Object Linker combines relocatable objects created by the MPASM Assembler and the MPLAB C18 C Compiler. It can link relocatable objects from precompiled libraries, using directives from a linker script.

The MPLIB Object Librarian manages the creation and modification of library files of precompiled code. When a routine from a library is called from a source file, only the modules that contain that routine will be linked in with the application. This allows large libraries to be used efficiently in many different applications.

The object linker/library features include:

- Efficient linking of single libraries instead of many smaller files
- Enhanced code maintainability by grouping related modules together
- Flexible creation of libraries with easy module listing, replacement, deletion and extraction

## 25.6 MPLAB Assembler, Linker and Librarian for Various Device Families

MPLAB Assembler produces relocatable machine code from symbolic assembly language for PIC24, PIC32 and dsPIC devices. MPLAB C Compiler uses the assembler to produce its object file. The assembler generates relocatable object files that can then be archived or linked with other relocatable object files and archives to create an executable file. Notable features of the assembler include:

- Support for the entire device instruction set
- Support for fixed-point and floating-point data
- Command line interface
- Rich directive set
- Flexible macro language
- MPLAB IDE compatibility

**FIGURE 26-24: I2Cx BUS START/STOP BITS TIMING CHARACTERISTICS (SLAVE MODE)**

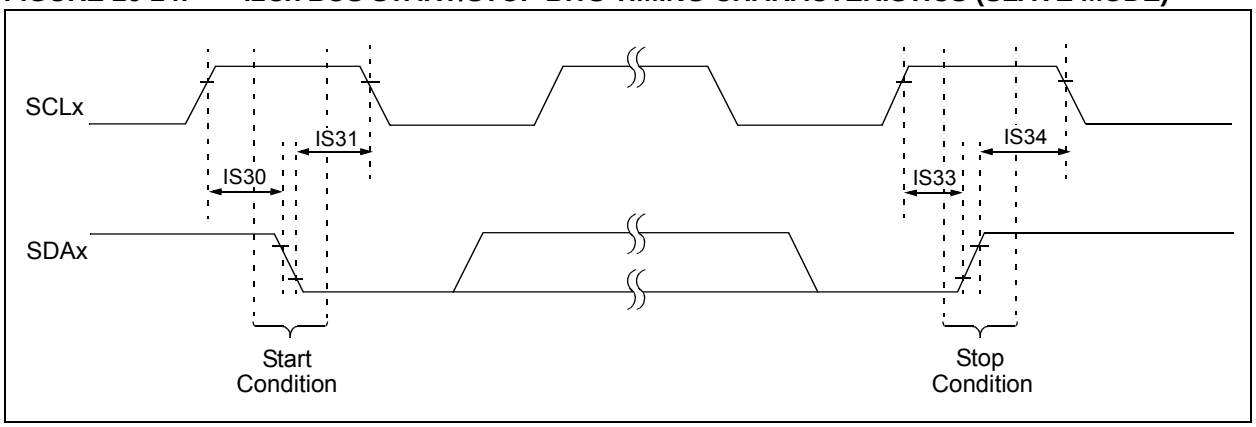



**FIGURE 26-25: I2Cx BUS DATA TIMING CHARACTERISTICS (SLAVE MODE)**

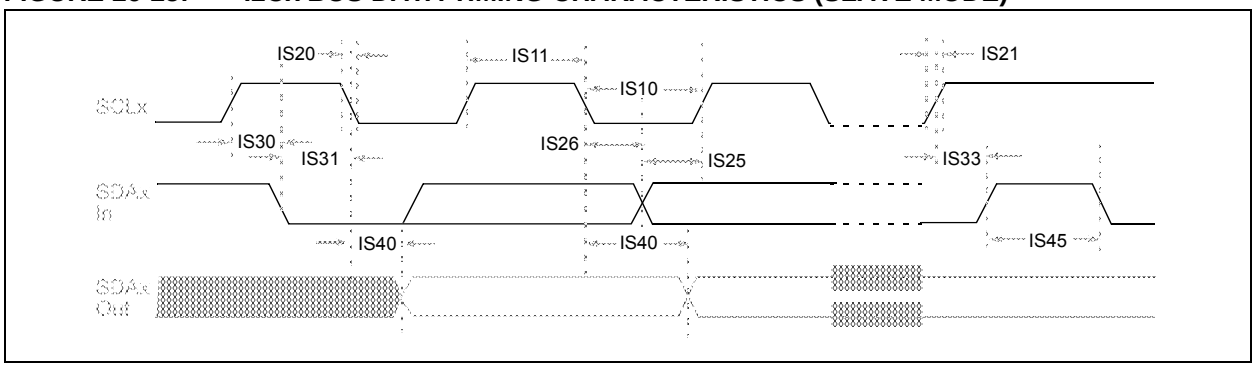


**TABLE 26-43: ADC MODULE SPECIFICATIONS**

| AC CHARACTERISTICS | | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +125°C for Extended | | | | |
|---|---|---|---|---|---|---|---|
| **Param No.** | **Symbol** | **Characteristic** | **Min.** | **Typ** | **Max.** | **Units** | **Conditions** |
| **Device Supply** | | | | | | | |
| AD01 | AVDD | Module VDD Supply | Greater of VDD – 0.3 or 3.0 | — | Lesser of VDD + 0.3 or 3.6 | V | — |
| AD02 | AVSS | Module VSS Supply | VSS – 0.3 | — | VSS + 0.3 | V | — |
| **Reference Inputs** | | | | | | | |
| AD05 | VREFH | Reference Voltage High | AVSS + 2.5 | — | AVDD | V | — |
| AD05a | | | 3.0 | — | 3.6 | V | VREFH = AVDD<br>VREFL = AVSS = 0 |
| AD06 | VREFL | Reference Voltage Low | AVSS | — | AVDD – 2.5 | V | — |
| AD06a | | | 0 | — | 0 | V | VREFH = AVDD<br>VREFL = AVSS = 0 |
| AD07 | VREF | Absolute Reference Voltage | 2.5 | — | 3.6 | V | VREF = VREFH - VREFL |
| AD08 | IREF | Current Drain | — | — | 10 | μA | ADC off |
| AD08a | IAD | Operating Current | —<br>— | 7.0<br>2.7 | 9.0<br>3.2 | mA<br>mA | 10-bit ADC mode, see **Note 1**<br>12-bit ADC mode, see **Note 1** |
| **Analog Input** | | | | | | | |
| AD12 | VINH | Input Voltage Range VINH | VINL | — | VREFH | V | This voltage reflects Sample and Hold Channels 0, 1, 2 and 3 (CH0-CH3), positive input |
| AD13 | VINL | Input Voltage Range VINL | VREFL | — | AVSS + 1V | V | This voltage reflects Sample and Hold Channels 0, 1, 2 and 3 (CH0-CH3), negative input |
| AD17 | RIN | Recommended Impedance of Analog Voltage Source | —<br>— | —<br>— | 200<br>200 | Ω<br>Ω | 10-bit ADC<br>12-bit ADC |

**Note 1:** These parameters are not characterized or tested in manufacturing.

**TABLE 27-9: INTERNAL LPRC ACCURACY**

| AC CHARACTERISTICS | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +150°C for High Temperature | | | | | | |
|---|---|---|---|---|---|---|---|
| Param No. | Characteristic | Min | Typ | Max | Units | Conditions | |
| | **LPRC @ 32.768 kHz (1)** | | | | | | |
| HF21 | LPRC | -70(2) | — | +70(2) | % | -40°C ≤ TA ≤ +150°C | — |

**Note 1:** Change of LPRC frequency as VDD changes.

**2:** Characterized but not tested.

**TABLE 27-10: SPIx MASTER MODE (CKE = 0) TIMING REQUIREMENTS**

| AC CHARACTERISTICS | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +150°C for High Temperature | | | | | |
|---|---|---|---|---|---|---|---|
| Param No. | Symbol | Characteristic(1) | Min | Typ | Max | Units | Conditions |
| HSP35 | TscH2doV, TscL2doV | SDOx Data Output Valid after SCKx Edge | — | 10 | 25 | ns | — |
| HSP40 | TdiV2scH, TdiV2scL | Setup Time of SDIx Data Input to SCKx Edge | 28 | — | — | ns | — |
| HSP41 | TscH2diL, TscL2diL | Hold Time of SDIx Data Input to SCKx Edge | 35 | — | — | ns | — |

**Note 1:** These parameters are characterized but not tested in manufacturing.

**TABLE 27-11: SPIx MODULE MASTER MODE (CKE = 1) TIMING REQUIREMENTS**

| AC CHARACTERISTICS | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +150°C for High Temperature | | | | | |
|---|---|---|---|---|---|---|---|
| Param No. | Symbol | Characteristic(1) | Min | Typ | Max | Units | Conditions |
| HSP35 | TscH2doV, TscL2doV | SDOx Data Output Valid after SCKx Edge | — | 10 | 25 | ns | — |
| HSP36 | TdoV2sc, TdoV2scL | SDOx Data Output Setup to First SCKx Edge | 35 | — | — | ns | — |
| HSP40 | TdiV2scH, TdiV2scL | Setup Time of SDIx Data Input to SCKx Edge | 28 | — | — | ns | — |
| HSP41 | TscH2diL, TscL2diL | Hold Time of SDIx Data Input to SCKx Edge | 35 | — | — | ns | — |

**Note 1:** These parameters are characterized but not tested in manufacturing.

**TABLE 27-14: ADC MODULE SPECIFICATIONS**

| AC CHARACTERISTICS | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +150°C for High Temperature | | | | | |
|---|---|---|---|---|---|---|---|
| **Param No.** | **Symbol** | **Characteristic** | **Min** | **Typ** | **Max** | **Units** | **Conditions** |
| **Reference Inputs** | | | | | | | |
| HAD08 | IREF | Current Drain | —<br>— | 250<br>— | 600<br>50 | μA<br>μA | ADC operating, See **Note 1**<br>ADC off, See **Note 1** |

**Note 1:** These parameters are not characterized or tested in manufacturing.

**TABLE 27-15: ADC MODULE SPECIFICATIONS (12-BIT MODE)(3)**

| AC CHARACTERISTICS | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +150°C for High Temperature | | | | | |
|---|---|---|---|---|---|---|---|
| **Param No.** | **Symbol** | **Characteristic** | **Min** | **Typ** | **Max** | **Units** | **Conditions** |
| **ADC Accuracy (12-bit Mode) – Measurements with external VREF+/VREF-(1)** | | | | | | | |
| AD23a | GERR | Gain Error | — | 5 | 10 | LSb | VINL = AVSS = VREFL = 0V,<br>AVDD = VREFH = 3.6V |
| AD24a | EOFF | Offset Error | — | 2 | 5 | LSb | VINL = AVSS = VREFL = 0V,<br>AVDD = VREFH = 3.6V |
| **ADC Accuracy (12-bit Mode) – Measurements with internal VREF+/VREF-(1)** | | | | | | | |
| AD23a | GERR | Gain Error | 2 | 10 | 20 | LSb | VINL = AVSS = 0V, AVDD = 3.6V |
| AD24a | EOFF | Offset Error | 2 | 5 | 10 | LSb | VINL = AVSS = 0V, AVDD = 3.6V |
| **Dynamic Performance (12-bit Mode)(2)** | | | | | | | |
| HAD33a | FNYQ | Input Signal Bandwidth | — | — | 200 | kHz | — |

**Note 1:** These parameters are characterized, but are tested at 20 ksps only.

**2:** These parameters are characterized by similarity, but are not tested in manufacturing.

**3:** Injection currents > | 0 | can affect the ADC results by approximately 4-6 counts.

**TABLE 27-16: ADC MODULE SPECIFICATIONS (10-BIT MODE)(3)**

| AC CHARACTERISTICS | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +150°C for High Temperature | | | | | |
|---|---|---|---|---|---|---|---|
| **Param No.** | **Symbol** | **Characteristic** | **Min** | **Typ** | **Max** | **Units** | **Conditions** |
| **ADC Accuracy (12-bit Mode) – Measurements with external VREF+/VREF-(1)** | | | | | | | |
| AD23b | GERR | Gain Error | — | 3 | 6 | LSb | VINL = AVSS = VREFL = 0V,<br>AVDD = VREFH = 3.6V |
| AD24b | EOFF | Offset Error | — | 2 | 5 | LSb | VINL = AVSS = VREFL = 0V,<br>AVDD = VREFH = 3.6V |
| **ADC Accuracy (12-bit Mode) – Measurements with internal VREF+/VREF-(1)** | | | | | | | |
| AD23b | GERR | Gain Error | — | 7 | 15 | LSb | VINL = AVSS = 0V, AVDD = 3.6V |
| AD24b | EOFF | Offset Error | — | 3 | 7 | LSb | VINL = AVSS = 0V, AVDD = 3.6V |
| **Dynamic Performance (10-bit Mode)(2)** | | | | | | | |
| HAD33b | FNYQ | Input Signal Bandwidth | — | — | 400 | kHz | — |

**Note 1:** These parameters are characterized, but are tested at 20 ksps only.

**2:** These parameters are characterized by similarity, but are not tested in manufacturing.

**3:** Injection currents > | 0 | can affect the ADC results by approximately 4-6 counts.

**TABLE 27-17: ADC CONVERSION (12-BIT MODE) TIMING REQUIREMENTS**

| AC CHARACTERISTICS | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +150°C for High Temperature | | | | | |
|---|---|---|---|---|---|---|---|
| **Param No.** | **Symbol** | **Characteristic** | **Min** | **Typ** | **Max** | **Units** | **Conditions** |
| **Clock Parameters** | | | | | | | |
| HAD50 | TAD | ADC Clock Period(1) | 147 | — | — | ns | — |
| **Conversion Rate** | | | | | | | |
| HAD56 | FCNV | Throughput Rate(1) | — | — | 400 | Ksps | — |

**Note 1:** These parameters are characterized but not tested in manufacturing.

**TABLE 27-18: ADC CONVERSION (10-BIT MODE) TIMING REQUIREMENTS**

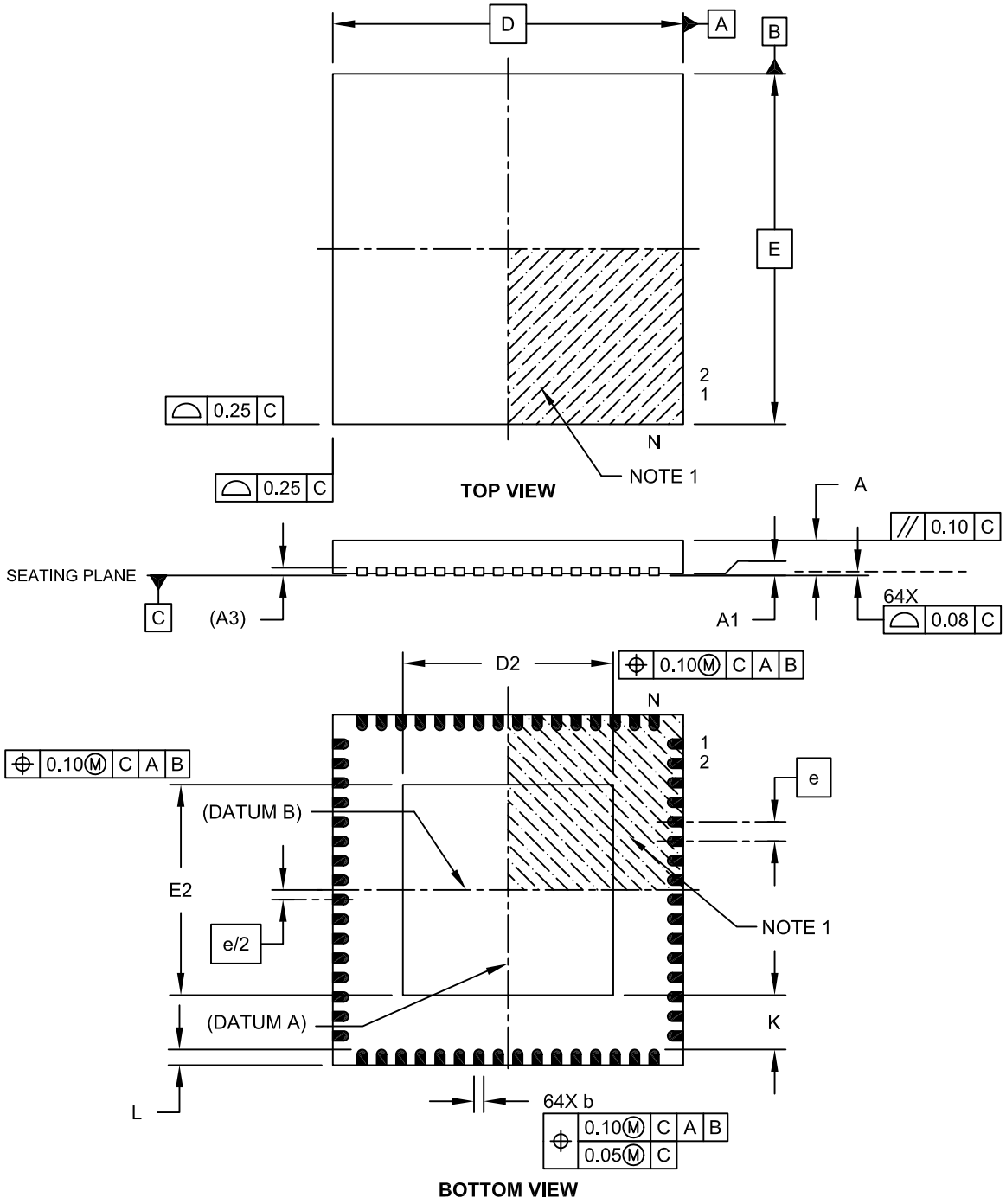
| AC CHARACTERISTICS | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +150°C for High Temperature | | | | | |
|---|---|---|---|---|---|---|---|
| **Param No.** | **Symbol** | **Characteristic** | **Min** | **Typ** | **Max** | **Units** | **Conditions** |
| **Clock Parameters** | | | | | | | |
| HAD50 | TAD | ADC Clock Period(1) | 104 | — | — | ns | — |
| **Conversion Rate** | | | | | | | |
| HAD56 | FCNV | Throughput Rate(1) | — | — | 800 | Ksps | — |

**Note 1:** These parameters are characterized but not tested in manufacturing.

## 29.2 Package Details

### 64-Lead Plastic Quad Flat, No Lead Package (MR) – 9x9x0.9 mm Body with 5.40 x 5.40 Exposed Pad [QFN]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




Microchip Technology Drawing C04-154A Sheet 1 of 2

## Revision D (June 2012)

This revision includes typographical and formatting changes throughout the data sheet text.

All other major changes are referenced by their respective section in the following table.

**TABLE B-3: MAJOR SECTION UPDATES**

| Section Name | Update Description |
|---|---|
| **Section 2.0 "Guidelines for Getting Started with 16-bit Digital Signal Controllers"** | Updated the Recommended Minimum Connection (see Figure 2-1). |
| **Section 9.0 "Oscillator Configuration"** | Updated the COSC<2:0> and NOSC<2:0> bit value definitions for '001' (see Register 9-1). |
| **Section 22.0 "10-bit/12-bit Analog-to-Digital Converter (ADC)"** | Updated the Analog-to-Digital Conversion Clock Period Block Diagram (see Figure 22-2). |
| **Section 23.0 "Special Features"** | Added Note 3 to the On-chip Voltage Regulator Connections (see Figure 23-1). |
| **Section 26.0 "Electrical Characteristics"** | Updated **"Absolute Maximum Ratings"**.<br>Updated Operating MIPS vs. Voltage (see Table 26-1).<br>Removed parameter DC18 from the DC Temperature and Voltage Specifications (see Table 26-4).<br>Updated the notes in the following tables:<br>• Table 26-5<br>• Table 26-6<br>• Table 26-7<br>• Table 26-8<br>Updated the I/O Pin Output Specifications (see Table 26-10).<br>Updated the Conditions for parameter BO10 (see Table 26-11).<br>Updated the Conditions for parameters D136b, D137b and D138b ($T_A$ = 150ºC) (see Table 26-12). |
| **Section 27.0 "High Temperature Electrical Characteristics"** | Updated **"Absolute Maximum Ratings(1)"**.<br>Updated the I/O Pin Output Specifications (see Table 27-6).<br>Removed Table 26-7: DC Characteristics: Program Memory. |

**NOTES:**