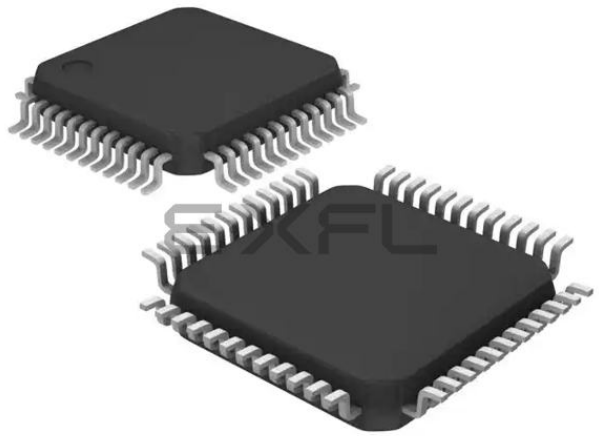

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	56800
Core Size	16-Bit
Speed	60MHz
Connectivity	SCI, SPI
Peripherals	POR, PWM, WDT
Number of I/O	11
Program Memory Size	16KB (8K x 16)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 16
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 8x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/dsp56f801fa60e

Part 1 Overview

1.1 56F801 Features

1.1.1 Digital Signal Processing Core

- Efficient 16-bit 56800 family controller engine with dual Harvard architecture
- As many as 40 Million Instructions Per Second (MIPS) at 80MHz core frequency
- Single-cycle 16 × 16-bit parallel Multiplier-Accumulator (MAC)
- Two 36-bit accumulators including extension bits
- 16-bit bidirectional barrel shifter
- Parallel instruction set with unique processor addressing modes
- Hardware DO and REP loops
- Three internal address buses and one external address bus
- Four internal data buses and one external data bus
- Instruction set supports both DSP and controller functions
- Controller style addressing modes and instructions for compact code
- Efficient C compiler and local variable support
- Software subroutine and interrupt stack with depth limited only by memory
- JTAG/OnCE debug programming interface

1.1.2 Memory

- Harvard architecture permits as many as three simultaneous accesses to Program and Data memory
- On-chip memory including a low-cost, high-volume Flash solution
  - 8K × 16 bit words of Program Flash
  - 1K × 16-bit words of Program RAM
  - 2K × 16-bit words of Data Flash
  - 1K × 16-bit words of Data RAM
  - 2K × 16-bit words of Boot Flash
- Programmable Boot Flash supports customized boot code and field upgrades of stored code through a variety of interfaces (JTAG, SPI)

1.1.3 Peripheral Circuits for 56F801

- Pulse Width Modulator (PWM) with six PWM outputs, two Fault inputs, fault-tolerant design with deadtime insertion; supports both center- and edge-aligned modes
- Two 12-bit, Analog-to-Digital Converters (ADCs), which support two simultaneous conversions with two 4-multiplexed inputs; ADC and PWM modules can be synchronized
- General Purpose Quad Timer: Timer D with three pins (or three additional GPIO lines)
- Serial Communication Interface (SCI) with two pins (or two additional GPIO lines)
- Serial Peripheral Interface (SPI) with configurable four-pin port (or four additional GPIO lines)

A key application-specific feature of the 56F801 is the inclusion of a Pulse Width Modulator (PWM) module. This modules incorporates six complementary, individually programmable PWM signal outputs to enhance motor control functionality. Complementary operation permits programmable dead-time insertion, and separate top and bottom output polarity control. The up-counter value is programmable to support a continuously variable PWM frequency. Both edge- and center-aligned synchronous pulse width control (0% to 100% modulation) are supported. The device is capable of controlling most motor types: ACIM (AC Induction Motors), both BDC and BLDC (Brush and Brushless DC motors), SRM and VRM (Switched and Variable Reluctance Motors), and stepper motors. The PWMs incorporate fault protection and cycle-by-cycle current limiting with sufficient output drive capability to directly drive standard opto-isolators. A “smoke-inhibit”, write-once protection feature for key parameters is also included. The PWM is double-buffered and includes interrupt control to permit integral reload rates to be programmable from 1 to 16. The PWM modules provide a reference output to synchronize the Analog-to-Digital Converters.

The 56F801 incorporates an 8 input, 12-bit Analog-to-Digital Converter (ADC). A full set of standard programmable peripherals is provided that include a Serial Communications Interface (SCI), a Serial Peripheral Interface (SPI), and two Quad Timers. Any of these interfaces can be used as General-Purpose Input/Outputs (GPIO) if that function is not required. An on-chip relaxation oscillator provides flexibility in the choice of either on-chip or externally supplied frequency reference for chip timing operations. Application code is used to select which source is to be used.

1.3 State of the Art Development Environment

- Processor Expert™ (PE) provides a Rapid Application Design (RAD) tool that combines easy-to-use component-based software application creation with an expert knowledge system.
- The Code Warrior Integrated Development Environment is a sophisticated tool for code navigation, compiling, and debugging. A complete set of evaluation modules (EVMs) and development system cards will support concurrent engineering. Together, PE, Code Warrior and EVMs create a complete, scalable tools solution for easy, fast, and efficient development.

1.4 Product Documentation

The four documents listed in **Table 1-1** are required for a complete description and proper design with the 56F801. Documentation is available from local Freescale distributors, Freescale semiconductor sales offices, Freescale Literature Distribution Centers, or online at **www.freescale.com**.

Table 1-1 56F801 Chip Documentation

Topic	Description	Order Number
56800E Family Manual	Detailed description of the 56800 family architecture, and 16-bit core processor and the instruction set	56800EFM
DSP56F801/803/805/807 User's Manual	Detailed description of memory, peripherals, and interfaces of the 56F801, 56F803, 56F805, and 56F807	DSP56F801-7UM
56F801 Technical Data Sheet	Electrical and timing specifications, pin descriptions, and package descriptions (this document)	DSP56F801
56F801 Errata	Details any chip issues that might be present	56F801E

1.5 Data Sheet Conventions

This data sheet uses the following conventions:

$\overline{\text{OVERBAR}}$	This is used to indicate a signal that is active when pulled low. For example, the $\overline{\text{RESET}}$ pin is active when low.
"asserted"	A high true (active high) signal is high or a low true (active low) signal is low.
"deasserted"	A high true (active high) signal is low or a low true (active low) signal is high.

Examples:	Signal/Symbol	Logic State	Signal State	Voltage[1]
	$\overline{\text{PIN}}$	True	Asserted	V_{IL}/V_{OL}
	$\overline{\text{PIN}}$	False	Deasserted	V_{IH}/V_{OH}
	PIN	True	Asserted	V_{IH}/V_{OH}
	PIN	False	Deasserted	V_{IL}/V_{OL}

1. Values for V_{IL}, V_{OL}, V_{IH}, and V_{OH} are defined by individual product specifications.

Part 2 Signal/Connection Descriptions

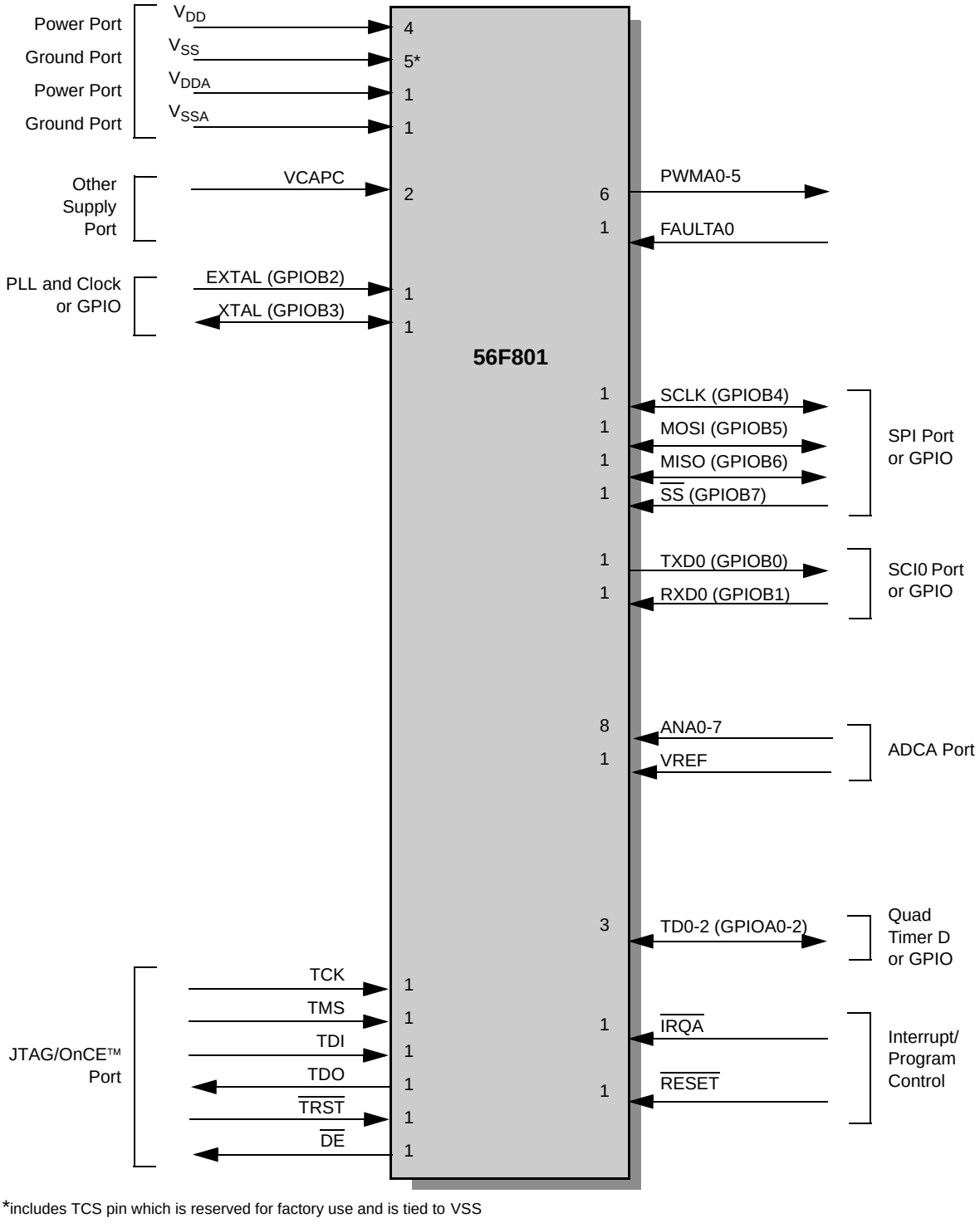
2.1 Introduction

The input and output signals of the 56F801 are organized into functional groups, as shown in **Table 2-1** and as illustrated in **Figure 2-1**. In **Table 2-2** through **Table 2-12**, each table row describes the signal or signals present on a pin.

Table 2-1 Functional Group Pin Allocations

Functional Group	Number of Pins	Detailed Description
Power (V_{DD} or V_{DDA})	5	**Table 2-2**
Ground (V_{SS} or V_{SSA})	6	**Table 2-3**
Supply Capacitors	2	**Table 2-4**
PLL and Clock	2	**Table 2-5**
Interrupt and Program Control	2	**Table 2-6**
Pulse Width Modulator (PWM) Port	7	**Table 2-7**
Serial Peripheral Interface (SPI) Port[1]	4	**Table 2-8**
Serial Communications Interface (SCI) Port[1]	2	**Table 2-9**
Analog-to-Digital Converter (ADC) Port	9	**Table 2-10**
Quad Timer Module Port	3	**Table 2-11**
JTAG/On-Chip Emulation (OnCE)	6	**Table 2-12**

1. Alternately, GPIO pins



*includes TCS pin which is reserved for factory use and is tied to VSS

Figure 2-1 56F801 Signals Identified by Functional Group[1]

1. Alternate pin functionality is shown in parenthesis.

Table 2-5 PLL and Clock (Continued)

No. of Pins	Signal Name	Signal Type	State During Reset	Signal Description
1	**XTAL**	Output	Chip-driven	**Crystal Oscillator Output**—This output should be connected to an 8MHz external crystal or ceramic resonator. For more information, please refer to Section 3.5. This pin can also be connected to an external clock source. For more information, please refer to Section 3.5.3.
	GPIOB3	Input/ Output	Input	**Port B GPIO**—This multiplexed pin is a General Purpose I/O (GPIO) pin that can be programmed as an input or output pin. This I/O can be utilized when using the on-chip relaxation oscillator so the XTAL pin is not needed.

2.4 Interrupt and Program Control Signals

Table 2-6 Interrupt and Program Control Signals

No. of Pins	Signal Name	Signal Type	State During Reset	Signal Description
1	**$\overline{\text{IRQA}}$**	Input (Schmitt)	Input	**External Interrupt Request A**—The $\overline{\text{IRQA}}$ input is a synchronized external interrupt request that indicates that an external device is requesting service. It can be programmed to be level-sensitive or negative-edge- triggered.
1	**$\overline{\text{RESET}}$**	Input (Schmitt)	Input	**Reset**—This input is a direct hardware reset on the processor. When $\overline{\text{RESET}}$ is asserted low, the controller is initialized and placed in the Reset state. A Schmitt trigger input is used for noise immunity. When the $\overline{\text{RESET}}$ pin is deasserted, the initial chip operating mode is latched from the EXTBOOT pin. The internal reset signal will be deasserted synchronous with the internal clocks, after a fixed number of internal clocks. To ensure complete hardware reset, $\overline{\text{RESET}}$ and $\overline{\text{TRST}}$ should be asserted together. The only exception occurs in a debugging environment when a hardware device reset is required and it is necessary not to reset the OnCE/JTAG module. In this case, assert $\overline{\text{RESET}}$, but do not assert $\overline{\text{TRST}}$.

2.5 Pulse Width Modulator (PWM) Signals

Table 2-7 Pulse Width Modulator (PWMA) Signals

No. of Pins	Signal Name	Signal Type	State During Reset	Signal Description
6	**PWMA0-5**	Output	Tri-stated	**PWMA0-5**— These are six PWMA output pins.
1	**FAULTA0**	Input (Schmitt)	Input	**FAULTA0**— This fault input pin is used for disabling selected PWMA outputs in cases where fault conditions originate off-chip.

2.6 Serial Peripheral Interface (SPI) Signals

Table 2-8 Serial Peripheral Interface (SPI) Signals

No. of Pins	Signal Name	Signal Type	State During Reset	Signal Description
1	**MISO** **GPIOB6**	Input/Output Input/Output	Input Input	**SPI Master In/Slave Out (MISO)**—This serial data pin is an input to a master device and an output from a slave device. The MISO line of a slave device is placed in the high-impedance state if the slave device is not selected. **Port E GPIO**—This pin is a General Purpose I/O (GPIO) pin that can be individually programmed as input or output pin. After reset, the default state is MISO.
1	**MOSI** **GPIOB5**	Input/Output Input/Output	Input Input	**SPI Master Out/Slave In (MOSI)**—This serial data pin is an output from a master device and an input to a slave device. The master device places data on the MOSI line a half-cycle before the clock edge that the slave device uses to latch the data. **Port E GPIO**—This pin is a General Purpose I/O (GPIO) pin that can be individually programmed as input or output pin. After reset, the default state is MOSI.
1	**SCLK** **GPIOB4**	Input/Output Input/Output	Input Input	**SPI Serial Clock**—In master mode, this pin serves as an output, clocking slaved listeners. In slave mode, this pin serves as the data clock input. **Port E GPIO**—This pin is a General Purpose I/O (GPIO) pin that can be individually programmed as an input or output pin. After reset, the default state is SCLK.
1	**$\overline{SS}$** **GPIOB7**	Input Input/Output	Input Input	**SPI Slave Select**—In master mode, this pin is used to arbitrate multiple masters. In slave mode, this pin is used to select the slave. **Port E GPIO**—This pin is a General Purpose I/O (GPIO) pin that can be individually programmed as an input or output pin. After reset, the default state is $\overline{SS}$.

3.2 DC Electrical Characteristics

Table 3-4 DC Electrical Characteristics

Operating Conditions: $V_{SS} = V_{SSA} = 0$ V, $V_{DD} = V_{DDA} = 3.0–3.6$V, $T_A = –40°$ to $+85°C$, $C_L \leq 50$pF

Characteristic	Symbol	Min	Typ	Max	Unit
Input high voltage (XTAL/EXTAL)	V_{IHC}	2.25	—	2.75	V
Input low voltage (XTAL/EXTAL)	V_{ILC}	0	—	0.5	V
Input high voltage [GPIOB(2:3)][1]	$V_{IH[GPIOB(2:3)]}$	2.0	—	3.6	V
Input low voltage [GPIOB(2:3)][1]	$V_{IL[GPIOB(2:3)]}$	-0.3	—	0.8	V
Input high voltage (Schmitt trigger inputs)[2]	V_{IHS}	2.2	—	5.5	V
Input low voltage (Schmitt trigger inputs)[2]	V_{ILS}	-0.3	—	0.8	V
Input high voltage (all other digital inputs)	V_{IH}	2.0	—	5.5	V
Input low voltage (all other digital inputs)	V_{IL}	-0.3	—	0.8	V
Input current high (pullup/pulldown resistors disabled, $V_{IN}=V_{DD}$)	I_{IH}	-1	—	1	µA
Input current low (pullup/pulldown resistors disabled, $V_{IN}=V_{SS}$)	I_{IL}	-1	—	1	µA
Input current high (with pullup resistor, $V_{IN}=V_{DD}$)	I_{IHPU}	-1	—	1	µA
Input current low (with pullup resistor, $V_{IN}=V_{SS}$)	I_{ILPU}	-210	—	-50	µA
Input current high (with pulldown resistor, $V_{IN}=V_{DD}$)	I_{IHPD}	20	—	180	µA
Input current low (with pulldown resistor, $V_{IN}=V_{SS}$)	I_{ILPD}	-1	—	1	µA
Nominal pullup or pulldown resistor value	R_{PU}, R_{PD}		30		KΩ
Output tri-state current low	I_{OZL}	-10	—	10	µA
Output tri-state current high	I_{OZH}	-10	—	10	µA
Input current high (analog inputs, $V_{IN}=V_{DDA}$)[3]	I_{IHA}	-15	—	15	µA
Input current low (analog inputs, $V_{IN}=V_{SSA}$)[3]	I_{ILA}	-15	—	15	µA
Output High Voltage (at I_{OH})	V_{OH}	$V_{DD} – 0.7$	—	—	V
Output Low Voltage (at I_{OL})	V_{OL}	—	—	0.4	V
Output source current	I_{OH}	4	—	—	mA
Output sink current	I_{OL}	4	—	—	mA
PWM pin output source current[4]	I_{OHP}	10	—	—	mA
PWM pin output sink current[5]	I_{OLP}	16	—	—	mA
Input capacitance	C_{IN}	—	8	—	pF
Output capacitance	C_{OUT}	—	12	—	pF

Table 3-4 DC Electrical Characteristics (Continued)

Operating Conditions: $V_{SS} = V_{SSA} = 0$ V, $V_{DD} = V_{DDA} = 3.0–3.6$V, $T_A = –40°$ to $+85°$C, $C_L \leq 50$pF

Characteristic	Symbol	Min	Typ	Max	Unit
V_{DD} supply current	I_{DDT}[6]				
Run[7] (80MHz operation)		—	120	130	mA
Run[7] (60MHz operation)		—	102	111	mA
Wait[8]		—	96	102	mA
Stop		—	62	70	mA
Low Voltage Interrupt, external power supply[9]	V_{EIO}	2.4	2.7	3.0	V
Low Voltage Interrupt, internal power supply[10]	V_{EIC}	2.0	2.2	2.4	V
Power on Reset[11]	V_{POR}	—	1.7	2.0	V

1. Since the GPIOB[2:3] signals are shared with the XTAL/EXTAL function, these inputs are not 5.5 volt tolerant.
2. Schmitt Trigger inputs are: FAULTA0, $\overline{\text{IRQA}}$, $\overline{\text{RESET}}$, TCS, TCK, TMS, TDI, and $\overline{\text{TRST}}$.
3. Analog inputs are: ANA[0:7], XTAL and EXTAL. Specification assumes ADC is not sampling.
4. PWM pin output source current measured with 50% duty cycle.
5. PWM pin output sink current measured with 50% duty cycle.
6. $I_{DDT} = I_{DD} + I_{DDA}$ (Total supply current for $V_{DD} + V_{DDA}$)
7. Run (operating) I_{DD} measured using 8MHz clock source. All inputs 0.2V from rail; outputs unloaded. All ports configured as inputs; measured with all modules enabled.
8. Wait I_{DD} measured using external square wave clock source (f_{osc} = 8MHz) into XTAL; all inputs 0.2V from rail; no DC loads; less than 50pF on all outputs. C_L = 20pF on EXTAL; all ports configured as inputs; EXTAL capacitance linearly affects wait I_{DD}; measured with PLL enabled.
9. This low voltage interrupt monitors the V_{DDA} external power supply. V_{DDA} is generally connected to the same potential as V_{DD} via separate traces. If V_{DDA} drops below V_{EIO}, an interrupt is generated. Functionality of the device is guaranteed under transient conditions when $V_{DDA} \geq V_{EIO}$ (between the minimum specified V_{DD} and the point when the V_{EIO} interrupt is generated).
10. This low voltage interrupt monitors the internally regulated core power supply. If the output from the internal voltage is regulator drops below V_{EIC}, an interrupt is generated. Since the core logic supply is internally regulated, this interrupt will not be generated unless the external power supply drops below the minimum specified value (3.0V).
11. Power–on reset occurs whenever the internally regulated 2.5V digital supply drops below 1.5V typical. While power is ramping up, this signal remains active for as long as the internal 2.5V is below 1.5V typical no matter how long the ramp up rate is. The internally regulated voltage is typically 100 mV less than V_{DD} during ramp up until 2.5V is reached, at which time it self regulates.

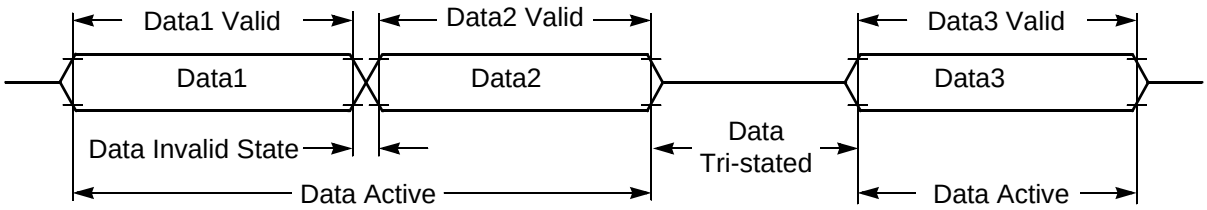


Figure 3-3 Signal States

3.4 Flash Memory Characteristics

Table 3-5 Flash Memory Truth Table

Mode	XE[1]	YE[2]	SE[3]	OE[4]	PROG[5]	ERASE[6]	MAS1[7]	NVSTR[8]
Standby	L	L	L	L	L	L	L	L
Read	H	H	H	H	L	L	L	L
Word Program	H	H	L	L	H	L	L	H
Page Erase	H	L	L	L	L	H	L	H
Mass Erase	H	L	L	L	L	H	H	H

1. X address enable, all rows are disabled when XE = 0
2. Y address enable, YMUX is disabled when YE = 0
3. Sense amplifier enable
4. Output enable, tri-state Flash data out bus when OE = 0
5. Defines program cycle
6. Defines erase cycle
7. Defines mass erase cycle, erase whole block
8. Defines non-volatile store cycle

Table 3-6 IFREN Truth Table

Mode	IFREN = 1	IFREN = 0
Read	Read information block	Read main memory block
Word program	Program information block	Program main memory block
Page erase	Erase information block	Erase main memory block
Mass erase	Erase both block	Erase main memory block

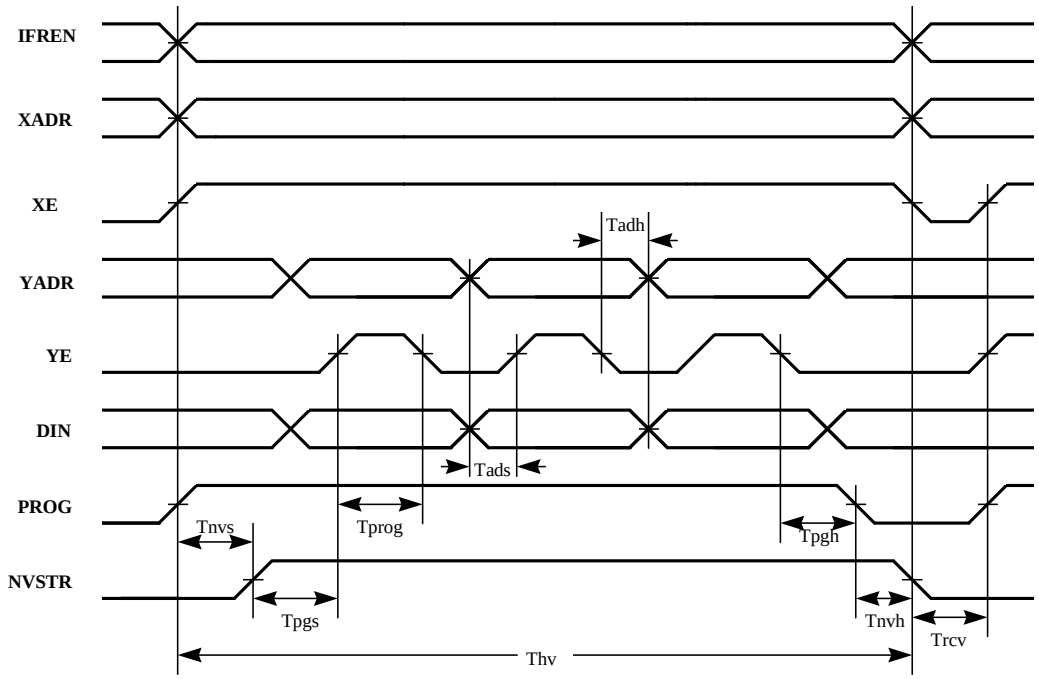


Figure 3-4 Flash Program Cycle

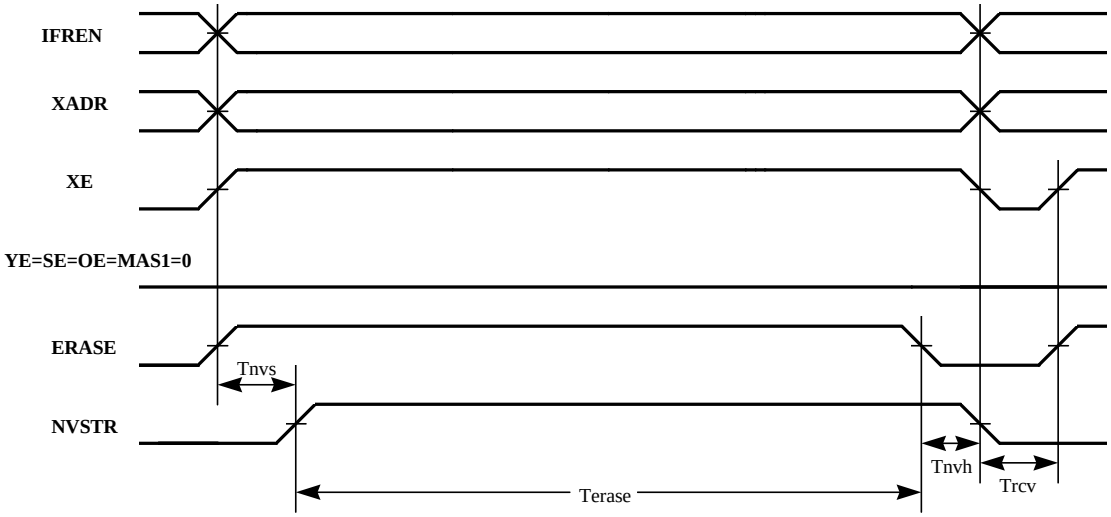


Figure 3-5 Flash Erase Cycle

3.5.3 External Clock Source

The recommended method of connecting an external clock is given in **Figure 3-9**. The external clock source is connected to XTAL and the EXTAL pin is grounded.

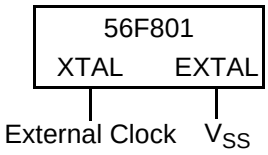


Figure 3-9 Connecting an External Clock Signal

Table 3-8 External Clock Operation Timing Requirements[3]

Operating Conditions: $V_{SS} = V_{SSA} = 0$ V, $V_{DD} = V_{DDA} = 3.0–3.6$ V, $T_A = –40°$ to $+85°C$

Characteristic	Symbol	Min	Typ	Max	Unit
Frequency of operation (external clock driver)[1]	f_{osc}	0	—	80[2]	MHz
Clock Pulse Width[3, 4]	t_{PW}	6.25	—	—	ns

1. See **Figure 3-9** for details on using the recommended connection of an external clock driver.
2. May not exceed 60MHz for the DSP56F801FA60 device.
3. The high or low pulse width must be no smaller than 6.25ns or the chip will not function. However, the high pulse width does not have to be any particular percent of the low pulse width.
4. Parameters listed are guaranteed by design.

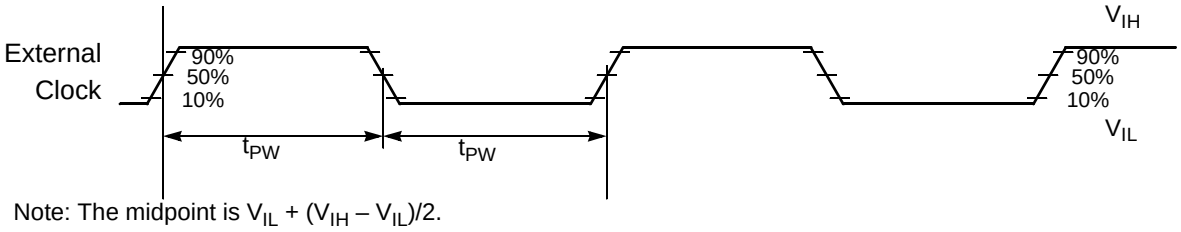


Figure 3-10 External Clock Timing

3.5.4 Use of On-Chip Relaxation Oscillator

An internal relaxation oscillator can supply the reference frequency when an external frequency source or crystal are not used. During a 56F801 boot or reset sequence, the relaxation oscillator is enabled by default, and the PRECS bit in the PLLCR word is set to 0 (**Section 3.5**). If an external oscillator is connected, the relaxation oscillator can be deselected instead by setting the PRECS bit in the PLLCR to 1. When this occurs, the PRECSS bit in the PLLSR (prescaler clock select status register) data word also sets to 1. If a changeover between internal and external oscillators is required at startup, internal device circuits

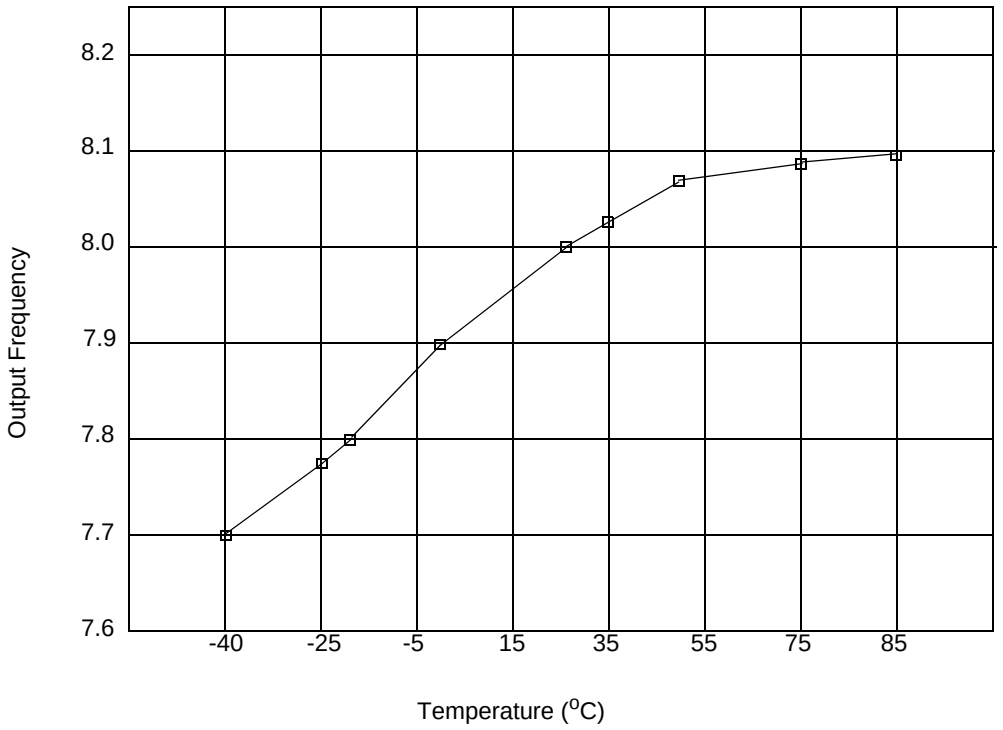


Figure 3-11 Typical Relaxation Oscillator Frequency vs. Temperature (Trimmed to 8MHz @ 25°C)

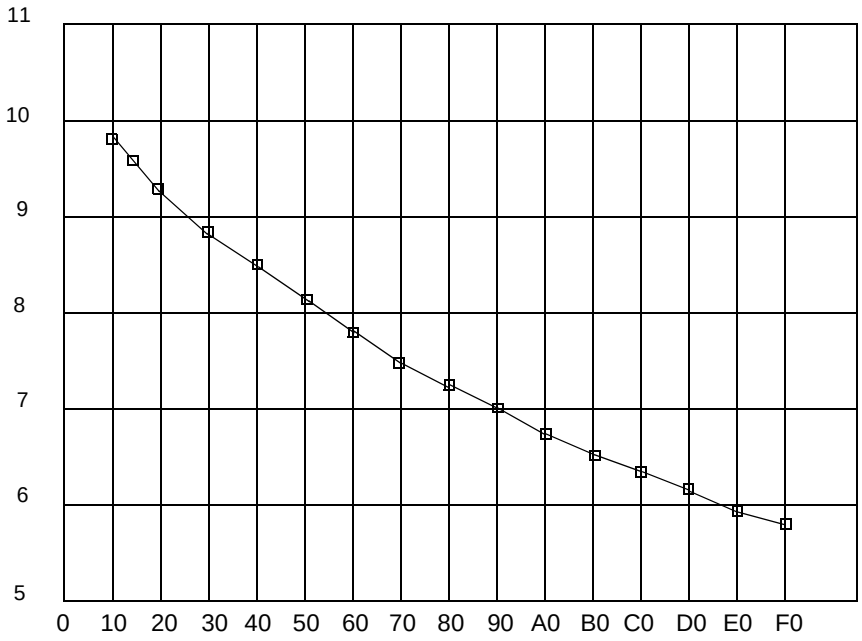


Figure 3-12 Typical Relaxation Oscillator Frequency vs. Trim Value @ 25°C

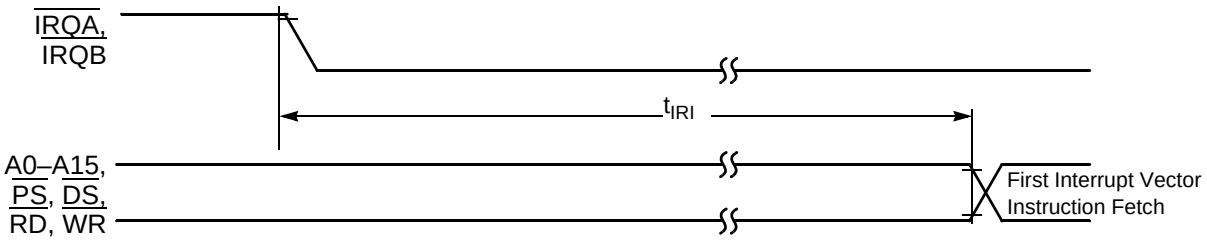


Figure 3-16 Interrupt from Wait State Timing

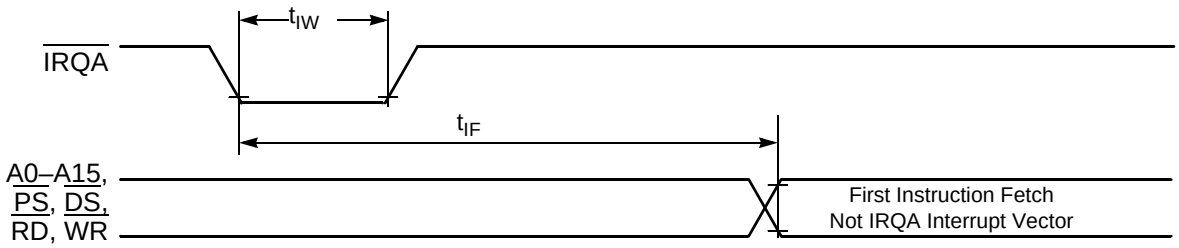


Figure 3-17 Recovery from Stop State Using Asynchronous Interrupt Timing

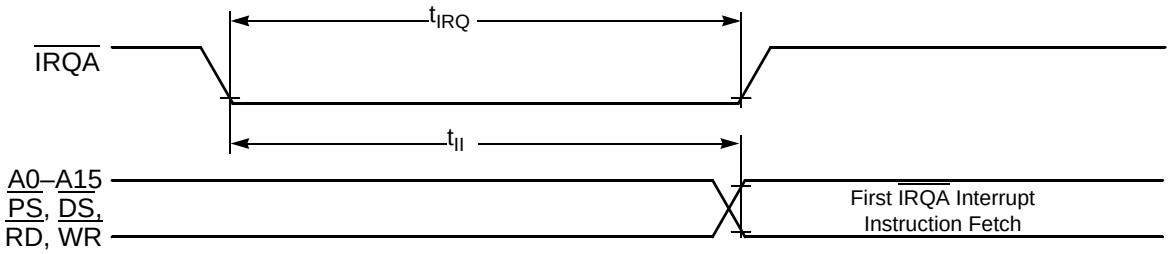


Figure 3-18 Recovery from Stop State Using $\overline{\text{IRQA}}$ Interrupt Service

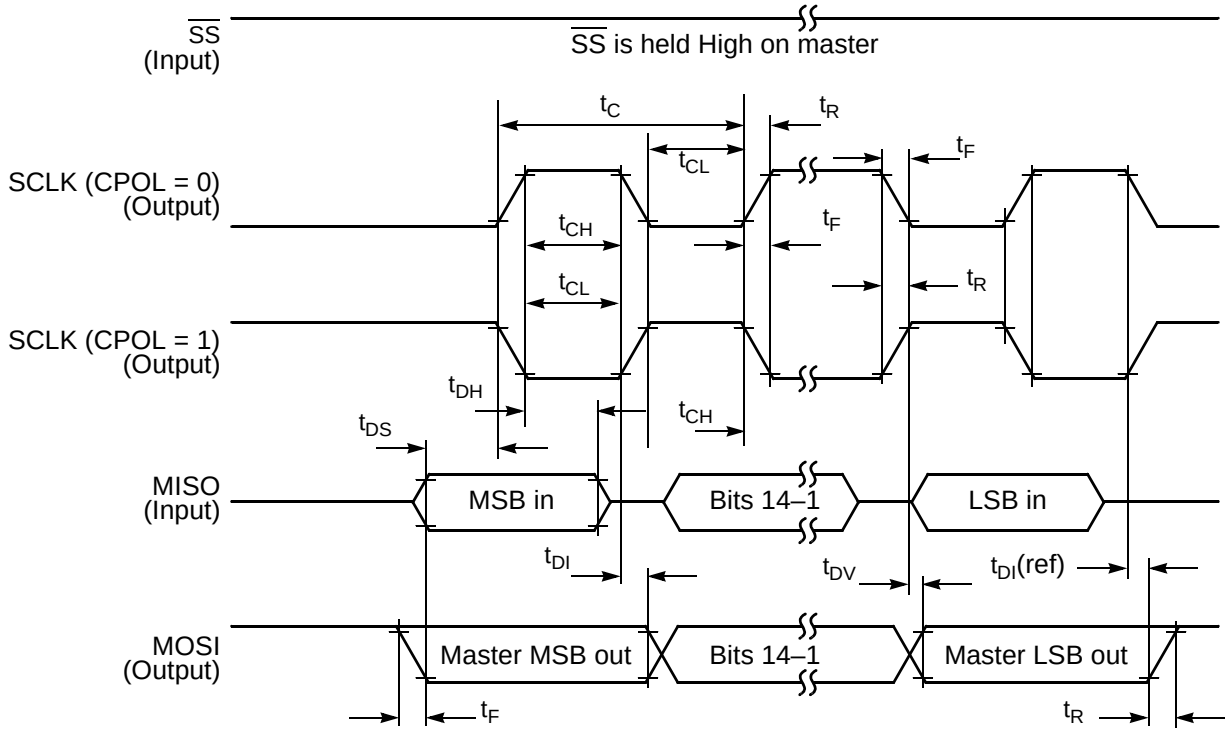


Figure 3-19 SPI Master Timing (CPHA = 0)

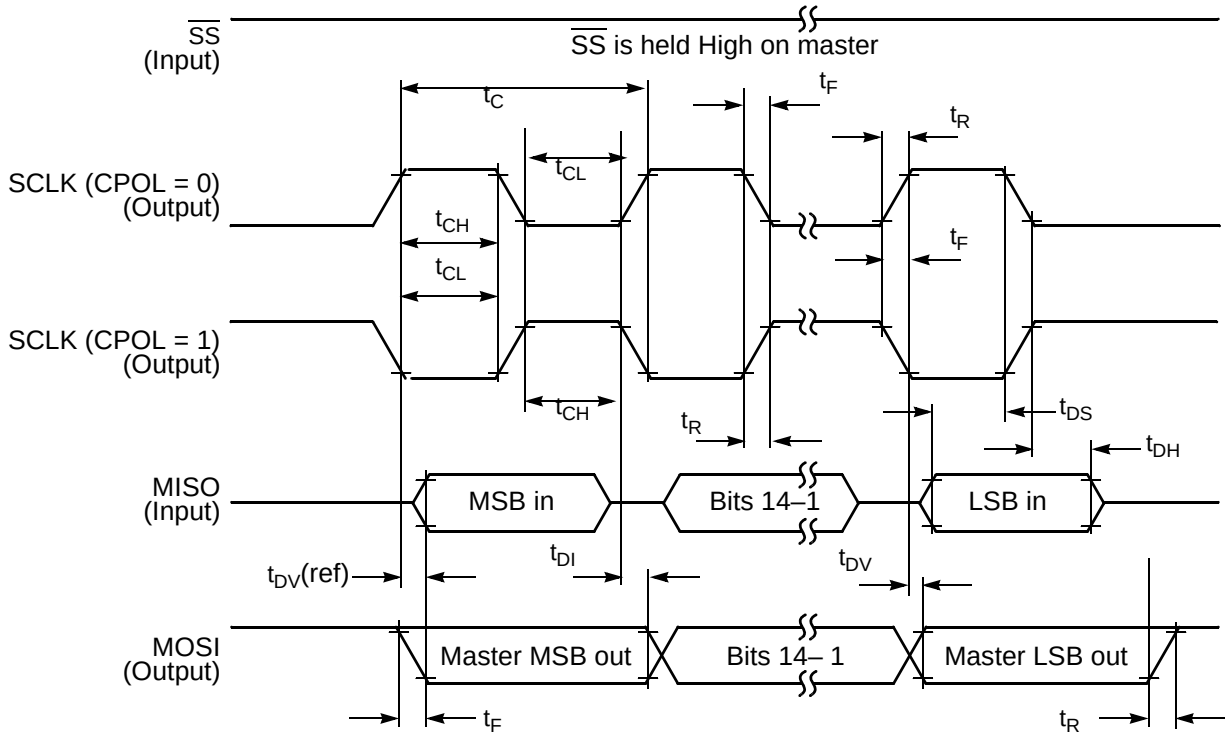


Figure 3-20 SPI Master Timing (CPHA = 1)

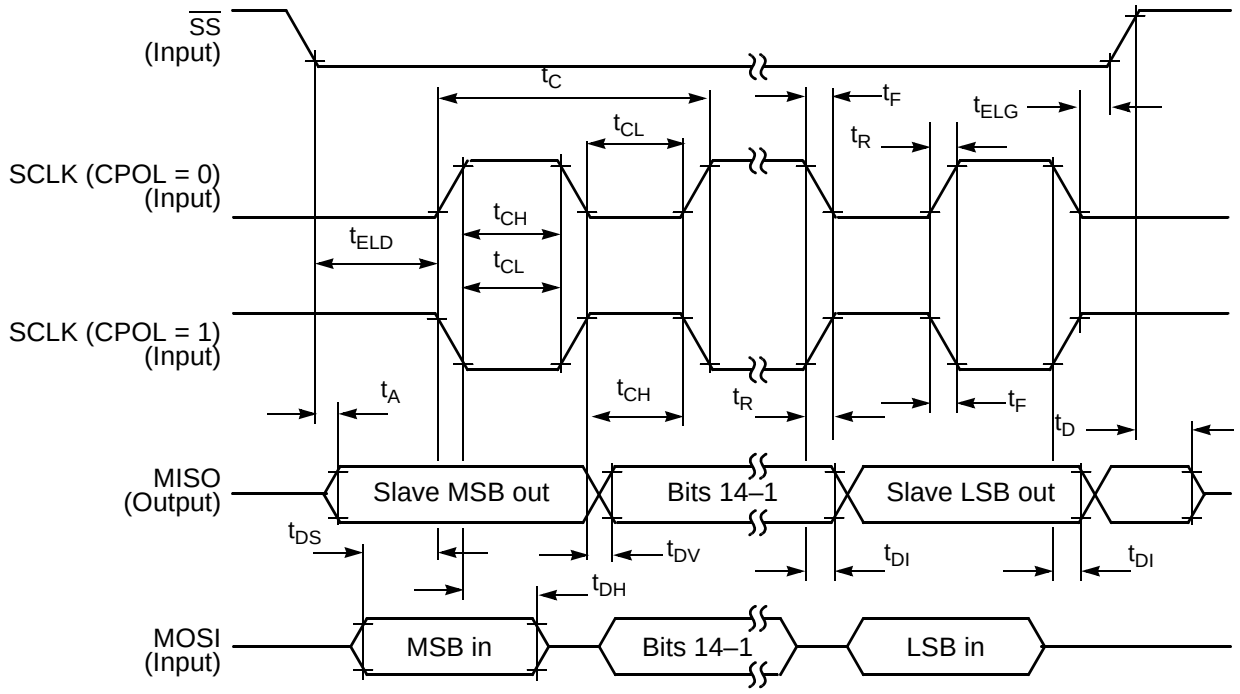


Figure 3-21 SPI Slave Timing (CPHA = 0)

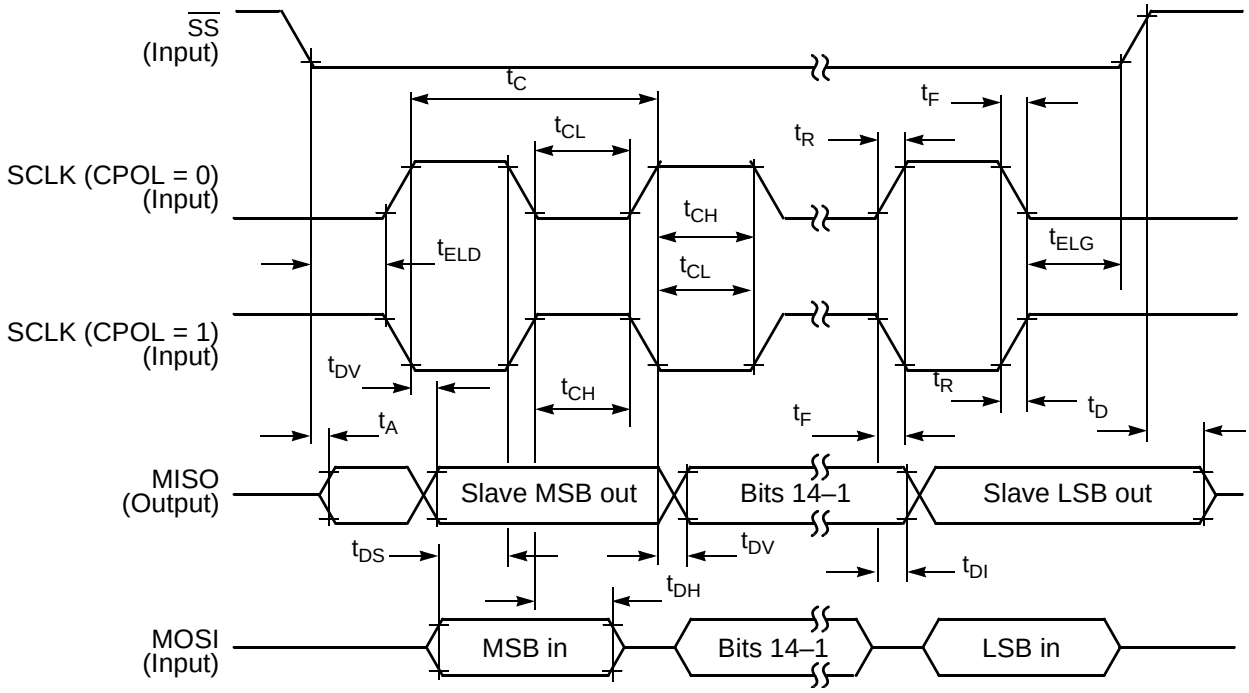


Figure 3-22 SPI Slave Timing (CPHA = 1)

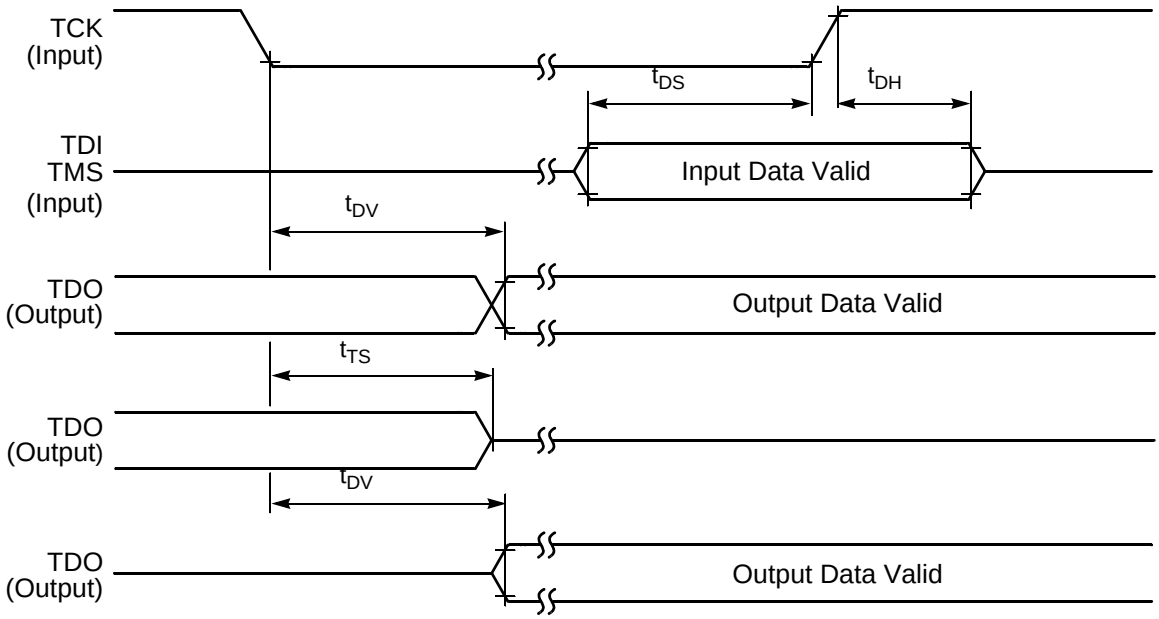


Figure 3-28 Test Access Port Timing Diagram

Figure 3-29 $\overline{\text{TRST}}$ Timing Diagram

Figure 3-30 OnCE—Debug Event

Part 4 Packaging

4.1 Package and Pin-Out Information 56F801

This section contains package and pin-out information for the 48-pin LQFP configuration of the 56F801.

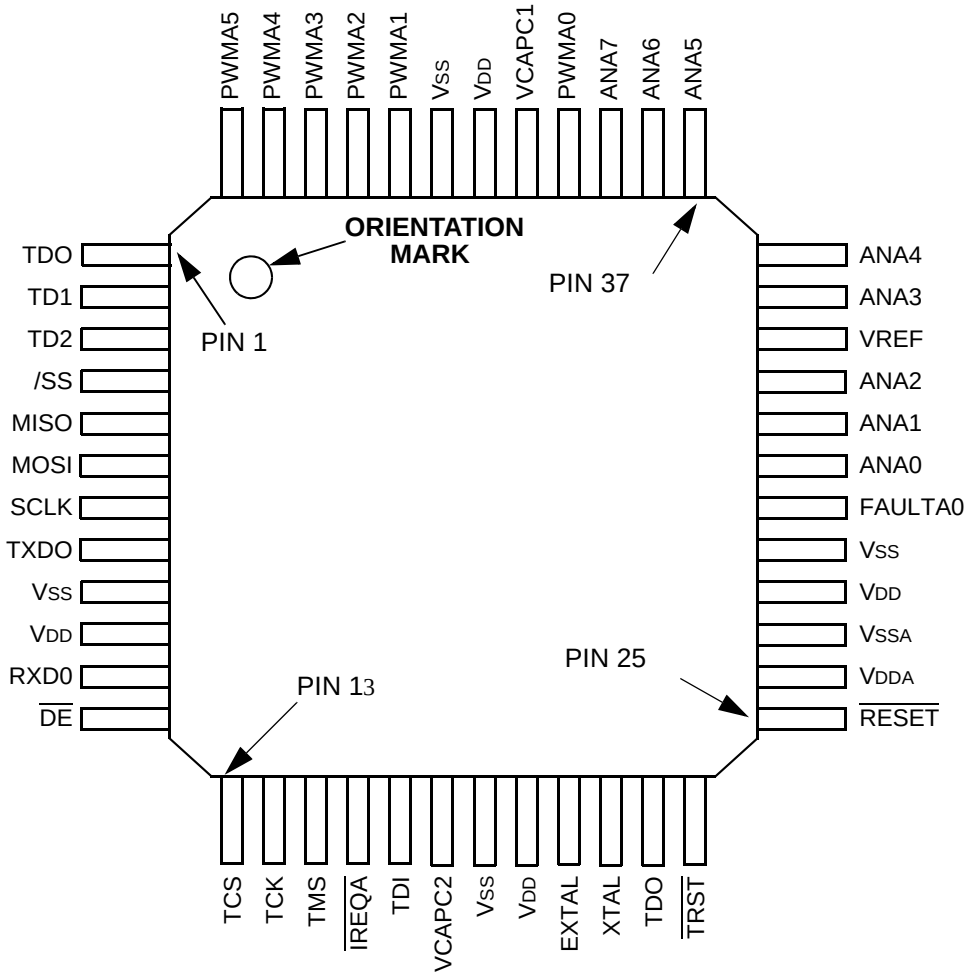


Figure 4-1 Top View, 56F801 48-pin LQFP Package

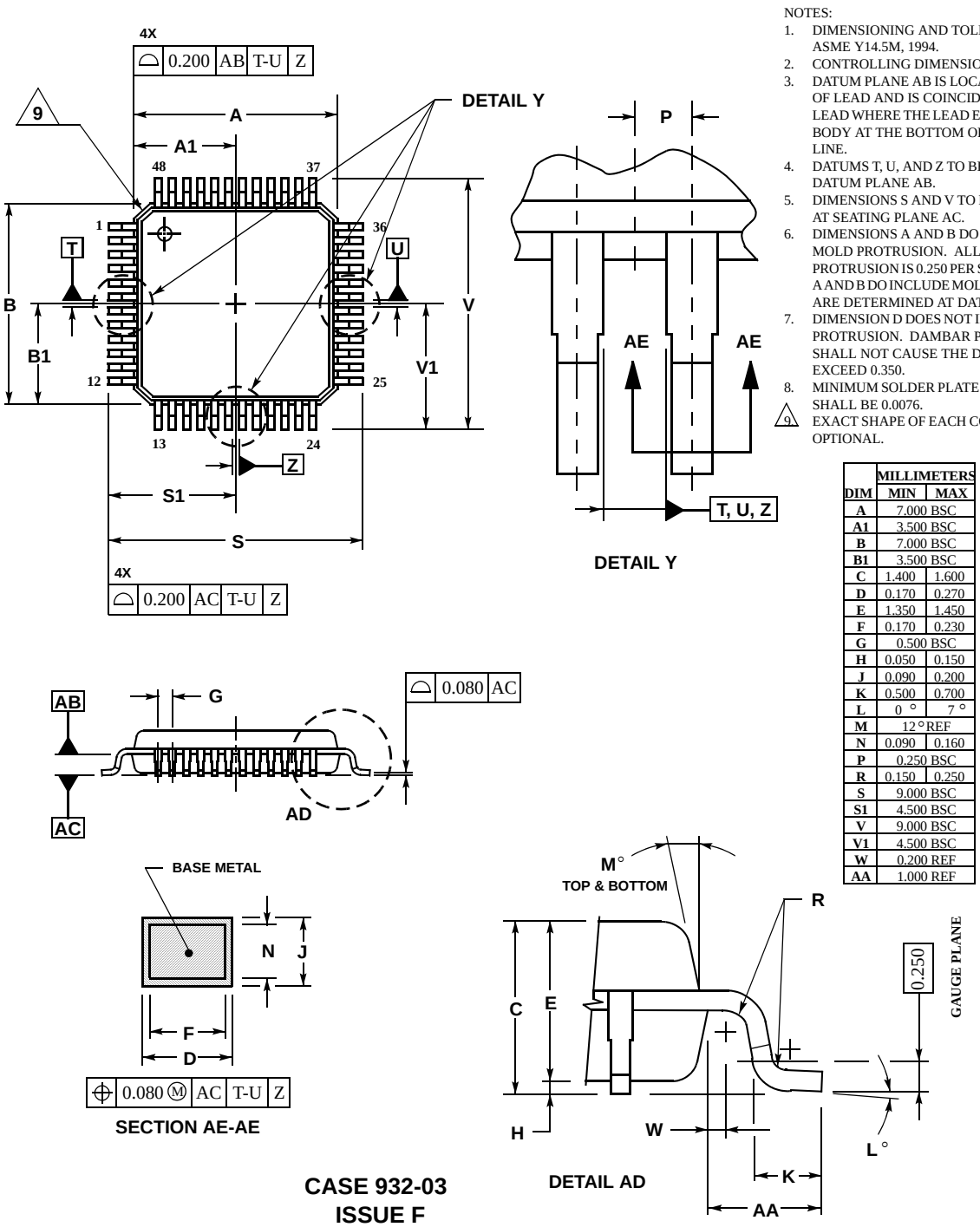


Figure 4-2 48-pin LQFP Mechanical Information

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