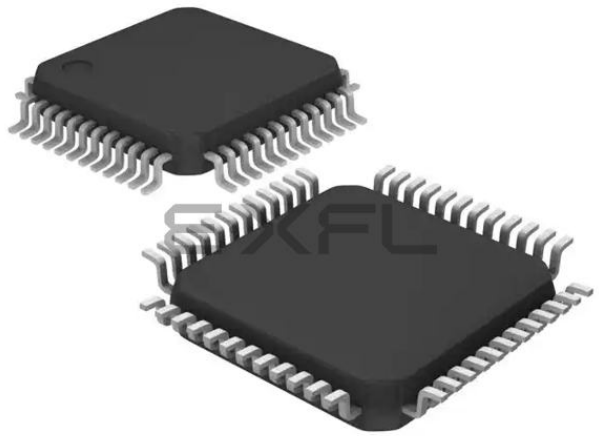

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	56800
Core Size	16-Bit
Speed	80MHz
Connectivity	SCI, SPI
Peripherals	POR, PWM, WDT
Number of I/O	11
Program Memory Size	16KB (8K x 16)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 16
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 8x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/dsp56f801fa80e

Document Revision History

Version History	Description of Change
Rev. 17	Added revision history. Added this text to footnote 2 in **Table 3-8**: “However, the high pulse width does not have to be any particular percent of the low pulse width.”

Part 1 Overview

1.1 56F801 Features

1.1.1 Digital Signal Processing Core

- Efficient 16-bit 56800 family controller engine with dual Harvard architecture
- As many as 40 Million Instructions Per Second (MIPS) at 80MHz core frequency
- Single-cycle 16 × 16-bit parallel Multiplier-Accumulator (MAC)
- Two 36-bit accumulators including extension bits
- 16-bit bidirectional barrel shifter
- Parallel instruction set with unique processor addressing modes
- Hardware DO and REP loops
- Three internal address buses and one external address bus
- Four internal data buses and one external data bus
- Instruction set supports both DSP and controller functions
- Controller style addressing modes and instructions for compact code
- Efficient C compiler and local variable support
- Software subroutine and interrupt stack with depth limited only by memory
- JTAG/OnCE debug programming interface

1.1.2 Memory

- Harvard architecture permits as many as three simultaneous accesses to Program and Data memory
- On-chip memory including a low-cost, high-volume Flash solution
  - 8K × 16 bit words of Program Flash
  - 1K × 16-bit words of Program RAM
  - 2K × 16-bit words of Data Flash
  - 1K × 16-bit words of Data RAM
  - 2K × 16-bit words of Boot Flash
- Programmable Boot Flash supports customized boot code and field upgrades of stored code through a variety of interfaces (JTAG, SPI)

1.1.3 Peripheral Circuits for 56F801

- Pulse Width Modulator (PWM) with six PWM outputs, two Fault inputs, fault-tolerant design with deadtime insertion; supports both center- and edge-aligned modes
- Two 12-bit, Analog-to-Digital Converters (ADCs), which support two simultaneous conversions with two 4-multiplexed inputs; ADC and PWM modules can be synchronized
- General Purpose Quad Timer: Timer D with three pins (or three additional GPIO lines)
- Serial Communication Interface (SCI) with two pins (or two additional GPIO lines)
- Serial Peripheral Interface (SPI) with configurable four-pin port (or four additional GPIO lines)

1.4 Product Documentation

The four documents listed in **Table 1-1** are required for a complete description and proper design with the 56F801. Documentation is available from local Freescale distributors, Freescale semiconductor sales offices, Freescale Literature Distribution Centers, or online at **www.freescale.com**.

Table 1-1 56F801 Chip Documentation

Topic	Description	Order Number
56800E Family Manual	Detailed description of the 56800 family architecture, and 16-bit core processor and the instruction set	56800EFM
DSP56F801/803/805/807 User's Manual	Detailed description of memory, peripherals, and interfaces of the 56F801, 56F803, 56F805, and 56F807	DSP56F801-7UM
56F801 Technical Data Sheet	Electrical and timing specifications, pin descriptions, and package descriptions (this document)	DSP56F801
56F801 Errata	Details any chip issues that might be present	56F801E

1.5 Data Sheet Conventions

This data sheet uses the following conventions:

$\overline{\text{OVERBAR}}$	This is used to indicate a signal that is active when pulled low. For example, the $\overline{\text{RESET}}$ pin is active when low.
"asserted"	A high true (active high) signal is high or a low true (active low) signal is low.
"deasserted"	A high true (active high) signal is low or a low true (active low) signal is high.

Examples:	Signal/Symbol	Logic State	Signal State	Voltage[1]
	$\overline{\text{PIN}}$	True	Asserted	V_{IL}/V_{OL}
	$\overline{\text{PIN}}$	False	Deasserted	V_{IH}/V_{OH}
	PIN	True	Asserted	V_{IH}/V_{OH}
	PIN	False	Deasserted	V_{IL}/V_{OL}

1. Values for V_{IL}, V_{OL}, V_{IH}, and V_{OH} are defined by individual product specifications.

Part 2 Signal/Connection Descriptions

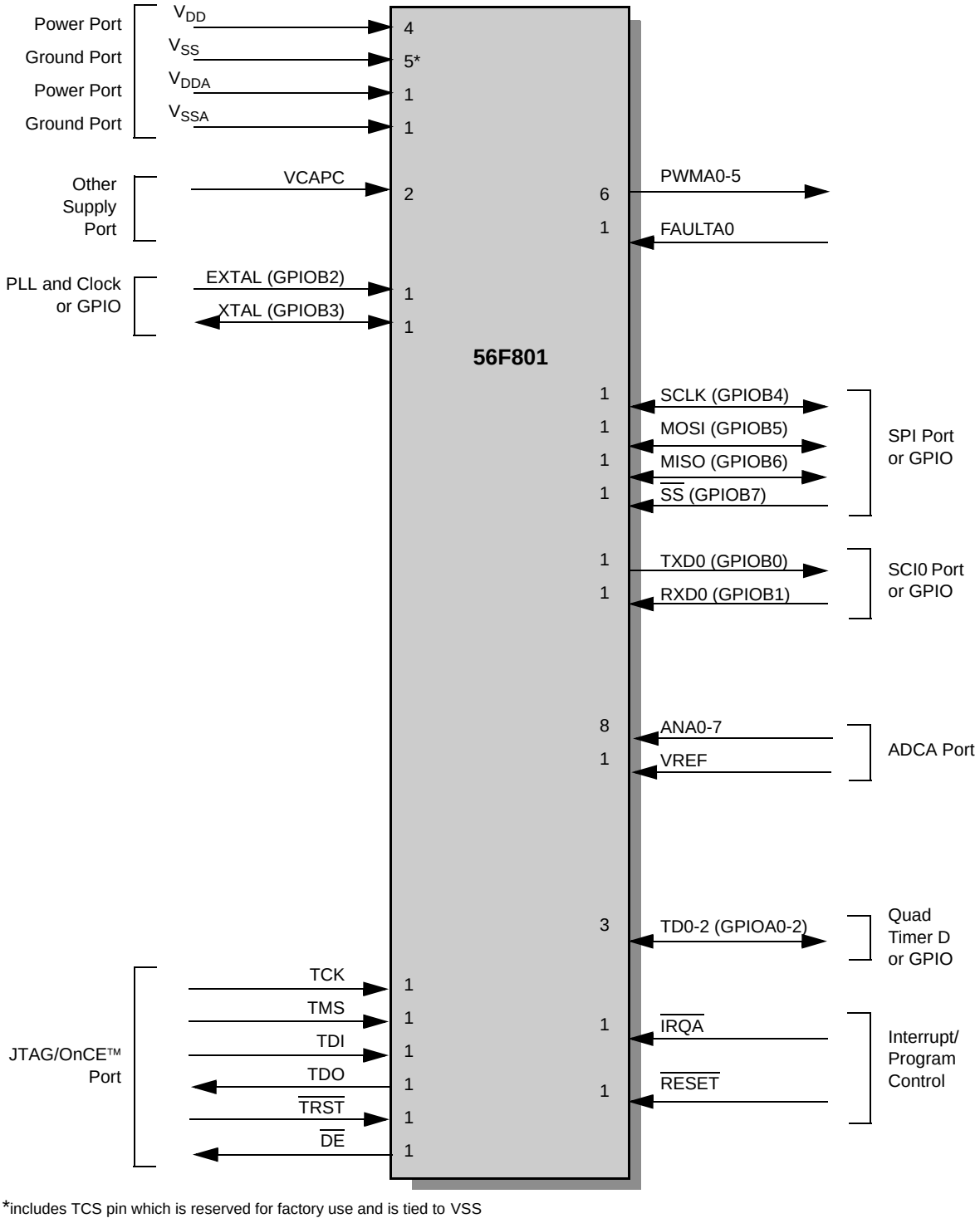
2.1 Introduction

The input and output signals of the 56F801 are organized into functional groups, as shown in **Table 2-1** and as illustrated in **Figure 2-1**. In **Table 2-2** through **Table 2-12**, each table row describes the signal or signals present on a pin.

Table 2-1 Functional Group Pin Allocations

Functional Group	Number of Pins	Detailed Description
Power (V_{DD} or V_{DDA})	5	**Table 2-2**
Ground (V_{SS} or V_{SSA})	6	**Table 2-3**
Supply Capacitors	2	**Table 2-4**
PLL and Clock	2	**Table 2-5**
Interrupt and Program Control	2	**Table 2-6**
Pulse Width Modulator (PWM) Port	7	**Table 2-7**
Serial Peripheral Interface (SPI) Port[1]	4	**Table 2-8**
Serial Communications Interface (SCI) Port[1]	2	**Table 2-9**
Analog-to-Digital Converter (ADC) Port	9	**Table 2-10**
Quad Timer Module Port	3	**Table 2-11**
JTAG/On-Chip Emulation (OnCE)	6	**Table 2-12**

1. Alternately, GPIO pins



*includes TCS pin which is reserved for factory use and is tied to VSS

Figure 2-1 56F801 Signals Identified by Functional Group[1]

1. Alternate pin functionality is shown in parenthesis.

2.6 Serial Peripheral Interface (SPI) Signals

Table 2-8 Serial Peripheral Interface (SPI) Signals

No. of Pins	Signal Name	Signal Type	State During Reset	Signal Description
1	**MISO** **GPIOB6**	Input/Output Input/Output	Input Input	**SPI Master In/Slave Out (MISO)**—This serial data pin is an input to a master device and an output from a slave device. The MISO line of a slave device is placed in the high-impedance state if the slave device is not selected. **Port E GPIO**—This pin is a General Purpose I/O (GPIO) pin that can be individually programmed as input or output pin. After reset, the default state is MISO.
1	**MOSI** **GPIOB5**	Input/Output Input/Output	Input Input	**SPI Master Out/Slave In (MOSI)**—This serial data pin is an output from a master device and an input to a slave device. The master device places data on the MOSI line a half-cycle before the clock edge that the slave device uses to latch the data. **Port E GPIO**—This pin is a General Purpose I/O (GPIO) pin that can be individually programmed as input or output pin. After reset, the default state is MOSI.
1	**SCLK** **GPIOB4**	Input/Output Input/Output	Input Input	**SPI Serial Clock**—In master mode, this pin serves as an output, clocking slaved listeners. In slave mode, this pin serves as the data clock input. **Port E GPIO**—This pin is a General Purpose I/O (GPIO) pin that can be individually programmed as an input or output pin. After reset, the default state is SCLK.
1	**$\overline{SS}$** **GPIOB7**	Input Input/Output	Input Input	**SPI Slave Select**—In master mode, this pin is used to arbitrate multiple masters. In slave mode, this pin is used to select the slave. **Port E GPIO**—This pin is a General Purpose I/O (GPIO) pin that can be individually programmed as an input or output pin. After reset, the default state is $\overline{SS}$.

2.7 Serial Communications Interface (SCI) Signals

Table 2-9 Serial Communications Interface (SCI0) Signals

No. of Pins	Signal Name	Signal Type	State During Reset	Signal Description
1	**TXD0** **GPIOB0**	Output Input/Output	Input Input	**Transmit Data (TXD0)**—SCI0 transmit data output **Port B GPIO**—This pin is a General Purpose I/O (GPIO) pin that can be individually programmed as an input or output pin. After reset, the default state is SCI output.
1	**RXD0** **GPIOB1**	Input Input/Output	Input Input	**Receive Data (RXD0)**—SCI0 receive data input **Port B GPIO**—This pin is a General Purpose I/O (GPIO) pin that can be individually programmed as an input or output pin. After reset, the default state is SCI input.

2.8 Analog-to-Digital Converter (ADC) Signals

Table 2-10 Analog to Digital Converter Signals

No. of Pins	Signal Name	Signal Type	State During Reset	Signal Description
4	**ANA0-3**	Input	Input	**ANA0-3**—Analog inputs to ADC, channel 1
4	**ANA4-7**	Input	Input	**ANA4-7**—Analog inputs to ADC, channel 2
1	**VREF**	Input	Input	**VREF**—Analog reference voltage for ADC. Must be set to V_{DDA}-0.3V for optimal performance.

2.9 Quad Timer Module Signals

Table 2-11 Quad Timer Module Signals

No. of Pins	Signal Name	Signal Type	State During Reset	Signal Description
3	**TD0-2** **GPIOA0-2**	Input/Output Input/Output	Input Input	**TD0-2**—Timer D Channel 0-2 **Port A GPIO**—This pin is a General Purpose I/O (GPIO) pin that can be individually programmed as an input or output pin. After reset, the default state is the quad timer input.

The 56F801 DC and AC electrical specifications are preliminary and are from design simulations. These specifications may not be fully tested or guaranteed at this early stage of the product life cycle. Finalized specifications will be published after complete characterization and device qualifications have been completed.

CAUTION

This device contains protective circuitry to guard against damage due to high static voltage or electrical fields. However, normal precautions are advised to avoid application of any voltages higher than maximum rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate voltage level.

Table 3-1 Absolute Maximum Ratings

Characteristic	Symbol	Min	Max	Unit
Supply voltage	V_{DD}	V_{SS} – 0.3	V_{SS} + 4.0	V
All other input voltages, excluding Analog inputs	V_{IN}	V_{SS} – 0.3	V_{SS} + 5.5V	V
Voltage difference V_{DD} to V_{DDA}	ΔV_{DD}	- 0.3	0.3	V
Voltage difference V_{SS} to V_{SSA}	ΔV_{SS}	- 0.3	0.3	V
Analog inputs ANA0-7 and VREF	V_{IN}	V_{SSA}– 0.3	V_{DDA}+ 0.3	V
Analog inputs EXTAL, XTAL	V_{IN}	V_{SSA}– 0.3	V_{SSA}+ 3.0	V
Current drain per pin excluding V_{DD}, V_{SS}, & PWM ouputs	I	—	10	mA

Table 3-2 Recommended Operating Conditions

Characteristic	Symbol	Min	Typ	Max	Unit
Supply voltage, digital	V_{DD}	3.0	3.3	3.6	V
Supply Voltage, analog	V_{DDA}	3.0	3.3	3.6	V
Voltage difference V_{DD} to V_{DDA}	ΔV_{DD}	-0.1	-	0.1	V
Voltage difference V_{SS} to V_{SSA}	ΔV_{SS}	-0.1	-	0.1	V
ADC reference voltage[1]	VREF	2.7	–	3.3V	V
Ambient operating temperature	T_A	–40	–	85	°C

1. VREF must be 0.3 below V_{DDA}.

Table 3-3 Thermal Characteristics[6]

Characteristic	Comments	Symbol	Value	Unit	Notes
			48-pin LQFP		
Junction to ambient Natural convection		$R_{\theta JA}$	50.6	°C/W	2
Junction to ambient (@1m/sec)		$R_{\theta JMA}$	47.4	°C/W	2
Junction to ambient Natural convection	Four layer board (2s2p)	$R_{\theta JMA}$ (2s2p)	39.1	°C/W	1,2
Junction to ambient (@1m/sec)	Four layer board (2s2p)	$R_{\theta JMA}$	37.9	°C/W	1,2
Junction to case		$R_{\theta JC}$	17.3	°C/W	3
Junction to center of case		Ψ_{JT}	1.2	°C/W	4, 5
I/O pin power dissipation		$P_{I/O}$	User Determined	W	
Power dissipation		P_D	$P_D = (I_{DD} \times V_{DD} + P_{I/O})$	W	
Junction to center of case		P_{DMAX}	(TJ - TA) /RθJA	W	7

Notes:

1. Theta-JA determined on 2s2p test boards is frequently lower than would be observed in an application. Determined on 2s2p thermal test board.
2. Junction to ambient thermal resistance, Theta-JA ($R_{\theta JA}$) was simulated to be equivalent to the JEDEC specification JESD51-2 in a horizontal configuration in natural convection. Theta-JA was also simulated on a thermal test board with two internal planes (2s2p where s is the number of signal layers and p is the number of planes) per JESD51-6 and JESD51-7. The correct name for Theta-JA for forced convection or with the non-single layer boards is Theta-JMA.
3. Junction to case thermal resistance, Theta-JC ($R_{\theta JC}$), was simulated to be equivalent to the measured values using the cold plate technique with the cold plate temperature used as the "case" temperature. The basic cold plate measurement technique is described by MIL-STD 883D, Method 1012.1. This is the correct thermal metric to use to calculate thermal performance when the package is being used with a heat sink.
4. Thermal Characterization Parameter, Psi-JT (Ψ_{JT}), is the "resistance" from junction to reference point thermocouple on top center of case as defined in JESD51-2. Ψ_{JT} is a useful value to use to estimate junction temperature in steady state customer environments.
5. Junction temperature is a function of on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
6. See Section 5.1 from more details on thermal design considerations.
7. TJ = Junction Temperature
   TA = Ambient Temperature

3.2 DC Electrical Characteristics

Table 3-4 DC Electrical Characteristics

Operating Conditions: $V_{SS} = V_{SSA} = 0$ V, $V_{DD} = V_{DDA} = 3.0–3.6$V, $T_A = –40°$ to $+85°C$, $C_L \leq 50$pF

Characteristic	Symbol	Min	Typ	Max	Unit
Input high voltage (XTAL/EXTAL)	V_{IHC}	2.25	—	2.75	V
Input low voltage (XTAL/EXTAL)	V_{ILC}	0	—	0.5	V
Input high voltage [GPIOB(2:3)][1]	$V_{IH[GPIOB(2:3)]}$	2.0	—	3.6	V
Input low voltage [GPIOB(2:3)][1]	$V_{IL[GPIOB(2:3)]}$	-0.3	—	0.8	V
Input high voltage (Schmitt trigger inputs)[2]	V_{IHS}	2.2	—	5.5	V
Input low voltage (Schmitt trigger inputs)[2]	V_{ILS}	-0.3	—	0.8	V
Input high voltage (all other digital inputs)	V_{IH}	2.0	—	5.5	V
Input low voltage (all other digital inputs)	V_{IL}	-0.3	—	0.8	V
Input current high (pullup/pulldown resistors disabled, $V_{IN}=V_{DD}$)	I_{IH}	-1	—	1	µA
Input current low (pullup/pulldown resistors disabled, $V_{IN}=V_{SS}$)	I_{IL}	-1	—	1	µA
Input current high (with pullup resistor, $V_{IN}=V_{DD}$)	I_{IHPU}	-1	—	1	µA
Input current low (with pullup resistor, $V_{IN}=V_{SS}$)	I_{ILPU}	-210	—	-50	µA
Input current high (with pulldown resistor, $V_{IN}=V_{DD}$)	I_{IHPD}	20	—	180	µA
Input current low (with pulldown resistor, $V_{IN}=V_{SS}$)	I_{ILPD}	-1	—	1	µA
Nominal pullup or pulldown resistor value	R_{PU}, R_{PD}		30		KΩ
Output tri-state current low	I_{OZL}	-10	—	10	µA
Output tri-state current high	I_{OZH}	-10	—	10	µA
Input current high (analog inputs, $V_{IN}=V_{DDA}$)[3]	I_{IHA}	-15	—	15	µA
Input current low (analog inputs, $V_{IN}=V_{SSA}$)[3]	I_{ILA}	-15	—	15	µA
Output High Voltage (at I_{OH})	V_{OH}	$V_{DD} – 0.7$	—	—	V
Output Low Voltage (at I_{OL})	V_{OL}	—	—	0.4	V
Output source current	I_{OH}	4	—	—	mA
Output sink current	I_{OL}	4	—	—	mA
PWM pin output source current[4]	I_{OHP}	10	—	—	mA
PWM pin output sink current[5]	I_{OLP}	16	—	—	mA
Input capacitance	C_{IN}	—	8	—	pF
Output capacitance	C_{OUT}	—	12	—	pF

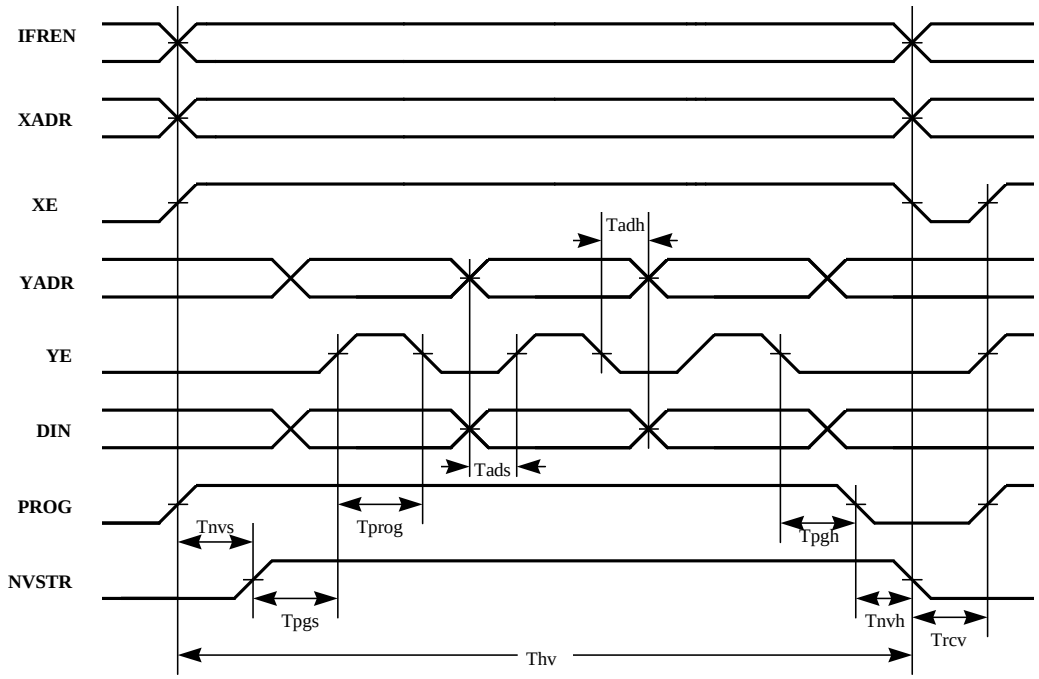


Figure 3-4 Flash Program Cycle

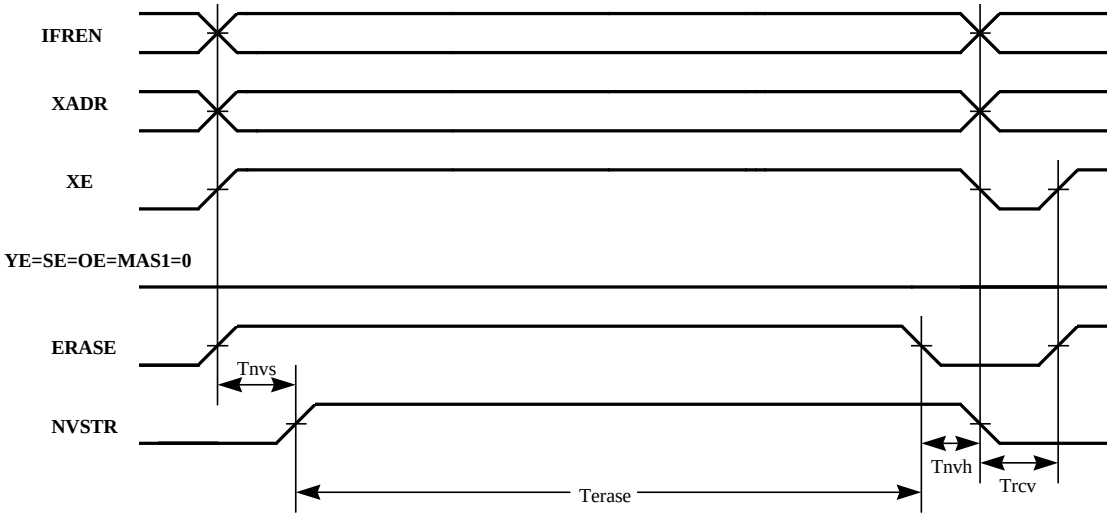


Figure 3-5 Flash Erase Cycle

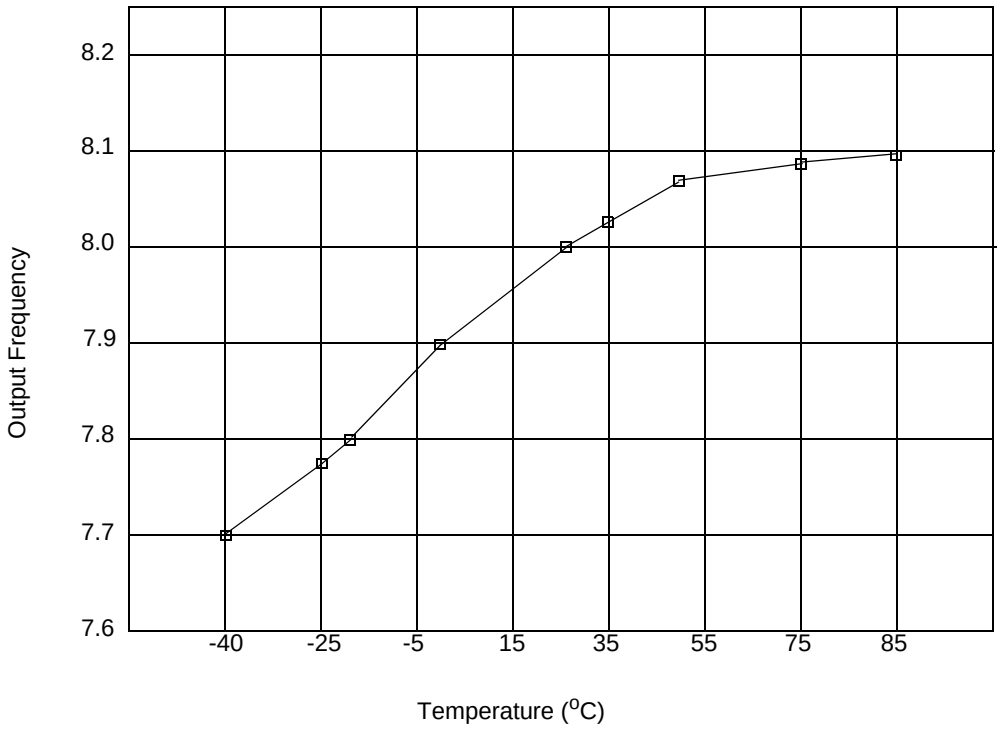


Figure 3-11 Typical Relaxation Oscillator Frequency vs. Temperature (Trimmed to 8MHz @ 25°C)

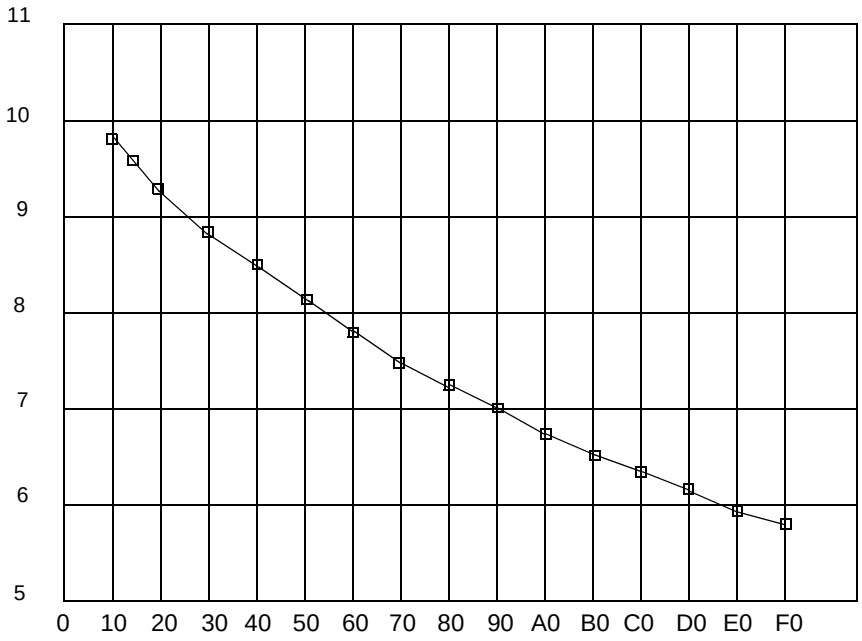


Figure 3-12 Typical Relaxation Oscillator Frequency vs. Trim Value @ 25°C

3.5.5 Phase Locked Loop Timing

Table 3-10 PLL Timing

Operating Conditions: $V_{SS} = V_{SSA} = 0$ V, $V_{DD} = V_{DDA} = 3.0–3.6$ V, $T_A = –40°$ to $+85°C$

Characteristic	Symbol	Min	Typ	Max	Unit
External reference crystal frequency for the PLL[1]	f_{osc}	4	8	10	MHz
PLL output frequency[2]	$f_{out}/2$	40	—	80[3]	MHz
PLL stabilization time[4] 0^o to $+85^oC$	t_{plls}	—	10	—	ms
PLL stabilization time[4] -40^o to 0^oC	t_{plls}	—	100	200	ms

1. An externally supplied reference clock should be as free as possible from any phase jitter for the PLL to work correctly. The PLL is optimized for 8MHz input crystal.
2. ZCLK may not exceed 80MHz. For additional information on ZCLK and $f_{out}/2$, please refer to the OCCS chapter in the User Manual. ZCLK = f_{op}
3. Will not exceed 60MHz for the DSP56F801FA60 device.
4. This is the minimum time required after the PLL setup is changed to ensure reliable operation.

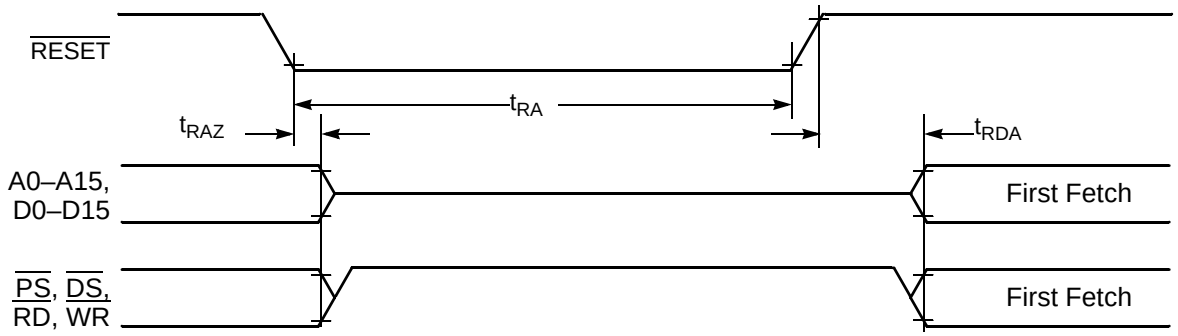


Figure 3-13 Asynchronous Reset Timing

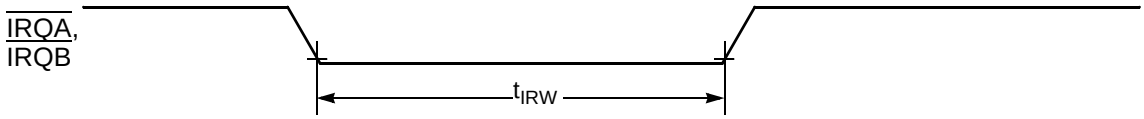
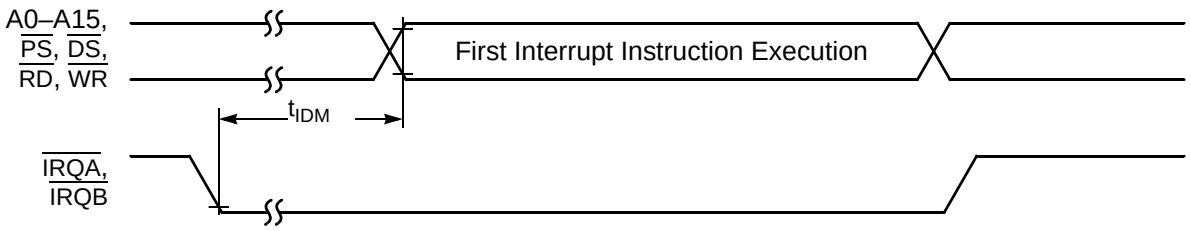
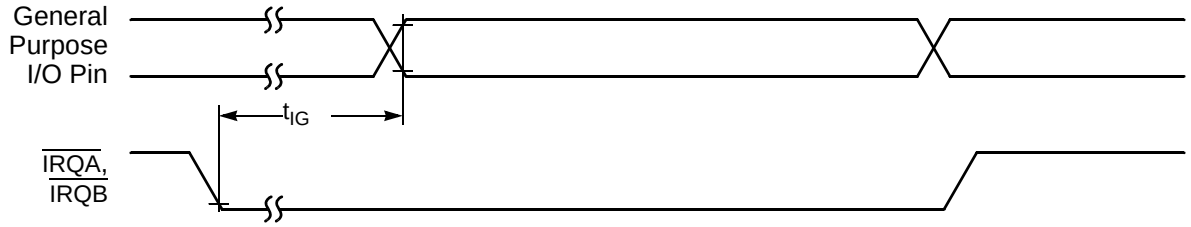


Figure 3-14 External Interrupt Timing (Negative-Edge-Sensitive)



a) First Interrupt Instruction Execution



b) General Purpose I/O

Figure 3-15 External Level-Sensitive Interrupt Timing

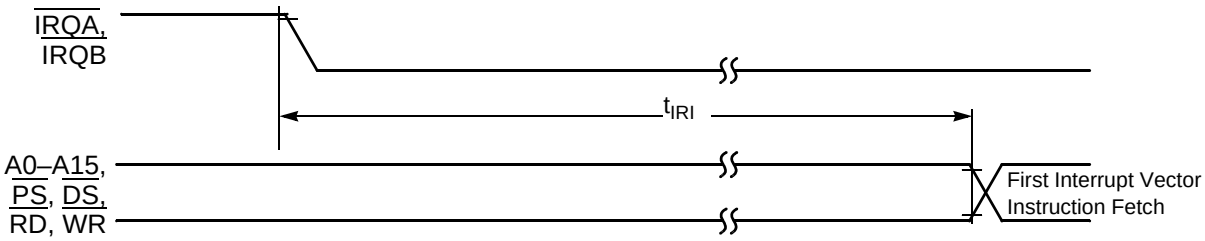


Figure 3-16 Interrupt from Wait State Timing

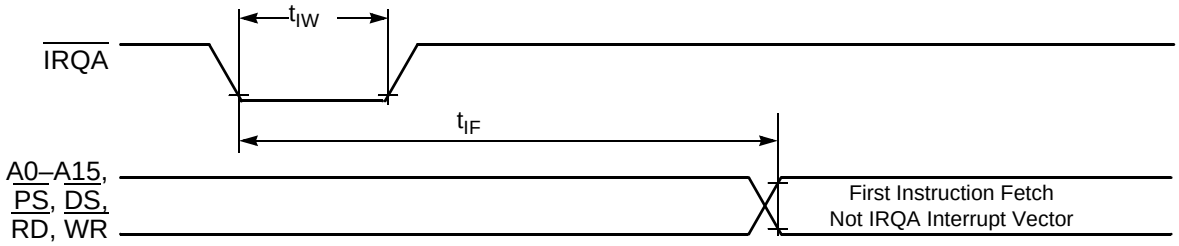


Figure 3-17 Recovery from Stop State Using Asynchronous Interrupt Timing

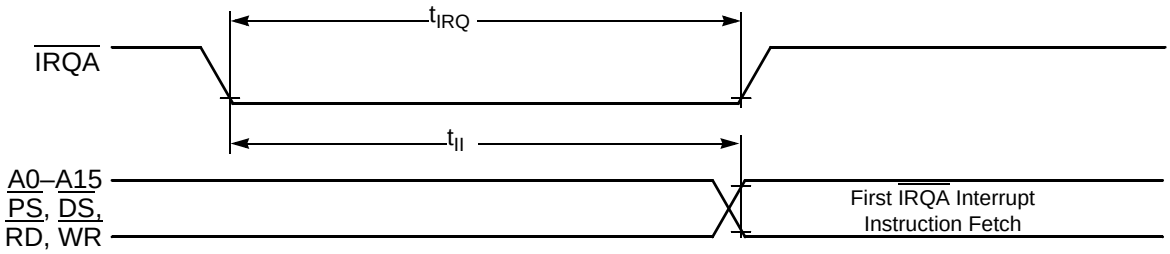


Figure 3-18 Recovery from Stop State Using $\overline{\text{IRQA}}$ Interrupt Service

3.7 Serial Peripheral Interface (SPI) Timing

Table 3-12 SPI Timing[1]

Operating Conditions: $V_{SS} = V_{SSA} = 0$ V, $V_{DD} = V_{DDA} = 3.0–3.6$ V, $T_A = –40°$ to $+85°C$, $C_L \leq 50pF$

Characteristic	Symbol	Min	Max	Unit	See Figure
Cycle time Master Slave	t_C	 50 25	 — —	 ns ns	Figures 3-19, 3-20, 3-21, 3-22
Enable lead time Master Slave	t_{ELD}	 — 25	 — —	 ns ns	Figure 3-22
Enable lag time Master Slave	t_{ELG}	 — 100	 — —	 ns ns	Figure 3-22
Clock (SCK) high time Master Slave	t_{CH}	 17.6 12.5	 — —	 ns ns	Figures 3-19, 3-20, 3-21, 3-22
Clock (SCK) low time Master Slave	t_{CL}	 24.1 25	 — —	 ns ns	Figures 3-19, 3-20, 3-21, 3-22
Data setup time required for inputs Master Slave	t_{DS}	 20 0	 — —	 ns ns	Figures 3-19, 3-20, 3-21, 3-22
Data hold time required for inputs Master Slave	t_{DH}	 0 2	 — —	 ns ns	Figures 3-19, 3-20, 3-21, 3-22
Access time (time to data active from high-impedance state) Slave	t_A	4.8	15	ns	Figure 3-22
Disable time (hold time to high-impedance state) Slave	t_D	3.7	15.2	ns	Figure 3-22
Data Valid for outputs Master Slave (after enable edge)	t_{DV}	 — —	 4.5 20.4	 ns ns	Figures 3-19, 3-20, 3-21, 3-22
Data invalid Master Slave	t_{DI}	 0 0	 — —	 ns ns	Figures 3-19, 3-20, 3-21, 3-22
Rise time Master Slave	t_R	 — —	 11.5 10.0	 ns ns	Figures 3-19, 3-20, 3-21, 3-22
Fall time Master Slave	t_F	 — —	 9.7 9.0	 ns ns	Figures 3-19, 3-20, 3-21, 3-22

1. Parameters listed are guaranteed by design.

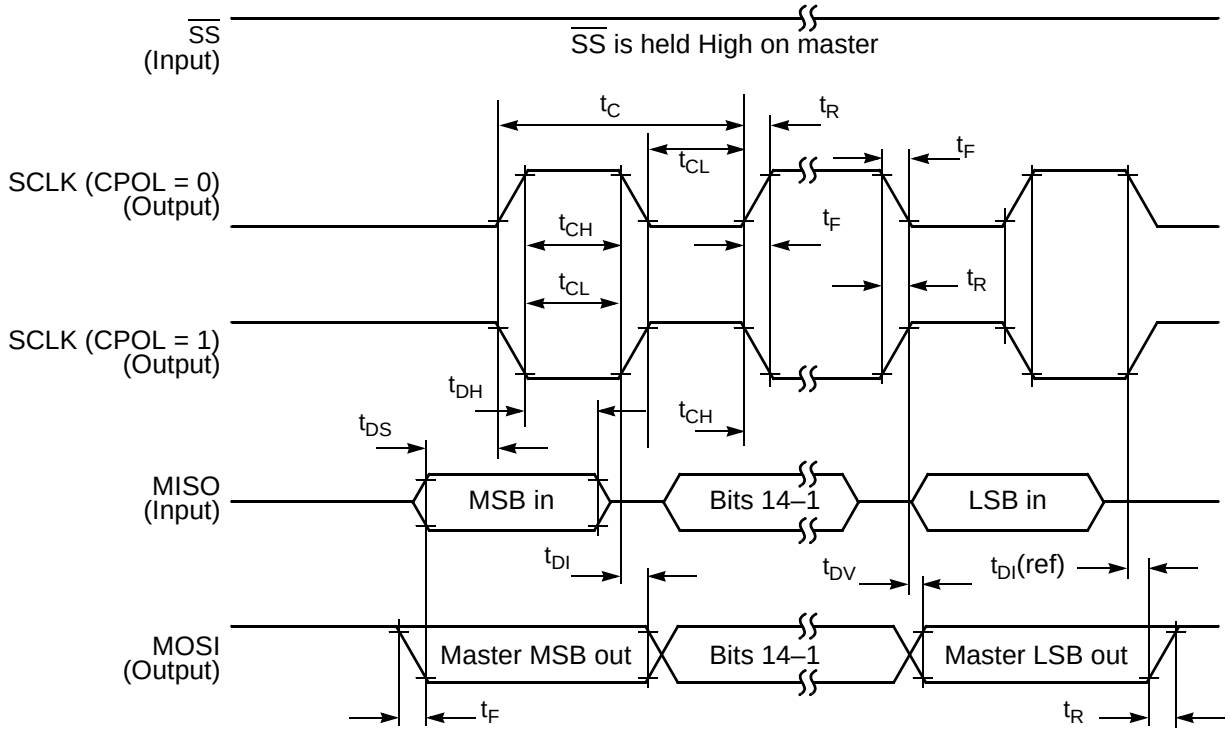


Figure 3-19 SPI Master Timing (CPHA = 0)

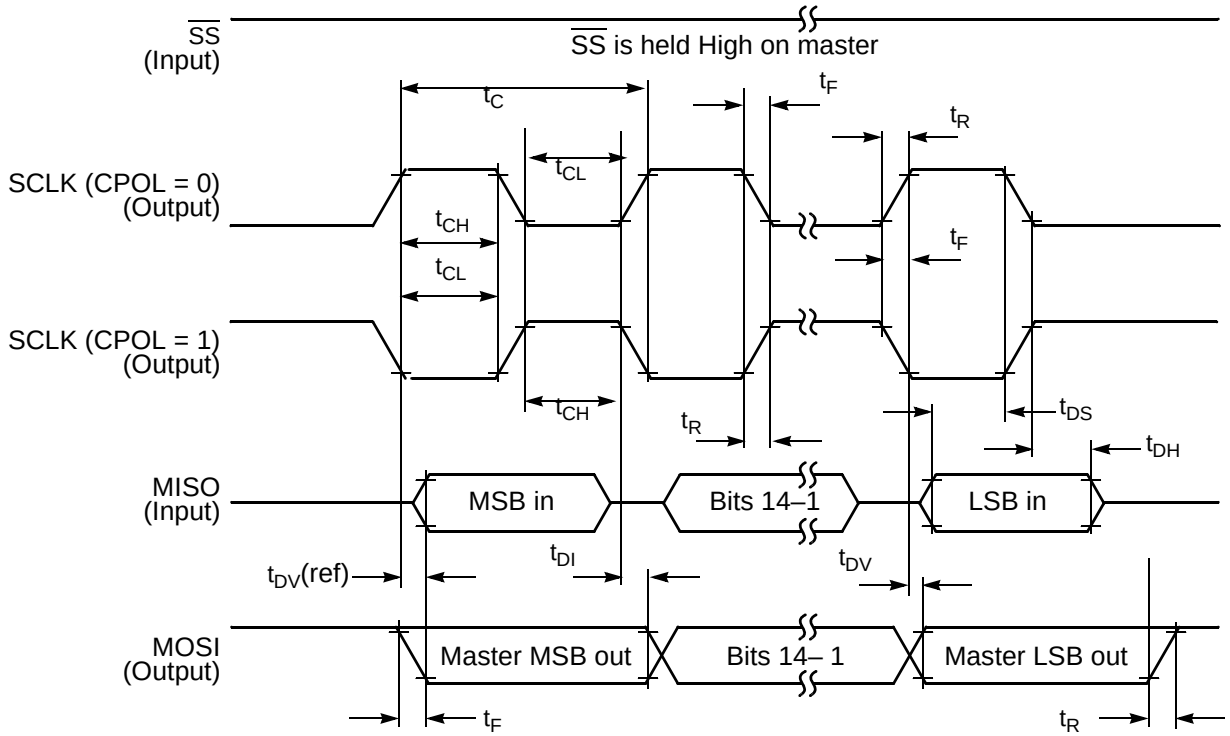


Figure 3-20 SPI Master Timing (CPHA = 1)

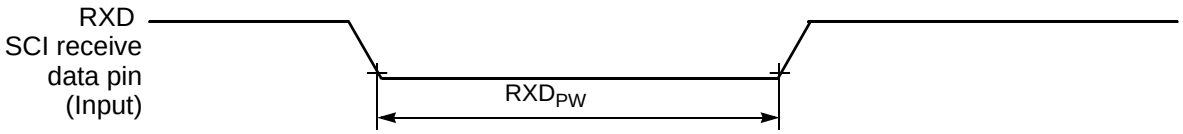


Figure 3-24 RXD Pulse Width

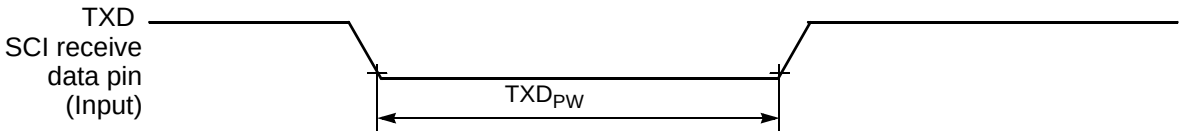


Figure 3-25 TXD Pulse Width

3.10 Analog-to-Digital Converter (ADC) Characteristics

Table 3-15 ADC Characteristics

Characteristic	Symbol	Min	Typ	Max	Unit
ADC input voltages	V_{ADCIN}	0[1]	—	V_{REF}[2]	V
Resolution	R_{ES}	12	—	12	Bits
Integral Non-Linearity[3]	INL	—	+/- 4	+/- 5	LSB[4]
Differential Non-Linearity	DNL	—	+/- 0.9	+/- 1	LSB[4]
Monotonicity	GUARANTEED				
ADC internal clock[5]	f_{ADIC}	0.5	—	5	MHz
Conversion range	R_{AD}	V_{SSA}	—	V_{DDA}	V
Conversion time	t_{ADC}	—	6	—	t_{AIC} cycles[6]
Sample time	t_{ADS}	—	1	—	t_{AIC} cycles[6]
Input capacitance	C_{ADI}	—	5	—	pF[6]
Gain Error (transfer gain)[5]	E_{GAIN}	1.00	1.10	1.15	—
Offset Voltage[5]	V_{OFFSET}	+10	+230	+325	mV

- Bypass the V_{DD} and V_{SS} layers of the PCB with approximately 100 µF, preferably with a high-grade capacitor such as a tantalum capacitor.
- Because the controller's output signals have fast rise and fall times, PCB trace lengths should be minimal.
- Consider all device loads as well as parasitic capacitance due to PCB traces when calculating capacitance. This is especially critical in systems with higher capacitive loads that could create higher transient currents in the V_{DD} and GND circuits.
- Take special care to minimize noise levels on the VREF, V_{DDA} and V_{SSA} pins.
- Designs that utilize the $\overline{\text{TRST}}$ pin for JTAG port or OnCE module functionality (such as development or debugging systems) should allow a means to assert $\overline{\text{TRST}}$ whenever $\overline{\text{RESET}}$ is asserted, as well as a means to assert $\overline{\text{TRST}}$ independently of $\overline{\text{RESET}}$. $\overline{\text{TRST}}$ must be asserted at power up for proper operation. Designs that do not require debugging functionality, such as consumer products, $\overline{\text{TRST}}$ should be tied low.
- Because the Flash memory is programmed through the JTAG/OnCE port, designers should provide an interface to this port to allow in-circuit Flash programming.

Part 6 Ordering Information

Table 6-1 lists the pertinent information needed to place an order. Consult a Freescale Semiconductor sales office or authorized distributor to determine availability and to order parts.

Table 6-1 56F801 Ordering Information

Part	Supply Voltage	Package Type	Pin Count	Ambient Frequency (MHz)	Order Number
56F801	3.0–3.6 V	Low Profile Plastic Quad Flat Pack (LQFP)	48	80	DSP56F801FA80
56F801	3.0–3.6 V	Low Profile Plastic Quad Flat Pack (LQFP)	48	60	DSP56F801FA60
56F801	3.0–3.6 V	Low Profile Plastic Quad Flat Pack (LQFP)	48	80	DSP56F801FA80E*
56F801	3.0–3.6 V	Low Profile Plastic Quad Flat Pack (LQFP)	48	60	DSP56F801FA60E*

*This package is RoHS compliant.