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Applications of "Embedded - Microcontrollers"

Details

Product Status	Active
Core Processor	HCS12X
Core Size	16-Bit
Speed	50MHz
Connectivity	CANbus, EBI/EMI, I²C, IrDA, SCI, SPI
Peripherals	LVD, POR, PWM, WDT
Number of I/O	59
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	12K x 8
Voltage - Supply (Vcc/Vdd)	1.72V ~ 5.5V
Data Converters	A/D 12x12b
Oscillator Type	External
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	80-QFP
Supplier Device Package	80-QFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc9s12xeg128maa

- — Flexible identifier filter programmable as 2 x 32 bit, 4 x 16 bit, or 8 x 8 bit
- — Four separate interrupt channels for Rx, Tx, error, and wake-up
- — Low-pass filter wake-up function
- — Loop-back for self-test operation
- ECT (enhanced capture timer)
  - — 8 x 16-bit channels for input capture or output compare
  - — 16-bit free-running counter with 8-bit precision prescaler
  - — 16-bit modulus down counter with 8-bit precision prescaler
  - — Four 8-bit or two 16-bit pulse accumulators
- TIM (standard timer module)
  - — 8 x 16-bit channels for input capture or output compare
  - — 16-bit free-running counter with 8-bit precision prescaler
  - — 1 x 16-bit pulse accumulator
- PIT (periodic interrupt timer)
  - — Up to eight timers with independent time-out periods
  - — Time-out periods selectable between 1 and 2^{24} bus clock cycles
  - — Time-out interrupt and peripheral triggers
- 8 PWM (pulse-width modulator) channels
  - — 8 channel x 8-bit or 4 channel x 16-bit Pulse Width Modulator
  - — programmable period and duty cycle per channel
  - — Center- or left-aligned outputs
  - — Programmable clock select logic with a wide range of frequencies
  - — Fast emergency shutdown input
- Three Serial Peripheral Interface Modules (SPI)
  - — Configurable for 8 or 16-bit data size
- Eight Serial Communication Interfaces (SCI)
  - — Standard mark/space non-return-to-zero (NRZ) format
  - — Selectable IrDA 1.4 return-to-zero-inverted (RZI) format with programmable pulse widths
- Two Inter-IC bus (IIC) Modules
  - — Multi-master operation
  - — Software programmable for one of 256 different serial clock frequencies
  - — Broadcast mode support
  - — 10-bit address support
- On-Chip Voltage Regulator
  - — Two parallel, linear voltage regulators with bandgap reference
  - — Low-voltage detect (LVD) with low-voltage interrupt (LVI)
  - — Power-on reset (POR) circuit
  - — 3.3V and 5V range operation
  - — Low-voltage reset (LVR)

Table 1-14. Interrupt Vector Locations (Sheet 4 of 4)

Vector Address[1]	XGATE Channel ID[2]	Interrupt Source	CCR Mask	Local Enable	STOP Wake up	WAIT Wake up
Vector base+ $4E	$27	TIM timer channel 3	I bit	TIE (C3I)	No	Yes
Vector base + $4C	$26	TIM timer channel 4	I bit	TIE (C4I)	No	Yes
Vector base+ $4A	$25	TIM timer channel 5	I bit	TIE (C5I)	No	Yes
Vector base+ $48	$24	TIM timer channel 6	I bit	TIE (C6I)	No	Yes
Vector base+ $46	$23	TIM timer channel 7	I bit	TIE (C7I)	No	Yes
Vector base+ $44	$22	TIM timer overflow	I bit	TSRC2 (TOF)	No	Yes
Vector base + $42	$21	TIM Pulse accumulator A overflow	I bit	PACTL (PAOVI)	No	Yes
Vector base+ $40	$20	TIM Pulse accumulator input edge	I bit	PACTL (PAI)	No	Yes
Vector base + $3E	$1F	ATD0 Compare Interrupt	I bit	ATD0CTL2 (ACMPIE)	Yes	Yes
Vector base + $3C	$1E	ATD1 Compare Interrupt	I bit	ATD1CTL2 (ACMPIE)	Yes	Yes
Vector base+ $18 to Vector base + $3A		Reserved				
Vector base + $16	—	XGATE software error interrupt	None	None	No	Yes
Vector base + $14	—	MPU Access Error	None	None	No	No
Vector base + $12	—	System Call Interrupt (SYS)	—	None	—	—
Vector base + $10	—	Spurious interrupt	—	None	—	—

1. 16 bits vector address based
2. For detailed description of XGATE channel ID refer to XGATE Block Guide

1.6.3   Effects of Reset

When a reset occurs, MCU registers and control bits are initialized. Refer to the respective block descriptions for register reset states.

On each reset, the Flash module executes a reset sequence to load Flash configuration registers and initialize the buffer RAM EEE partition, if required.

1.6.3.1   Flash Configuration Reset Sequence (Core Hold Phase)

On each reset, the Flash module will hold CPU activity while loading Flash module registers and configuration from the Flash memory. The duration of this phase is given as t_{RST} in the device electrical parameter specification. If double faults are detected in the reset phase, Flash module protection and security may be active on leaving reset. This is explained in more detail in the Flash module section.

1.6.3.2   EEE Reset Sequence Phase (Core Active Phase)

During this phase of the reset sequence (following on from the core hold phase) the CPU can execute instructions while the FTM initialization completes and, if configured for EEE operation, the EEE RAM

NOTE

Care must be taken to ensure that all exception requests remain active until the system begins execution of the applicable service routine; otherwise, the exception request may not get processed at all or the result may be a spurious interrupt request (vector at address (vector base + 0x0010)).

6.4.5 Reset Exception Requests

The XINT module supports three system reset exception request types (for details please refer to the Clock and Reset Generator module (CRG)):

1. Pin reset, power-on reset, low-voltage reset, or illegal address reset
2. Clock monitor reset request
3. COP watchdog reset request

6.4.6 Exception Priority

The priority (from highest to lowest) and address of all exception vectors issued by the XINT module upon request by the CPU is shown in Table 6-10. Generally, all non-maskable interrupts have higher priorities than maskable interrupts. Please note that between the three software interrupts (Unimplemented op-code trap request, SWI/BGND request, SYS request) there is no real priority defined because they cannot occur simultaneously (the S12XCPU executes one instruction at a time).

Table 6-10. Exception Vector Map and Priority

Vector Address[1]	Source
0xFFFE	Pin reset, power-on reset, low-voltage reset, illegal address reset
0xFFFC	Clock monitor reset
0xFFFA	COP watchdog reset
(Vector base + 0x00F8)	Unimplemented op-code trap
(Vector base + 0x00F6)	Software interrupt instruction (SWI) or BDM vector request
(Vector base + 0x0012)	System call interrupt instruction (SYS)
(Vector base + 0x0018)	(reserved for future use)
(Vector base + 0x0016)	XGATE Access violation interrupt request[2]
(Vector base + 0x0014)	CPU Access violation interrupt request[3]
(Vector base + 0x00F4)	$\overline{XIRQ}$ interrupt request
(Vector base + 0x00F2)	$\overline{IRQ}$ interrupt request
(Vector base + 0x00F0–0x001A)	Device specific I bit maskable interrupt sources (priority determined by the associated configuration registers, in descending order)
(Vector base + 0x0010)	Spurious interrupt

1. 16 bits vector address based

2. only implemented if device features both a Memory Protection Unit (MPU) and an XGATE co-processor

3. only implemented if device features a Memory Protection Unit (MPU)

Write: If DBG not armed. See Table 8-29 for visible register encoding.

The DBGC1_COMRV bits determine which comparator control, address, data and datamask registers are visible in the 8-byte window from 0x0028 to 0x002F as shown in Section Table 8-29.

Table 8-29. Comparator Address Register Visibility

COMRV	Visible Comparator
00	DBGACTL, DBGAAH ,DBGAAM, DBGAAL, DBGADH, DBGADL, DBGADHM, DBGADLM
01	DBGBCTL, DBGBAH, DBGBAM, DBGBAL
10	DBGCCTL, DBGCAH, DBGCAM, DBGCAL, DBGCDH, DBGCDL, DBGCDHM, DBGCDLM
11	DBGDCTL, DBGDAH, DBGDAM, DBGDAL

Table 8-30. DBGXCTL Field Descriptions

Field	Description
7 SZE (Comparators B and D)	**Size Comparator Enable Bit** — The SZE bit controls whether access size comparison is enabled for the associated comparator. This bit is ignored if the TAG bit in the same register is set. 0 Word/Byte access size is not used in comparison 1 Word/Byte access size is used in comparison
6 NDB (Comparators A and C	**Not Data Bus** — The NDB bit controls whether the match occurs when the data bus matches the comparator register value or when the data bus differs from the register value. Furthermore data bus bits can be individually masked using the comparator data mask registers. This bit is only available for comparators A and C. This bit is ignored if the TAG bit in the same register is set. This bit position has an SZ functionality for comparators B and D. 0 Match on data bus equivalence to comparator register contents 1 Match on data bus difference to comparator register contents
6 SZ (Comparators B and D)	**Size Comparator Value Bit** — The SZ bit selects either word or byte access size in comparison for the associated comparator. This bit is ignored if the SZE bit is cleared or if the TAG bit in the same register is set. This bit position has NDB functionality for comparators A and C 0 Word access size will be compared 1 Byte access size will be compared
5 TAG	**Tag Select** — This bit controls whether the comparator match will cause a trigger or tag the opcode at the matched address. Tagged opcodes trigger only if they reach the execution stage of the instruction queue. 0 Trigger immediately on match 1 On match, tag the opcode. If the opcode is about to be executed a trigger is generated
4 BRK	**Break** — This bit controls whether a channel match terminates a debug session immediately, independent of state sequencer state. To generate an immediate breakpoint the module breakpoints must be enabled using DBGBRK. 0 The debug session termination is dependent upon the state sequencer and trigger conditions. 1 A match on this channel terminates the debug session immediately; breakpoints if active are generated, tracing, if active, is terminated and the module disarmed.
3 RW	**Read/Write Comparator Value Bit** — The RW bit controls whether read or write is used in compare for the associated comparator . The RW bit is not used if RWE = 0. 0 Write cycle will be matched 1 Read cycle will be matched
2 RWE	**Read/Write Enable Bit** — The RWE bit controls whether read or write comparison is enabled for the associated comparator. This bit is not used for tagged operations. 0 Read/Write is not used in comparison 1 Read/Write is used in comparison

9.1.2   Modes of Operation

Table 9-2 gives an overview over availability of security relevant features in unsecure and secure modes.

Table 9-2. Feature Availability in Unsecure and Secure Modes on S12XE

	Unsecure Mode						Secure Mode					
	NS	SS	NX	ES	EX	ST	NS	SS	NX	ES	EX	ST
Flash Array Access	✔	✔	✔[1]	✔[1]	✔[1]	✔[1]	✔	✔	—	—	—	—
EEPROM Array Access	✔	✔	✔	✔	✔	✔	✔	✔	—	—	—	—
NVM Commands	✔[2]	✔	✔[2]	✔[2]	✔[2]	✔	✔[2]	✔[2]	✔[2]	✔[2]	✔[2]	✔[2]
BDM	✔	✔	✔	✔	✔	✔	—	✔[3]	—	—	—	—
DBG Module Trace	✔	✔	✔	✔	✔	✔	—	—	—	—	—	—
XGATE Debugging	✔	✔	✔	✔	✔	✔	—	—	—	—	—	—
External Bus Interface	—	—	✔	✔	✔	✔	—	—	✔	✔	✔	✔
Internal status visible multiplexed on external bus	—	—	—	✔	✔	—	—	—	—	✔	✔	—
Internal accesses visible on external bus	—	—	—	—	—	✔	—	—	—	—	—	✔

1. Availability of Flash arrays in the memory map depends on ROMCTL/EROMCTL pins and/or the state of the ROMON/EROMON bits in the MMCCTL1 register. Please refer to the S12X_MMC block guide for detailed information.

2. Restricted NVM command set only. Please refer to the NVM wrapper block guides for detailed information.

3. BDM hardware commands restricted to peripheral registers only.

9.1.3   Securing the Microcontroller

Once the user has programmed the Flash and EEPROM, the chip can be secured by programming the security bits located in the options/security byte in the Flash memory array. These non-volatile bits will keep the device secured through reset and power-down.

The options/security byte is located at address 0xFF0F (= global address 0x7F_FF0F) in the Flash memory array. This byte can be erased and programmed like any other Flash location. Two bits of this byte are used for security (SEC[1:0]). On devices which have a memory page window, the Flash options/security byte is also available at address 0xBF0F by selecting page 0x3F with the PPAGE register. The contents of this byte are copied into the Flash security register (FSEC) during a reset sequence.

	7	6	5	4	3	2	1	0
0xFF0F	KEYEN1	KEYEN0	NV5	NV4	NV3	NV2	SEC1	SEC0

Figure 9-1. Flash Options/Security Byte

The meaning of the bits KEYEN[1:0] is shown in Table 9-3. Please refer to Section 9.1.5.1, "Unsecuring the MCU Using the Backdoor Key Access" for more information.

Table 10-2. XGMCTL Field Descriptions (Sheet 2 of 3)

Field	Description
11 XGFACTM	**XGFACT Mask** — This bit controls the write access to the XGFACT bit. The XGFACT bit can only be set or cleared if a "1" is written to the XGFACTM bit in the same register access. Read: This bit will always read "0". Write: 0 Disable write access to the XGFACT in the same bus cycle 1 Enable write access to the XGFACT in the same bus cycle
9 XGSWEFM	**XGSWEF Mask** — This bit controls the write access to the XGSWEF bit. The XGSWEF bit can only be cleared if a "1" is written to the XGSWEFM bit in the same register access. Read: This bit will always read "0". Write: 0 Disable write access to the XGSWEF in the same bus cycle 1 Enable write access to the XGSWEF in the same bus cycle
8 XGIEM	**XGIE Mask** — This bit controls the write access to the XGIE bit. The XGIE bit can only be set or cleared if a "1" is written to the XGIEM bit in the same register access. Read: This bit will always read "0". Write: 0 Disable write access to the XGIE in the same bus cycle 1 Enable write access to the XGIE in the same bus cycle
7 XGE	**XGATE Module Enable (Request Enable)**— This bit enables incoming XGATE requests from the S12X_INT module. If the XGE bit is cleared, pending XGATE requests will be ignored. The thread that is executed by the RISC core while the XGE bit is cleared will continue to run. Read: 0 Incoming requests are disabled 1 Incoming requests are enabled Write: 0 Disable incoming requests 1 Enable incoming requests
6 XGFRZ	**Halt XGATE in Freeze Mode** — The XGFRZ bit controls the XGATE operation in Freeze Mode (BDM active). Read: 0 RISC core operates normally in Freeze (BDM active) 1 RISC core stops in Freeze Mode (BDM active) Write: 0 Don't stop RISC core in Freeze Mode (BDM active) 1 Stop RISC core in Freeze Mode (BDM active)
5 XGDBG	**XGATE Debug Mode** — This bit indicates that the XGATE is in Debug Mode (see Section 10.6, "Debug Mode"). Debug Mode can be entered by Software Breakpoints (BRK instruction), Tagged or Forced Breakpoints (see **S12X_DBG Section**), or by writing a "1" to this bit. Read: 0 RISC core is not in Debug Mode 1 RISC core is in Debug Mode Write: 0 Leave Debug Mode 1 Enter Debug Mode **Note:** Freeze Mode and Software Error Interrupts have no effect on the XGDBG bit.

LDW

Load Word from Memory

LDW

Operation

$M[RB, \#OFFS5] \Rightarrow RD$
$M[RB, RI] \Rightarrow RD$
$M[RB, RI] \Rightarrow RD; \quad RI+2 \quad \Rightarrow RI^{1}$
$RI-2 \quad \Rightarrow RI; \quad M[RS, RI] \Rightarrow RD$
$IMM16 \quad \Rightarrow RD$ (translates to LDL RD, #IMM16[7:0]; LDH RD, #IMM16[15:8])

Loads a 16 bit value into the register RD.

CCR Effects

N	Z	V	C
—	—	—	—

N: Not affected.
Z: Not affected.
V: Not affected.
C: Not affected.

Code and CPU Cycles

Source Form	Address Mode	Machine Code										Cycles
LDW RD, (RB, #OFFS5)	IDO5	0	1	0	0	1	RD	RB	OFFS5			PR
LDW RD, (RB, RI)	IDR	0	1	1	0	1	RD	RB	RI	0	0	PR
LDW RD, (RB, RI+)	IDR+	0	1	1	0	1	RD	RB	RI	0	1	PR
LDW RD, (RB, -RI)	-IDR	0	1	1	0	1	RD	RB	RI	1	0	PR
LDW RD, #IMM16	IMM8	1	1	1	1	0	RD	IMM16[7:0]				P
	IMM8	1	1	1	1	1	RD	IMM16[15:8]				P

1. If the same general purpose register is used as index (RI) and destination register (RD), the content of the register will not be incremented after the data move: $M[RB, RI] \Rightarrow RD$

Table 10-24. Instruction Set Summary (Sheet 2 of 3)

Functionality	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Branches																
BCC REL9	0	0	1	0	0	0	0					REL9				
BCS REL9	0	0	1	0	0	0	1					REL9				
BNE REL9	0	0	1	0	0	1	0					REL9				
BEQ REL9	0	0	1	0	0	1	1					REL9				
BPL REL9	0	0	1	0	1	0	0					REL9				
BMI REL9	0	0	1	0	1	0	1					REL9				
BVC REL9	0	0	1	0	1	1	0					REL9				
BVS REL9	0	0	1	0	1	1	1					REL9				
BHI REL9	0	0	1	1	0	0	0					REL9				
BLS REL9	0	0	1	1	0	0	1					REL9				
BGE REL9	0	0	1	1	0	1	0					REL9				
BLT REL9	0	0	1	1	0	1	1					REL9				
BGT REL9	0	0	1	1	1	0	0					REL9				
BLE REL9	0	0	1	1	1	0	1					REL9				
BRA REL10	0	0	1	1	1	1						REL10				
Load and Store Instructions																
LDB RD, (RB, #OFFS5)	0	1	0	0	0		RD			RB			OFFS5			
LDW RD, (RB, #OFFS5)	0	1	0	0	1		RD			RB			OFFS5			
STB RS, (RB, #OFFS5)	0	1	0	1	0		RS			RB			OFFS5			
STW RS, (RB, #OFFS5)	0	1	0	1	1		RS			RB			OFFS5			
LDB RD, (RB, RI)	0	1	1	0	0		RD			RB			RI		0	0
LDW RD, (RB, RI)	0	1	1	0	1		RD			RB			RI		0	0
STB RS, (RB, RI)	0	1	1	1	0		RS			RB			RI		0	0
STW RS, (RB, RI)	0	1	1	1	1		RS			RB			RI		0	0
LDB RD, (RB, RI+)	0	1	1	0	0		RD			RB			RI		0	1
LDW RD, (RB, RI+)	0	1	1	0	1		RD			RB			RI		0	1
STB RS, (RB, RI+)	0	1	1	1	0		RS			RB			RI		0	1
STW RS, (RB, RI+)	0	1	1	1	1		RS			RB			RI		0	1
LDB RD, (RB, –RI)	0	1	1	0	0		RD			RB			RI		1	0
LDW RD, (RB, –RI)	0	1	1	0	1		RD			RB			RI		1	0
STB RS, (RB, –RI)	0	1	1	1	0		RS			RB			RI		1	0
STW RS, (RB, –RI)	0	1	1	1	1		RS			RB			RI		1	0
Bit Field Instructions																
BFEXT RD, RS1, RS2	0	1	1	0	0		RD			RS1			RS2		1	1
BFINS RD, RS1, RS2	0	1	1	0	1		RD			RS1			RS2		1	1
BFINSI RD, RS1, RS2	0	1	1	1	0		RD			RS1			RS2		1	1
BFINSX RD, RS1, RS2	0	1	1	1	1		RD			RS1			RS2		1	1
Logic Immediate Instructions																
ANDL RD, #IMM8	1	0	0	0	0		RD					IMM8				
ANDH RD, #IMM8	1	0	0	0	1		RD					IMM8				
BITL RD, #IMM8	1	0	0	1	0		RD					IMM8				
BITH RD, #IMM8	1	0	0	1	1		RD					IMM8				
ORL RD, #IMM8	1	0	1	0	0		RD					IMM8				
ORH RD, #IMM8	1	0	1	0	1		RD					IMM8				
XNORL RD, #IMM8	1	0	1	1	0		RD					IMM8				
XNORH RD, #IMM8	1	0	1	1	1		RD					IMM8				

Module Base + 0x0002

	7	6	5	4	3	2	1	0
R	0	0	0			POSTDIV[4:0]		
W								
Reset	0	0	0	0	0	0	0	0

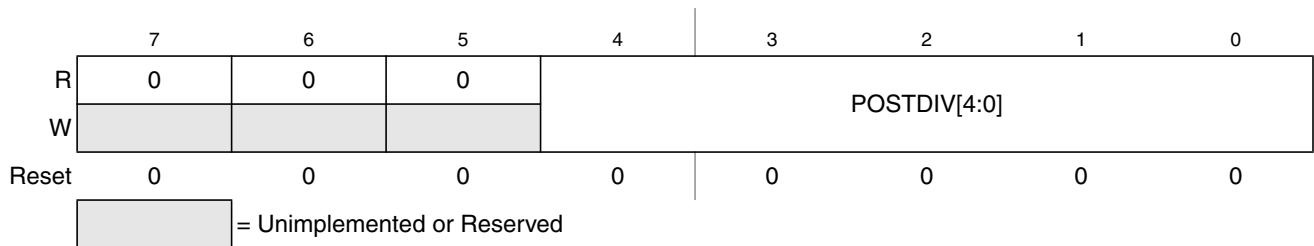|	= Unimplemented or Reserved

Figure 11-5. S12XECRG Post Divider Register (POSTDIV)

Read: Anytime

Write: Anytime except if PLLSEL = 1
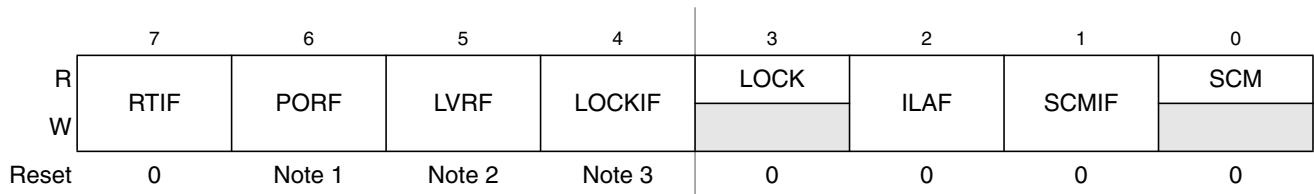
$$f_{PLL} = \frac{f_{VCO}}{(2 \times POSTDIV)}$$

NOTE

If POSTDIV = $00 then f_{PLL} is identical to f_{VCO} (divide by one).

11.3.2.4   S12XECRG Flags Register (CRGFLG)

This register provides S12XECRG status bits and flags.

Module Base + 0x0003

	7	6	5	4	3	2	1	0
R	RTIF	PORF	LVRF	LOCKIF	LOCK	ILAF	SCMIF	SCM
W								
Reset	0	Note 1	Note 2	Note 3	0	0	0	0

1. PORF is set to 1 when a power on reset occurs. Unaffected by system reset.
2. LVRF is set to 1 when a low voltage reset occurs. Unaffected by system reset.
3. ILAF is set to 1 when an illegal address reset occurs. Unaffected by system reset. Cleared by power on or low voltage reset.

	= Unimplemented or Reserved

Figure 11-6. S12XECRG Flags Register (CRGFLG)

Read: Anytime

Write: Refer to each bit for individual write conditions

14.4.3.5 Pulse Accumulator A Overflow Interrupt

This active high output will be asserted by the module to request a timer pulse accumulator A overflow interrupt to be serviced by the system controller.

14.4.3.6 Timer Overflow Interrupt

This active high output will be asserted by the module to request a timer overflow interrupt to be serviced by the system controller.

1. Read: Anytime
 Write: Anytime in initialization mode (INITRQ = 1 and INITAK = 1)

Table 16-25. CANIDMR4–CANIDMR7 Register Field Descriptions

Field	Description
7-0 AM[7:0]	**Acceptance Mask Bits** — If a particular bit in this register is cleared, this indicates that the corresponding bit in the identifier acceptance register must be the same as its identifier bit before a match is detected. The message is accepted if all such bits match. If a bit is set, it indicates that the state of the corresponding bit in the identifier acceptance register does not affect whether or not the message is accepted. 0 Match corresponding acceptance code register and identifier bits 1 Ignore corresponding acceptance code register bit

16.3.3   Programmer's Model of Message Storage

The following section details the organization of the receive and transmit message buffers and the associated control registers.

To simplify the programmer interface, the receive and transmit message buffers have the same outline. Each message buffer allocates 16 bytes in the memory map containing a 13 byte data structure.

An additional transmit buffer priority register (TBPR) is defined for the transmit buffers. Within the last two bytes of this memory map, the MSCAN stores a special 16-bit time stamp, which is sampled from an internal timer after successful transmission or reception of a message. This feature is only available for transmit and receiver buffers, if the TIME bit is set (see Section 16.3.2.1, "MSCAN Control Register 0 (CANCTL0)").

The time stamp register is written by the MSCAN. The CPU can only read these registers.

17.3.0.1 PIT Control and Force Load Micro Timer Register (PITCFLMT)

Module Base + 0x0000

	7	6	5	4	3	2	1	0
R	PITE	PITSWAI	PITFRZ	0	0	0	0	0
W							PFLMT1	PFLMT0
Reset	0	0	0	0	0	0	0	0

☐ = Unimplemented or Reserved

Figure 17-3. PIT Control and Force Load Micro Timer Register (PITCFLMT)

Read: Anytime

Write: Anytime; writes to the reserved bits have no effect

Table 17-2. PITCFLMT Field Descriptions

Field	Description
7 PITE	**PIT Module Enable Bit** — This bit enables the PIT module. If PITE is cleared, the PIT module is disabled and flag bits in the PITTF register are cleared. When PITE is set, individually enabled timers (PCE set) start down-counting with the corresponding load register values. 0 PIT disabled (lower power consumption). 1 PIT is enabled.
6 PITSWAI	**PIT Stop in Wait Mode Bit** — This bit is used for power conservation while in wait mode. 0 PIT operates normally in wait mode 1 PIT clock generation stops and freezes the PIT module when in wait mode
5 PITFRZ	**PIT Counter Freeze while in Freeze Mode Bit** — When during debugging a breakpoint (freeze mode) is encountered it is useful in many cases to freeze the PIT counters to avoid e.g. interrupt generation. The PITFRZ bit controls the PIT operation while in freeze mode. 0 PIT operates normally in freeze mode 1 PIT counters are stalled when in freeze mode
1:0 PFLMT[1:0]	**PIT Force Load Bits for Micro Timer 1:0** — These bits have only an effect if the corresponding micro timer is active and if the PIT module is enabled (PITE set). Writing a one into a PFLMT bit loads the corresponding 8-bit micro timer load register into the 8-bit micro timer down-counter. Writing a zero has no effect. Reading these bits will always return zero. **Note:** A micro timer force load affects all timer channels that use the corresponding micro time base.

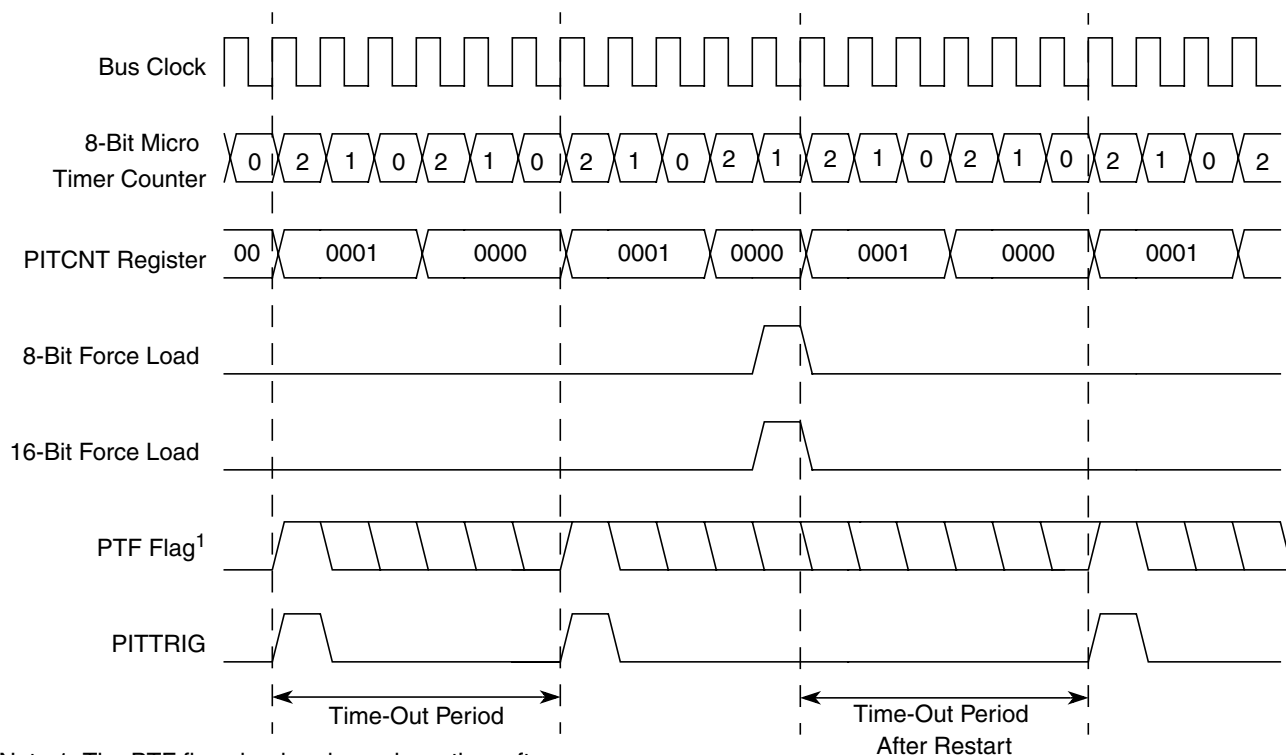### 17.3.0.2 PIT Force Load Timer Register (PITFLT)

Module Base + 0x0001

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	0
W	PFLT7	PFLT6	PFLT5	PFLT4	PFLT3	PFLT2	PFLT1	PFLT0
Reset	0	0	0	0	0	0	0	0

Figure 17-4. PIT Force Load Timer Register (PITFLT)

Read: Anytime

Write: Anytime

Note 1. The PTF flag clearing depends on the software

Figure 17-28. PIT Trigger and Flag Signal Timing

17.4.2 Interrupt Interface

Each time-out event can be used to trigger an interrupt service request. For each timer channel, an individual bit PINTE in the PIT interrupt enable (PITINTE) register exists to enable this feature. If PINTE is set, an interrupt service is requested whenever the corresponding time-out flag PTF in the PIT time-out flag (PITTF) register is set. The flag can be cleared by writing a one to the flag bit.

NOTE

Be careful when resetting the PITE, PINTE or PITCE bits in case of pending PIT interrupt requests, to avoid spurious interrupt requests.

17.4.3 Hardware Trigger

The PIT module contains eight hardware trigger signal lines PITTRIG[7:0], one for each timer channel. These signals can be connected on SoC level to peripheral modules enabling e.g. periodic ATD conversion (please refer to the device overview for the mapping of PITTRIG[7:0] signals to peripheral modules).

Whenever a timer channel time-out is reached, the corresponding PTF flag is set and the corresponding trigger signal PITTRIG triggers a rising edge. The trigger feature requires a minimum time-out period of two bus clock cycles because the trigger is asserted high for at least one bus clock cycle. For load register values PITLD = 0x0001 and PITMTLD = 0x0002 the flag setting, trigger timing and a restart with force load is shown in Figure 17-28.

On the front end of the PWM timer, the clock is enabled to the PWM circuit by the PWMEx bit being high. There is an edge-synchronizing circuit to guarantee that the clock will only be enabled or disabled at an edge. When the channel is disabled (PWMEx = 0), the counter for the channel does not count.

19.4.2.2   PWM Polarity

Each channel has a polarity bit to allow starting a waveform cycle with a high or low signal. This is shown on the block diagram as a mux select of either the Q output or the $\overline{Q}$ output of the PWM output flip flop. When one of the bits in the PWMPOL register is set, the associated PWM channel output is high at the beginning of the waveform, then goes low when the duty count is reached. Conversely, if the polarity bit is zero, the output starts low and then goes high when the duty count is reached.

19.4.2.3   PWM Period and Duty

Dedicated period and duty registers exist for each channel and are double buffered so that if they change while the channel is enabled, the change will NOT take effect until one of the following occurs:

- The effective period ends
- The counter is written (counter resets to $00)
- The channel is disabled

In this way, the output of the PWM will always be either the old waveform or the new waveform, not some variation in between. If the channel is not enabled, then writes to the period and duty registers will go directly to the latches as well as the buffer.

A change in duty or period can be forced into effect "immediately" by writing the new value to the duty and/or period registers and then writing to the counter. This forces the counter to reset and the new duty and/or period values to be latched. In addition, since the counter is readable, it is possible to know where the count is with respect to the duty value and software can be used to make adjustments

NOTE

When forcing a new period or duty into effect immediately, an irregular PWM cycle can occur.

Depending on the polarity bit, the duty registers will contain the count of either the high time or the low time.

19.4.2.4   PWM Timer Counters

Each channel has a dedicated 8-bit up/down counter which runs at the rate of the selected clock source (see Section 19.4.1, "PWM Clock Select" for the available clock sources and rates). The counter compares to two registers, a duty register and a period register as shown in Figure 19-19. When the PWM counter matches the duty register, the output flip-flop changes state, causing the PWM waveform to also change state. A match between the PWM counter and the period register behaves differently depending on what output mode is selected as shown in Figure 19-19 and described in Section 19.4.2.5, "Left Aligned Outputs" and Section 19.4.2.6, "Center Aligned Outputs".

Table 23-13. Interrupt Vectors

Interrupt Source	Local Enable
Low-voltage interrupt (LVI)	LVIE = 1; available only in Full Performance Mode
High Temperature Interrupt (HTI)	HTIE=1; available only in Full Performance Mode
Autonomous periodical interrupt (API)	APIE = 1

23.4.11.1 Low-Voltage Interrupt (LVI)

In FPM, VREG_3V3 monitors the input voltage V_{DDA}. Whenever V_{DDA} drops below level V_{LVIA}, the status bit LVDS is set to 1. On the other hand, LVDS is reset to 0 when V_{DDA} rises above level V_{LVID}. An interrupt, indicated by flag LVIF = 1, is triggered by any change of the status bit LVDS if interrupt enable bit LVIE = 1.

NOTE

On entering the Reduced Power Mode, the LVIF is not cleared by the VREG_3V3.

23.4.11.2 HTI - High Temperature Interrupt

In FPM VREG monitors the die temperature T_{DIE}. Whenever T_{DIE} exceeds level T_{HTIA} the status bit HTDS is set to 1. Vice versa, HTDS is reset to 0 when T_{DIE} get below level T_{HTID}. An interrupt, indicated by flag HTIF=1, is triggered by any change of the status bit HTDS if interrupt enable bit HTIE=1.

NOTE

On entering the Reduced Power Mode the HTIF is not cleared by the VREG.

23.4.11.3 Autonomous Periodical Interrupt (API)

As soon as the configured timeout period of the API has elapsed, the APIF bit is set. An interrupt, indicated by flag APIF = 1, is triggered if interrupt enable bit APIE = 1.

2. FDIV shown generates an FCLK frequency of 1.05 MHz

26.3.2.2   Flash Security Register (FSEC)

The FSEC register holds all bits associated with the security of the MCU and Flash module.
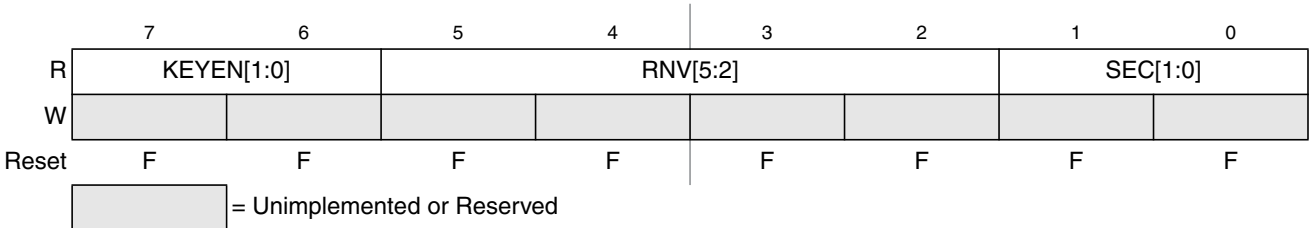
Offset Module Base + 0x0001

	7	6	5	4	3	2	1	0
R	KEYEN[1:0]		RNV[5:2]				SEC[1:0]	
W								
Reset	F	F	F	F	F	F	F	F

☐ = Unimplemented or Reserved

Figure 26-6. Flash Security Register (FSEC)

All bits in the FSEC register are readable but not writable.

During the reset sequence, the FSEC register is loaded with the contents of the Flash security byte in the Flash configuration field at global address 0x7F_FF0F located in P-Flash memory (see Table 26-3) as indicated by reset condition F in Figure 26-6. If a double bit fault is detected while reading the P-Flash phrase containing the Flash security byte during the reset sequence, all bits in the FSEC register will be set to leave the Flash module in a secured state with backdoor key access disabled.

Table 26-10. FSEC Field Descriptions

Field	Description
7–6 KEYEN[1:0]	**Backdoor Key Security Enable Bits** — The KEYEN[1:0] bits define the enabling of backdoor key access to the Flash module as shown in Table 26-11.
5–2 RNV[5:2}	**Reserved Nonvolatile Bits** — The RNV bits should remain in the erased state for future enhancements.
1–0 SEC[1:0]	**Flash Security Bits** — The SEC[1:0] bits define the security state of the MCU as shown in Table 26-12. If the Flash module is unsecured using backdoor key access, the SEC bits are forced to 10.

Table 26-11. Flash KEYEN States

KEYEN[1:0]	Status of Backdoor Key Access
00	DISABLED
01	DISABLED[1]
10	ENABLED
11	DISABLED

1. Preferred KEYEN state to disable backdoor key access.

- 32 Kbytes of D-Flash (Data Flash) memory, consisting of 1 physical Flash block, that can be used as nonvolatile storage to support the built-in hardware scheme for emulated EEPROM, as basic Flash memory primarily intended for nonvolatile data storage, or as a combination of both
- 4 Kbytes of buffer RAM, consisting of 1 physical RAM block, that can be used as emulated EEPROM using a built-in hardware scheme, as basic RAM, or as a combination of both

The Flash memory is ideal for single-supply applications allowing for field reprogramming without requiring external high voltage sources for program or erase operations. The Flash module includes a memory controller that executes commands to modify Flash memory contents or configure module resources for emulated EEPROM operation. The user interface to the memory controller consists of the indexed Flash Common Command Object (FCCOB) register which is written to with the command, global address, data, and any required command parameters. The memory controller must complete the execution of a command before the FCCOB register can be written to with a new command.

CAUTION

A Flash word or phrase must be in the erased state before being programmed. Cumulative programming of bits within a Flash word or phrase is not allowed.

The RAM and Flash memory may be read as bytes, aligned words, or misaligned words. Read access time is one bus cycle for bytes and aligned words, and two bus cycles for misaligned words. For Flash memory, an erased bit reads 1 and a programmed bit reads 0.

It is not possible to read from a Flash block while any command is executing on that specific Flash block. It is possible to read from a Flash block while a command is executing on a different Flash block.

Both P-Flash and D-Flash memories are implemented with Error Correction Codes (ECC) that can resolve single bit faults and detect double bit faults. For P-Flash memory, the ECC implementation requires that programming be done on an aligned 8 byte basis (a Flash phrase). Since P-Flash memory is always read by phrase, only one single bit fault in the phrase containing the byte or word accessed will be corrected.

28.1.1   Glossary

Buffer RAM — The buffer RAM constitutes the volatile memory store required for EEE. Memory space in the buffer RAM not required for EEE can be partitioned to provide volatile memory space for applications.

Command Write Sequence — An MCU instruction sequence to execute built-in algorithms (including program and erase) on the Flash memory.

D-Flash Memory — The D-Flash memory constitutes the nonvolatile memory store required for EEE. Memory space in the D-Flash memory not required for EEE can be partitioned to provide nonvolatile memory space for applications.

Table 28-4. Program IFR Fields

Global Address (PGMIFRON)	Size (Bytes)	Field Description
0x40_0000 – 0x40_0007	8	Device ID
0x40_0008 – 0x40_00E7	224	Reserved
0x40_00E8 – 0x40_00E9	2	Version ID
0x40_00EA – 0x40_00FF	22	Reserved
0x40_0100 – 0x40_013F	64	Program Once Field Refer to Section 28.4.2.7, "Program Once Command"
0x40_0140 – 0x40_01FF	192	Reserved

Table 28-5. P-Flash IFR Accessibility

Global Address (PGMIFRON)	Size (Bytes)	Accessed From
0x40_0000 – 0x40_01FF	512	XBUS0 (PBLK0S)[1]
0x40_0200 – 0x40_03FF	512	Unimplemented
0x40_0400 – 0x40_05FF	512	XBUS0 (PBLK1N)
0x40_0600 – 0x40_07FF	512	XBUS1 (PBLK1S)
0x40_0800 – 0x40_09FF	512	XBUS0 (PBLK2S)
0x40_0A00 – 0x40_0BFF	512	Unimplemented

1. Refer to Table 28-4 for more details.

Table 28-6. EEE Resource Fields

Global Address	Size (Bytes)	Description
0x10_0000 – 0x10_7FFF	32,768	D-Flash Memory (User and EEE)
0x10_8000 – 0x11_FFFF	98,304	Reserved
0x12_0000 – 0x12_007F	128	EEE Nonvolatile Information Register (EEEIFRON[1] = 1)
0x12_0080 – 0x12_0FFF	3,968	Reserved
0x12_1000 – 0x12_1EFF	3,840	Reserved
0x12_1F00 – 0x12_1FFF	256	EEE Tag RAM (TMGRAMON[1] = 1)
0x12_2000 – 0x12_3BFF	7,168	Reserved
0x12_3C00 – 0x12_3FFF	1,024	Memory Controller Scratch RAM (TMGRAMON[1] = 1)
0x12_4000 – 0x12_DFFF	40,960	Reserved
0x12_E000 – 0x12_FFFF	8,192	Reserved
0x13_0000 – 0x13_EFFF	61,440	Reserved
0x13_F000 – 0x13_FFFF	4,096	Buffer RAM (User and EEE)

Table 29-66. Erase Verify D-Flash Section Command Error Handling

Register	Error Bit	Error Condition
FSTAT	ACCERR	Set if CCOBIX[2:0] != 010 at command launch
		Set if a Load Data Field command sequence is currently active
		Set if command not available in current mode (see Table 29-30)
		Set if an invalid global address [22:0] is supplied
		Set if a misaligned word address is supplied (global address [0] != 0)
		Set if the global address [22:0] points to an area of the D-Flash EEE partition
		Set if the requested section breaches the end of the D-Flash block or goes into the D-Flash EEE partition
	FPVIOL	None
	MGSTAT1	Set if any errors have been encountered during the read
	MGSTAT0	Set if any non-correctable errors have been encountered during the read
FERSTAT	EPVIOLIF	None

29.4.2.17 Program D-Flash Command

The Program D-Flash operation programs one to four previously erased words in the D-Flash user partition. The Program D-Flash operation will confirm that the targeted location(s) were successfully programmed upon completion.

CAUTION

A Flash word must be in the erased state before being programmed. Cumulative programming of bits within a Flash word is not allowed.

Table 29-67. Program D-Flash Command FCCOB Requirements

CCOBIX[2:0]	FCCOB Parameters	
000	0x11	Global address [22:16] to identify the D-Flash block
001	Global address [15:0] of word to be programmed	
010	Word 0 program value	
011	Word 1 program value, if desired	
100	Word 2 program value, if desired	
101	Word 3 program value, if desired	

Upon clearing CCIF to launch the Program D-Flash command, the user-supplied words will be transferred to the Memory Controller and be programmed. The CCOBIX index value at Program D-Flash command launch determines how many words will be programmed in the D-Flash block. No protection checks are made in the Program D-Flash operation on the D-Flash block, only access error checks. The CCIF flag is set when the operation has completed.

A.3.1.9 Erase P-Flash Block (FCMD=0x09)

Erasing a 256K NVM block takes

$$t_{mass} \approx 100100 \cdot \frac{1}{f_{NVMOP}} + 70000 \cdot \frac{1}{f_{NVMBUS}}$$

Erasing a 128K NVM block takes

$$t_{mass} \approx 100100 \cdot \frac{1}{f_{NVMOP}} + 35000 \cdot \frac{1}{f_{NVMBUS}}$$

A.3.1.10 Erase P-Flash Sector (FCMD=0x0A)

The typical time to erase a1024-byte P-Flash sector can be calculated using

$$t_{era} = \left(20020 \cdot \frac{1}{f_{NVMOP}} \right) + \left(700 \cdot \frac{1}{f_{NVMBUS}} \right)$$

The maximum time to erase a1024-byte P-Flash sector can be calculated using

$$t_{era} = \left(20020 \cdot \frac{1}{f_{NVMOP}} \right) + \left(1100 \cdot \frac{1}{f_{NVMBUS}} \right)$$

A.3.1.11 Unsecure Flash (FCMD=0x0B)

The maximum time for unsecuring the flash is given by

$$t_{uns} = \left(100100 \cdot \frac{1}{f_{NVMOP}} + 70000 \cdot \frac{1}{f_{NVMBUS}} \right)$$

A.3.1.12 Verify Backdoor Access Key (FCMD=0x0C)

The maximum verify backdoor access key time is given by

$$t = 400 \cdot \frac{1}{f_{NVMBUS}}$$

A.3.1.13 Set User Margin Level (FCMD=0x0D)

The maximum set user margin level time is given by

$$t = 350 \cdot \frac{1}{f_{NVMBUS}}$$

A.3.1.14 Set Field Margin Level (FCMD=0x0E)

The maximum set field margin level time is given by