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Details

Product Status	Obsolete
Core Processor	HCS12X
Core Size	16-Bit
Speed	50MHz
Connectivity	CANbus, EBI/EMI, I ² C, IrDA, SCI, SPI
Peripherals	LVD, POR, PWM, WDT
Number of I/O	119
Program Memory Size	384KB (384K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	24K x 8
Voltage - Supply (Vcc/Vdd)	1.72V ~ 5.5V
Data Converters	A/D 24x12b
Oscillator Type	External
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mc9s12xeq384vag

Table 1-8. Peripheral - Port Routing Options⁽¹⁾ (continued)

	CAN0	CAN1	CAN2	CAN3	CAN4	SCI0	SCI1	SCI2	SCI3	SCI4	SCI5	SCI6	SCI7	SPI0	SPI1	SPI2	IIC0	IIC1	CS0	CS1	CS2	CS3	TIM
PS[1:0]						O																	
PS[3:2]							O																
PS[7:4]														O									

1. "O" denotes reset condition, "X" denotes a possible rerouting under software control

Table 1-9. Pin-Out Summary (Sheet 1 of 7)

208 MAPBGA	LQFP 144	LQFP 112	QFP ⁽¹⁾ 80	Pin	2nd Func.	3rd Func.	4th Func.	5th Func.
D4	1	1	1	PP3	KWP3	PWM3	SS1	TIMIOC3
B2	2	2	2	PP2	KWP2	PWM2	SCK1	TIMIOC2
C2	3	3	3	PP1	KWP1	PWM1	MOSI1	TIMIOC1
D3	4	4	4	PP0	KWP0	PWM0	MISO1	TIMIOC0
D2				PJ3	KWJ3			
C1	5			PJ2	KWJ2	CS1		
E4	6			PK6	ADDR22	ACC2		
E2	7	5		PK3	ADDR19	IQSTAT3		
E3	8	6		PK2	ADDR18	IQSTAT2		
D1	9	7		PK1	ADDR17	IQSTAT1		
E1	10	8		PK0	ADDR16	IQSTAT0		
VDDX				VDDX7				
VSSX				VSSX7				
F3	11	9	5	PT0	IOC0			
F2				PR0	TIMIOC0			
G4	12	10	6	PT1	IOC1			
F1				PR1	TIMIOC1			
G1	13	11	7	PT2	IOC2			
G3				PR2	TIMIOC2			
G2	14	12	8	PT3	IOC3			
H1				PR3	TIMIOC3			
H4	15	13	9	VDDF				

The ECLKCTL register is used to control the availability of the free-running clocks and the free-running clock divider.

Table 2-16. ECLKCTL Register Field Descriptions

Field	Description
7 NECLK	No ECLK —Disable ECLK output This bit controls the availability of a free-running clock on the ECLK pin. Clock output is always active in emulation modes and if enabled in all other operating modes. 1 ECLK disabled 0 ECLK enabled
6 NCLKX2	No ECLKX2 —Disable ECLKX2 output This bit controls the availability of a free-running clock on the ECLKX2 pin. This clock has a fixed rate of twice the internal Bus Clock. Clock output is always active in emulation modes and if enabled in all other operating modes. 1 ECLKX2 disabled 0 ECLKX2 enabled
5 DIV16	Free-running ECLK predivider —Divide by 16 This bit enables a divide-by-16 stage on the selected EDIV rate. 1 Divider enabled: ECLK rate = EDIV rate divided by 16 0 Divider disabled: ECLK rate = EDIV rate
4-0 EDIV	Free-running ECLK Divider —Configure ECLK rate These bits determine the rate of the free-running clock on the ECLK pin. Divider is always disabled in emulation modes and active as programmed in all other operating modes. 00000 ECLK rate = Bus Clock rate 00001 ECLK rate = Bus Clock rate divided by 2 00010 ECLK rate = Bus Clock rate divided by 3, ... 11111 ECLK rate = Bus Clock rate divided by 32

2.3.16 PIM Reserved Register

Address 0x001D (PRR)

Access: User read⁽¹⁾

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	0
W								
Reset	0	0	0	0	0	0	0	0


 = Unimplemented or Reserved

Figure 2-14. PIM Reserved Register

1. Read: Always reads 0x00
Write: Unimplemented

3.3 Memory Map and Registers

3.3.1 Module Memory Map

A summary of the registers associated with the MMC block is shown in [Figure 3-2](#). Detailed descriptions of the registers and bits are given in the subsections that follow.

Address	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
0x000A	MMCCTL0	R W	CS3E1	CS3E0	CS2E1	CS2E0	CS1E1	CS1E0	CS0E1	CS0E0
0x000B	MODE	R W	MODC	MODB	MODA	0	0	0	0	0
0x0010	GPAGE	R W	0	GP6	GP5	GP4	GP3	GP2	GP1	GP0
0x0011	DIRECT	R W	DP15	DP14	DP13	DP12	DP11	DP10	DP9	DP8
0x0012	Reserved	R W	0	0	0	0	0	0	0	0
0x0013	MMCCTL1	R W	TGMRAMON	0	EEEEIFRON	PGMIFRON	RAMHM	EROMON	ROMHM	ROMON
0x0014	Reserved	R W	0	0	0	0	0	0	0	0
0x0015	PPAGE	R W	PIX7	PIX6	PIX5	PIX4	PIX3	PIX2	PIX1	PIX0
0x0016	RPAGE	R W	RP7	RP6	RP5	RP4	RP3	RP2	RP1	RP0
0x0017	EPAGE	R W	EP7	EP6	EP5	EP4	EP3	EP2	EP1	EP0

= Unimplemented or Reserved

Figure 3-2. MMC Register Summary

Table 3-11. MMCCTL1 Field Descriptions (continued)

Field	Description
2 EROMON	Enables emulated Flash or ROM memory in the memory map Write: Never This bit is used in some modes to define the placement of the Emulated Flash or ROM (Refer to Table 3-12) 0 Disables the emulated Flash or ROM in the memory map. 1 Enables the emulated Flash or ROM in the memory map.
1 ROMHM	FLASH or ROM only in higher Half of Memory Map Write: Once in normal and emulation modes and anytime in special modes 0 The fixed page of Flash or ROM can be accessed in the lower half of the memory map. Accesses to 0x4000–0x7FFF will be mapped to 0x7F_4000–0x7F_7FFF in the global memory space. 1 Disables access to the Flash or ROM in the lower half of the memory map. These physical locations of the Flash or ROM can still be accessed through the program page window. Accesses to 0x4000–0x7FFF will be mapped to 0x14_4000–0x14_7FFF in the global memory space (external access).
0 ROMON	Enable FLASH or ROM in the memory map Write: Once in normal and emulation modes and anytime in special modes. This bit is used in some modes to define the placement of the ROM (Refer to Table 3-12) 0 Disables the Flash or ROM from the memory map. 1 Enables the Flash or ROM in the memory map.

EROMON and ROMON control the visibility of the Flash in the memory map for CPU or BDM (not for XGATE). Both local and global memory maps are affected.

Table 3-12. Data Sources when CPU or BDM is Accessing Flash Area

Chip Modes	ROMON	EROMON	DATA SOURCE ⁽¹⁾	Stretch ⁽²⁾
Normal Single Chip	X	X	Internal Flash	N
Special Single Chip				
Emulation Single Chip	X	0	Emulation Memory	N
	X	1	Internal Flash	
Normal Expanded	0	X	External Application	Y
	1	X	Internal Flash	N
Emulation Expanded	0	X	External Application	Y
	1	0	Emulation Memory	N
	1	1	Internal Flash	
Special Test	0	X	External Application	N
	1	X	Internal Flash	

1. Internal Flash means Flash resources inside the MCU are read/written.

Emulation memory means resources inside the emulator are read/written (PRU registers, flash replacement, RAM, EEPROM and register space are always considered internal).

External application means resources residing outside the MCU are read/written.

2. The external access stretch mechanism is part of the EBI module (refer to EBI Block Guide for details).

The fixed 16K page from 0x4000–0x7FFF (when ROMHM = 0) is the page number 0xFD.

The reset value of 0xFE ensures that there is linear Flash space available between addresses 0x4000 and 0xFFFF out of reset.

The fixed 16K page from 0xC000-0xFFFF is the page number 0xFF.

3.3.2.7 RAM Page Index Register (RPAGE)

Address: 0x0016

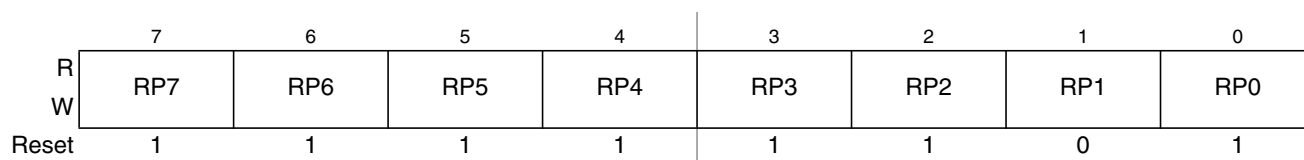


Figure 3-13. RAM Page Index Register (RPAGE)

Read: Anytime

Write: Anytime

These eight index bits are used to page 4 KByte blocks into the RAM page window located in the local (CPU or BDM) memory map from address 0x1000 to address 0x1FFF (see [Figure 3-14](#)). This supports accessing up to 1022 KByte of RAM (in the Global map) within the 64 KByte Local map. The RAM page index register is effectively used to construct paged RAM addresses in the Local map format.

CAUTION

XGATE write access to this register during an CPU access which makes use of this register could lead to unexpected results.

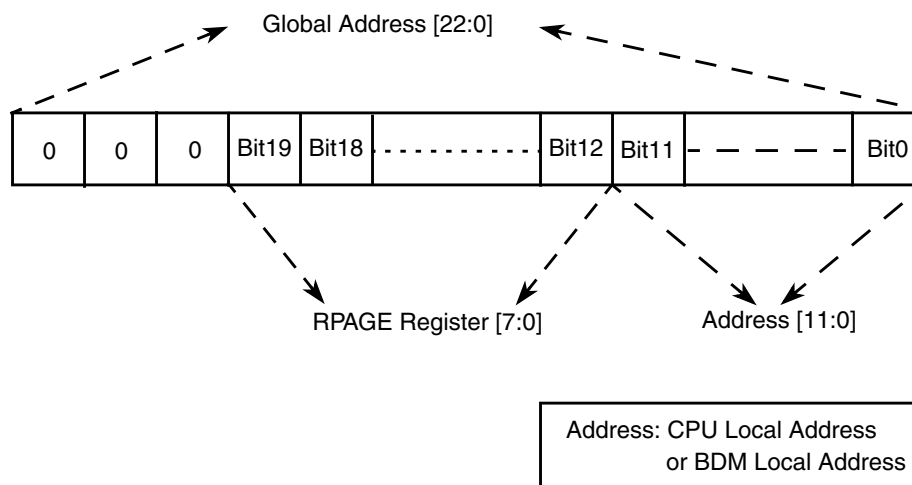


Figure 3-14. RPAGE Address Mapping

NOTE

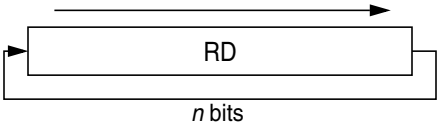
Because RAM page 0 has the same global address as the register space, it is possible to write to registers through the RAM space when `RPAGE = 0x00`.

ROR

Rotate Right

ROR

Operation



$n = \text{RS or IMM4}$

Rotates the bits in register RD n positions to the right. The upper n bits of the register RD are filled with the lower n bits. Two source forms are available. In the first form, the parameter n is contained in the instruction code as an immediate operand. In the second form, the parameter is contained in the lower bits of the source register RS[3:0]. All other bits in RS are ignored. If n is zero no shift will take place and the register RD will be unaffected; however, the condition code flags will be updated.

CCR Effects

N	Z	V	C
Δ	Δ	0	—

- N: Set if bit 15 of the result is set; cleared otherwise.
Z: Set if the result is \$0000; cleared otherwise.
V: 0; cleared.
C: Not affected.

Code and CPU Cycles

Source Form	Address Mode	Machine Code											Cycles	
ROR RD, #IMM4	IMM4	0	0	0	0	1	RD	IMM4		1	1	1	1	P
ROR RD, RS	DYA	0	0	0	0	1	RD	RS	1	0	1	1	1	P

Register Name		Bit 7	6	5	4	3	2	1	Bit 0
0x0000 TIOS	R W	IOS7	IOS6	IOS5	IOS4	IOS3	IOS2	IOS1	IOS0
0x0001 CFORC	R W	0 FOC7	0 FOC6	0 FOC5	0 FOC4	0 FOC3	0 FOC2	0 FOC1	0 FOC0
0x0002 OC7M	R W	OC7M7	OC7M6	OC7M5	OC7M4	OC7M3	OC7M2	OC7M1	OC7M0
0x0003 OC7D	R W	OC7D7	OC7D6	OC7D5	OC7D4	OC7D3	OC7D2	OC7D1	OC7D0
0x0004 TCNT (High)	R W	TCNT15	TCNT14	TCNT13	TCNT12	TCNT11	TCNT10	TCNT9	TCNT8
0x0005 TCNT (Low)	R W	TCNT7	TCNT6	TCNT5	TCNT4	TCNT3	TCNT2	TCNT1	TCNT0
0x0006 TSCR1	R W	TEN	TSWAI	TSFRZ	TFFCA	PRNT	0	0	0
0x0007 TTOF	R W	TOV7	TOV6	TOV5	TOV4	TOV3	TOV2	TOV1	TOV0
0x0008 TCTL1	R W	OM7	OL7	OM6	OL6	OM5	OL5	OM4	OL4
0x0009 TCTL2	R W	OM3	OL3	OM2	OL2	OM1	OL1	OM0	OL0
0x000A TCTL3	R W	EDG7B	EDG7A	EDG6B	EDG6A	EDG5B	EDG5A	EDG4B	EDG4A
0x000B TCTL4	R W	EDG3B	EDG3A	EDG2B	EDG2A	EDG1B	EDG1A	EDG0B	EDG0A
0x000C TIE	R W	C7I	C6I	C5I	C4I	C3I	C2I	C1I	C0I

= Unimplemented or Reserved

Figure 14-2. ECT Register Summary (Sheet 1 of 5)

Register Name		Bit 7	6	5	4	3	2	1	Bit 0
0x003A TC1H (High)	R	TC15	TC14	TC13	TC12	TC11	TC10	TC9	TC8
	W								
0x003B TC1H (Low)	R	TC7	TC6	TC5	TC4	TC3	TC2	TC1	TC0
	W								
0x003C TC2H (High)	R	TC15	TC14	TC13	TC12	TC11	TC10	TC9	TC8
	W								
0x003D TC2H (Low)	R	TC7	TC6	TC5	TC4	TC3	TC2	TC1	TC0
	W								
0x003E TC3H (High)	R	TC15	TC14	TC13	TC12	TC11	TC10	TC9	TC8
	W								
0x003F TC3H (Low)	R	TC7	TC6	TC5	TC4	TC3	TC2	TC1	TC0
	W								

= Unimplemented or Reserved

Figure 14-2. ECT Register Summary (Sheet 5 of 5)

14.3.2.1 Timer Input Capture/Output Compare Select Register (TIOS)

Module Base + 0x0000

	7	6	5	4	3	2	1	0
R	IOS7	IOS6	IOS5	IOS4	IOS3	IOS2	IOS1	IOS0
W								
Reset	0	0	0	0	0	0	0	0

Figure 14-3. Timer Input Capture/Output Compare Register (TIOS)

Read or write: Anytime

All bits reset to zero.

Table 14-2. TIOS Field Descriptions

Field	Description
7:0 IOS[7:0]	Input Capture or Output Compare Channel Configuration 0 The corresponding channel acts as an input capture. 1 The corresponding channel acts as an output compare.

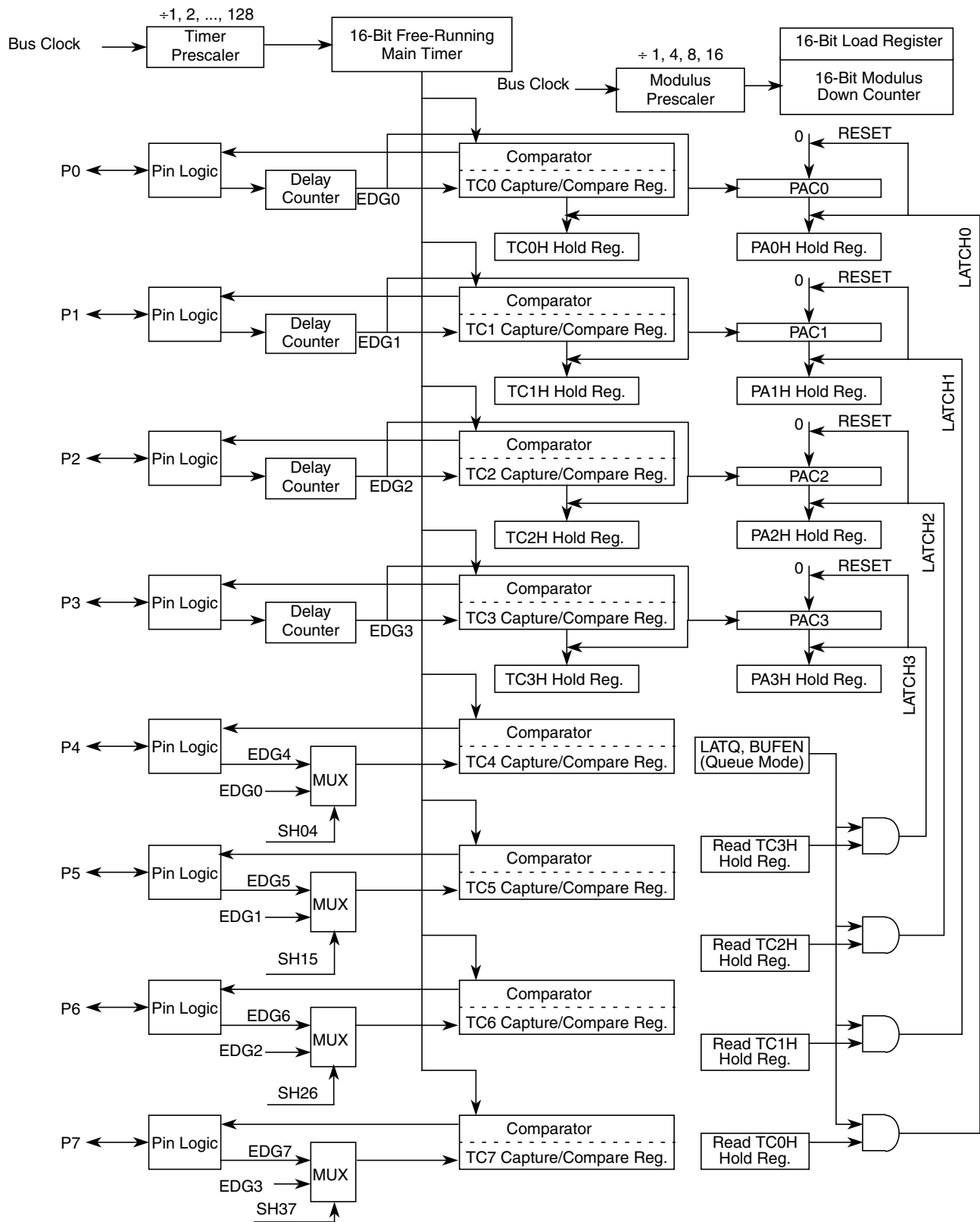


Figure 14-69. Detailed Timer Block Diagram in Queue Mode when PRNT = 0

If it were the case that the IBSWAI bit was cleared when the WAI instruction was executed, the IIC internal clocks and interface would remain alive, continuing the operation which was currently underway. It is also possible to configure the IIC such that it will wake up the CPU via an interrupt at the conclusion of the current operation. See the discussion on the IBIF and IBIE bits in the IBSR and IBCR, respectively.

15.3.1.4 IIC Status Register (IBSR)

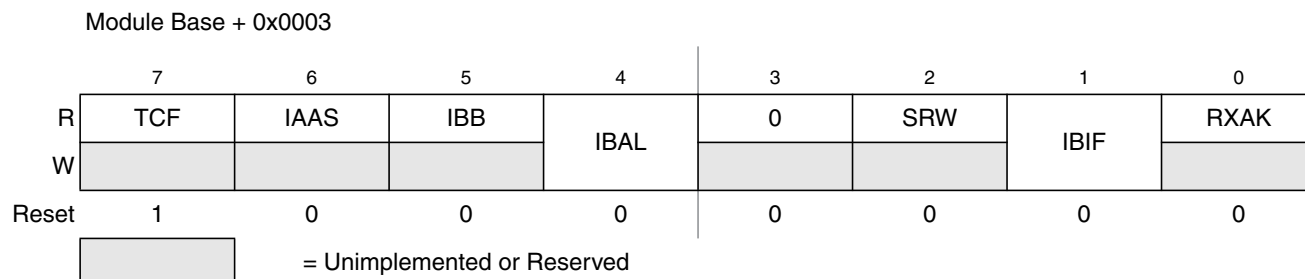


Figure 15-7. IIC Bus Status Register (IBSR)

This status register is read-only with exception of bit 1 (IBIF) and bit 4 (IBAL), which are software clearable.

Table 15-9. IBSR Field Descriptions

Field	Description
7 TCF	Data Transferring Bit — While one byte of data is being transferred, this bit is cleared. It is set by the falling edge of the 9th clock of a byte transfer. Note that this bit is only valid during or immediately following a transfer to the IIC module or from the IIC module. 0 Transfer in progress 1 Transfer complete
6 IAAS	Addressed as a Slave Bit — When its own specific address (I-bus address register) is matched with the calling address or it receives the general call address with GCEN== 1, this bit is set. The CPU is interrupted provided the IBIE is set. Then the CPU needs to check the SRW bit and set its Tx/Rx mode accordingly. Writing to the I-bus control register clears this bit. 0 Not addressed 1 Addressed as a slave
5 IBB	Bus Busy Bit 0 This bit indicates the status of the bus. When a START signal is detected, the IBB is set. If a STOP signal is detected, IBB is cleared and the bus enters idle state. 1 Bus is busy
4 IBAL	Arbitration Lost — The arbitration lost bit (IBAL) is set by hardware when the arbitration procedure is lost. Arbitration is lost in the following circumstances: 1. SDA sampled low when the master drives a high during an address or data transmit cycle. 2. SDA sampled low when the master drives a high during the acknowledge bit of a data receive cycle. 3. A start cycle is attempted when the bus is busy. 4. A repeated start cycle is requested in slave mode. 5. A stop condition is detected when the master did not request it. This bit must be cleared by software, by writing a one to it. A write of 0 has no effect on this bit.
3 RESERVED	Reserved — Bit 3 of IBSR is reserved for future use. A read operation on this bit will return 0.

16.1.1 Glossary

Table 16-2. Terminology

ACK	Acknowledge of CAN message
CAN	Controller Area Network
CRC	Cyclic Redundancy Code
EOF	End of Frame
FIFO	First-In-First-Out Memory
IFS	Inter-Frame Sequence
SOF	Start of Frame
CPU bus	CPU related read/write data bus
CAN bus	CAN protocol related serial bus
oscillator clock	Direct clock from external oscillator
bus clock	CPU bus related clock
CAN clock	CAN protocol related clock

16.1.2 Block Diagram

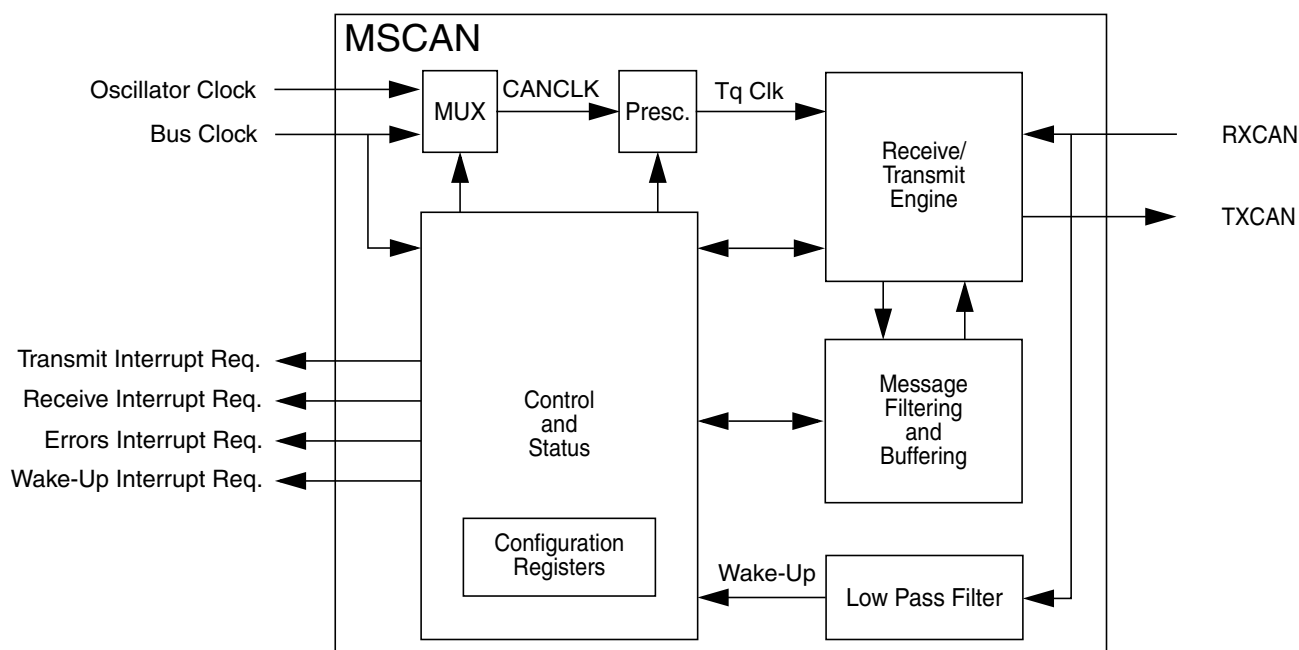


Figure 16-1. MSCAN Block Diagram

Table 20-4. SCICR1 Field Descriptions (continued)

Field	Description
2 ILT	Idle Line Type Bit — ILT determines when the receiver starts counting logic 1s as idle character bits. The counting begins either after the start bit or after the stop bit. If the count begins after the start bit, then a string of logic 1s preceding the stop bit may cause false recognition of an idle character. Beginning the count after the stop bit avoids false idle character recognition, but requires properly synchronized transmissions. 0 Idle character bit count begins after start bit 1 Idle character bit count begins after stop bit
1 PE	Parity Enable Bit — PE enables the parity function. When enabled, the parity function inserts a parity bit in the most significant bit position. 0 Parity function disabled 1 Parity function enabled
0 PT	Parity Type Bit — PT determines whether the SCI generates and checks for even parity or odd parity. With even parity, an even number of 1s clears the parity bit and an odd number of 1s sets the parity bit. With odd parity, an odd number of 1s clears the parity bit and an even number of 1s sets the parity bit. 0 Even parity 1 Odd parity

Table 20-5. Loop Functions

LOOPS	RSRC	Function
0	x	Normal operation
1	0	Loop mode with transmitter output internally connected to receiver input
1	1	Single-wire mode with TXD pin connected to receiver input

When all bits are clear (the default condition), the SPI module clock is divided by 2. When the selection bits (SPR2–SPR0) are 001 and the preselection bits (SPPR2–SPPR0) are 000, the module clock divisor becomes 4. When the selection bits are 010, the module clock divisor becomes 8, etc.

When the preselection bits are 001, the divisor determined by the selection bits is multiplied by 2. When the preselection bits are 010, the divisor is multiplied by 3, etc. See [Table 21-7](#) for baud rate calculations for all bit conditions, based on a 25 MHz bus clock. The two sets of selects allows the clock to be divided by a non-power of two to achieve other baud rates such as divide by 6, divide by 10, etc.

The baud rate generator is activated only when the SPI is in master mode and a serial transfer is taking place. In the other cases, the divider is disabled to decrease I_{DD} current.

NOTE

For maximum allowed baud rates, please refer to the SPI Electrical Specification in the Electricals chapter of this data sheet.

21.4.5 Special Features

21.4.5.1 \overline{SS} Output

The \overline{SS} output feature automatically drives the \overline{SS} pin low during transmission to select external devices and drives it high during idle to deselect external devices. When \overline{SS} output is selected, the \overline{SS} output pin is connected to the \overline{SS} input pin of the external device.

The \overline{SS} output is available only in master mode during normal SPI operation by asserting SSOE and MODFEN bit as shown in [Table 21-3](#).

The mode fault feature is disabled while \overline{SS} output is enabled.

NOTE

Care must be taken when using the \overline{SS} output feature in a multimaster system because the mode fault feature is not available for detecting system errors between masters.

21.4.5.2 Bidirectional Mode (MOMI or SISO)

The bidirectional mode is selected when the SPC0 bit is set in SPI control register 2 (see [Table 21-11](#)). In this mode, the SPI uses only one serial data pin for the interface with external device(s). The MSTR bit decides which pin to use. The MOSI pin becomes the serial data I/O (MOMI) pin for the master mode, and the MISO pin becomes serial data I/O (SISO) pin for the slave mode. The MISO pin in master mode and MOSI pin in slave mode are not used by the SPI.

22.3.2.8 Timer Control Register 1/Timer Control Register 2 (TCTL1/TCTL2)

Module Base + 0x0008

	7	6	5	4	3	2	1	0
R	OM7	OL7	OM6	OL6	OM5	OL5	OM4	OL4
W								
Reset	0	0	0	0	0	0	0	0

Figure 22-14. Timer Control Register 1 (TCTL1)

Module Base + 0x0009

	7	6	5	4	3	2	1	0
R	OM3	OL3	OM2	OL2	OM1	OL1	OM0	OL0
W								
Reset	0	0	0	0	0	0	0	0

Figure 22-15. Timer Control Register 2 (TCTL2)

Read: Anytime

Write: Anytime

Table 22-8. TCTL1/TCTL2 Field Descriptions

Field	Description
7:0 OMx	Output Mode — These eight pairs of control bits are encoded to specify the output action to be taken as a result of a successful OCx compare. When either OMx or OLx is 1, the pin associated with OCx becomes an output tied to OCx. Note: To enable output action by OMx bits on timer port, the corresponding bit in OC7M should be cleared. For an output line to be driven by an OCx the OCPDx must be cleared.
7:0 OLx	Output Level — These eight pairs of control bits are encoded to specify the output action to be taken as a result of a successful OCx compare. When either OMx or OLx is 1, the pin associated with OCx becomes an output tied to OCx. Note: To enable output action by OLx bits on timer port, the corresponding bit in OC7M should be cleared. For an output line to be driven by an OCx the OCPDx must be cleared.

Table 22-9. Compare Result Output Action

OMx	OLx	Action
0	0	No output compare action on the timer output signal
0	1	Toggle OCx output line
1	0	Clear OCx output line to zero
1	1	Set OCx output line to one



Figure 25-4. FTM256K2 Register Summary (continued)

25.3.2.1 Flash Clock Divider Register (FCLKDIV)

The FCLKDIV register is used to control timed events in program and erase algorithms.

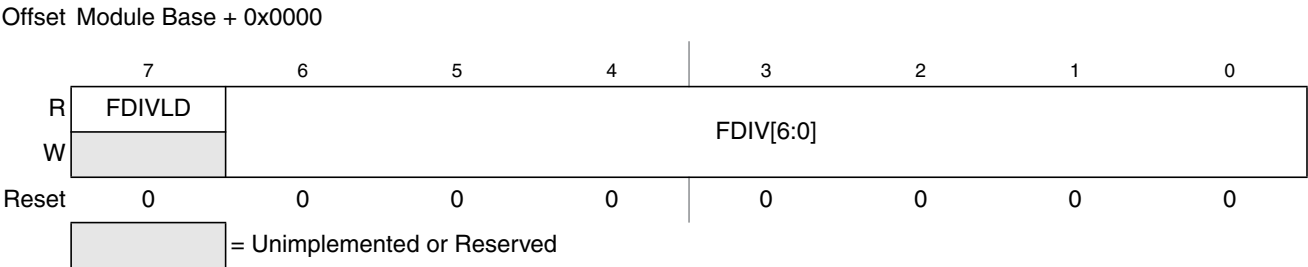


Figure 25-5. Flash Clock Divider Register (FCLKDIV)

All bits in the FCLKDIV register are readable, bits 6–0 are write once and bit 7 is not writable.

Table 25-8. FCLKDIV Field Descriptions

Field	Description
7 FDIVLD	Clock Divider Loaded 0 FCLKDIV register has not been written 1 FCLKDIV register has been written since the last reset
6–0 FDIV[6:0]	Clock Divider Bits — FDIV[6:0] must be set to effectively divide OSCCLK down to generate an internal Flash clock, FCLK, with a target frequency of 1 MHz for use by the Flash module to control timed events during program and erase algorithms. Table 25-9 shows recommended values for FDIV[6:0] based on OSCCLK frequency. Please refer to Section 25.4.1, “Flash Command Operations,” for more information.

CAUTION

The FCLKDIV register should never be written while a Flash command is executing (CCIF=0). The FCLKDIV register is writable during the Flash reset sequence even though CCIF is clear.

Table 25-32. D-Flash Commands

FCMD	Command	Function on D-Flash Memory
0x08	Erase All Blocks	Erase all D-Flash (and P-Flash) blocks. An erase of all Flash blocks is only possible when the FPLDIS, FPHDIS, and FPOPEN bits in the FPROT register and the EPDIS and EPOPEN bits in the EPROT register are set prior to launching the command.
0x0B	Unsecure Flash	Supports a method of releasing MCU security by erasing all D-Flash (and P-Flash) blocks and verifying that all D-Flash (and P-Flash) blocks are erased.
0x0D	Set User Margin Level	Specifies a user margin read level for the D-Flash block.
0x0E	Set Field Margin Level	Specifies a field margin read level for the D-Flash block (special modes only).
0x0F	Full Partition D-Flash	Erase the D-Flash block and partition an area of the D-Flash block for user access.
0x10	Erase Verify D-Flash Section	Verify that a given number of words starting at the address provided are erased.
0x11	Program D-Flash	Program up to four words in the D-Flash block.
0x12	Erase D-Flash Sector	Erase all bytes in a sector of the D-Flash block.
0x13	Enable EEPROM Emulation	Enable EEPROM emulation where writes to the buffer RAM EEE partition will be copied to the D-Flash EEE partition.
0x14	Disable EEPROM Emulation	Suspend all current erase and program activity related to EEPROM emulation but leave current EEE tags set.
0x15	EEPROM Emulation Query	Returns EEE partition and status variables.
0x20	Partition D-Flash	Partition an area of the D-Flash block for user access.

25.4.2 Flash Command Description

This section provides details of all available Flash commands launched by a command write sequence. The ACCERR bit in the FSTAT register will be set during the command write sequence if any of the following illegal steps are performed, causing the command not to be processed by the Memory Controller:

- Starting any command write sequence that programs or erases Flash memory before initializing the FCLKDIV register
- Writing an invalid command as part of the command write sequence
- For additional possible errors, refer to the error handling table provided for each command

If a Flash block is read during execution of an algorithm (CCIF = 0) on that same block, the read operation will return invalid data. If the SFDIF or DFDIF flags were not previously set when the invalid read operation occurred, both the SFDIF and DFDIF flags will be set and the FECCR registers will be loaded with the global address used in the invalid read operation with the data and parity fields set to all 0.

If the ACCERR or FPVIOL bits are set in the FSTAT register, the user must clear these bits before starting any command write sequence (see [Section 25.3.2.7](#)).

Table 27-4. Program IFR Fields

Global Address (PGMIFRON)	Size (Bytes)	Field Description
0x40_0000 – 0x40_0007	8	Device ID
0x40_0008 – 0x40_00E7	224	Reserved
0x40_00E8 – 0x40_00E9	2	Version ID
0x40_00EA – 0x40_00FF	22	Reserved
0x40_0100 – 0x40_013F	64	Program Once Field Refer to Section 27.4.2.7 , “Program Once Command”
0x40_0140 – 0x40_01FF	192	Reserved

Table 27-5. P-Flash IFR Accessibility

Global Address (PGMIFRON)	Size (Bytes)	Accessed From
0x40_0000 – 0x40_01FF	512	XBUS0 (PBLK0S) ⁽¹⁾
0x40_0200 – 0x40_03FF	512	Unimplemented
0x40_0400 – 0x40_05FF	512	XBUS0 (PBLK1N)
0x40_0600 – 0x40_07FF	512	XBUS1 (PBLK1S)

1. Refer to [Table 27-4](#) for more details.

Table 27-6. EEE Resource Fields

Global Address	Size (Bytes)	Description
0x10_0000 – 0x10_7FFF	32,768	D-Flash Memory (User and EEE)
0x10_8000 – 0x11_FFFF	98,304	Reserved
0x12_0000 – 0x12_007F	128	EEE Nonvolatile Information Register (EEEIFRON ⁽¹⁾ = 1)
0x12_0080 – 0x12_0FFF	3,968	Reserved
0x12_1000 – 0x12_1EFF	3,840	Reserved
0x12_1F00 – 0x12_1FFF	256	EEE Tag RAM (TMGRAMON ¹ = 1)
0x12_2000 – 0x12_3BFF	7,168	Reserved
0x12_3C00 – 0x12_3FFF	1,024	Memory Controller Scratch RAM (TMGRAMON ¹ = 1)
0x12_4000 – 0x12_DFFF	40,960	Reserved
0x12_E000 – 0x12_FFFF	8,192	Reserved
0x13_0000 – 0x13_EFFF	61,440	Reserved
0x13_F000 – 0x13_FFFF	4,096	Buffer RAM (User and EEE)

1. MMCCTL1 register bit

28.4.2.10 Erase P-Flash Sector Command

The Erase P-Flash Sector operation will erase all addresses in a P-Flash sector.

Table 28-51. Erase P-Flash Sector Command FCCOB Requirements

CCOBIX[2:0]	FCCOB Parameters	
000	0x0A	Global address [22:16] to identify P-Flash block to be erased
001	Global address [15:0] anywhere within the sector to be erased. Refer to Section 28.1.2.1 for the P-Flash sector size.	

Upon clearing CCIF to launch the Erase P-Flash Sector command, the Memory Controller will erase the selected Flash sector and then verify that it is erased. The CCIF flag will be set after the Erase P-Flash Sector operation has completed.

Table 28-52. Erase P-Flash Sector Command Error Handling

Register	Error Bit	Error Condition
FSTAT	ACCERR	Set if CCOBIX[2:0] != 001 at command launch
		Set if a Load Data Field command sequence is currently active
		Set if command not available in current mode (see Table 28-30)
		Set if an invalid global address [22:16] is supplied ⁽¹⁾
		Set if a misaligned phrase address is supplied (global address [2:0] != 000)
	FPVIOL	Set if the selected P-Flash sector is protected
	MGSTAT1	Set if any errors have been encountered during the verify operation
FERSTAT	MGSTAT0	Set if any non-correctable errors have been encountered during the verify operation
	EPVIOLIF	None

1. As defined by the memory map for FTM1024K5.

28.4.2.11 Unsecure Flash Command

The Unsecure Flash command will erase the entire P-Flash and D-Flash memory space and, if the erase is successful, will release security.

Table 28-53. Unsecure Flash Command FCCOB Requirements

CCOBIX[2:0]	FCCOB Parameters	
000	0x0B	Not required

Upon clearing CCIF to launch the Unsecure Flash command, the Memory Controller will erase the entire P-Flash and D-Flash memory space and verify that it is erased. If the Memory Controller verifies that the entire Flash memory space was properly erased, security will be released. If the erase verify is not successful, the Unsecure Flash operation sets MGSTAT1 and terminates without changing the security

Table A-14. Pseudo Stop and Full Stop Current

Conditions are shown in Table A-4 , junction temperature, unless otherwise noted							
Num	C	Rating	Symbol	Min	Typ	Max	Unit
Pseudo stop current (API, RTI, and COP disabled) PLL off, LCP mode							
10	C	−40°C	I _{DDPS}	—	175	—	μA
	P	27°C		—	185	255	
	C	70°C		—	255	—	
	C	85°C		—	305	—	
	C	105°C		—	455	—	
	P	110°C		—	505	2155	
	P	130°C		—	805	3655	
	P	150°C		—	1555	7655	
Pseudo stop current (API, RTI, and COP enabled) PLL off, LCP mode							
11	C	27°C	I _{DDPS}	—	205	—	μA
	C	70°C		—	275	—	
	C	85°C		—	325	—	
	C	105°C		—	475	—	
	C	125°C		—	810	—	
	C	150°C		—	1575	—	
Stop Current							
12	C	−40°C	I _{DDS}	—	20	—	μA
	P	27°C		—	30	100	
	C	70°C		—	100	—	
	C	85°C		—	150	—	
	C	105°C		—	300	—	
	P	110°C		—	350	2000	
	C	125°C		—	550	—	
	P	130°C		—	650	3500	
P	150°C	—	1400	7500			
Stop Current (API active)							
13	T	−40°C	I _{DDS}	—	32	—	μA
	T	27°C		—	42	—	
	T	85°C		—	162	—	
	T	110°C		—	362	—	
	T	130°C		—	662	—	
Stop Current (one ATD active)							
14	T	27°C	I _{DDS}	—	300	—	μA
	T	85°C		—	420	—	
	T	125°C		—	820	—	

