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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	HCS12X
Core Size	16-Bit
Speed	50MHz
Connectivity	CANbus, EBI/EMI, I²C, IrDA, SCI, SPI
Peripherals	LVD, POR, PWM, WDT
Number of I/O	119
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.72V ~ 5.5V
Data Converters	A/D 24x12b
Oscillator Type	External
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mc9s12xeq512mag

  - No external components required
  - Configurable option to spread spectrum for reduced EMC radiation (frequency modulation)
- CRG (clock and reset generation)
  - COP watchdog
  - Real time interrupt
  - Clock monitor
  - Fast wake up from STOP in self clock mode
- Memory Options
  - 128K, 256k, 384K, 512K, 768K and 1M byte Flash
  - 2K, 4K byte emulated EEPROM
  - 12K, 16K, 24K, 32K, 48K and 64K Byte RAM
- Flash General Features
  - 64 data bits plus 8 syndrome ECC (Error Correction Code) bits allow single bit failure correction and double fault detection
  - Erase sector size 1024 bytes
  - Automated program and erase algorithm
- D-Flash Features
  - Up to 32 Kbytes of D-Flash memory with 256 byte sectors for user access.
  - Dedicated commands to control access to the D-Flash memory over EEE operation.
  - Single bit fault correction and double bit fault detection within a word during read operations.
  - Automated program and erase algorithm with verify and generation of ECC parity bits.
  - Fast sector erase and word program operation.
  - Ability to program up to four words in a burst sequence
- Emulated EEPROM Features
  - Automatic EEE file handling using an internal Memory Controller.
  - Automatic transfer of valid EEE data from D-Flash memory to buffer RAM on reset.
  - Ability to monitor the number of outstanding EEE related buffer RAM words left to be programmed into D-Flash memory.
  - Ability to disable EEE operation and allow priority access to the D-Flash memory.
  - Ability to cancel all pending EEE operations and allow priority access to the D-Flash memory.
- Two 16-channel, 12-bit Analog-to-Digital Converters
  - 8/10/12 Bit resolution
  - 3µs, 10-bit single conversion time
  - Left/right, signed/unsigned result data
  - External and internal conversion trigger capability
  - Internal oscillator for conversion in Stop modes
  - Wake from low power modes on analog comparison > or <= match
- Five MSCAN (1 M bit per second, CAN 2.0 A, B software compatible modules)
  - Five receive and three transmit buffers

Table 1-5. Derivative Dependent Flash Block Mapping (continued)

Device	0x70_0000	0x74_0000	0x78_0000	0x7A_0000	0x7C_0000	0x7E_0000
9S12XET256 9S12XEA256 (1)	—	—	B1S	—	—	B0(128K)
9S12XEG128 9S12XEA128[1]	—	—	B1S (64K)	—	—	B0 (64K)

1. The 9S12XEA devices are special bondouts for access to extra ADC channels in 80QFP. Available in 80QFP only. WARNING: NOT PIN-COMPATIBLE WITH REST OF FAMILY.

Block B1 is divided into two 128K blocks. The XGATE is always mapped to block B1S.

On the 9S12XEG128 the flash is divided into two 64K blocks B0 and B1S, the B1S range extending from 0x78_0000 to 0x78_FFFF, the B0 range extending from 0x7F_0000 to 0x7F_FFFF.

The block B0 is a reduced size 128K block on the 256K derivative. On the larger derivatives B0 is a 256K block. The block B0 is a reduced size 64K block on the 128K derivative.

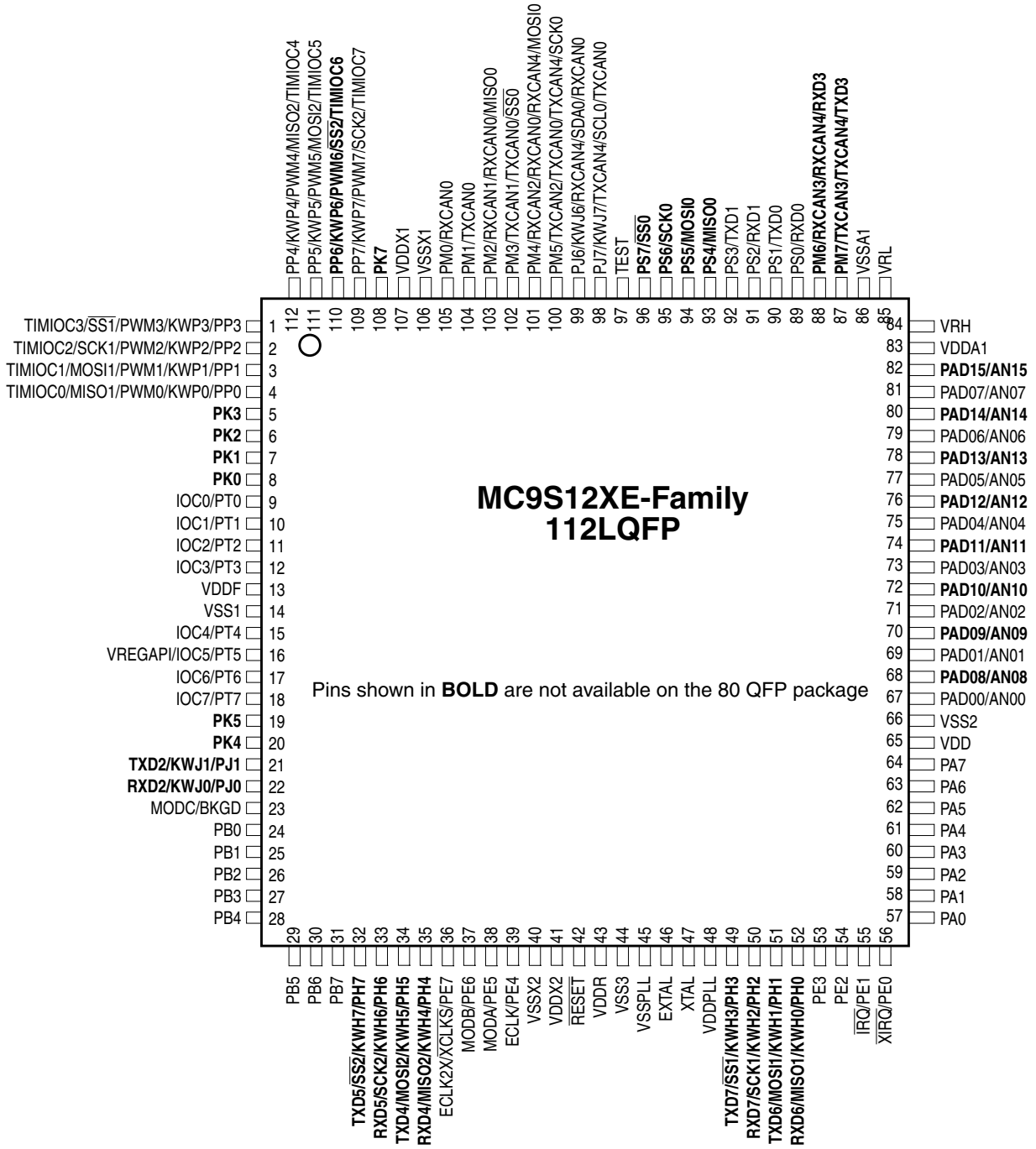


Figure 1-6. MC9S12XE-Family Pin Assignments 112-pin LQFP Package

2.3.3 Port A Data Register (PORTA)

Address 0x0000 (PRR) Access: User read/write(1)

	7	6	5	4	3	2	1	0
R W	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0
Altern. Function	ADDR15 mux IVD15	ADDR14 mux IVD14	ADDR13 mux IVD13	ADDR12 mux IVD12	ADDR11 mux IVD11	ADDR10 mux IVD10	ADDR9 mux IVD9	ADDR8 mux IVD8
Reset	0	0	0	0	0	0	0	0

Figure 2-1. Port A Data Register (PORTA)

1. Read: Anytime. In emulation modes, read operations will return the data from the external bus, in all other modes the data source is depending on the data direction value.
   Write: Anytime. In emulation modes, write operations will also be directed to the external bus.

Table 2-4. PORTA Register Field Descriptions

Field	Description
7-0 PA	**Port A general purpose input/output data**—Data Register Port A pins 7 through 0 are associated with address outputs ADDR[15:8] respectively in expanded modes. In emulation modes the address is multiplexed with IVD[15:8]. When not used with the alternative function, these pins can be used as general purpose I/O. If the associated data direction bits of these pins are set to 1, a read returns the value of the port register, otherwise the buffered pin input state is read.

2.3.4 Port B Data Register (PORTB)

Address 0x0001 (PRR) Access: User read/write(1)

	7	6	5	4	3	2	1	0
R W	PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0
Altern. Function	ADDR7 mux IVD7	ADDR6 mux IVD6	ADDR5 mux IVD5	ADDR4 mux IVD4	ADDR3 mux IVD3	ADDR2 mux IVD2	ADDR1 mux IVD1	ADDR0 mux IVD0 or $\overline{\text{UDS}}$
Reset	0	0	0	0	0	0	0	0

Figure 2-2. Port B Data Register (PORTB)

1. Read: Anytime. In emulation modes, read operations will return the data from the external bus, in all other modes the data source is depending on the data direction value.
   Write: Anytime. In emulation modes, write operations will also be directed to the external bus.

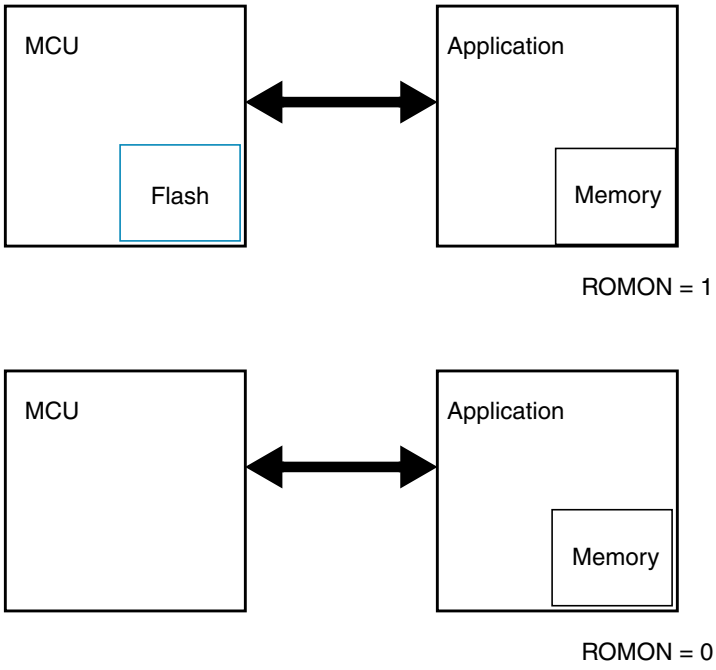


Figure 3-26. ROM in Normal Expanded Mode

Table 4-9. MPUDESC1 Field Descriptions

Field	Description
7–0 LOW_ADDR[18:11]	**Memory range lower boundary address bits** — The LOW_ADDR[18:11] bits represent bits [18:11] of the global memory address that is used as the lower boundary for the described memory range.

4.3.1.8 MPU Descriptor Register 2 (MPUDESC2)

Address: Module Base + 0x0008

	7	6	5	4	3	2	1	0
R W	LOW_ADDR[10:3]							
Reset	0	0	0	0	0	0	0	0

Figure 4-10. MPU Descriptor Register 2 (MPUDESC2)

Read: Anytime

Write: Anytime

Table 4-10. MPUDESC2 Field Descriptions

Field	Description
7–0 LOW_ADDR[10:3]	**Memory range lower boundary address bits** — The LOW_ADDR[10:3] bits represent bits [10:3] of the global memory address that is used as the lower boundary for the described memory range.

4.3.1.9 MPU Descriptor Register 3 (MPUDESC3)

Address: Module Base + 0x0009

	7	6	5	4	3	2	1	0
R	WP	NEX	0	0	HIGH_ADDR[22:19]			
W								
Reset	0	0	0	0	1	1	1	1

Figure 4-11. MPU Descriptor Register 3 (MPUDESC3)

Read: Anytime

Write: Anytime

Table 4-11. MPUDESC3 Field Descriptions

Field	Description
7 WP	**Write-Protect bit** — The WP bit causes the described memory range to be treated as write-protected. If this bit is set every attempt to write in the described memory range causes an access violation.

BCS

Branch if Carry Set (Same as BLO)

BCS

Operation

If C = 1, then PC + $0002 + (REL9 << 1) ⇒ PC

Tests the Carry flag and branches if C = 1.

CCR Effects

N	Z	V	C
—	—	—	—

N: Not affected.
Z: Not affected.
V: Not affected.
C: Not affected.

Code and CPU Cycles

Source Form	Address Mode	Machine Code								Cycles
BCS REL9	REL9	0	0	1	0	0	0	1	REL9	PP/P

BFFO Bit Field Find First One BFFO

Operation

FirstOne(RS) ⇒ RD;

Searches the first “1” in register RS (from MSB to LSB) and writes the bit position into the destination register RD. The upper bits of RD are cleared. In case the content of RS is equal to $0000, RD will be cleared and the carry flag will be set. This is used to distinguish a “1” in position 0 versus no “1” in the whole RS register at all.

CCR Effects

N	Z	V	C
0	Δ	0	Δ

N: 0; cleared.

Z: Set if the result is $0000; cleared otherwise.

V: 0; cleared.

C: Set if RS = $0000(1); cleared otherwise.

1. Before executing the instruction

Code and CPU Cycles

Source Form	Address Mode	Machine Code												Cycles
BFFO RD, RS	DYA	0	0	0	0	1	RD	RS	1	0	0	0	0	P

BGT Branch if Greater than Zero BGT

Operation

If Z | (N ^ V) = 0, then PC + $0002 + (REL9 << 1) ⇒ PC

Branch instruction to compare signed numbers.

Branch if RS1 > RS2:

```
SUB     R0,RS1,RS2
BGT     REL9
```

CCR Effects

N	Z	V	C
—	—	—	—

N: Not affected.
Z: Not affected.
V: Not affected.
C: Not affected.

Code and CPU Cycles

Source Form	Address Mode	Machine Code								Cycles
BGT REL9	REL9	0	0	1	1	1	0	0	REL9	PP/P

BVS Branch if Overflow Set BVS

Operation

If V = 1, then PC + $0002 + (REL9 << 1) ⇒ PC

Tests the Overflow flag and branches if V = 1.

CCR Effects

N	Z	V	C
—	—	—	—

N: Not affected.
Z: Not affected.
V: Not affected.
C: Not affected.

Code and CPU Cycles

Source Form	Address Mode	Machine Code								Cycles
BVS REL9	REL9	0	0	1	0	1	1	1	REL9	PP/P

Table 15-7. IIC Divider and Hold Values (Sheet 5 of 6)

IBC[7:0] (hex)	SCL Divider (clocks)	SDA Hold (clocks)	SCL Hold (start)	SCL Hold (stop)
82	88	32	32	52
83	96	32	36	56
84	104	36	40	60
85	112	36	44	64
86	128	40	52	72
87	152	40	64	84
88	112	28	40	60
89	128	28	48	68
8A	144	36	56	76
8B	160	36	64	84
8C	176	44	72	92
8D	192	44	80	100
8E	224	52	96	116
8F	272	52	120	140
90	192	36	72	100
91	224	36	88	116
92	256	52	104	132
93	288	52	120	148
94	320	68	136	164
95	352	68	152	180
96	416	84	184	212
97	512	84	232	260
98	320	36	152	164
99	384	36	184	196
9A	448	68	216	228
9B	512	68	248	260
9C	576	100	280	292
9D	640	100	312	324
9E	768	132	376	388
9F	960	132	472	484
A0	640	68	312	324
A1	768	68	376	388
A2	896	132	440	452
A3	1024	132	504	516
A4	1152	196	568	580
A5	1280	196	632	644
A6	1536	260	760	772
A7	1920	260	952	964
A8	1280	132	632	644
A9	1536	132	760	772
AA	1792	260	888	900
AB	2048	260	1016	1028

16.4.4.2 Special System Operating Modes

The MSCAN module behaves as described within this specification in all special system operating modes. Write restrictions which exist on specific registers in normal modes are lifted for test purposes in special modes.

16.4.4.3 Emulation Modes

In all emulation modes, the MSCAN module behaves just like in normal system operating modes as described within this specification.

16.4.4.4 Listen-Only Mode

In an optional CAN bus monitoring mode (listen-only), the CAN node is able to receive valid data frames and valid remote frames, but it sends only "recessive" bits on the CAN bus. In addition, it cannot start a transmission.

If the MAC sub-layer is required to send a "dominant" bit (ACK bit, overload flag, or active error flag), the bit is rerouted internally so that the MAC sub-layer monitors this "dominant" bit, although the CAN bus may remain in recessive state externally.

16.4.4.5 MSCAN Initialization Mode

The MSCAN enters initialization mode when it is enabled (CANE=1).

When entering initialization mode during operation, any on-going transmission or reception is immediately aborted and synchronization to the CAN bus is lost, potentially causing CAN protocol violations. To protect the CAN bus system from fatal consequences of violations, the MSCAN immediately drives TXCAN into a recessive state.

NOTE

The user is responsible for ensuring that the MSCAN is not active when initialization mode is entered. The recommended procedure is to bring the MSCAN into sleep mode (SLPRQ = 1 and SLPAK = 1) before setting the INITRQ bit in the CANCTL0 register. Otherwise, the abort of an on-going message can cause an error condition and can impact other CAN bus devices.

In initialization mode, the MSCAN is stopped. However, interface registers remain accessible. This mode is used to reset the CANCTL0, CANRFLG, CANRIER, CANTFLG, CANTIER, CANTARQ, CANTAAK, and CANTBSEL registers to their default values. In addition, the MSCAN enables the configuration of the CANBTR0, CANBTR1 bit timing registers; CANIDAC; and the CANIDAR, CANIDMR message filters. See Section 16.3.2.1, "MSCAN Control Register 0 (CANCTL0)," for a detailed description of the initialization mode.

The API Trimming bits APITR[5:0] must be set so the minimum period equals 0.2 ms if stable frequency is desired.

See Table 23-7 for the trimming effect of APITR.

NOTE

The first period after enabling the counter by APIFE might be reduced by API start up delay t_{sdel}. The API internal RC oscillator clock is not available if VREG_3V3 is in Shutdown Mode.

It is possible to generate with the API a waveform at an external pin by enabling the API by setting APIFE and enabling the external access with setting APIEA. By setting APIES the waveform can be selected. If APIES is set, then at the external pin a clock is visible with 2 times the selected API Period (Table 23-9). If APIES is not set, then at the external pin will be a high pulse at the end of every selected period with the size of half of the min period (Table 23-9). See device level specification for connectivity.

23.4.9 Resets

This section describes how VREG_3V3 controls the reset of the MCU.The reset values of registers and signals are provided in Section 23.3, “Memory Map and Register Definition”. Possible reset sources are listed in Table 23-12.

Table 23-12. Reset Sources

Reset Source	Local Enable
Power-on reset	Always active
Low-voltage reset	Available only in Full Performance Mode

23.4.10 Description of Reset Operation

23.4.10.1 Power-On Reset (POR)

During chip power-up the digital core may not work if its supply voltage V_{DD} is below the POR deassertion level (V_{PORD}). Therefore, signal POR, which forces the other blocks of the device into reset, is kept high until V_{DD} exceeds V_{PORD}. The MCU will run the start-up sequence after POR deassertion. The power-on reset is active in all operation modes of VREG_3V3.

23.4.10.2 Low-Voltage Reset (LVR)

For details on low-voltage reset, see Section 23.4.5, “Low-Voltage Reset (LVR)”.

23.4.11 Interrupts

This section describes all interrupts originated by VREG_3V3.

The interrupt vectors requested by VREG_3V3 are listed in Table 23-13. Vector addresses and interrupt priorities are defined at MCU level.

Table 25-64. Full Partition D-Flash Command Error Handling

Register	Error Bit	Error Condition
FSTAT	ACCERR	Set if CCOBIX[2:0] != 010 at command launch
		Set if a Load Data Field command sequence is currently active
		Set if command not available in current mode (see Table 25-30)
		Set if an invalid DFPART or ERPART selection is supplied
	FPVIOL	None
	MGSTAT1	Set if any errors have been encountered during the read
	MGSTAT0	Set if any non-correctable errors have been encountered during the read
FERSTAT	EPVIOLIF	None

25.4.2.16 Erase Verify D-Flash Section Command

The Erase Verify D-Flash Section command will verify that a section of code in the D-Flash user partition is erased. The Erase Verify D-Flash Section command defines the starting point of the data to be verified and the number of words.

Table 25-65. Erase Verify D-Flash Section Command FCCOB Requirements

CCOBIX[2:0]	FCCOB Parameters	
000	0x10	Global address [22:16] to identify the D-Flash block
001	Global address [15:0] of the first word to be verified	
010	Number of words to be verified	

Upon clearing CCIF to launch the Erase Verify D-Flash Section command, the Memory Controller will verify the selected section of D-Flash memory is erased. The CCIF flag will set after the Erase Verify D-Flash Section operation has completed.

Table 27-16. FERCNFG Field Descriptions (continued)

Field	Description
3 ERSVIE1	**EEE Error Type 1 Interrupt Enable** — The ERSVIE1 bit controls interrupt generation when a change state error is detected during an EEE operation. 0 ERSVIF1 interrupt disabled 1 An interrupt will be requested whenever the ERSVIF1 flag is set (see Section 27.3.2.8)
2 ERSVIE0	**EEE Error Type 0 Interrupt Enable** — The ERSVIE0 bit controls interrupt generation when a sector format error is detected during an EEE operation. 0 ERSVIF0 interrupt disabled 1 An interrupt will be requested whenever the ERSVIF0 flag is set (see Section 27.3.2.8)
1 DFDIE	**Double Bit Fault Detect Interrupt Enable** — The DFDIE bit controls interrupt generation when a double bit fault is detected during a Flash block read operation. 0 DFDIF interrupt disabled 1 An interrupt will be requested whenever the DFDIF flag is set (see Section 27.3.2.8)
0 SFDIE	**Single Bit Fault Detect Interrupt Enable** — The SFDIE bit controls interrupt generation when a single bit fault is detected during a Flash block read operation. 0 SFDIF interrupt disabled whenever the SFDIF flag is set (see Section 27.3.2.8) 1 An interrupt will be requested whenever the SFDIF flag is set (see Section 27.3.2.8)

27.3.2.7 Flash Status Register (FSTAT)

The FSTAT register reports the operational status of the Flash module.

Offset Module Base + 0x0006

	7	6	5	4	3	2	1	0
R	CCIF	0	ACCERR	FPVIOL	MGBUSY	RSVD	MGSTAT[1:0]	
W								
Reset	1	0	0	0	0	0	0(1)	0[1]

= Unimplemented or Reserved

Figure 27-11. Flash Status Register (FSTAT)

1. Reset value can deviate from the value shown if a double bit fault is detected during the reset sequence (see Section 27.6).

CCIF, ACCERR, and FPVIOL bits are readable and writable, MGBUSY and MGSTAT bits are readable but not writable, while remaining bits read 0 and are not writable.

Table 27-64. Full Partition D-Flash Command Error Handling

Register	Error Bit	Error Condition
FSTAT	ACCERR	Set if CCOBIX[2:0] != 010 at command launch
		Set if a Load Data Field command sequence is currently active
		Set if command not available in current mode (see Table 27-30)
		Set if an invalid DFPART or ERPART selection is supplied
	FPVIOL	None
	MGSTAT1	Set if any errors have been encountered during the read
	MGSTAT0	Set if any non-correctable errors have been encountered during the read
FERSTAT	EPVIOLIF	None

27.4.2.16 Erase Verify D-Flash Section Command

The Erase Verify D-Flash Section command will verify that a section of code in the D-Flash user partition is erased. The Erase Verify D-Flash Section command defines the starting point of the data to be verified and the number of words.

Table 27-65. Erase Verify D-Flash Section Command FCCOB Requirements

CCOBIX[2:0]	FCCOB Parameters	
000	0x10	Global address [22:16] to identify the D-Flash block
001	Global address [15:0] of the first word to be verified	
010	Number of words to be verified	

Upon clearing CCIF to launch the Erase Verify D-Flash Section command, the Memory Controller will verify the selected section of D-Flash memory is erased. The CCIF flag will set after the Erase Verify D-Flash Section operation has completed.

Table 28-16. FERCNFG Field Descriptions (continued)

Field	Description
3 ERSVIE1	**EEE Error Type 1 Interrupt Enable** — The ERSVIE1 bit controls interrupt generation when a change state error is detected during an EEE operation. 0 ERSVIF1 interrupt disabled 1 An interrupt will be requested whenever the ERSVIF1 flag is set (see Section 28.3.2.8)
2 ERSVIE0	**EEE Error Type 0 Interrupt Enable** — The ERSVIE0 bit controls interrupt generation when a sector format error is detected during an EEE operation. 0 ERSVIF0 interrupt disabled 1 An interrupt will be requested whenever the ERSVIF0 flag is set (see Section 28.3.2.8)
1 DFDIE	**Double Bit Fault Detect Interrupt Enable** — The DFDIE bit controls interrupt generation when a double bit fault is detected during a Flash block read operation. 0 DFDIF interrupt disabled 1 An interrupt will be requested whenever the DFDIF flag is set (see Section 28.3.2.8)
0 SFDIE	**Single Bit Fault Detect Interrupt Enable** — The SFDIE bit controls interrupt generation when a single bit fault is detected during a Flash block read operation. 0 SFDIF interrupt disabled whenever the SFDIF flag is set (see Section 28.3.2.8) 1 An interrupt will be requested whenever the SFDIF flag is set (see Section 28.3.2.8)

28.3.2.7 Flash Status Register (FSTAT)

The FSTAT register reports the operational status of the Flash module.

Offset Module Base + 0x0006

	7	6	5	4	3	2	1	0
R	CCIF	0	ACCERR	FPVIOL	MGBUSY	RSVD	MGSTAT[1:0]	
W								
Reset	1	0	0	0	0	0	0(1)	0[1]

= Unimplemented or Reserved

Figure 28-11. Flash Status Register (FSTAT)

1. Reset value can deviate from the value shown if a double bit fault is detected during the reset sequence (see Section 28.6).

CCIF, ACCERR, and FPVIOL bits are readable and writable, MGBUSY and MGSTAT bits are readable but not writable, while remaining bits read 0 and are not writable.

(0x7F_FF0F). The Verify Backdoor Access Key command sequence has no effect on the program and erase protections defined in the Flash protection register, FPROT.

28.5.2 Unsecuring the MCU in Special Single Chip Mode using BDM

The MCU can be unsecured in special single chip mode by erasing the P-Flash and D-Flash memory by one of the following methods:

- Reset the MCU into special single chip mode, delay while the erase test is performed by the BDM, send BDM commands to disable protection in the P-Flash and D-Flash memory, and execute the Erase All Blocks command write sequence to erase the P-Flash and D-Flash memory.
- Reset the MCU into special expanded wide mode, disable protection in the P-Flash and D-Flash memory and run code from external memory to execute the Erase All Blocks command write sequence to erase the P-Flash and D-Flash memory.

After the CCIF flag sets to indicate that the Erase All Blocks operation has completed, reset the MCU into special single chip mode. The BDM will execute the Erase Verify All Blocks command write sequence to verify that the P-Flash and D-Flash memory is erased. If the P-Flash and D-Flash memory are verified as erased the MCU will be unsecured. All BDM commands will be enabled and the Flash security byte may be programmed to the unsecure state by the following method:

- Send BDM commands to execute a ‘Program P-Flash’ command sequence to program the Flash security byte to the unsecured state and reset the MCU.

28.5.3 Mode and Security Effects on Flash Command Availability

The availability of Flash module commands depends on the MCU operating mode and security state as shown in Table 28-30.

28.6 Initialization

On each system reset the Flash module executes a reset sequence which establishes initial values for the Flash Block Configuration Parameters, the FPROT and DFPROT protection registers, and the FOPT and FSEC registers. The Flash module reverts to built-in default values that leave the module in a fully protected and secured state if errors are encountered during execution of the reset sequence. If a double bit fault is detected during the reset sequence, both MGSTAT bits in the FSTAT register will be set. The ACCERR bit in the FSTAT register is set if errors are encountered while initializing the EEE buffer ram during the reset sequence.

CCIF remains clear throughout the reset sequence. The Flash module holds off all CPU access for the initial portion of the reset sequence. While Flash reads are possible when the hold is removed, writes to the FCCOBIX, FCCOBHI, and FCCOBLO registers are ignored to prevent command activity while the Memory Controller remains busy. Completion of the reset sequence is marked by setting CCIF high which enables writes to the FCCOBIX, FCCOBHI, and FCCOBLO registers to launch any available Flash command.

If a reset occurs while any Flash command is in progress, that command will be immediately aborted. The state of the word being programmed or the sector/block being erased is not guaranteed.

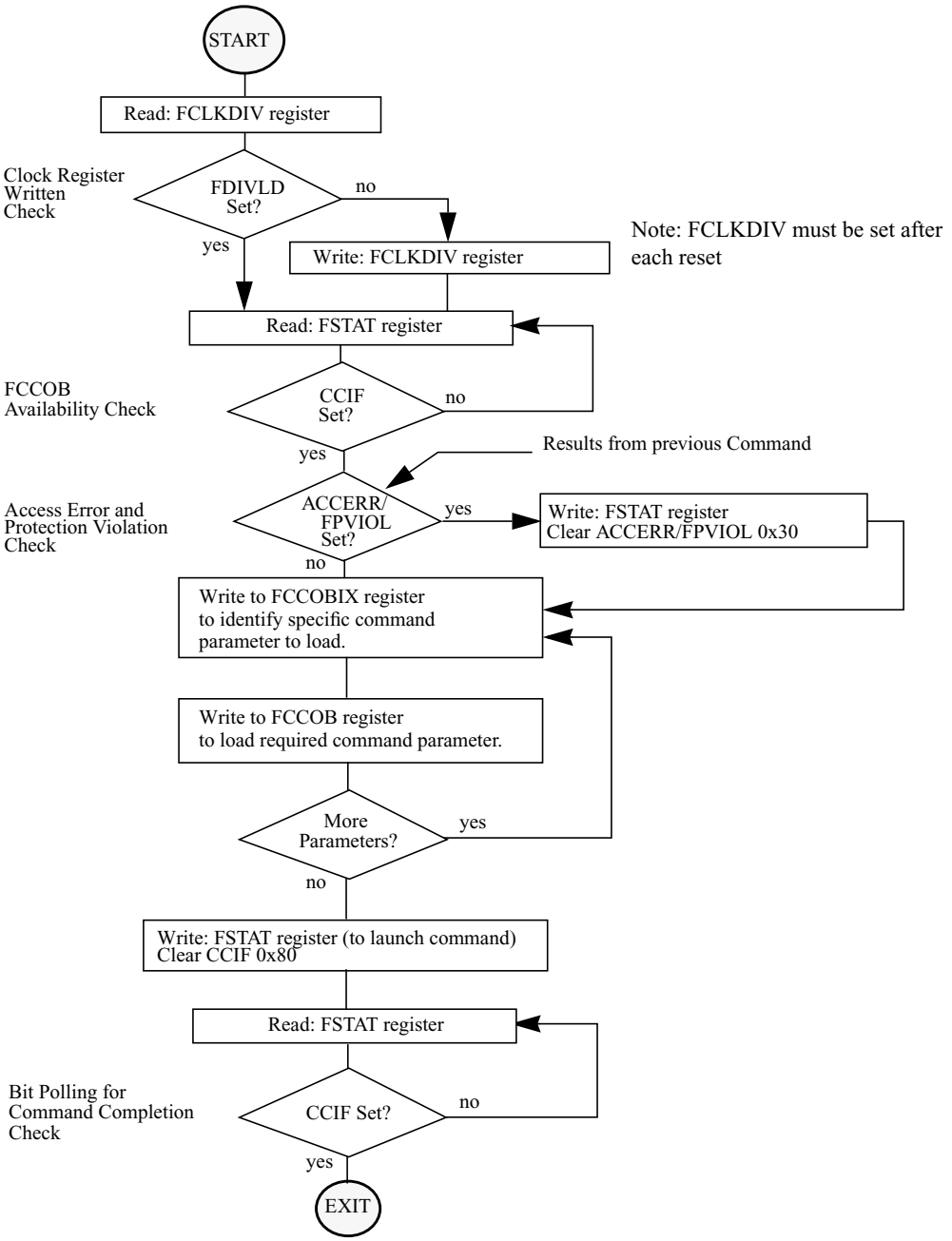
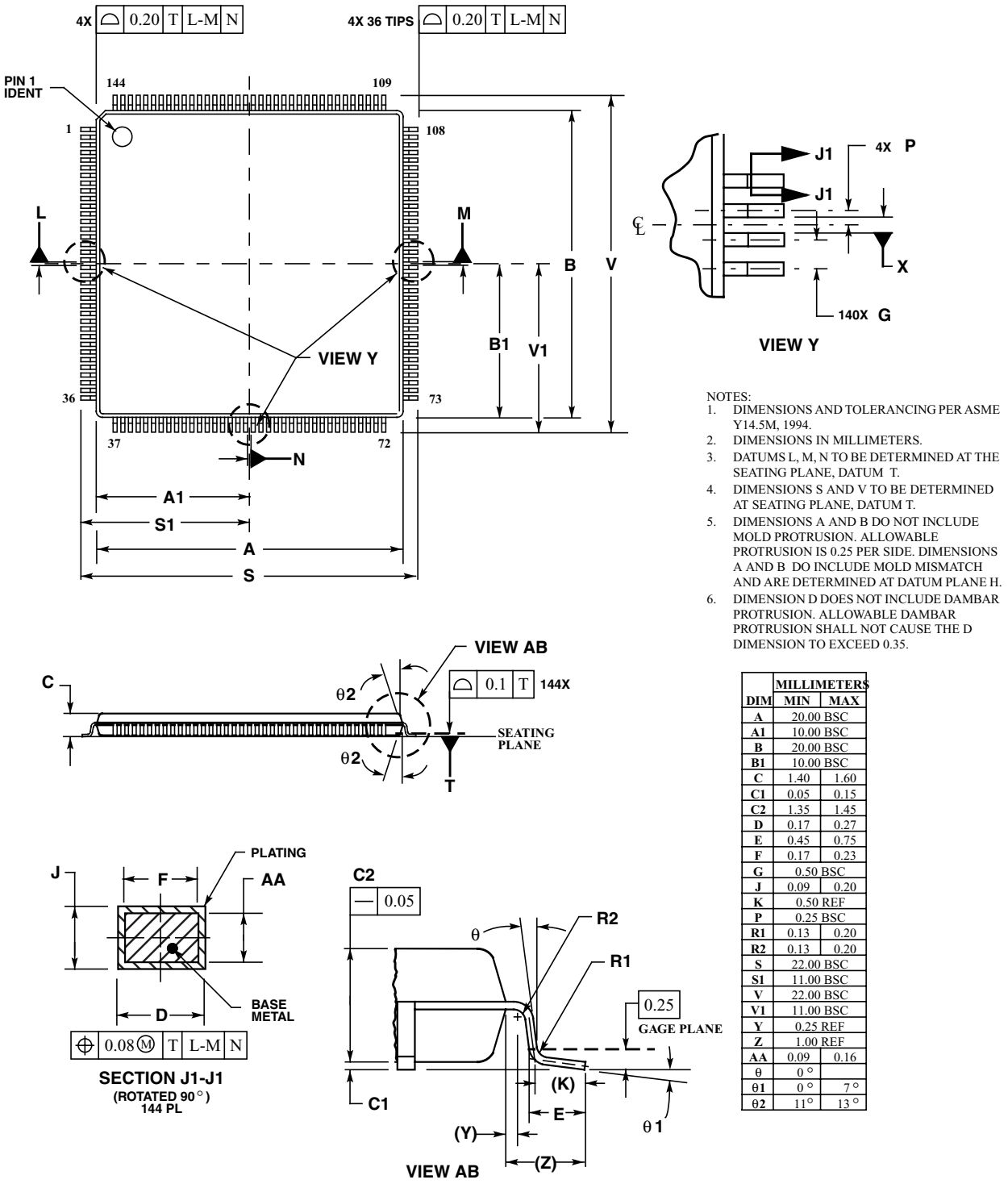


Figure 29-26. Generic Flash Command Write Sequence Flowchart



DIM	MILLIMETERS MIN	MAX
A	20.00 BSC	
A1	10.00 BSC	
B	20.00 BSC	
B1	10.00 BSC	
C	1.40	1.60
C1	0.05	0.15
C2	1.35	1.45
D	0.17	0.27
E	0.45	0.75
F	0.17	0.23
G	0.50 BSC	
J	0.09	0.20
K	0.50 REF	
P	0.25 BSC	
R1	0.13	0.20
R2	0.13	0.20
S	22.00 BSC	
S1	11.00 BSC	
V	22.00 BSC	
V1	11.00 BSC	
Y	0.25 REF	
Z	1.00 REF	
AA	0.09	0.16
θ	0°	
θ1	0°	7°
θ2	11°	13°

Figure B-2. 144-Pin LQFP Mechanical Dimensions (Case No. 918-03)