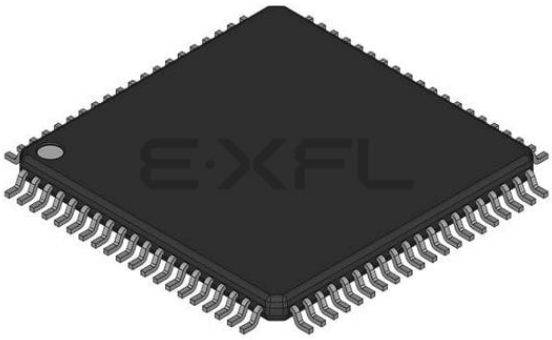

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Details	
Product Status	Obsolete
Core Processor	HCS12X
Core Size	16-Bit
Speed	50MHz
Connectivity	CANbus, EBI/EMI, I²C, IrDA, SCI, SPI
Peripherals	LVD, POR, PWM, WDT
Number of I/O	59
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.72V ~ 5.5V
Data Converters	A/D 12x12b
Oscillator Type	External
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	80-QFP
Supplier Device Package	80-QFP (14x14)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mc9s12xeq512vaa

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
A	N.C.	N.C.	PP7	PM0	PM1	PF5	PF3	PF1	PJ6	PS6	PS5	PS3	PM6	PAD19	N.C.	N.C.
B	N.C.	PP2	PP6	PF7	PF6	PF4	PF2	PF0	TEST	PS4	PS1	PAD23	PAD21	PAD18	PAD31	N.C.
C	PJ2	PP1	PP4	PP5	PK7	PM2	PM4	PJ5	PS7	PS2	PM7	PAD20	VRL	PAD16	PAD07	PAD14
D	PK1	PJ3	PP0	PP3	VDDX	PM3	PM5	PJ4	PJ7	VDDX	PS0	PAD22	VRH	PAD17	PAD30	PAD29
E	PK0	PK3	PK2	PK6									VSSA	PAD15	PAD06	PAD28
F	PR1	PR0	PT0	VDDX									VDDA	PAD05	PAD13	PAD27
G	PT2	PT3	PR2	PT1			VSSX	VSSX	VSSX	VSSX			VDDA	PAD12	PAD04	PAD11
H	PR3	PR4	PT4	VDDF			VSSX	VSSX	VSSX	VSSX			VSSA	PAD26	PAD03	PAD10
J	PT5	PR5	PT6	VSS1			VSSX	VSSX	VSSX	VSSX			VSS2	PAD09	PAD25	PAD02
K	PR6	PT7	PK4	PR7			VSSX	VSSX	VSSX	VSSX			VDD	PD7	PAD24	PAD01
L	PK5	PJ1	BKGD	VDDX									VDDX	PD4	PAD00	PAD08
M	PJ0	PC0	PB1	PC1									PA6	PA2	PD5	PD6
N	PC2	PC3	PB2	PC7	PL1	PE6	VDDX	VDDR	VSS3	PH3	PH1	VDDX	PE1	PA1	PA5	PA7
P	PB0	PB3	PB4	PC4	PL2	PL0	PE4	RESET	PL7	PL6	PH0	PE2	PE0	PA0	PA3	PA4
R	N.C.	PB5	PB6	PB7	PC6	PH6	PH4	PE5	VSS PLL	VDD PLL	PH2	PL4	PD1	PD3	PE3	N.C.
T	N.C.	N.C.	PC5	PL3	PH7	PH5	PE7	VSS PLL	EXTAL	XTAL	VDD PLL	PL5	PD0	PD2	N.C.	N.C.

Figure 1-4. - Pin Assignments, 208 MAPBGA Package

8.3.2.2 Debug Status Register (DBGSR)

Address: 0x0021

	7	6	5	4	3	2	1	0
R	TBF	EXTF	0	0	0	SSF2	SSF1	SSF0
W								
Reset	—	0	0	0	0	0	0	0
POR	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 8-4. Debug Status Register (DBGSR)

Read: Anytime

Write: Never

Table 8-8. DBGSR Field Descriptions

Field	Description
7 TBF	**Trace Buffer Full** — The TBF bit indicates that the trace buffer has stored 64 or more lines of data since it was last armed. If this bit is set, then all 64 lines will be valid data, regardless of the value of DBGCNT bits CNT[6:0]. The TBF bit is cleared when ARM in DBGC1 is written to a one. The TBF is cleared by the power on reset initialization. Other system generated resets have no affect on this bit.
6 EXTF	**External Tag Hit Flag** — The EXTF bit indicates if a tag hit condition from an external $\overline{\text{TAGHI}}$/$\overline{\text{TAGLO}}$ tag was met since arming. This bit is cleared when ARM in DBGC1 is written to a one. 0 External tag hit has not occurred 1 External tag hit has occurred
2–0 SSF[2:0]	**State Sequencer Flag Bits** — The SSF bits indicate in which state the State Sequencer is currently in. During a debug session on each transition to a new state these bits are updated. If the debug session is ended by software clearing the ARM bit, then these bits retain their value to reflect the last state of the state sequencer before disarming. If a debug session is ended by an internal trigger, then the state sequencer returns to state0 and these bits are cleared to indicate that state0 was entered during the session. On arming the module the state sequencer enters state1 and these bits are forced to SSF[2:0] = 001. See Table 8-9**.**

Table 8-9. SSF[2:0] — State Sequence Flag Bit Encoding

SSF[2:0]	Current State
000	State0 (disarmed)
001	State1
010	State2
011	State3
100	Final State
101,110,111	Reserved

Table 8-46. CXINF Field Descriptions (continued)

Field	Description
6 CSZ	**Access Type Indicator** — This bit indicates if the access was a byte or word size access.This bit only contains valid information when tracing CPU12X activity in Detail Mode. 0 Word Access 1 Byte Access
5 CRW	**Read Write Indicator** — This bit indicates if the corresponding stored address corresponds to a read or write access. This bit only contains valid information when tracing CPU12X activity in Detail Mode. 0 Write Access 1 Read Access
4 COCF	**CPU12X Opcode Fetch Indicator** — This bit indicates if the stored address corresponds to an opcode fetch cycle. This bit only contains valid information when tracing the XGATE accesses in Detail Mode. 0 Stored information does not correspond to opcode fetch cycle 1 Stored information corresponds to opcode fetch cycle
3 XACK	**XGATE Access Indicator** — This bit indicates if the stored XGATE address corresponds to a free cycle. This bit only contains valid information when tracing the CPU12X accesses in Detail Mode. 0 Stored information corresponds to free cycle 1 Stored information does not correspond to free cycle
2 XSZ	**Access Type Indicator** — This bit indicates if the access was a byte or word size access. This bit only contains valid information when tracing XGATE activity in Detail Mode. 0 Word Access 1 Byte Access
1 XRW	**Read Write Indicator** — This bit indicates if the corresponding stored address corresponds to a read or write access. This bit only contains valid information when tracing XGATE activity in Detail Mode. 0 Write Access 1 Read Access
0 XOCF	**XGATE Opcode Fetch Indicator** — This bit indicates if the stored address corresponds to an opcode fetch cycle.This bit only contains valid information when tracing the CPU12X accesses in Detail Mode. 0 Stored information does not correspond to opcode fetch cycle 1 Stored information corresponds to opcode fetch cycle

8.4.5.4 Reading Data from Trace Buffer

The data stored in the Trace Buffer can be read using either the background debug module (BDM) module, the XGATE or the CPU12X provided the S12XDBG module is not armed, is configured for tracing and the system not secured. When the ARM bit is written to 1 the trace buffer is locked to prevent reading. The trace buffer can only be unlocked for reading by an aligned word write to DBGTB when the module is disarmed.

The Trace Buffer can only be read through the DBGTB register using aligned word reads, any byte or misaligned reads return 0 and do not cause the trace buffer pointer to increment to the next trace buffer address. The Trace Buffer data is read out first-in first-out. By reading CNT in DBGCNT the number of valid 64-bit lines can be determined. DBGCNT will not decrement as data is read.

Whilst reading an internal pointer is used to determine the next line to be read. After a tracing session, the pointer points to the oldest data entry, thus if no overflow has occurred, the pointer points to line0, otherwise it points to the line with the oldest entry. The pointer is initialized by each aligned write to DBGTBH to point to the oldest data again. This enables an interrupted trace buffer read sequence to be easily restarted from the oldest data entry.

TST — Test Register — TST

Operation

RS – 0 ⇒ NONE (translates to SUB R0, RS, R0)

Subtracts zero from the content of register RS using binary subtraction and discards the result.

CCR Effects

N	Z	V	C
Δ	Δ	Δ	Δ

N: Set if bit 15 of the result is set; cleared otherwise.

Z: Set if the result is $0000; cleared otherwise.

V: Set if a two´s complement overflow resulted from the operation; cleared otherwise.
RS[15] & $\overline{\text{result[15]}}$

C: Set if there is a carry from the bit 15 of the result; cleared otherwise.
$\overline{\text{RS1[15]}}$ & result[15]

Code and CPU Cycles

Source Form	Address Mode	Machine Code													Cycles
TST RS	TRI	0	0	0	1	1	0	0	0	RS1	0	0	0	0	0	P

Table 11-4. CRGFLG Field Descriptions

Field	Description
7 RTIF	**Real Time Interrupt Flag** — RTIF is set to 1 at the end of the RTI period. This flag can only be cleared by writing a 1. Writing a 0 has no effect. If enabled (RTIE=1), RTIF causes an interrupt request. 0 RTI time-out has not yet occurred. 1 RTI time-out has occurred.
6 PORF	**Power on Reset Flag** — PORF is set to 1 when a power on reset occurs. This flag can only be cleared by writing a 1. Writing a 0 has no effect. 0 Power on reset has not occurred. 1 Power on reset has occurred.
5 LVRF	**Low Voltage Reset Flag** — LVRF is set to 1 when a low voltage reset occurs. This flag can only be cleared by writing a 1. Writing a 0 has no effect. 0 Low voltage reset has not occurred. 1 Low voltage reset has occurred.
4 LOCKIF	IPLL **Lock Interrupt Flag** — LOCKIF is set to 1 when LOCK status bit changes. This flag can only be cleared by writing a 1. Writing a 0 has no effect.If enabled (LOCKIE=1), LOCKIF causes an interrupt request. 0 No change in LOCK bit. 1 LOCK bit has changed.
3 LOCK	**Lock Status Bit** — LOCK reflects the current state of IPLL lock condition. This bit is cleared in Self Clock Mode. Writes have no effect. 0 VCOCLK is not within the desired tolerance of the target frequency. 1 VCOCLK is within the desired tolerance of the target frequency.
2 ILAF	**Illegal Address Reset Flag** — ILAF is set to 1 when an illegal address reset occurs. Refer to S12XMMC Block Guide for details. This flag can only be cleared by writing a 1. Writing a 0 has no effect. 0 Illegal address reset has not occurred. 1 Illegal address reset has occurred.
1 SCMIF	**Self Clock Mode Interrupt Flag** — SCMIF is set to 1 when SCM status bit changes. This flag can only be cleared by writing a 1. Writing a 0 has no effect. If enabled (SCMIE=1), SCMIF causes an interrupt request. 0 No change in SCM bit. 1 SCM bit has changed.
0 SCM	**Self Clock Mode Status Bit** — SCM reflects the current clocking mode. Writes have no effect. 0 MCU is operating normally with OSCCLK available. 1 MCU is operating in Self Clock Mode with OSCCLK in an unknown state. All clocks are derived from PLLCLK running at its minimum frequency f_{SCM}.

11.3.2.5 S12XECRG Interrupt Enable Register (CRGINT)

This register enables S12XECRG interrupt requests.

Module Base + 0x0004

	7	6	5	4	3	2	1	0
R	RTIE	0	0	LOCKIE	0	0	SCMIE	0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 11-7. S12XECRG Interrupt Enable Register (CRGINT)

Table 11-16. Reset Summary

Reset Source	Local Enable
COP Watchdog Reset	COPCTL (CR[2:0] nonzero)

11.5.1 Description of Reset Operation

The reset sequence is initiated by any of the following events:

- Low level is detected at the $\overline{\text{RESET}}$ pin (External Reset).
- Power on is detected.
- Low voltage is detected.
- Illegal Address Reset is detected (refer to device MMC information for details).
- COP watchdog times out.
- Clock monitor failure is detected and Self-Clock Mode was disabled (SCME=0).

Upon detection of any reset event, an internal circuit drives the $\overline{\text{RESET}}$ pin low for 128 SYSCLK cycles (see Figure 11-21). Since entry into reset is asynchronous it does not require a running SYSCLK. However, the internal reset circuit of the S12XECRG cannot sequence out of current reset condition without a running SYSCLK. The number of 128 SYSCLK cycles might be increased by n = 3 to 6 additional SYSCLK cycles depending on the internal synchronization latency. After 128+n SYSCLK cycles the $\overline{\text{RESET}}$ pin is released. The reset generator of the S12XECRG waits for additional 64 SYSCLK cycles and then samples the RESET pin to determine the originating source. Table 11-17 shows which vector will be fetched.

Table 11-17. Reset Vector Selection

Sampled $\overline{\text{RESET}}$ Pin (64 cycles after release)	Clock Monitor Reset Pending	COP Reset Pending	Vector Fetch
1	0	0	POR / LVR / Illegal Address Reset/ External Reset
1	1	X	Clock Monitor Reset
1	0	1	COP Reset
0	X	X	POR / LVR / Illegal Address Reset/ External Reset with rise of $\overline{\text{RESET}}$ pin

NOTE

External circuitry connected to the RESET pin should be able to raise the signal to a valid logic one within 64 SYSCLK cycles after the low drive is released by the MCU. If this requirement is not adhered to the reset source will always be recognized as “External Reset” even if the reset was initially caused by an other reset source.

Module Base + 0x0013

	7	6	5	4	3	2	1	0
R W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reset	0	0	0	0	0	0	0	0

Figure 14-23. Timer Input Capture/Output Compare Register 1 Low (TC1)

Module Base + 0x0014

	15	14	13	12	11	10	9	8
R W	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Reset	0	0	0	0	0	0	0	0

Figure 14-24. Timer Input Capture/Output Compare Register 2 High (TC2)

Module Base + 0x0015

	7	6	5	4	3	2	1	0
R W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reset	0	0	0	0	0	0	0	0

Figure 14-25. Timer Input Capture/Output Compare Register 2 Low (TC2)

Module Base + 0x0016

	15	14	13	12	11	10	9	8
R W	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Reset	0	0	0	0	0	0	0	0

Figure 14-26. Timer Input Capture/Output Compare Register 3 High (TC3)

Module Base + 0x0017

	7	6	5	4	3	2	1	0
R W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reset	0	0	0	0	0	0	0	0

Figure 14-27. Timer Input Capture/Output Compare Register 3 Low (TC3)

Module Base + 0x0018

	15	14	13	12	11	10	9	8
R W	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Reset	0	0	0	0	0	0	0	0

Figure 14-28. Timer Input Capture/Output Compare Register 4 High (TC4)

15.3 Memory Map and Register Definition

This section provides a detailed description of all memory and registers for the IIC module.

15.3.1 Register Descriptions

This section consists of register descriptions in address order. Each description includes a standard register diagram with an associated figure number. Details of register bit and field function follow the register diagrams, in bit order.

Register Name		Bit 7	6	5	4	3	2	1	Bit 0
0x0000 IBAD	R	ADR7	ADR6	ADR5	ADR4	ADR3	ADR2	ADR1	0
	W								
0x0001 IBFD	R	IBC7	IBC6	IBC5	IBC4	IBC3	IBC2	IBC1	IBC0
	W								
0x0002 IBCR	R	IBEN	IBIE	MS/$\overline{SL}$	Tx/$\overline{Rx}$	TXAK	0	0	IBSWAI
	W						RSTA		
0x0003 IBSR	R	TCF	IAAS	IBB	IBAL	0	SRW	IBIF	RXAK
	W								
0x0004 IBDR	R	D7	D6	D5	D4	D3	D2	D1	D0
	W								
0x0005 IBCR2	R	GCEN	ADTYPE	0	0	0	ADR10	ADR9	ADR8
	W								

= Unimplemented or Reserved

Figure 15-2. IIC Register Summary

15.3.1.1 IIC Address Register (IBAD)

Module Base +0x0000

	7	6	5	4	3	2	1	0
R	ADR7	ADR6	ADR5	ADR4	ADR3	ADR2	ADR1	0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 15-3. IIC Bus Address Register (IBAD)

Read and write anytime

attempt to engage the bus is failed. When considering these cases, the slave service routine should test the IBAL first and the software should clear the IBAL bit if it is set.

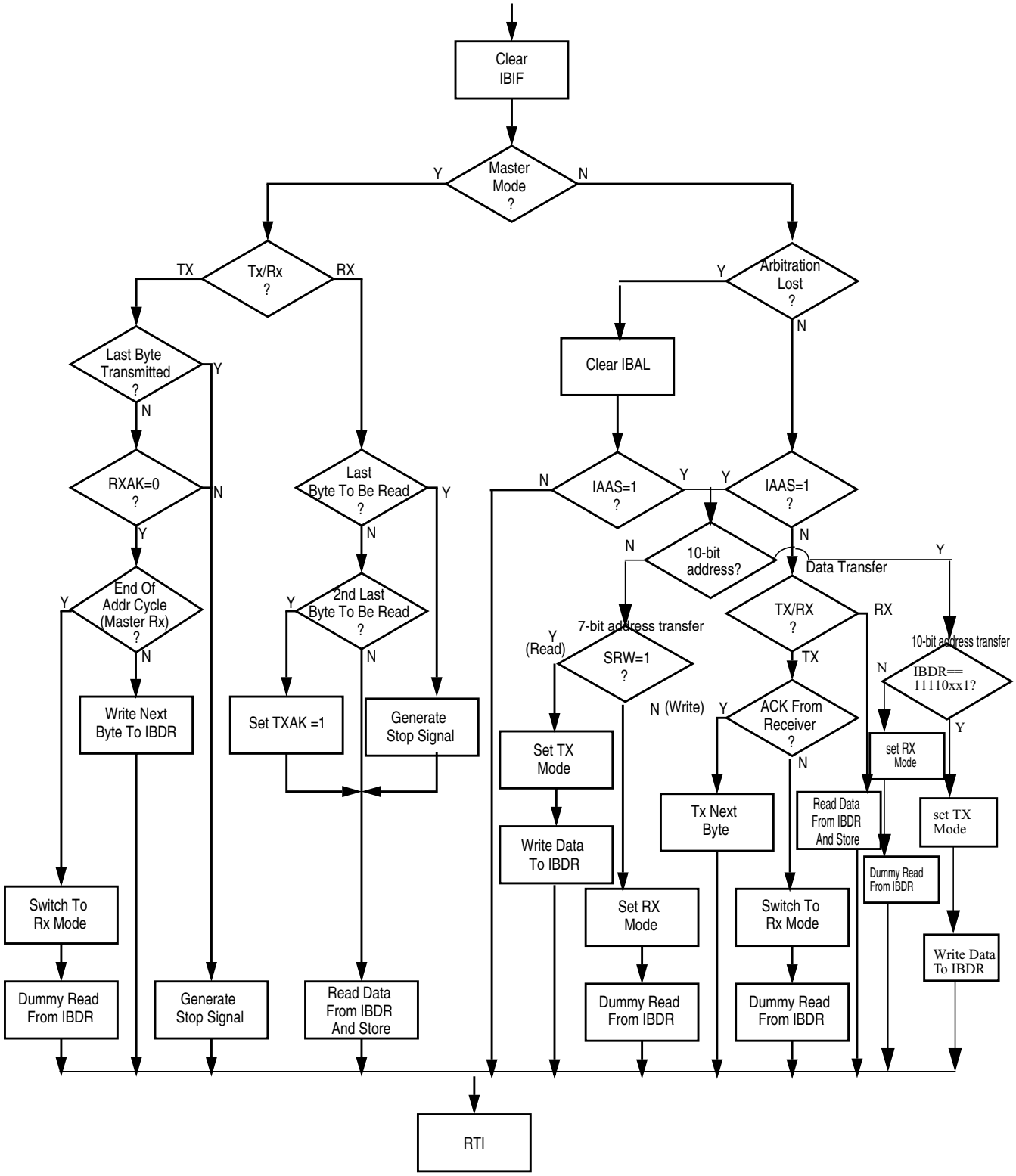

Figure 15-15. Flow-Chart of Typical IIC Interrupt Routine

17.4 Functional Description

Figure 17-27 shows a detailed block diagram of the PIT module. The main parts of the PIT are status, control and data registers, two 8-bit down-counters, eight 16-bit down-counters and an interrupt/trigger interface.

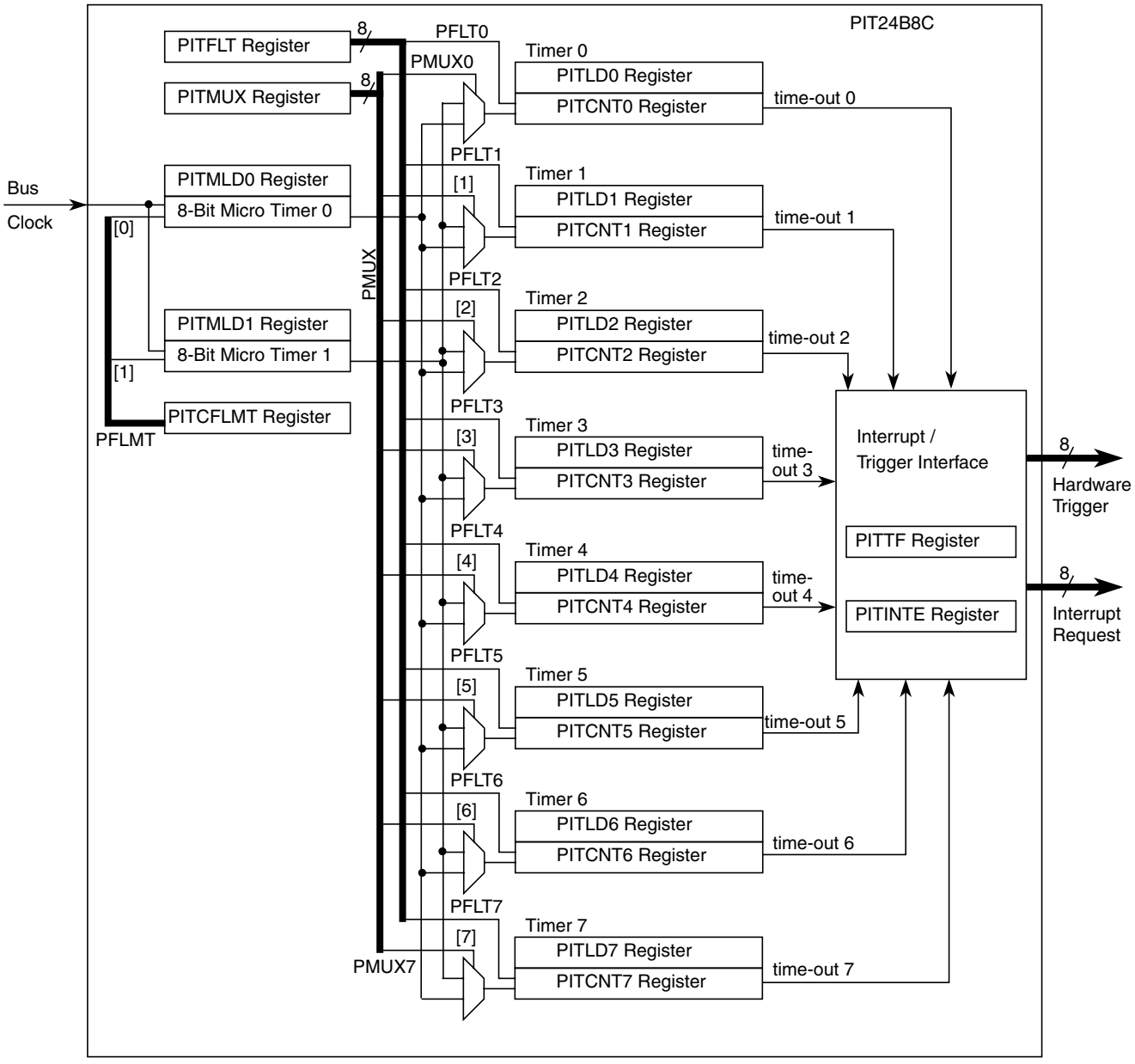

Figure 17-27. PIT24B8C Detailed Block Diagram

20.4.5.5 LIN Transmit Collision Detection

This module allows to check for collisions on the LIN bus.

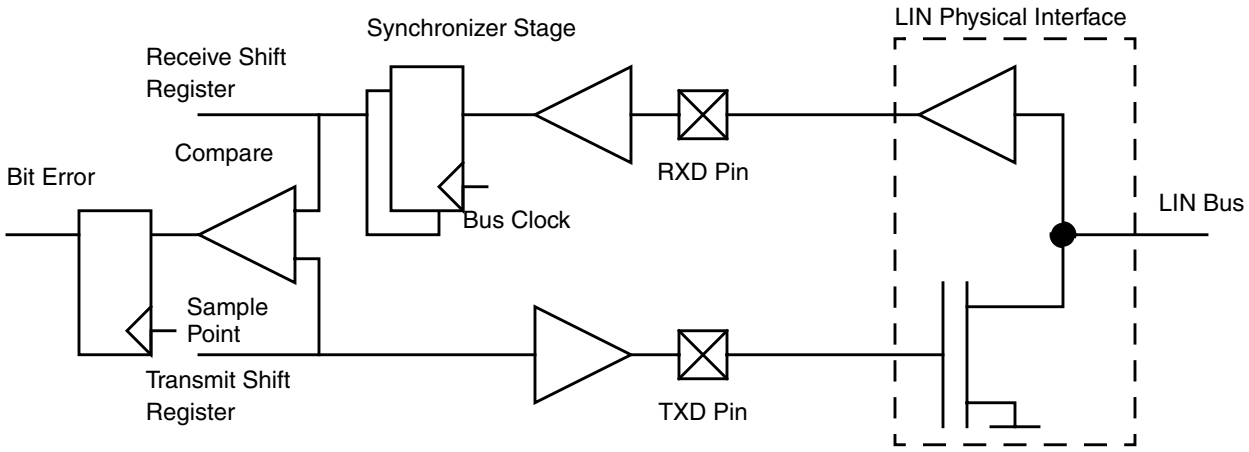

Figure 20-18. Collision Detect Principle

If the bit error circuit is enabled (BERRM[1:0] = 0:1 or = 1:0]), the error detect circuit will compare the transmitted and the received data stream at a point in time and flag any mismatch. The timing checks run when transmitter is active (not idle). As soon as a mismatch between the transmitted data and the received data is detected the following happens:

- The next bit transmitted will have a high level (TXPOL = 0) or low level (TXPOL = 1)
- The transmission is aborted and the byte in transmit buffer is discarded.
- the transmit data register empty and the transmission complete flag will be set
- The bit error interrupt flag, BERRIF, will be set.
- No further transmissions will take place until the BERRIF is cleared.

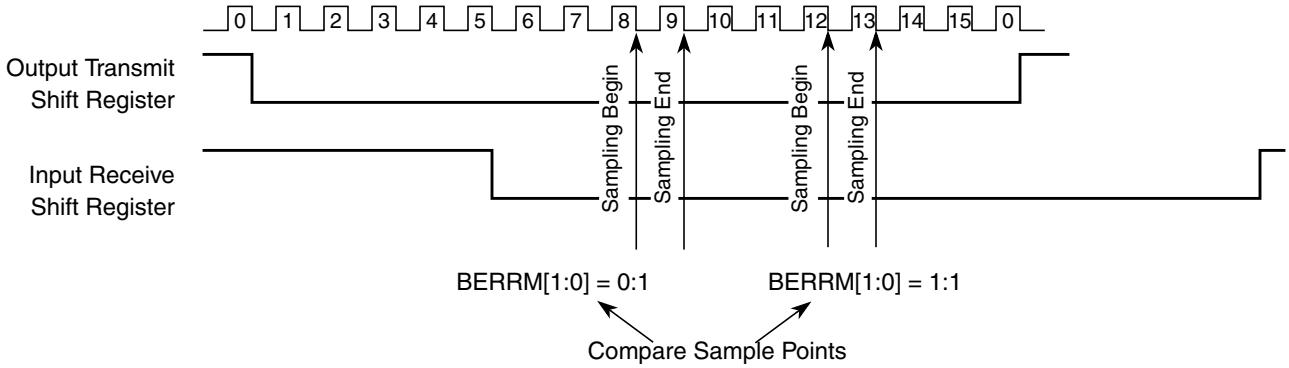

Figure 20-19. Timing Diagram Bit Error Detection

If the bit error detect feature is disabled, the bit error interrupt flag is cleared.

NOTE

The RXPOL and TXPOL bit should be set the same when transmission collision detect feature is enabled, otherwise the bit error interrupt flag may be set incorrectly.

D-Flash Sector — The D-Flash sector is the smallest portion of the D-Flash memory that can be erased. The D-Flash sector consists of four 64 byte rows for a total of 256 bytes.

EEE (Emulated EEPROM) — A method to emulate the small sector size features and endurance characteristics associated with an EEPROM.

EEE IFR — Nonvolatile information register located in the D-Flash block that contains data required to partition the D-Flash memory and buffer RAM for EEE. The EEE IFR is visible in the global memory map by setting the EEEIFRON bit in the MMCCTL1 register.

NVM Command Mode — An NVM mode using the CPU to setup the FCCOB register to pass parameters required for Flash command execution.

Phrase — An aligned group of four 16-bit words within the P-Flash memory. Each phrase includes eight ECC bits for single bit fault correction and double bit fault detection within the phrase.

P-Flash Memory — The P-Flash memory constitutes the main nonvolatile memory store for applications.

P-Flash Sector — The P-Flash sector is the smallest portion of the P-Flash memory that can be erased. Each P-Flash sector contains 1024 bytes.

Program IFR — Nonvolatile information register located in the P-Flash block that contains the Device ID, Version ID, and the Program Once field. The Program IFR is visible in the global memory map by setting the PGMIFRON bit in the MMCCTL1 register.

25.1.2 Features

25.1.2.1 P-Flash Features

- 256 Kbytes of P-Flash memory composed of two 128 Kbyte Flash blocks. The 128 Kbyte Flash blocks are each divided into 128 sectors of 1024 bytes.
- Single bit fault correction and double bit fault detection within a 64-bit phrase during read operations
- Automated program and erase algorithm with verify and generation of ECC parity bits
- Fast sector erase and phrase program operation
- Ability to program up to one phrase in each P-Flash block simultaneously
- Flexible protection scheme to prevent accidental program or erase of P-Flash memory

25.1.2.2 D-Flash Features

- Up to 32 Kbytes of D-Flash memory with 256 byte sectors for user access
- Dedicated commands to control access to the D-Flash memory over EEE operation
- Single bit fault correction and double bit fault detection within a word during read operations
- Automated program and erase algorithm with verify and generation of ECC parity bits
- Fast sector erase and word program operation
- Ability to program up to four words in a burst sequence

2. FDIV shown generates an FCLK frequency of 1.05 MHz

26.3.2.2 Flash Security Register (FSEC)

The FSEC register holds all bits associated with the security of the MCU and Flash module.

Offset Module Base + 0x0001

	7	6	5	4	3	2	1	0
R	KEYEN[1:0]		RNV[5:2]				SEC[1:0]	
W								
Reset	F	F	F	F	F	F	F	F

= Unimplemented or Reserved

Figure 26-6. Flash Security Register (FSEC)

All bits in the FSEC register are readable but not writable.

During the reset sequence, the FSEC register is loaded with the contents of the Flash security byte in the Flash configuration field at global address 0x7F_FF0F located in P-Flash memory (see Table 26-3) as indicated by reset condition F in Figure 26-6. If a double bit fault is detected while reading the P-Flash phrase containing the Flash security byte during the reset sequence, all bits in the FSEC register will be set to leave the Flash module in a secured state with backdoor key access disabled.

Table 26-10. FSEC Field Descriptions

Field	Description
7–6 KEYEN[1:0]	**Backdoor Key Security Enable Bits** — The KEYEN[1:0] bits define the enabling of backdoor key access to the Flash module as shown in Table 26-11.
5–2 RNV[5:2}	**Reserved Nonvolatile Bits** — The RNV bits should remain in the erased state for future enhancements.
1–0 SEC[1:0]	**Flash Security Bits** — The SEC[1:0] bits define the security state of the MCU as shown in Table 26-12. If the Flash module is unsecured using backdoor key access, the SEC bits are forced to 10.

Table 26-11. Flash KEYEN States

KEYEN[1:0]	Status of Backdoor Key Access
00	DISABLED
01	DISABLED(1)
10	ENABLED
11	DISABLED

1. Preferred KEYEN state to disable backdoor key access.

Table 27-32. D-Flash Commands

FCMD	Command	Function on D-Flash Memory
0x08	Erase All Blocks	Erase all D-Flash (and P-Flash) blocks. An erase of all Flash blocks is only possible when the FPLDIS, FPHDIS, and FPOPEN bits in the FPROT register and the EPDIS and EPOPEN bits in the EPROT register are set prior to launching the command.
0x0B	Unsecure Flash	Supports a method of releasing MCU security by erasing all D-Flash (and P-Flash) blocks and verifying that all D-Flash (and P-Flash) blocks are erased.
0x0D	Set User Margin Level	Specifies a user margin read level for the D-Flash block.
0x0E	Set Field Margin Level	Specifies a field margin read level for the D-Flash block (special modes only).
0x0F	Full Partition D-Flash	Erase the D-Flash block and partition an area of the D-Flash block for user access.
0x10	Erase Verify D-Flash Section	Verify that a given number of words starting at the address provided are erased.
0x11	Program D-Flash	Program up to four words in the D-Flash block.
0x12	Erase D-Flash Sector	Erase all bytes in a sector of the D-Flash block.
0x13	Enable EEPROM Emulation	Enable EEPROM emulation where writes to the buffer RAM EEE partition will be copied to the D-Flash EEE partition.
0x14	Disable EEPROM Emulation	Suspend all current erase and program activity related to EEPROM emulation but leave current EEE tags set.
0x15	EEPROM Emulation Query	Returns EEE partition and status variables.
0x20	Partition D-Flash	Partition an area of the D-Flash block for user access.

27.4.2 Flash Command Description

This section provides details of all available Flash commands launched by a command write sequence. The ACCERR bit in the FSTAT register will be set during the command write sequence if any of the following illegal steps are performed, causing the command not to be processed by the Memory Controller:

- Starting any command write sequence that programs or erases Flash memory before initializing the FCLKDIV register
- Writing an invalid command as part of the command write sequence
- For additional possible errors, refer to the error handling table provided for each command

If a Flash block is read during execution of an algorithm (CCIF = 0) on that same block, the read operation will return invalid data. If the SFDIF or DFDIF flags were not previously set when the invalid read operation occurred, both the SFDIF and DFDIF flags will be set and the FECCR registers will be loaded with the global address used in the invalid read operation with the data and parity fields set to all 0.

If the ACCERR or FPVIOL bits are set in the FSTAT register, the user must clear these bits before starting any command write sequence (see Section 27.3.2.7).

Table 27-38. Erase Verify P-Flash Section Command Error Handling

Register	Error Bit	Error Condition
FERSTAT	EPVIOLIF	None

27.4.2.4 Read Once Command

The Read Once command provides read access to a reserved 64 byte field (8 phrases) located in the nonvolatile information register of P-Flash block 0. The Read Once field is programmed using the Program Once command described in Section 27.4.2.7. The Read Once command must not be executed from the Flash block containing the Program Once reserved field to avoid code runaway.

Table 27-39. Read Once Command FCCOB Requirements

CCOBIX[2:0]	FCCOB Parameters	
000	0x04	Not Required
001	Read Once phrase index (0x0000 - 0x0007)	
010	Read Once word 0 value	
011	Read Once word 1 value	
100	Read Once word 2 value	
101	Read Once word 3 value	

Upon clearing CCIF to launch the Read Once command, a Read Once phrase is fetched and stored in the FCCOB indexed register. The CCIF flag will set after the Read Once operation has completed. Valid phrase index values for the Read Once command range from 0x0000 to 0x0007. During execution of the Read Once command, any attempt to read addresses within P-Flash block 0 will return invalid data.

Table 27-40. Read Once Command Error Handling

Register	Error Bit	Error Condition
FSTAT	ACCERR	Set if CCOBIX[2:0] != 001 at command launch
		Set if a Load Data Field command sequence is currently active
		Set if command not available in current mode (see Table 27-30)
		Set if an invalid phrase index is supplied
	FPVIOL	None
	MGSTAT1	Set if any errors have been encountered during the read
	MGSTAT0	Set if any non-correctable errors have been encountered during the read
FERSTAT	EPVIOLIF	None

27.4.2.5 Load Data Field Command

The Load Data Field command is executed to provide FCCOB parameters for multiple P-Flash blocks for a future simultaneous program operation in the P-Flash memory space.

27.4.3 Interrupts

The Flash module can generate an interrupt when a Flash command operation has completed or when a Flash command operation has detected an EEE error or an ECC fault.

Table 27-79. Flash Interrupt Sources

Interrupt Source	Interrupt Flag	Local Enable	Global (CCR) Mask
Flash Command Complete	CCIF (FSTAT register)	CCIE (FCNFG register)	I Bit
Flash EEE Erase Error	ERSERIF (FERSTAT register)	ERSERIE (FERCNFG register)	I Bit
Flash EEE Program Error	PGMERIF (FERSTAT register)	PGMERIE (FERCNFG register)	I Bit
Flash EEE Protection Violation	EPVIOLIF (FERSTAT register)	EPVIOLIE (FERCNFG register)	I Bit
Flash EEE Error Type 1 Violation	ERSVIF1 (FERSTAT register)	ERSVIE1 (FERCNFG register)	I Bit
Flash EEE Error Type 0 Violation	ERSVIF0 (FERSTAT register)	ERSVIE0 (FERCNFG register)	I Bit
ECC Double Bit Fault on Flash Read	DFDIF (FERSTAT register)	DFDIE (FERCNFG register)	I Bit
ECC Single Bit Fault on Flash Read	SFDIF (FERSTAT register)	SFDIE (FERCNFG register)	I Bit

NOTE

Vector addresses and their relative interrupt priority are determined at the MCU level.

27.4.3.1 Description of Flash Interrupt Operation

The Flash module uses the CCIF flag in combination with the CCIE interrupt enable bit to generate the Flash command interrupt request. The Flash module uses the ERSEIF, PGMEIF, EPVIOLIF, ERSVIF1, ERSVIF0, DFDIF and SFDIF flags in combination with the ERSEIE, PGMEIE, EPVIOLIE, ERSVIE1, ERSVIE0, DFDIE and SFDIE interrupt enable bits to generate the Flash error interrupt request. For a detailed description of the register bits involved, refer to Section 27.3.2.5, “Flash Configuration Register (FCNFG)”, Section 27.3.2.6, “Flash Error Configuration Register (FERCNFG)”, Section 27.3.2.7, “Flash Status Register (FSTAT)”, and Section 27.3.2.8, “Flash Error Status Register (FERSTAT)”.

The logic used for generating the Flash module interrupts is shown in Figure 27-27.

Chapter 28
768 KByte Flash Module (S12XFTM768K4V2)

Table 28-1. Revision History

Revision Number	Revision Date	Sections Affected	Description of Changes
V02.09	29 Nov 2007		- Cleanup
V02.10	19 Dec 2007	28.4.2/28-1113 28.4.2/28-1113 28.3.1/28-1082	- Updated Command Error Handling tables based on parent-child relationship with FTM1024K5 - Corrected Error Handling table for Full Partition D-Flash, Partition D-Flash, and EEPROM Emulation Query commands - Corrected P-Flash Memory Addressing table
V02.11	25 Sep 2009	28.1/28-1077 28.3.2.1/28-1089 28.4.2.4/28-1116 28.4.2.7/28-1119 28.4.2.12/28-1123 28.4.2.12/28-1123 28.4.2.12/28-1123 28.4.2.20/28-1132 28.3.2/28-1087 28.3.2.1/28-1089 28.4.1.2/28-1108 28.6/28-1138	- Clarify single bit fault correction for P-Flash phrase - Expand FDIV vs OSCCLK Frequency table - Add statement concerning code runaway when executing Read Once command from Flash block containing associated fields - Add statement concerning code runaway when executing Program Once command from Flash block containing associated fields - Add statement concerning code runaway when executing Verify Backdoor Access Key command from Flash block containing associated fields - Relate Key 0 to associated Backdoor Comparison Key address - Change “power down reset” to “reset” - Add ACCERR condition for Disable EEPROM Emulation command The following changes were made to clarify module behavior related to Flash register access during reset sequence and while Flash commands are active: - Add caution concerning register writes while command is active - Writes to FCLKDIV are allowed during reset sequence while CCIF is clear - Add caution concerning register writes while command is active - Writes to FCCOBIX, FCCOBHI, FCCOBLO registers are ignored during reset sequence

28.1 Introduction

The FTM768K4 module implements the following:

- 768 Kbytes of P-Flash (Program Flash) memory, consisting of 4 physical Flash blocks, intended primarily for nonvolatile code storage

A.3.1.24 EEE Copy Down

The typical EEE copy down time is given by the following equation

$$t_{dfcd} = (14000 + (316 \cdot ERPART) + (1500 \cdot (124 - DFPART))) \times \frac{1}{f_{NVMBUS}}$$

The maximum EEE copy down time is given by the following equation

$$t_{dfcd} = (34000 + (316 \cdot ERPART) + (1500 \cdot (124 - DFPART))) \times \frac{1}{f_{NVMBUS}}$$

Worst case for Enable EEPROM Emulation allows for all the EEE records to have to be copied which is a very low probability scenario only likely in the case that the EEE is mostly full of unchanging data (the records for which are stored in consecutive D-Flash sectors).

Table A-19. NVM Timing Characteristics

Conditions are as shown in Table A-4, with f_{NVMBUS} = 50MHz and f_{NVMOP}= 1MHz unless otherwise noted.

Num	C	Rating	Symbol	Min	Typ	Max	Unit
1	D	External oscillator clock	f_{NVMOSC}	2	—	50(1)	MHz
2	D	Bus frequency for programming or erase operations	f_{NVMBUS}	1	—	50	MHz
3	D	Operating frequency	f_{NVMOP}	800	—	1050	kHz
4	D	P-Flash phrase programming	t_{bwpgm}	—	162	173	µs
5a	D	P- Flash phrase program time using D-LOAD on 4 blocks	t_{bwpgm4}	—	231	264	µs
5b	D	P-Flash phrase program time using D-LOAD on 3 blocks	t_{bwpgm3}	—	208	233	µs
5c	D	P-Flash phrase program time using D-LOAD on 2 blocks	t_{bwpgm2}	—	185	202	µs
6	P	P-Flash sector erase time	t_{era}	—	20	21	ms
7	P	Erase All Blocks (Mass erase) time	t_{mass}	—	101	102	ms
7a	D	Unsecure Flash	t_{uns}	—	101	102	ms
8	D	P-Flash erase verify (blank check) time(2)	t_{check}	—	—	335002	t_{cyc}
9a	D	D-Flash word programming one word	t_{dpgm}	—	88	95	µs
9b	D	D-Flash word programming two words	t_{dpgm}	—	153	165	µs
9c	D	D-Flash word programming three words	t_{dpgm}	—	212	230	µs
9d	D	D-Flash word programming four words	t_{dpgm}	—	282	316	µs
9e	D	D-Flash word programming four words crossing row boundary	t_{dpgm}	—	298	342	µs
10	D	D-Flash sector erase time	t_{eradf}	—	5.2(3)	21	ms
11	D	D-Flash erase verify (blank check) time	t_{check}	—	—	17500	t_{cyc}
12	D	EEE copy down (mask sets 5M48H, 3M25J, 2M53J, 1M12S, 1N35H, 1N36H)	t_{dfrcd}	—	255000	275000(4)	t_{cyc}
12	D	EEE copy down (other mask sets)	t_{dfrcd}	—	205000	225000(5)	t_{cyc}

1. Restrictions for oscillator in crystal mode apply.
2. Valid for both “Erase verify all” or “Erase verify block” on 256K block without failing locations
3. This is a typical value for a new device
4. Maximum partitioning

A.5 Output Loads

A.5.1 Resistive Loads

The voltage regulator is intended to supply the internal logic and oscillator. It allows no external DC loads.

A.5.2 Capacitive Loads

The capacitive loads are specified in Table A-22. Ceramic capacitors with X7R dielectricum are required.

Table A-22. - Required Capacitive Loads

Num	Characteristic	Symbol	Min	Recommended	Max	Unit
1	VDD/VDDF external capacitive load	C_{DDext}	176	220	264	nF
3	VDDPLL external capacitive load	$C_{DDPLLext}$	80	220	264	nF

A.5.3 Chip Power-up and Voltage Drops

LVI (low voltage interrupt), POR (power-on reset) and LVRs (low voltage reset) handle chip power-up or drops of the supply voltage. Their function is shown in Figure A-3 .

Figure A-3. MC9S12XE-Family - Chip Power-up and Voltage Drops (not scaled)