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Details

Product Status	Active
Core Processor	HCS12X
Core Size	16-Bit
Speed	50MHz
Connectivity	CANbus, EBI/EMI, I ² C, IrDA, SCI, SPI
Peripherals	LVD, POR, PWM, WDT
Number of I/O	59
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	12K x 8
Voltage - Supply (Vcc/Vdd)	1.72V ~ 5.5V
Data Converters	A/D 8x12b
Oscillator Type	External
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	80-QFP
Supplier Device Package	80-QFP (14x14)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=s912xeg128j2maar

2.3.94 Port L Input Register (PTIL)

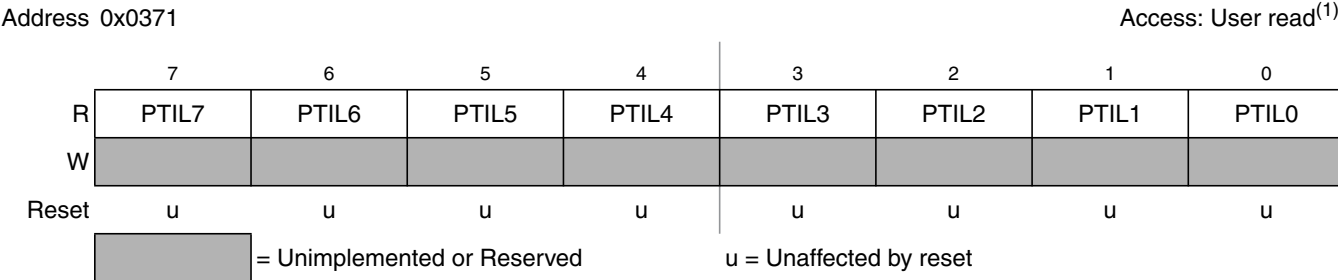


Figure 2-92. Port L Input Register (PTIL)

1. Read: Anytime.
Write: Never, writes to this register have no effect.

Table 2-89. PTIL Register Field Descriptions

Field	Description
7-0 PTIL	Port L input data— This register always reads back the buffered state of the associated pins. This can also be used to detect overload or short circuit conditions on output pins.

2.3.95 Port L Data Direction Register (DDRL)

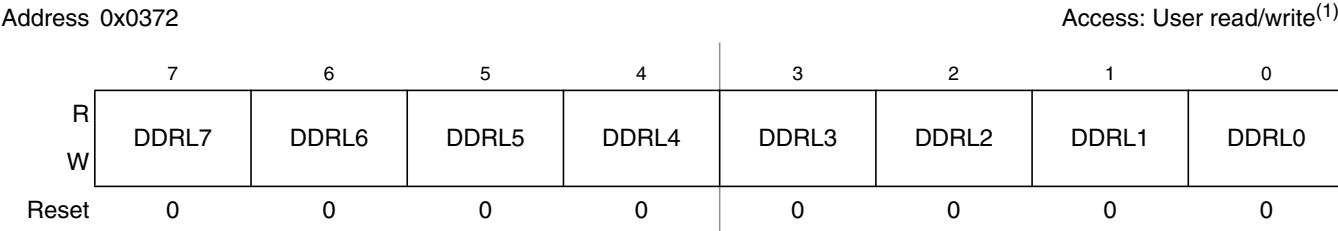


Figure 2-93. Port L Data Direction Register (DDRL)

1. Read: Anytime.
Write: Anytime.

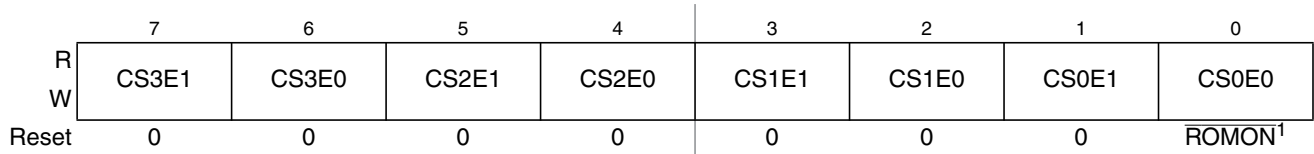
Table 2-90. DDRL Register Field Descriptions

Field	Description
7-0 DDRL	Port L data direction— This register controls the data direction of pins 7 through 0. This register configures each Port L pin as either input or output. If SPI0 is enabled, the SPI0 determines the pin direction. <i>Refer to SPI section for details.</i> If the associated SCI transmit or receive channel is enabled this register has no effect on the pins. The pin is forced to be an output if a SCI transmit channel is enabled, it is forced to be an input if the SCI receive channel is enabled. The data direction bits revert to controlling the I/O direction of a pin when the associated channel is disabled. 1 Associated pin is configured as output. 0 Associated pin is configured as input.

3.3.2 Register Descriptions

3.3.2.1 MMC Control Register (MMCCTL0)

Address: 0x000A PRR



1. ROMON is bit[0] of the register MMCTL1 (see [Figure 3-10](#))

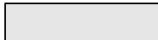
 = Unimplemented or Reserved

Figure 3-3. MMC Control Register (MMCCTL0)

Read: Anytime. In emulation modes read operations will return the data from the external bus. In all other modes the data is read from this register.

Write: Anytime. In emulation modes write operations will also be directed to the external bus.

Table 3-5. Chip Selects Function Activity

Register Bit	Chip Modes					
	NS	SS	NX	ES	EX	ST
CS0E[1:0], CS1E[1:0], CS2E[1:0], CS3E[1:0]	Disabled ⁽¹⁾	Disabled	Enabled ⁽²⁾	Disabled	Enabled	Disabled

1. Disabled: feature always inactive.

2. Enabled: activity is controlled by the appropriate register bit value.

The MMCCTL0 register is used to control external bus functions, like:

- Availability of chip selects. (See [Table 3-5](#) and [Table 3-6](#))
- Control of different external stretch mechanism. For more detail refer to the S12X_EBI BlockGuide.

CAUTION

XGATE write access to this register during an CPU access which makes use of this register could lead to unexpected results.

6.3.2 Register Descriptions

This section describes in address order all the XINT module registers and their individual bits.

Address	Register Name	Bit 7	6	5	4	3	2	1	Bit 0
0x0121	IVBR	R	IVB_ADDR[7:0]7						
		W							
0x0126	INT_XGPRIOR	R	0	0	0	0	0	XILVL[2:0]	
		W							
0x0127	INT_CFADDR	R	INT_CFADDR[7:4]				0	0	0
		W							
0x0128	INT_CFDATA0	R	RQST	0	0	0	0	PRIOLVL[2:0]	
		W							
0x0129	INT_CFDATA1	R	RQST	0	0	0	0	PRIOLVL[2:0]	
		W							
0x012A	INT_CFDATA2	R	RQST	0	0	0	0	PRIOLVL[2:0]	
		W							
0x012B	INT_CFDATA3	R	RQST	0	0	0	0	PRIOLVL[2:0]	
		W							
0x012C	INT_CFDATA4	R	RQST	0	0	0	0	PRIOLVL[2:0]	
		W							
0x012D	INT_CFDATA5	R	RQST	0	0	0	0	PRIOLVL[2:0]	
		W							
0x012E	INT_CFDATA6	R	RQST	0	0	0	0	PRIOLVL[2:0]	
		W							
0x012F	INT_CFDATA7	R	RQST	0	0	0	0	PRIOLVL[2:0]	
		W							

= Unimplemented or Reserved

Figure 6-2. XINT Register Summary



BLS

Branch if Lower or Same

BLS

Operation

If $C \mid Z = 1$, then $PC + \$0002 + (REL9 \ll 1) \Rightarrow PC$

Branch instruction to compare unsigned numbers.

Branch if $RS1 \leq RS2$:

SUB	R0, RS1, RS2
BLS	REL9

CCR Effects

N	Z	V	C
—	—	—	—

- N: Not affected.
- Z: Not affected.
- V: Not affected.
- C: Not affected.

Code and CPU Cycles

Source Form	Address Mode	Machine Code								Cycles
BLS REL9	REL9	0	0	1	1	0	0	1	REL9	PP/P

CPC

Compare with Carry

CPC

Operation

$RS1 - RS2 - C \Rightarrow \text{NONE}$ (translates to SBC R0, RS1, RS2)

Subtracts the carry bit and the content of register RS2 from the content of register RS1 using binary subtraction and discards the result.

CCR Effects

N	Z	V	C
Δ	Δ	Δ	Δ

- N: Set if bit 15 of the result is set; cleared otherwise.
- Z: Set if the result is \$0000; cleared otherwise.
- V: Set if a two's complement overflow resulted from the operation; cleared otherwise.
 $RS1[15] \& \overline{RS2[15]} \& \overline{result[15]} \mid \overline{RS1[15]} \& RS2[15] \& result[15]$
- C: Set if there is a carry from the bit 15 of the result; cleared otherwise.
 $\overline{RS1[15]} \& RS2[15] \mid RS1[15] \& \overline{result[15]} \mid RS2[15] \& result[15]$

Code and CPU Cycles

Source Form	Address Mode	Machine Code												Cycles
CPC RS1, RS2	TRI	0	0	0	1	1	0	0	0	RS1	RS2	0	1	P

11.3 Memory Map and Registers

This section provides a detailed description of all registers accessible in the S12XECRG.

11.3.1 Module Memory Map

Figure 11-2 gives an overview on all S12XECRG registers.

Address	Name		Bit 7	6	5	4	3	2	1	Bit 0
0x0000	SYNR	R	VCOFRQ[1:0]		SYNDIV[5:0]					
		W								
0x0001	REFDV	R	REFFRQ[1:0]		REFDIV[5:0]					
		W								
0x0002	POSTDIV	R	0	0	0	POSTDIV[4:0]				
		W								
0x0003	CRGFLG	R	RTIF	PORF	LVRF	LOCKIF	LOCK	ILAF	SCMIF	SCM
		W								
0x0004	CRGINT	R	RTIE	0	0	LOCKIE	0	0	SCMIE	0
		W								
0x0005	CLKSEL	R	PLLSEL	PSTP	XCLKS	0	PLLWAI	0	RTIWAI	COPWAI
		W								
0x0006	PLLCTL	R	CME	PLLON	FM1	FM0	FSTWKP	PRE	PCE	SCME
		W								
0x0007	RTICTL	R	RTDEC	RTR6	RTR5	RTR4	RTR3	RTR2	RTR1	RTR0
		W								
0x0008	COPCTL	R	WCOP	RSBCK	0	0	0	CR2	CR1	CR0
		W			WRTMASK					
0x0009	FORBYP ²	R	0	0	0	0	0	0	0	0
		W								
0x000A	CTCTL ²	R	0	0	0	0	0	0	0	0
		W								
0x000B	ARMCOP	R	0	0	0	0	0	0	0	0
		W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

2. FORBYP and CTCTL are intended for factory test purposes only.


 = Unimplemented or Reserved

Figure 11-2. CRG Register Summary

NOTE

Register Address = Base Address + Address Offset, where the Base Address is defined at the MCU level and the Address Offset is defined at the module level.

11.3.2.2 S12XECRG Reference Divider Register (REFDV)

The REFDV register provides a finer granularity for the IPLL multiplier steps.

Module Base + 0x0001

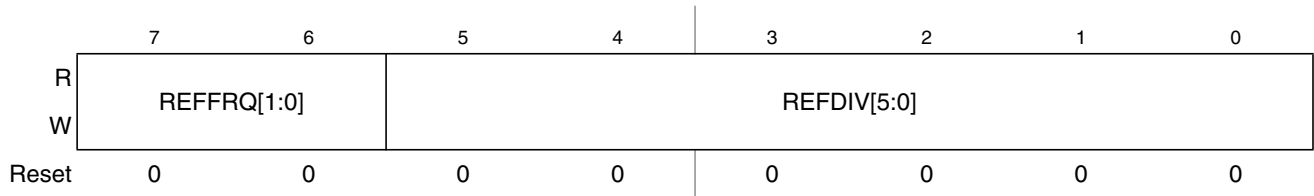


Figure 11-4. S12XECRG Reference Divider Register (REFDV)

Read: Anytime

Write: Anytime except when PLLSEL = 1

NOTE

Write to this register initializes the lock detector bit.

$$f_{REF} = \frac{f_{OSC}}{(REFDIV + 1)}$$

The REFFRQ[1:0] bit are used to configure the internal PLL filter for optimal stability and lock time. For correct IPLL operation the REFFRQ[1:0] bits have to be selected according to the actual REFCLK frequency as shown in Figure 11-3. Setting the REFFRQ[1:0] bits wrong can result in a non functional IPLL (no locking and/or insufficient stability).

Table 11-3. Reference Clock Frequency Selection

REFCLK Frequency Ranges	REFFRQ[1:0]
1MHz <= f _{REF} <= 2MHz	00
2MHz < f _{REF} <= 6MHz	01
6MHz < f _{REF} <= 12MHz	10
f _{REF} >12MHz	11

11.3.2.3 S12XECRG Post Divider Register (POSTDIV)

The POSTDIV register controls the frequency ratio between the VCOCLK and PLLCLK. The count in the final divider divides VCOCLK frequency by 1 or 2*POSTDIV. Note that if POSTDIV = \$00 f_{PLL} = f_{VCO} (divide by one).

Chapter 12

Pierce Oscillator (S12XOSCLCPV2)

Table 12-1. Revision History

Revision Number	Revision Date	Sections Affected	Description of Changes
V01.05	19 Jul 2006		- All xclks info was removed
V02.00	04 Aug 2006		- Incremented revision to match the design system spec revision

12.1 Introduction

The Pierce oscillator (XOSC) module provides a robust, low-noise and low-power clock source. The module will be operated from the V_{DDPLL} supply rail (1.8 V nominal) and require the minimum number of external components. It is designed for optimal start-up margin with typical crystal oscillators.

12.1.1 Features

The XOSC will contain circuitry to dynamically control current gain in the output amplitude. This ensures a signal with low harmonic distortion, low power and good noise immunity.

- High noise immunity due to input hysteresis
- Low RF emissions with peak-to-peak swing limited dynamically
- Transconductance (gm) sized for optimum start-up margin for typical oscillators
- Dynamic gain control eliminates the need for external current limiting resistor
- Integrated resistor eliminates the need for external bias resistor in loop controlled Pierce mode.
- Low power consumption:
 - Operates from 1.8 V (nominal) supply
 - Amplitude control limits power
- Clock monitor

12.1.2 Modes of Operation

Two modes of operation exist:

1. Loop controlled Pierce (LCP) oscillator
2. External square wave mode featuring also full swing Pierce (FSP) without internal bias resistor

The oscillator mode selection is described in the Device Overview section, subsection Oscillator Configuration.

Write used in the flag clearing mechanism. Writing a one to the flag clears the flag. Writing a zero will not affect the current status of the bit.

NOTE

When TFFCA = 1, the flag cannot be cleared via the normal flag clearing mechanism (writing a one to the flag). Reference [Section 14.3.2.6, “Timer System Control Register 1 \(TSCR1\)”](#).

All bits reset to zero.

TFLG2 indicates when interrupt conditions have occurred. The flag can be cleared via the normal flag clearing mechanism (writing a one to the flag) or via the fast flag clearing mechanism (Reference TFFCA bit in [Section 14.3.2.6, “Timer System Control Register 1 \(TSCR1\)”](#)).

Table 14-18. TFLG2 Field Descriptions

Field	Description
7 TOF	Timer Overflow Flag — Set when 16-bit free-running timer overflows from 0xFFFF to 0x0000.

14.3.2.14 Timer Input Capture/Output Compare Registers 0–7

Module Base + 0x0010

	15	14	13	12	11	10	9	8
R	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
W								
Reset	0	0	0	0	0	0	0	0

Figure 14-20. Timer Input Capture/Output Compare Register 0 High (TC0)

Module Base + 0x0011

	7	6	5	4	3	2	1	0
R	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W								
Reset	0	0	0	0	0	0	0	0

Figure 14-21. Timer Input Capture/Output Compare Register 0 Low (TC0)

Module Base + 0x0012

	15	14	13	12	11	10	9	8
R	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
W								
Reset	0	0	0	0	0	0	0	0

Figure 14-22. Timer Input Capture/Output Compare Register 1 High (TC1)

3. Input pulses with a duration between (DLY_CNT – 1) and DLY_CNT cycles may be rejected or accepted, depending on their relative alignment with the sample points.
4. Input pulses with a duration of DLY_CNT or longer are accepted.

14.4.1.2 OC Channel Initialization

An internal compare channel whose output drives OCx may be programmed before the timer drives the output compare state (OCx). The required output of the compare logic can be disconnected from the pin, leaving it driven by the GP IO port, by setting the appropriate OCPDx bit before enabling the output compare channel (by default the OCPD bits are cleared which would enable the output compare logic to drive the pin as soon as the timer output compare channel is enabled). The desired initial state can then be configured in the internal output compare logic by forcing a compare action with the logic disconnected from the IO (by writing a one to CFORCx bit with TIOSx, OCPDx and TEN bits set to one). Clearing the output compare disconnect bit (OCPDx) will then allow the internal compare logic to drive the programmed state to OCx. This allows a glitch free switching between general purpose I/O and timer output functionality.

14.4.1.3 Pulse Accumulators

There are four 8-bit pulse accumulators with four 8-bit holding registers associated with the four IC buffered channels 3–0. A pulse accumulator counts the number of active edges at the input of its channel.

The minimum pulse width for the PAI input is greater than two bus clocks. The maximum input frequency on the pulse accumulator channel is one half the bus frequency or Eclk.

The user can prevent the 8-bit pulse accumulators from counting further than 0x00FF by utilizing the PACMX control bit in the ICSYS register. In this case, a value of 0x00FF means that 255 counts or more have occurred.

Each pair of pulse accumulators can be used as a 16-bit pulse accumulator (see [Figure 14-72](#)).

Pulse accumulator B operates only as an event counter, it does not feature gated time accumulation mode. The edge control for pulse accumulator B as a 16-bit pulse accumulator is defined by TCTL4[1:0].

To operate the 16-bit pulse accumulators A and B (PACA and PACB) independently of input capture or output compare 7 and 0 respectively, the user must set the corresponding bits: IOSx = 1, OMx = 0, and OLx = 0. OC7M7 or OC7M0 in the OC7M register must also be cleared.

There are two modes of operation for the pulse accumulators:

- Pulse accumulator latch mode

The value of the pulse accumulator is transferred to its holding register when the modulus down-counter reaches zero, a write 0x0000 to the modulus counter or when the force latch control bit ICLAT is written.

At the same time the pulse accumulator is cleared.
- Pulse accumulator queue mode

When queue mode is enabled, reads of an input capture holding register will transfer the contents of the associated pulse accumulator to its holding register.

Chapter 20

Serial Communication Interface (S12SCIV5)

Table 20-1. Revision History

Version Number	Revision Date	Effective Date	Author	Description of Changes
05.03	12/25/2008			remove redundancy comments in Figure1-2
05.04	08/05/2009			fix typo, SCIBDL reset value be 0x04, not 0x00
05.05	06/03/2010			fix typo, Table 20-4 , SCICR1 Even parity should be PT=0 fix typo, on page 20-745 , should be BKDIF, not BLDIF

20.1 Introduction

This block guide provides an overview of the serial communication interface (SCI) module.
The SCI allows asynchronous serial communications with peripheral devices and other CPUs.

20.1.1 Glossary

- IR: InfraRed
- IrDA: Infrared Design Associate
- IRQ: Interrupt Request
- LIN: Local Interconnect Network
- LSB: Least Significant Bit
- MSB: Most Significant Bit
- NRZ: Non-Return-to-Zero
- RZI: Return-to-Zero-Inverted
- RXD: Receive Pin
- SCI : Serial Communication Interface
- TXD: Transmit Pin

22.1.3 Block Diagrams

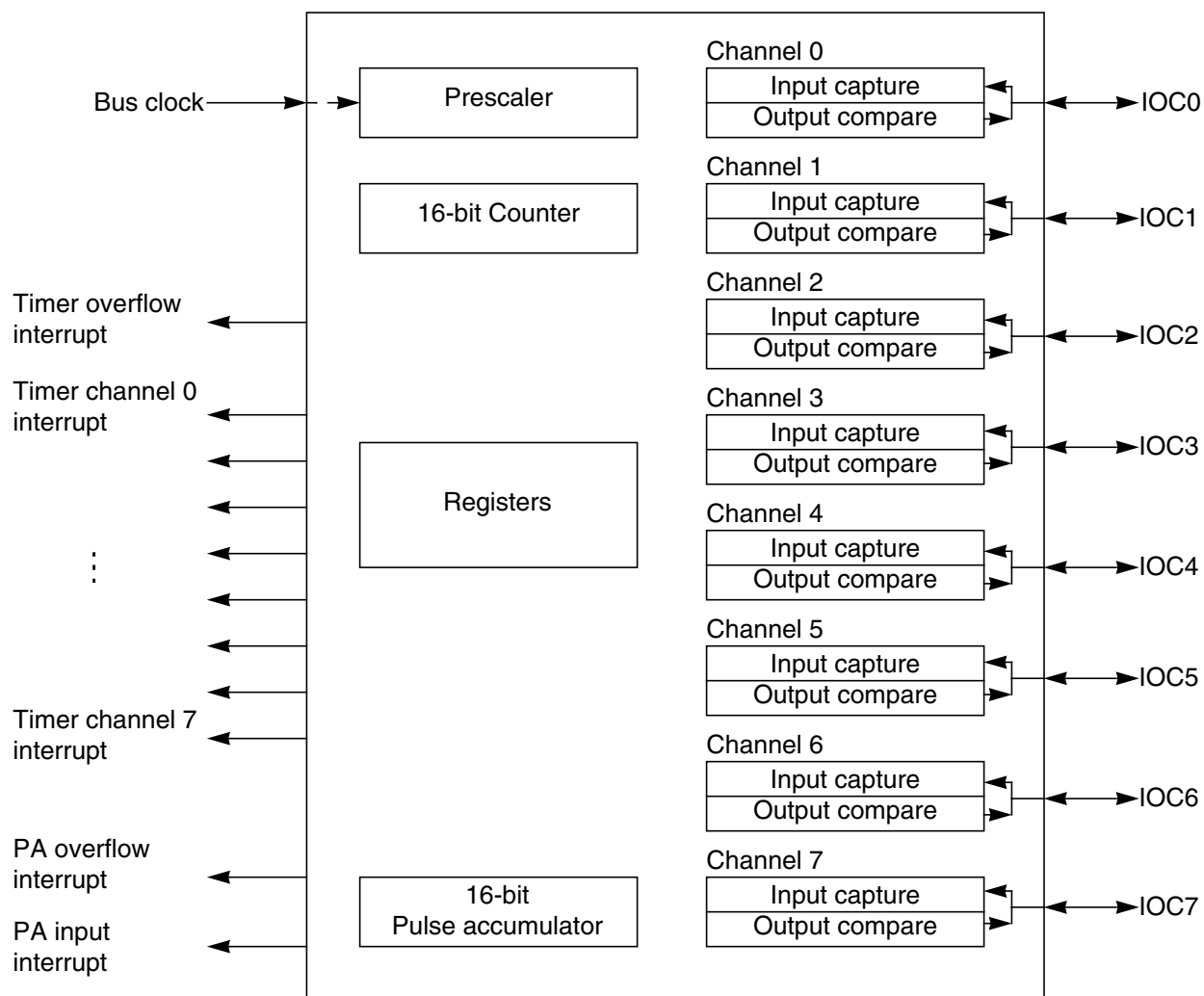


Figure 22-1. TIM16B8CV2 Block Diagram

Write: Has no meaning or effect in the normal mode; only writable in special modes (test_mode = 1).

The period of the first count after a write to the TCNT registers may be a different size because the write is not synchronized with the prescaler clock.

22.3.2.6 Timer System Control Register 1 (TSCR1)

Module Base + 0x0006

	7	6	5	4	3	2	1	0
R	TEN	TSWAI	TSFRZ	TFFCA	PRNT	0	0	0
W								
Reset	0	0	0	0	0	0	0	0
	= Unimplemented or Reserved							

Figure 22-12. Timer System Control Register 1 (TSCR1)

Read: Anytime

Write: Anytime

Table 22-6. TSCR1 Field Descriptions

Field	Description
7 TEN	Timer Enable 0 Disables the main timer, including the counter. Can be used for reducing power consumption. 1 Allows the timer to function normally. If for any reason the timer is not active, there is no +64 clock for the pulse accumulator because the +64 is generated by the timer prescaler.
6 TSWAI	Timer Module Stops While in Wait 0 Allows the timer module to continue running during wait. 1 Disables the timer module when the MCU is in the wait mode. Timer interrupts cannot be used to get the MCU out of wait. TSWAI also affects pulse accumulator.
5 TSFRZ	Timer Stops While in Freeze Mode 0 Allows the timer counter to continue running while in freeze mode. 1 Disables the timer counter whenever the MCU is in freeze mode. This is useful for emulation. TSFRZ does not stop the pulse accumulator.

22.3.2.8 Timer Control Register 1/Timer Control Register 2 (TCTL1/TCTL2)

Module Base + 0x0008

	7	6	5	4	3	2	1	0
R	OM7	OL7	OM6	OL6	OM5	OL5	OM4	OL4
W								
Reset	0	0	0	0	0	0	0	0

Figure 22-14. Timer Control Register 1 (TCTL1)

Module Base + 0x0009

	7	6	5	4	3	2	1	0
R	OM3	OL3	OM2	OL2	OM1	OL1	OM0	OL0
W								
Reset	0	0	0	0	0	0	0	0

Figure 22-15. Timer Control Register 2 (TCTL2)

Read: Anytime

Write: Anytime

Table 22-8. TCTL1/TCTL2 Field Descriptions

Field	Description
7:0 OMx	Output Mode — These eight pairs of control bits are encoded to specify the output action to be taken as a result of a successful OCx compare. When either OMx or OLx is 1, the pin associated with OCx becomes an output tied to OCx. Note: To enable output action by OMx bits on timer port, the corresponding bit in OC7M should be cleared. For an output line to be driven by an OCx the OCPDx must be cleared.
7:0 OLx	Output Level — These eight pairs of control bits are encoded to specify the output action to be taken as a result of a successful OCx compare. When either OMx or OLx is 1, the pin associated with OCx becomes an output tied to OCx. Note: To enable output action by OLx bits on timer port, the corresponding bit in OC7M should be cleared. For an output line to be driven by an OCx the OCPDx must be cleared.

Table 22-9. Compare Result Output Action

OMx	OLx	Action
0	0	No output compare action on the timer output signal
0	1	Toggle OCx output line
1	0	Clear OCx output line to zero
1	1	Set OCx output line to one

Table 22-17. TRLG2 Field Descriptions

Field	Description
7 TOF	Timer Overflow Flag — Set when 16-bit free-running timer overflows from 0xFFFF to 0x0000. Clearing this bit requires writing a one to bit 7 of TFLG2 register while the TEN bit of TSCR1 or PAEN bit of PACTL is set to one (See also TCRE control bit explanation.)

22.3.2.14 Timer Input Capture/Output Compare Registers High and Low 0–7 (TCxH and TCxL)

Module Base + 0x0010 = TC0H 0x0018 = TC4H
 0x0012 = TC1H 0x001A = TC5H
 0x0014 = TC2H 0x001C = TC6H
 0x0016 = TC3H 0x001E = TC7H

	15	14	13	12	11	10	9	0
R	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
W								
Reset	0	0	0	0	0	0	0	0

Figure 22-22. Timer Input Capture/Output Compare Register x High (TCxH)

Module Base + 0x0011 = TC0L 0x0019 = TC4L
 0x0013 = TC1L 0x001B = TC5L
 0x0015 = TC2L 0x001D = TC6L
 0x0017 = TC3L 0x001F = TC7L

	7	6	5	4	3	2	1	0
R	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W								
Reset	0	0	0	0	0	0	0	0

Figure 22-23. Timer Input Capture/Output Compare Register x Low (TCxL)

Depending on the TIOS bit for the corresponding channel, these registers are used to latch the value of the free-running counter when a defined transition is sensed by the corresponding input capture edge detector or to trigger an output action for output compare.

Read: Anytime

Write: Anytime for output compare function. Writes to these registers have no meaning or effect during input capture. All timer input capture/output compare registers are reset to 0x0000.

NOTE

Read/Write access in byte mode for high byte should takes place before low byte otherwise it will give a different result.



Figure 25-4. FTM256K2 Register Summary (continued)

25.3.2.1 Flash Clock Divider Register (FCLKDIV)

The FCLKDIV register is used to control timed events in program and erase algorithms.

Offset Module Base + 0x0000

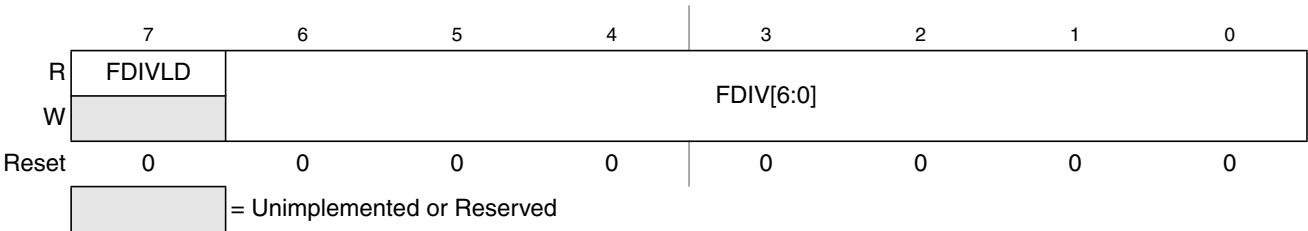


Figure 25-5. Flash Clock Divider Register (FCLKDIV)

All bits in the FCLKDIV register are readable, bits 6–0 are write once and bit 7 is not writable.

Table 25-8. FCLKDIV Field Descriptions

Field	Description
7 FDIVLD	Clock Divider Loaded 0 FCLKDIV register has not been written 1 FCLKDIV register has been written since the last reset
6–0 FDIV[6:0]	Clock Divider Bits — FDIV[6:0] must be set to effectively divide OSCCLK down to generate an internal Flash clock, FCLK, with a target frequency of 1 MHz for use by the Flash module to control timed events during program and erase algorithms. Table 25-9 shows recommended values for FDIV[6:0] based on OSCCLK frequency. Please refer to Section 25.4.1, “Flash Command Operations,” for more information.

CAUTION

The FCLKDIV register should never be written while a Flash command is executing (CCIF=0). The FCLKDIV register is writable during the Flash reset sequence even though CCIF is clear.

- Program a duplicate DFPART to the EEE nonvolatile information register at global address 0x12_0002 (see [Table 25-7](#))
- Program ERPART to the EEE nonvolatile information register at global address 0x12_0004 (see [Table 25-7](#))
- Program a duplicate ERPART to the EEE nonvolatile information register at global address 0x12_0006 (see [Table 25-7](#))

The D-Flash user partition will start at global address 0x10_0000. The buffer RAM EEE partition will end at global address 0x13_FFFF. After the Partition D-Flash operation has completed, the CCIF flag will set.

Running the Partition D-Flash command a second time will result in the ACCERR bit within the FSTAT register being set. The data value written corresponds to the number of 256 byte sectors allocated for either direct D-Flash access (DFPART) or buffer RAM EEE access (ERPART).

Table 25-78. Partition D-Flash Command Error Handling

Register	Error Bit	Error Condition
FSTAT	ACCERR	Set if CCOBIX[2:0] != 010 at command launch
		Set if a Load Data Field command sequence is currently active
		Set if command not available in current mode (see Table 25-30)
		Set if partitions have already been defined
		Set if an invalid DFPART or ERPART selection is supplied
	FPVIOL	None
	MGSTAT1	Set if any errors have been encountered during the read
	MGSTAT0	Set if any non-correctable errors have been encountered during the read
FERSTAT	EPVIOLIF	None

26.4.1.3 Valid Flash Module Commands

Table 26-30. Flash Commands by Mode

FCMD	Command	Unsecured				Secured			
		NS (1)	NX (2)	SS ⁽³⁾	ST ⁽⁴⁾	NS (5)	NX (6)	SS ⁽⁷⁾	ST ⁽⁸⁾
0x01	Erase Verify All Blocks	*	*	*	*	*	*	*	*
0x02	Erase Verify Block	*	*	*	*	*	*	*	*
0x03	Erase Verify P-Flash Section	*	*	*	*	*			
0x04	Read Once	*	*	*	*	*			
0x05	Load Data Field	*	*	*	*	*			
0x06	Program P-Flash	*	*	*	*	*			
0x07	Program Once	*	*	*	*	*			
0x08	Erase All Blocks			*	*			*	*
0x09	Erase P-Flash Block	*	*	*	*	*			
0x0A	Erase P-Flash Sector	*	*	*	*	*			
0x0B	Unsecure Flash			*	*			*	*
0x0C	Verify Backdoor Access Key	*				*			
0x0D	Set User Margin Level	*	*	*	*	*			
0x0E	Set Field Margin Level			*	*				
0x0F	Full Partition D-Flash			*	*				
0x10	Erase Verify D-Flash Section	*	*	*	*	*			
0x11	Program D-Flash	*	*	*	*	*			
0x12	Erase D-Flash Sector	*	*	*	*	*			
0x13	Enable EEPROM Emulation	*	*	*	*	*	*	*	*
0x14	Disable EEPROM Emulation	*	*	*	*	*	*	*	*
0x15	EEPROM Emulation Query	*	*	*	*	*	*	*	*
0x20	Partition D-Flash	*	*	*	*	*	*	*	*

1. Unsecured Normal Single Chip mode.

2. Unsecured Normal Expanded mode.

3. Unsecured Special Single Chip mode.

4. Unsecured Special Mode.

5. Secured Normal Single Chip mode.

6. Secured Normal Expanded mode.

7. Secured Special Single Chip mode.

8. Secured Special Mode.

Table 26-48. Erase All Blocks Command Error Handling

Register	Error Bit	Error Condition
FSTAT	ACCERR	Set if CCOBIX[2:0] != 000 at command launch
		Set if a Load Data Field command sequence is currently active
		Set if command not available in current mode (see Table 26-30)
	FPVIOL	Set if any area of the P-Flash memory is protected
	MGSTAT1	Set if any errors have been encountered during the verify operation ⁽¹⁾
	MGSTAT0	Set if any non-correctable errors have been encountered during the verify operation ¹
FERSTAT	EPVIOLIF	Set if any area of the buffer RAM EEE partition is protected

1. As found in the memory map for FTM512K3.

26.4.2.9 Erase P-Flash Block Command

The Erase P-Flash Block operation will erase all addresses in a P-Flash block.

Table 26-49. Erase P-Flash Block Command FCCOB Requirements

CCOBIX[2:0]	FCCOB Parameters	
000	0x09	Global address [22:16] to identify P-Flash block
001	Global address [15:0] in P-Flash block to be erased	

Upon clearing CCIF to launch the Erase P-Flash Block command, the Memory Controller will erase the selected P-Flash block and verify that it is erased. The CCIF flag will set after the Erase P-Flash Block operation has completed.

Table 26-50. Erase P-Flash Block Command Error Handling

Register	Error Bit	Error Condition
FSTAT	ACCERR	Set if CCOBIX[2:0] != 001 at command launch
		Set if a Load Data Field command sequence is currently active
		Set if command not available in current mode (see Table 26-30)
		Set if an invalid global address [22:16] is supplied ⁽¹⁾
	FPVIOL	Set if an area of the selected P-Flash block is protected
	MGSTAT1	Set if any errors have been encountered during the verify operation ⁽²⁾
	MGSTAT0	Set if any non-correctable errors have been encountered during the verify operation ²
FERSTAT	EPVIOLIF	None

1. As defined by the memory map for FTM512K3.

2. As found in the memory map for FTM512K3.

26.4.2.10 Erase P-Flash Sector Command

The Erase P-Flash Sector operation will erase all addresses in a P-Flash sector.

Table 26-51. Erase P-Flash Sector Command FCCOB Requirements

CCOBIX[2:0]	FCCOB Parameters	
000	0x0A	Global address [22:16] to identify P-Flash block to be erased
001	Global address [15:0] anywhere within the sector to be erased. Refer to Section 26.1.2.1 for the P-Flash sector size.	

Upon clearing CCIF to launch the Erase P-Flash Sector command, the Memory Controller will erase the selected Flash sector and then verify that it is erased. The CCIF flag will be set after the Erase P-Flash Sector operation has completed.

Table 26-52. Erase P-Flash Sector Command Error Handling

Register	Error Bit	Error Condition
FSTAT	ACCERR	Set if CCOBIX[2:0] != 001 at command launch
		Set if a Load Data Field command sequence is currently active
		Set if command not available in current mode (see Table 26-30)
		Set if an invalid global address [22:16] is supplied ⁽¹⁾
		Set if a misaligned phrase address is supplied (global address [2:0] != 000)
	FPVIOL	Set if the selected P-Flash sector is protected
	MGSTAT1	Set if any errors have been encountered during the verify operation
FERSTAT	MGSTAT0	Set if any non-correctable errors have been encountered during the verify operation
	EPVIOLIF	None

1. As defined by the memory map for FTM512K3.

26.4.2.11 Unsecure Flash Command

The Unsecure Flash command will erase the entire P-Flash and D-Flash memory space and, if the erase is successful, will release security.

Table 26-53. Unsecure Flash Command FCCOB Requirements

CCOBIX[2:0]	FCCOB Parameters	
000	0x0B	Not required

Upon clearing CCIF to launch the Unsecure Flash command, the Memory Controller will erase the entire P-Flash and D-Flash memory space and verify that it is erased. If the Memory Controller verifies that the entire Flash memory space was properly erased, security will be released. If the erase verify is not successful, the Unsecure Flash operation sets MGSTAT1 and terminates without changing the security