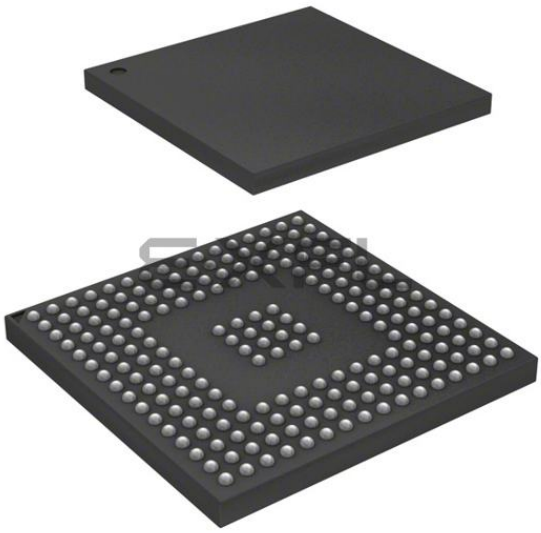

Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	HCS12X
Core Size	16-Bit
Speed	50MHz
Connectivity	CANbus, EBI/EMI, I²C, IrDA, SCI, SPI
Peripherals	LVD, POR, PWM, WDT
Number of I/O	152
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	1.72V ~ 5.5V
Data Converters	A/D 32x12b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	208-BGA
Supplier Device Package	208-BGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/s912xep100j5cvl

interrupt is level sensitive and active low. As XIRQ is level sensitive, while this pin is low the MCU will not enter STOP mode.

1.2.3.20 PF7 / TXD3 — Port F I/O Pin 7

PF7 is a general-purpose input or output pin. It can be configured as the transmit pin TXD of serial communication interface 3 (SCI3).

1.2.3.21 PF6 / RXD3 — Port F I/O Pin 6

PF6 is a general-purpose input or output pin. It can be configured as the transmit pin RXD of serial communication interface 3 (SCI3).

1.2.3.22 PF5 / SCL0 — Port F I/O Pin 5

PF5 is a general-purpose input or output pin. It can be configured as the serial clock pin SCL of the IIC0 module.

1.2.3.23 PF4 / SDA0 — Port F I/O Pin 4

PF4 is a general-purpose input or output pin. It can be configured as the serial data pin SDA of the IIC0 module.

1.2.3.24 PF[3:0] / $\overline{\text{CS}}$[3:0] — Port F I/O Pins 3 to 0

PF[3:0] are a general-purpose input or output pins. They can be configured as chip select outputs [3:0].

1.2.3.25 PH7 / KWH7 / $\overline{\text{SS2}}$ / TXD5 — Port H I/O Pin 7

PH7 is a general-purpose input or output pin. It can be configured as a keypad wakeup input. It can be configured as slave select pin $\overline{\text{SS}}$ of the serial peripheral interface 2 (SPI2). It can be configured as the transmit pin TXD of serial communication interface 5 (SCI5).

1.2.3.26 PH6 / KWH6 / SCK2 / RXD5 — Port H I/O Pin 6

PH6 is a general-purpose input or output pin. It can be configured as a keypad wakeup input. It can be configured as serial clock pin SCK of the serial peripheral interface 2 (SPI2). It can be configured as the receive pin (RXD) of serial communication interface 5 (SCI5).

1.2.3.27 PH5 / KWH5 / MOSI2 / TXD4 — Port H I/O Pin 5

PH5 is a general-purpose input or output pin. It can be configured as a keypad wakeup input. It can be configured as master output (during master mode) or slave input pin (during slave mode) MOSI of the serial peripheral interface 2 (SPI2). It can be configured as the transmit pin TXD of serial communication interface 4 (SCI4).

NOTE

Due to internal synchronization circuits, it can take up to 2 bus clock cycles until the correct value is read on PTT or PTIT registers, when changing the DDRT register.

2.3.24 Port T Reduced Drive Register (RDRT)

Address 0x0243 Access: User read/write(1)

	7	6	5	4	3	2	1	0
R W	RDRT7	RDRT6	RDRT5	RDRT4	RDRT3	RDRT2	RDRT1	RDRT0
Reset	0	0	0	0	0	0	0	0

Figure 2-22. Port T Reduced Drive Register (RDRT)

1. Read: Anytime.
   Write: Anytime.

Table 2-23. RDRT Register Field Descriptions

Field	Description
7-0 RDRT	**Port T reduced drive**—Select reduced drive for outputs This register configures the drive strength of output pins 7 through 0 as either full or reduced independent of the function used on the pins. If a pin is used as input this bit has no effect. 1 Reduced drive selected (approx. 1/5 of the full drive strength). 0 Full drive strength enabled.

2.3.25 Port T Pull Device Enable Register (PERT)

Address 0x0244 Access: User read/write(1)

	7	6	5	4	3	2	1	0
R W	PERT7	PERT6	PERT5	PERT4	PERT3	PERT2	PERT1	PERT0
Reset	0	0	0	0	0	0	0	0

Figure 2-23. Port T Pull Device Enable Register (PERT)

1. Read: Anytime.
   Write: Anytime.

Table 2-24. PERT Register Field Descriptions

Field	Description
7-0 PERT	**Port T pull device enable**—Enable pull devices on input pins These bits configure whether a pull device is activated, if the associated pin is used as an input. This bit has no effect if the pin is used as an output. Out of reset no pull device is enabled. 1 Pull device enabled. 0 Pull device disabled.

2.3.45 Port P Data Register (PTP)

Address 0x0258 Access: User read/write(1)

	7	6	5	4	3	2	1	0
R W	PTP7	PTP6	PTP5	PTP4	PTP3	PTP2	PTP1	PTP0
Altern. Function	PWM7	PWM6	PWM5	PWM4	PWM3	PWM2	PWM1	PWM0
	SCK2	$\overline{SS2}$	MOSI2	MISO2	$\overline{SS1}$	SCK1	MOSI1	MISO1
Reset	0	0	0	0	0	0	0	0

Figure 2-43. Port P Data Register (PTP)

1. Read: Anytime.
   Write: Anytime.

Table 2-41. PTP Register Field Descriptions

Field	Description
7 PTP	**Port P general purpose input/output data**—Data Register Port P pin 6 is associated with the PWM output channel 7 and the SCK signal of SPI2. The PWM function takes precedence over the SPI2 and the general purpose I/O function if the PWM channel 7 is enabled. The SPI2 function takes precedence of the general purpose I/O function if the routed SPI2 is enabled. When not used with the alternative functions, these pins can be used as general purpose I/O. If the associated data direction bits of these pins are set to 1, a read returns the value of the port register, otherwise the buffered pin input state is read.
6 PTP	**Port P general purpose input/output data**—Data Register Port P pin 6 is associated with the PWM output channel 6 and the $\overline{SS}$ signal of SPI2. The PWM function takes precedence over the SPI2 and the general purpose I/O function if the PWM channel 6 is enabled. The SPI2 function takes precedence of the general purpose I/O function if the routed SPI2 is enabled. When not used with the alternative functions, these pins can be used as general purpose I/O. If the associated data direction bits of these pins are set to 1, a read returns the value of the port register, otherwise the buffered pin input state is read.
5 PTP	**Port P general purpose input/output data**—Data Register Port P pin 5 is associated with the PWM output channel 5 and the MOSI signal of SPI2. The PWM function takes precedence over the SPI2 and the general purpose I/O function if the PWM channel 5 is enabled. The SPI2 function takes precedence of the general purpose I/O function if the routed SPI2 is enabled. When not used with the alternative functions, these pins can be used as general purpose I/O. If the associated data direction bits of these pins are set to 1, a read returns the value of the port register, otherwise the buffered pin input state is read.
4 PTP	**Port P general purpose input/output data**—Data Register Port P pin 4 is associated with the PWM output channel 4 and the MISO signal of SPI2. The PWM function takes precedence over the SPI2 and the general purpose I/O function if the PWM channel 4 is enabled. The SPI2 function takes precedence of the general purpose I/O function if the routed SPI2 is enabled. When not used with the alternative functions, these pins can be used as general purpose I/O. If the associated data direction bits of these pins are set to 1, a read returns the value of the port register, otherwise the buffered pin input state is read.

The ACK_ENABLE sends an ACK pulse when the command has been completed. This feature could be used by the host to evaluate if the target supports the hardware handshake protocol. If an ACK pulse is issued in response to this command, the host knows that the target supports the hardware handshake protocol. If the target does not support the hardware handshake protocol the ACK pulse is not issued. In this case, the ACK_ENABLE command is ignored by the target since it is not recognized as a valid command.

The BACKGROUND command will issue an ACK pulse when the CPU changes from normal to background mode. The ACK pulse related to this command could be aborted using the SYNC command.

The GO command will issue an ACK pulse when the CPU exits from background mode. The ACK pulse related to this command could be aborted using the SYNC command.

The GO_UNTIL command is equivalent to a GO command with exception that the ACK pulse, in this case, is issued when the CPU enters into background mode. This command is an alternative to the GO command and should be used when the host wants to trace if a breakpoint match occurs and causes the CPU to enter active background mode. Note that the ACK is issued whenever the CPU enters BDM, which could be caused by a breakpoint match or by a BGND instruction being executed. The ACK pulse related to this command could be aborted using the SYNC command.

The TRACE1 command has the related ACK pulse issued when the CPU enters background active mode after one instruction of the application program is executed. The ACK pulse related to this command could be aborted using the SYNC command.

7.4.9 SYNC — Request Timed Reference Pulse

The SYNC command is unlike other BDM commands because the host does not necessarily know the correct communication speed to use for BDM communications until after it has analyzed the response to the SYNC command. To issue a SYNC command, the host should perform the following steps:

1. Drive the BKGD pin low for at least 128 cycles at the lowest possible BDM serial communication frequency (the lowest serial communication frequency is determined by the crystal oscillator or the clock chosen by CLKSW.)
2. Drive BKGD high for a brief speedup pulse to get a fast rise time (this speedup pulse is typically one cycle of the host clock.)
3. Remove all drive to the BKGD pin so it reverts to high impedance.
4. Listen to the BKGD pin for the sync response pulse.

Upon detecting the SYNC request from the host, the target performs the following steps:

1. Discards any incomplete command received or bit retrieved.
2. Waits for BKGD to return to a logic one.
3. Delays 16 cycles to allow the host to stop driving the high speedup pulse.
4. Drives BKGD low for 128 cycles at the current BDM serial communication frequency.
5. Drives a one-cycle high speedup pulse to force a fast rise time on BKGD.
6. Removes all drive to the BKGD pin so it reverts to high impedance.

The host measures the low time of this 128 cycle SYNC response pulse and determines the correct speed for subsequent BDM communications. Typically, the host can determine the correct communication speed

Table 10-2. XGMCTL Field Descriptions (Sheet 3 of 3)

Field	Description
4 XGSS	**XGATE Single Step** — This bit forces the execution of a single instruction.(1) Read: 0 No single step in progress 1 Single step in progress Write 0 No effect 1 Execute a single RISC instruction **Note:** Invoking a Single Step will cause the XGATE to temporarily leave Debug Mode until the instruction has been executed.
3 XGFACT	**Fake XGATE Activity** — This bit forces the XGATE to flag activity to the MCU even when it is idle. When it is set the MCU will never enter system stop mode which assures that peripheral modules will be clocked during XGATE idle periods Read: 0 XGATE will only flag activity if it is not idle or in debug mode. 1 XGATE will always signal activity to the MCU. Write: 0 Only flag activity if not idle or in debug mode. 1 Always signal XGATE activity.
1 XGSWEF	**XGATE Software Error Flag** — This bit signals a software error. It is set whenever the RISC core detects an error condition(2). The RISC core is stopped while this bit is set. Clearing this bit will terminate the current thread and cause the XGATE to become idle. Read: 0 No software error detected 1 Software error detected Write: 0 No effect 1 Clears the XGSWEF bit
0 XGIE	**XGATE Interrupt Enable** — This bit acts as a global interrupt enable for the XGATE module Read: 0 All outgoing XGATE interrupts disabled (except software error interrupts) 1 All outgoing XGATE interrupts enabled Write: 0 Disable all outgoing XGATE interrupts (except software error interrupts) 1 Enable all outgoing XGATE interrupts

1. Refer to Section 10.6.1, "Debug Features"
2. Refer to Section 10.4.5, "Software Error Detection"

10.3.1.2 XGATE Channel ID Register (XGCHID)

The XGATE Channel ID Register (Figure 10-4) shows the identifier of the XGATE channel that is currently active. This register will read "$00" if the XGATE module is idle. In debug mode this register can be used to start and terminate threads. Refer to Section 10.6.1, "Debug Features" for further information.

BVS Branch if Overflow Set BVS

Operation

If V = 1, then PC + $0002 + (REL9 << 1) ⇒ PC

Tests the Overflow flag and branches if V = 1.

CCR Effects

N	Z	V	C
—	—	—	—

N: Not affected.
Z: Not affected.
V: Not affected.
C: Not affected.

Code and CPU Cycles

Source Form	Address Mode	Machine Code								Cycles
BVS REL9	REL9	0	0	1	0	1	1	1	REL9	PP/P

Address	Name		Bit 7	6	5	4	3	2	1	Bit 0
0x0003	ATDCTL3	R W	DJM	S8C	S4C	S2C	S1C	FIFO	FRZ1	FRZ0
0x0004	ATDCTL4	R W	SMP2	SMP1	SMP0	PRS[4:0]				
0x0005	ATDCTL5	R W	0	SC	SCAN	MULT	CD	CC	CB	CA
0x0006	ATDSTAT0	R W	SCF	0	ETORF	FIFOR	CC3	CC2	CC1	CC0
0x0007	Unimple-mented	R W	0	0	0	0	0	0	0	0
0x0008	ATDCMPEH	R W	CMPE[15:8]							
0x0009	ATDCMPEL	R W	CMPE[7:0]							
0x000A	ATDSTAT2H	R W	CCF[15:8]							
0x000B	ATDSTAT2L	R W	CCF[7:0]							
0x000C	ATDDIENH	R W	IEN[15:8]							
0x000D	ATDDIENL	R W	IEN[7:0]							
0x000E	ATDCMPHTH	R W	CMPHT[15:8]							
0x000F	ATDCMPHTL	R W	CMPHT[7:0]							
0x0010	ATDDR0	R W	See Section 13.3.2.12.1, “Left Justified Result Data (DJM=0)” and Section 13.3.2.12.2, “Right Justified Result Data (DJM=1)”							
0x0012	ATDDR1	R W	See Section 13.3.2.12.1, “Left Justified Result Data (DJM=0)” and Section 13.3.2.12.2, “Right Justified Result Data (DJM=1)”							
0x0014	ATDDR2	R W	See Section 13.3.2.12.1, “Left Justified Result Data (DJM=0)” and Section 13.3.2.12.2, “Right Justified Result Data (DJM=1)”							
0x0016	ATDDR3	R W	See Section 13.3.2.12.1, “Left Justified Result Data (DJM=0)” and Section 13.3.2.12.2, “Right Justified Result Data (DJM=1)”							
0x0018	ATDDR4	R W	See Section 13.3.2.12.1, “Left Justified Result Data (DJM=0)” and Section 13.3.2.12.2, “Right Justified Result Data (DJM=1)”							
0x001A	ATDDR5	R W	See Section 13.3.2.12.1, “Left Justified Result Data (DJM=0)” and Section 13.3.2.12.2, “Right Justified Result Data (DJM=1)”							
0x001C	ATDDR6	R W	See Section 13.3.2.12.1, “Left Justified Result Data (DJM=0)” and Section 13.3.2.12.2, “Right Justified Result Data (DJM=1)”							
0x001E	ATDDR7	R W	See Section 13.3.2.12.1, “Left Justified Result Data (DJM=0)” and Section 13.3.2.12.2, “Right Justified Result Data (DJM=1)”							
0x0020	ATDDR8	R W	See Section 13.3.2.12.1, “Left Justified Result Data (DJM=0)” and Section 13.3.2.12.2, “Right Justified Result Data (DJM=1)”							
0x0022	ATDDR9	R W	See Section 13.3.2.12.1, “Left Justified Result Data (DJM=0)” and Section 13.3.2.12.2, “Right Justified Result Data (DJM=1)”							

= Unimplemented or Reserved

Figure 13-2. ADC12B16C Register Summary (Sheet 2 of 3)

Table 13-3. Multi-Channel Wrap Around Coding

WRAP3	WRAP2	WRAP1	WRAP0	Multiple Channel Conversions (MULT = 1) Wraparound to AN0 after Converting
0	0	0	1	AN1
0	0	1	0	AN2
0	0	1	1	AN3
0	1	0	0	AN4
0	1	0	1	AN5
0	1	1	0	AN6
0	1	1	1	AN7
1	0	0	0	AN8
1	0	0	1	AN9
1	0	1	0	AN10
1	0	1	1	AN11
1	1	0	0	AN12
1	1	0	1	AN13
1	1	1	0	AN14
1	1	1	1	AN15

1. If only AN0 should be converted use MULT=0.

13.3.2.2 ATD Control Register 1 (ATDCTL1)

Writes to this register will abort current conversion sequence.

Module Base + 0x0001

	7	6	5	4	3	2	1	0
R W	ETRIGSEL	SRES1	SRES0	SMP_DIS	ETRIGCH3	ETRIGCH2	ETRIGCH1	ETRIGCH0
Reset	0	0	1	0	1	1	1	1

Figure 13-4. ATD Control Register 1 (ATDCTL1)

Read: Anytime

Write: Anytime

Table 13-4. ATDCTL1 Field Descriptions

Field	Description
7 ETRIGSEL	**External Trigger Source Select** — This bit selects the external trigger source to be either one of the AD channels or one of the ETRIG3-0 inputs. See device specification for availability and connectivity of ETRIG3-0 inputs. If a particular ETRIG3-0 input option is not available, writing a 1 to ETRISEL only sets the bit but has not effect, this means that one of the AD channels (selected by ETRIGCH3-0) is configured as the source for external trigger. The coding is summarized in Table 13-6.
6–5 SRES[1:0]	**A/D Resolution Select** — These bits select the resolution of A/D conversion results. See Table 13-5 for coding.

Table 13-7. ATDCTL2 Field Descriptions (continued)

Field	Description
1 ASCIE	**ATD Sequence Complete Interrupt Enable** 0 ATD Sequence Complete interrupt requests are disabled. 1 ATD Sequence Complete interrupt will be requested whenever SCF=1 is set.
0 ACMPIE	**ATD Compare Interrupt Enable** — If automatic compare is enabled for conversion *n* (CMPE[*n*]=1 in ATDCMPE register) this bit enables the compare interrupt. If the CCF[*n*] flag is set (showing a successful compare for conversion *n*), the compare interrupt is triggered. 0 ATD Compare interrupt requests are disabled. 1 For the conversions in a sequence for which automatic compare is enabled (CMPE[*n*]=1), ATD Compare Interrupt will be requested whenever any of the respective CCF flags is set.

Table 13-8. External Trigger Configurations

ETRIGLE	ETRIGP	External Trigger Sensitivity
0	0	Falling edge
0	1	Rising edge
1	0	Low level
1	1	High level

13.3.2.4 ATD Control Register 3 (ATDCTL3)

Writes to this register will abort current conversion sequence.

Module Base + 0x0003

	7	6	5	4	3	2	1	0
R W	DJM	S8C	S4C	S2C	S1C	FIFO	FRZ1	FRZ0
Reset	0	0	1	0	0	0	0	0

= Unimplemented or Reserved

Figure 13-6. ATD Control Register 3 (ATDCTL3)

Read: Anytime

Write: Anytime

Field	Description
7 DJM	**Result Register Data Justification** — Result data format is always unsigned. This bit controls justification of conversion data in the result registers. 0 Left justified data in the result registers. 1 Right justified data in the result registers. Table 13-10 gives examples ATD results for an input signal range between 0 and 5.12 Volts.

Table 13-9. ATDCTL3 Field Descriptions

- General Call Address detection
- Compliant to ten-bit address

15.1.2 Modes of Operation

The IIC functions the same in normal, special, and emulation modes. It has two low power modes: wait and stop modes.

15.1.3 Block Diagram

The block diagram of the IIC module is shown in Figure 15-1.

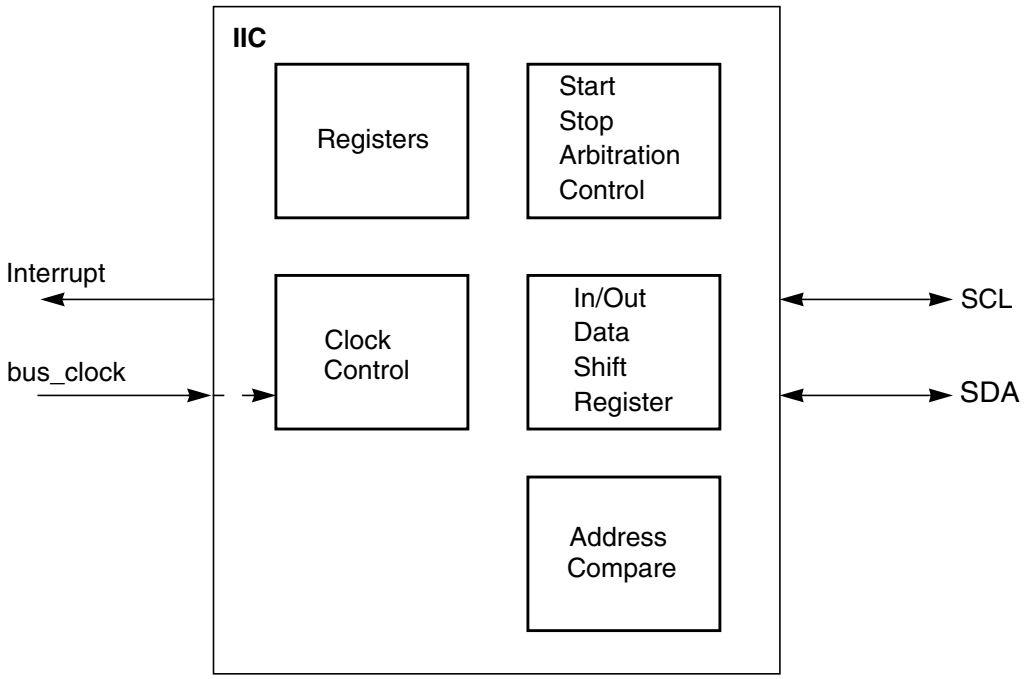

Figure 15-1. IIC Block Diagram

15.2 External Signal Description

The IICV3 module has two external pins.

15.2.1 IIC_SCL — Serial Clock Line Pin

This is the bidirectional serial clock line (SCL) of the module, compatible to the IIC bus specification.

15.2.2 IIC_SDA — Serial Data Line Pin

This is the bidirectional serial data line (SDA) of the module, compatible to the IIC bus specification.

15.4.1.8 Handshaking

The clock synchronization mechanism can be used as a handshake in data transfer. Slave devices may hold the SCL low after completion of one byte transfer (9 bits). In such case, it halts the bus clock and forces the master clock into wait states until the slave releases the SCL line.

15.4.1.9 Clock Stretching

The clock synchronization mechanism can be used by slaves to slow down the bit rate of a transfer. After the master has driven SCL low the slave can drive SCL low for the required period and then release it.If the slave SCL low period is greater than the master SCL low period then the resulting SCL bus signal low period is stretched.

15.4.1.10 Ten-bit Address

A ten-bit address is indicated if the first 5 bits of the first address byte are 0x11110. The following rules apply to the first address byte.

Table 15-11. Definition of Bits in the First Byte

SLAVE ADDRESS	R/W BIT	DESCRIPTION
0000000	0	General call address
0000010	x	Reserved for different bus format
0000011	x	Reserved for future purposes
11111XX	x	Reserved for future purposes
11110XX	x	10-bit slave addressing

The address type is identified by ADTYPE. When ADTYPE is 0, 7-bit address is applied. Reversely, the address is 10-bit address.Generally, there are two cases of 10-bit address.See the Fig.1-14 and 1-15.

S	Slave Add1st 7bits 11110+ADR10+ADR9	R/W 0	A1	Slave Add 2nd byte ADR[8:1]	A2	Data	A3

Figure 15-13. A master-transmitter addresses a slave-receiver with a 10-bit address

S	Slave Add1st 7bits 11110+ADR10+ADR9	R/W 0	A1	Slave Add 2nd byte ADR[8:1]	A2	Sr	Slave Add 1st 7bits 11110+ADR10+ADR9	R/W 1	A3	Data	A4

Figure 15-14. A master-receiver addresses a slave-transmitter with a 10-bit address

In the figure 1-15,the first two bytes are the similar to figure1-14.After the repeated START(Sr),the first slave address is transmitted again, but the R/W is 1, meaning that the slave is acted as a transmitter.

15.4.1.11 General Call Address

To broadcast using a general call, a device must first generate the general call address($00), then after receiving acknowledge, it must transmit data.

In communication, as a slave device, provided the GCEN is asserted, a device acknowledges the broadcast and receives data until the GCEN is disabled or the master device releases the bus or generates a new

Module Base + 0x0006 Access: User read/write(1)

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	TXE2	TXE1	TXE0
W								
Reset:	0	0	0	0	0	1	1	1

= Unimplemented

Figure 16-10. MSCAN Transmitter Flag Register (CANTFLG)

1. Read: Anytime
   Write: Anytime when not in initialization mode; write of 1 clears flag, write of 0 is ignored

NOTE

The CANTFLG register is held in the reset state when the initialization mode is active (INITRQ = 1 and INITAK = 1). This register is writable when not in initialization mode (INITRQ = 0 and INITAK = 0).

Table 16-13. CANTFLG Register Field Descriptions

Field	Description
2-0 TXE[2:0]	**Transmitter Buffer Empty** — This flag indicates that the associated transmit message buffer is empty, and thus not scheduled for transmission. The CPU must clear the flag after a message is set up in the transmit buffer and is due for transmission. The MSCAN sets the flag after the message is sent successfully. The flag is also set by the MSCAN when the transmission request is successfully aborted due to a pending abort request (see Section 16.3.2.9, "MSCAN Transmitter Message Abort Request Register (CANTARQ)"). If not masked, a transmit interrupt is pending while this flag is set. Clearing a TXEx flag also clears the corresponding ABTAKx (see Section 16.3.2.10, "MSCAN Transmitter Message Abort Acknowledge Register (CANTAAK)"). When a TXEx flag is set, the corresponding ABTRQx bit is cleared (see Section 16.3.2.9, "MSCAN Transmitter Message Abort Request Register (CANTARQ)"). When listen-mode is active (see Section 16.3.2.2, "MSCAN Control Register 1 (CANCTL1)") the TXEx flags cannot be cleared and no transmission is started. Read and write accesses to the transmit buffer will be blocked, if the corresponding TXEx bit is cleared (TXEx = 0) and the buffer is scheduled for transmission. 0 The associated message buffer is full (loaded with a message due for transmission) 1 The associated message buffer is empty (not scheduled)

16.3.2.8 MSCAN Transmitter Interrupt Enable Register (CANTIER)

This register contains the interrupt enable bits for the transmit buffer empty interrupt flags.

Module Base + 0x0007 Access: User read/write(1)

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	TXEIE2	TXEIE1	TXEIE0
W								
Reset:	0	0	0	0	0	0	0	0

= Unimplemented

Figure 16-11. MSCAN Transmitter Interrupt Enable Register (CANTIER)

- Program a duplicate DFPART to the EEE nonvolatile information register at global address 0x12_0002 (see Table 26-7)
- Program ERPART to the EEE nonvolatile information register at global address 0x12_0004 (see Table 26-7)
- Program a duplicate ERPART to the EEE nonvolatile information register at global address 0x12_0006 (see Table 26-7)

The D-Flash user partition will start at global address 0x10_0000. The buffer RAM EEE partition will end at global address 0x13_FFFF. After the Partition D-Flash operation has completed, the CCIF flag will set.

Running the Partition D-Flash command a second time will result in the ACCERR bit within the FSTAT register being set. The data value written corresponds to the number of 256 byte sectors allocated for either direct D-Flash access (DFPART) or buffer RAM EEE access (ERPART).

Table 26-78. Partition D-Flash Command Error Handling

Register	Error Bit	Error Condition
FSTAT	ACCERR	Set if CCOBIX[2:0] != 010 at command launch
		Set if a Load Data Field command sequence is currently active
		Set if command not available in current mode (see Table 26-30)
		Set if partitions have already been defined
		Set if an invalid DFPART or ERPART selection is supplied
	FPVIOL	None
	MGSTAT1	Set if any errors have been encountered during the read
	MGSTAT0	Set if any non-correctable errors have been encountered during the read
FERSTAT	EPVIOLIF	None

Address & Name	7	6	5	4	3	2	1	0

= Unimplemented or Reserved

Figure 29-4. FTM1024K5 Register Summary (continued)

29.3.2.1 Flash Clock Divider Register (FCLKDIV)

The FCLKDIV register is used to control timed events in program and erase algorithms.

Offset Module Base + 0x0000

	7	6	5	4	3	2	1	0
R	FDIVLD	FDIV[6:0]						
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 29-5. Flash Clock Divider Register (FCLKDIV)

All bits in the FCLKDIV register are readable, bits 6–0 are write once and bit 7 is not writable.

Table 29-8. FCLKDIV Field Descriptions

Field	Description
7 FDIVLD	**Clock Divider Loaded** 0 FCLKDIV register has not been written 1 FCLKDIV register has been written since the last reset
6–0 FDIV[6:0]	**Clock Divider Bits** — FDIV[6:0] must be set to effectively divide OSCCLK down to generate an internal Flash clock, FCLK, with a target frequency of 1 MHz for use by the Flash module to control timed events during program and erase algorithms. Table 29-9 shows recommended values for FDIV[6:0] based on OSCCLK frequency. Please refer to Section 29.4.1, “Flash Command Operations,” for more information.

CAUTION

The FCLKDIV register should never be written while a Flash command is executing (CCIF=0). The FCLKDIV register is writable during the Flash reset sequence even though CCIF is clear.

A.3.1.4 Read Once (FCMD=0x04)

The maximum read once time is given by

$$t = (400) \cdot \frac{1}{f_{NVMBUS}}$$

A.3.1.5 Load Data Field (FCMD=0x05)

The maximum load data field time is given by

$$t = (450) \cdot \frac{1}{f_{NVMBUS}}$$

A.3.1.6 Program P-Flash (FCMD=0x06)

The programming time for a single phrase of four P-Flash words + associated eight ECC bits is dependant on the bus frequency as a well as on the frequency f_{NVMOP} and can be calculated according to the following formulas, whereby N_{DLOAD} is the number of extra blocks being programmed by the Load Data Field command (DLOAD), i.e. programming 2,3,4 blocks using DLOAD, N_{DLOAD} =1,2,3 respectively.

The typical phrase programming time can be calculated using the following equation

$$t_{bwpgm} = (128 + (12 \cdot N_{DLOAD})) \cdot \frac{1}{f_{NVMOP}} + (1725 + (510 \cdot N_{DLOAD})) \cdot \frac{1}{f_{NVMBUS}}$$

The maximum phrase programming time can be calculated using the following equation

$$t_{bwpgm} = (130 + (14 \cdot N_{DLOAD})) \cdot \frac{1}{f_{NVMOP}} + (2125 + (510 \cdot N_{DLOAD})) \cdot \frac{1}{f_{NVMBUS}}$$

A.3.1.7 P-Flash Program Once (FCMD=0x07)

The maximum P-Flash Program Once time is given by

$$t_{bwpgm} \approx 162 \cdot \frac{1}{f_{NVMOP}} + 2400 \cdot \frac{1}{f_{NVMBUS}}$$

A.3.1.8 Erase All Blocks (FCMD=0x08)

For S12XEP100, S12XEP768, S12XEQ512 and S12XEQ384 erasing all blocks takes:

$$t_{mass} \approx 100100 \cdot \frac{1}{f_{NVMOP}} + 70000 \cdot \frac{1}{f_{NVMBUS}}$$

For S12XET256, S12XEA256 and S12XEG128 erasing all blocks takes:

$$t_{mass} \approx 100100 \cdot \frac{1}{f_{NVMOP}} + 35000 \cdot \frac{1}{f_{NVMBUS}}$$

A.3.1.20 Maximum CCOB Latency

The maximum time a CCOB command has to wait to be actioned due to an EEE clean up is given where BWN = 1 if a brownout has occured otherwise BWN = 0. BWN = 1 only for the first ENEEE after reset.

$$t \approx \left(32364 \cdot \frac{1}{f_{NVMOP}} + 292600 \cdot \frac{1}{f_{NVMBUS}}\right) \cdot (1 + BWN) + BWN \cdot \left(350 \cdot \frac{1}{f_{NVMOP}} + \frac{1100}{f_{NVMBUS}}\right)$$

A.3.1.21 Disable EEE (FCMD=0x14)

Maximum time to disable EPROM emulation is given by

$$t = 300 \cdot \frac{1}{f_{NVMBUS}}$$

A.3.1.22 EEE Query (FCMD=0x15)

Maximum time for the EEE query command is given by

$$t = 300 \cdot \frac{1}{f_{NVMBUS}}$$

A.3.1.23 Partition D-Flash (FCMD=0x20)

The maximum time for partitioning the D-flash (ERPART=16, DFPART=0) is given by

$$t \approx 21800 \cdot \frac{1}{f_{NVMOP}} + 400000 \cdot \frac{1}{f_{NVMBUS}}$$

A.7.3 External Bus Timing

The following conditions are assumed for all following external bus timing values:

- Crystal input within 45% to 55% duty
- Equal 25 pF load on all pins
- Pad full drive (reduced drive must be off)

A.7.3.1 Normal Expanded Mode (External Wait Feature Disabled)

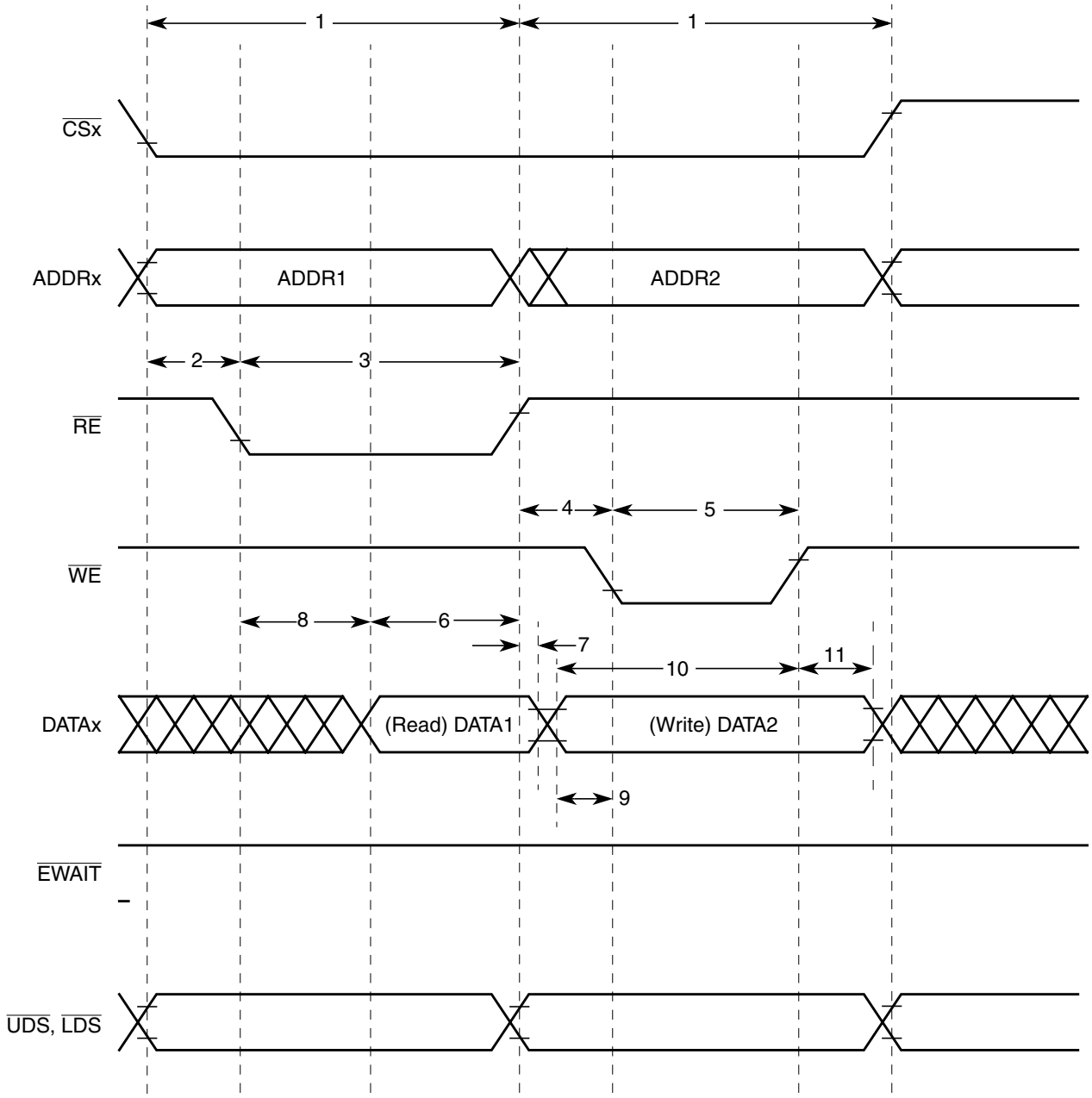

Figure A-12. Example 1a: Normal Expanded Mode — Read Followed by Write

Appendix C
PCB Layout Guidelines

The PCB must be carefully laid out to ensure proper operation of the voltage regulator as well as of the MCU itself. The following rules must be observed:

- Every supply pair must be decoupled by a ceramic capacitor connected as near as possible to the corresponding pins .
- Central point of the ground star should be the VSS3 pin.
- Use low ohmic low inductance connections between VSS1, VSS2 and VSS3.
- VSSPLL must be directly connected to VSS3.
- Keep traces of VSSPLL, EXTAL, and XTAL as short as possible and occupied board area for C7, C8, and Q1 as small as possible.
- Do not place other signals or supplies underneath area occupied by C7, C8, and Q1 and the connection area to the MCU.
- Central power input should be fed in at the VDDA/VSSA pins.

Example layouts are illustrated on the following pages.

Figure C-2. 112-Pin LQFP Recommended PCB Layout (Loop Controlled Pierce Oscillator)